Embedded Memory

Manual

February 1999

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Chapter 1: Overview of ASPEC Embedded Memory Cells

1.1 Introduction

This document provides datasheets for the ASPEC embedded memory cells.

1.2 Available Sizes

Table A shows the feature sizes available forASPEC Technology's Embedded Memories.

Table 1.1: Embedded Memory Availability

Name	Feature Size (μm)
Single-Port RAM (SL1RW)	0.8 - 0.35
One Read One Write Dual-Port RAM (SL1R1W)	0.8 - 0.35
One Read/Write One Read Dual-Port RAM (SL1RW1R)	0.8 - 0.35
SROM 5.0V	0.8 - 0.35
SROM 3.3V	0.8 - 0.35
CADROM	0.35
Synchronous High-Density Single-Port RAM - Version B (CS1RWB)	0.5 - 0.35
Synchronous High-Density Dual-Port RAM - Version B (CS2RWB)	0.5 - 0.35
Synchronous High-Density Single-Port RAM - Version D (CS1RWD)	0.25
Synchronous High-Density Dual-Port RAM - Version D(CS2RWD)	0.25

Chapter 2: Latch-Based Memories

2.1 Single-Port RAM Specifications

Description

This is a high-speed, low power, single-port RAM (SL1RW) with fully static and asynchronous operation. The number of words and word width can be configured with the MEMGEN memory compiler. The design has 1 read/write address port, 1 input data port and 1 output data port. Control pins are OEN (output enable) and WEN (write enable). During write operation, the output data port reflects data at the input port if the output 3-state buffers are enabled.

Three RAM architectures (Types 1, 2, 4) support varying aspect ratios consistent with word/bit configuration limitations.

Memories can be flipped left/right or up/down; ASPEC does not recommend rotating latch-based memories.

Features

- 1 read/write address port
- 1 input and 1 output data port
- Zero standby power
- High speed
- Asynchronous and fully static operation
- 3-state output buffers
- Parameter-driven compiler
- Up to 9K bit block
- Variable word depth to

  8,16,24,32,40,48,56,..... 256
- Variable word width to

  4,5,6,7,..... 72
- Available Architectures

  Type 1, Type 2, Type 4

Logic Symbol and Block Diagram

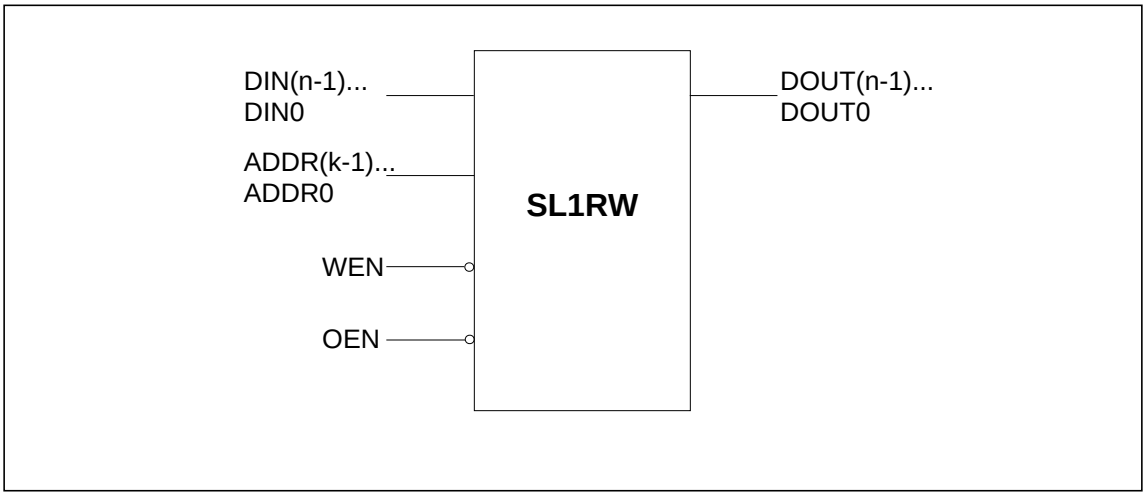


Figure 2.1: Logic Symbol for SL1RW RAM

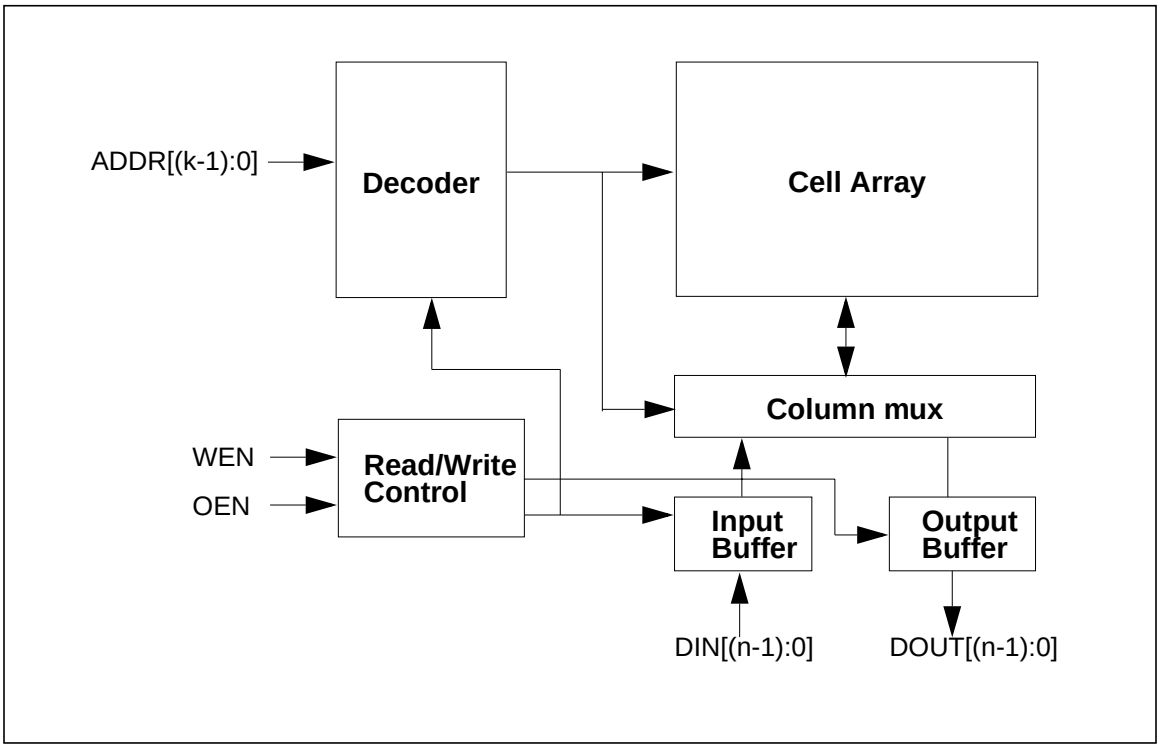


Figure 2.2: Block Diagram for SL1RW RAM

I/O Pin Description and Truth Table

Table 2.1: SL1RW RAM I/O Pin Description

Name	I/O	I/O Cap. (pF)	Description
DIN(n-1)...DIN0	I	1 * architecture type * iv input cap.	Data Input
ADDR(k-1)...ADDR0	I	2 * iv input cap.	Read/Write Address
OEN	I	1 * iv input cap.	Output Enable When OEN is high, the outputs are in high impedance state. When OEN is Low, the data outputs are enabled.
WEN	I	2 * iv input cap.	Memory Write operation is enabled when WEN is Low
DOUT(n-1)...DOUT0	O	3 * architecture type * output cap.	Output Data

Table 2.2: SL1RW RAM Truth Table

OE	WE	Mode
X	L	Write
L	H	Read
L	X	Read
H	X	Output = high impedance

Configuration and AC Parameters

Word: 8, 16, 24, 32, 40, 48, 56, 64, 72, 80, 96, 104, 112, 120, 128, 144, 60, 176, 192, 208, 224, 240, 256

Bit : 4, 5, 6, 7..... 69, 70, 71, 72

Type : 1 = 4 - 72, 2 = 4- 36, 4 = 4 - 18

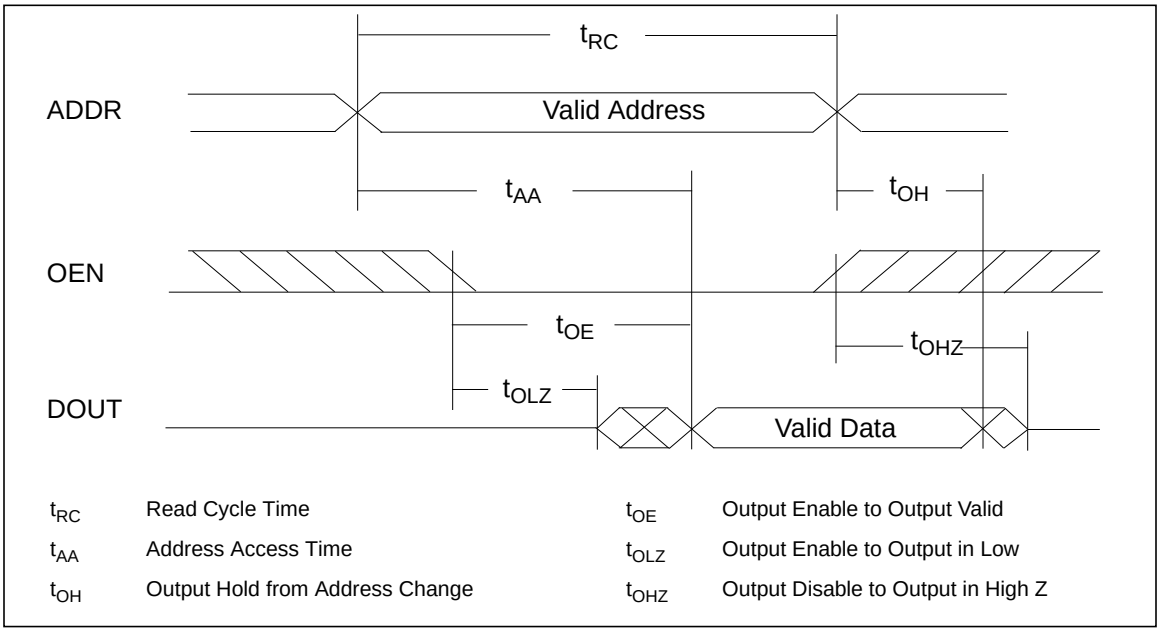
Table 2.3: SL1RW RAM Read Cycle

Parameters	Symbol
Read Cycle time	t_{RC}
Address Access time	t_{AA}
Address Output Data hold time	t_{OH}
Output Enable time	t_{OE}
Output Enable to Output in low Z	t_{OLZ}
Output Disable time	t_{OHZ}

Table 2.4: SL1RW RAM Write Cycle

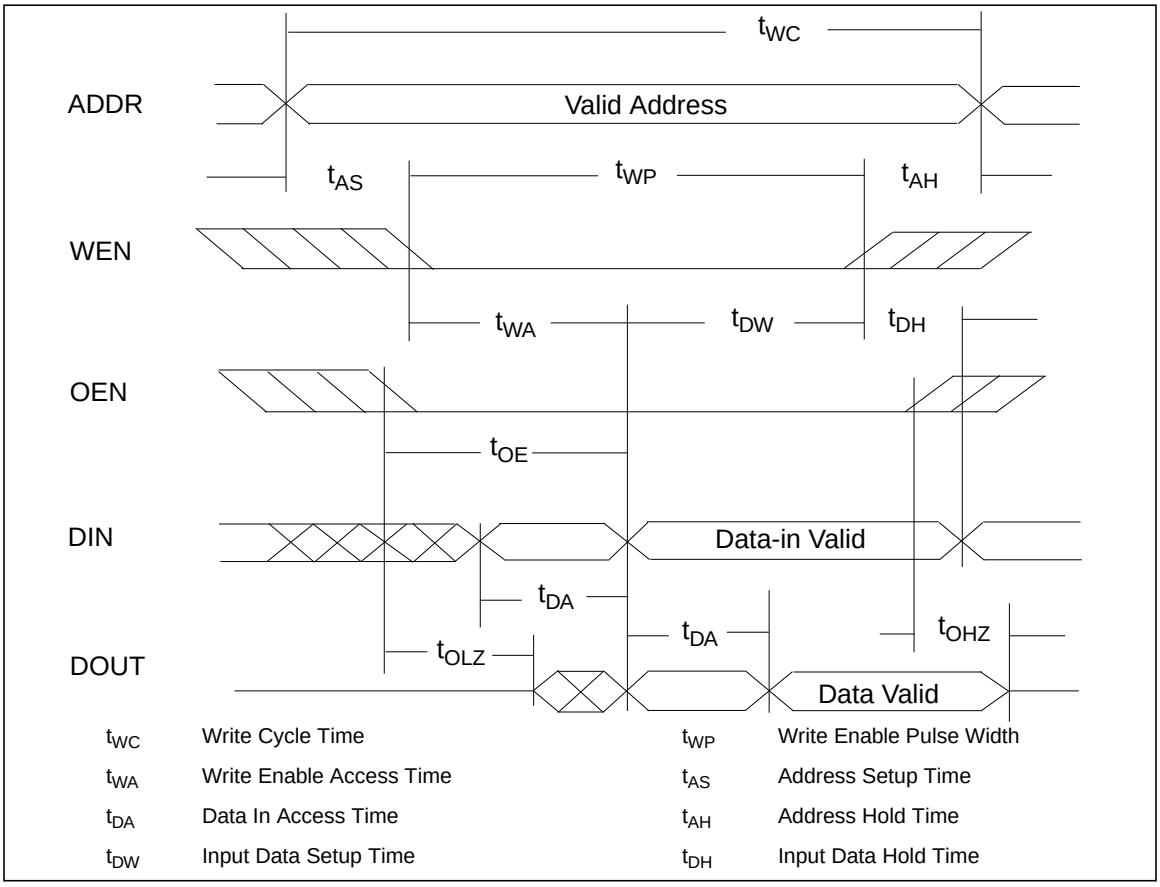
Parameters	Symbol
Write Cycle time	t_{WC}
Write Enable Access time	t_{WA}
Data-in Access time	t_{DA}
Write Pulse Width	t_{WP}
Address Setup time	t_{AS}
Address Hold time	t_{AH}
Data Setup time	t_{DW}
Data Hold time	t_{DH}

Timing Diagrams



t_{RC}	Read Cycle Time	t_{OE}	Output Enable to Output Valid
t_{AA}	Address Access Time	t_{OLZ}	Output Enable to Output in Low
t_{OH}	Output Hold from Address Change	t_{OHZ}	Output Disable to Output in High Z

Figure 2.3: SL1RW RAM Read Cycle



t_{WC}	Write Cycle Time	t_{WP}	Write Enable Pulse Width
t_{WA}	Write Enable Access Time	t_{AS}	Address Setup Time
t_{DA}	Data In Access Time	t_{AH}	Address Hold Time
t_{DW}	Input Data Setup Time	t_{DH}	Input Data Hold Time

Figure 2.4: SL1RW RAM Write Cycle

Architecture

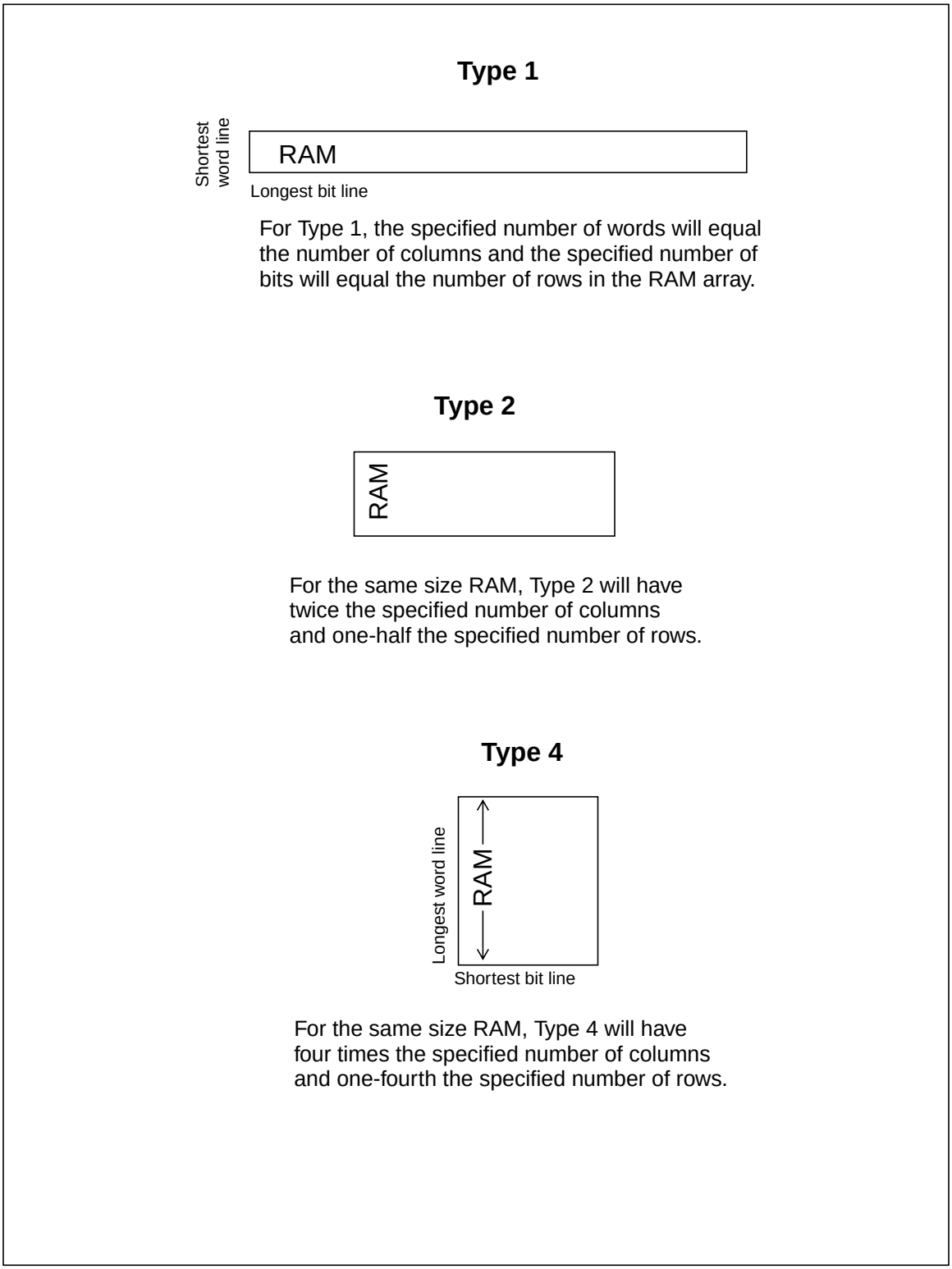


Figure 2.5: SL1RW RAM Architecture Options

2.2 One Read One Write Dual-Port RAM Specifications

Description

The high-speed, low power, dual-port RAM (SL1R1W) has fully static and asynchronous operation. The number of words and word width can be configured with MEMGEN - embedded memory compiler.

This configuration has 1 read address port and 1 write address port, 1 input data port and 1 output data port. Control pins are OEN (output enable) and WEN (write enable). During write operation, the output data port reflects data at the input port if the output 3-state buffers are enabled.

Four dual-port RAM architectures (Types 1, 2, 4, 8) support varying aspect ratios consistent with word/bit configuration limitations.

Memories can be flipped left/right or up/down; ASPEC does not recommend rotating latch-based memories.

Features

- Fully asynchronous Read/Write operation
- Variable size dual-port RAM with 1 read address port and 1 write address port
- 1 input and 1 output data port
- Zero standby power
- High speed
- 3-state output buffers
- Parameter-driven compiler
- Up to 9K bit block
- Variable word depth to

  8,16,24,32,40,48,56,..... 1024
- Variable word width to

  4,5,6,7,..... 72
- Available architectures

  Type 1, Type 2, Type 4, Type 8

Logic Symbol and Block Diagram

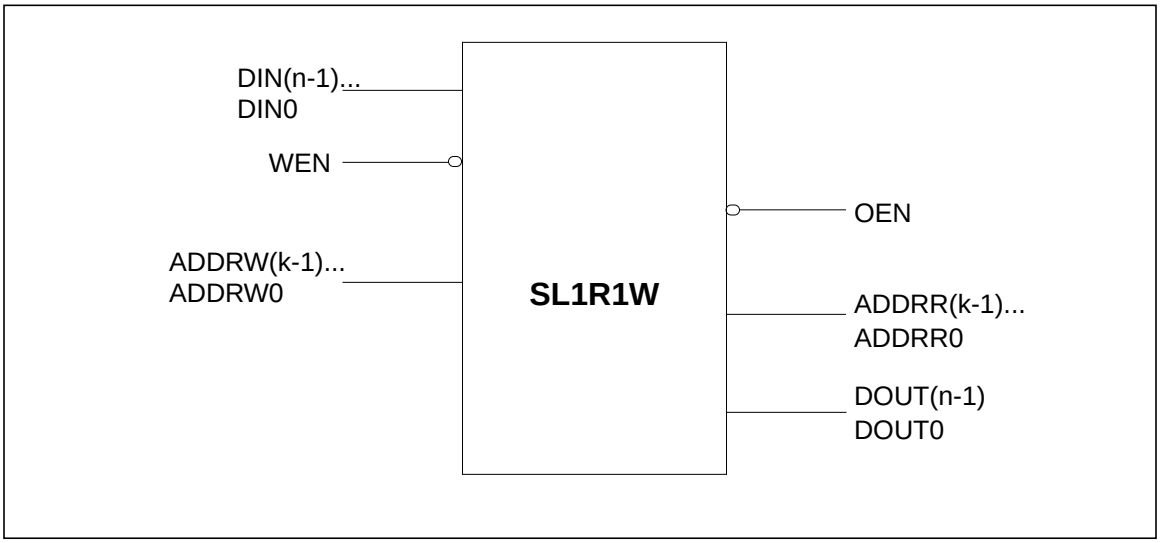


Figure 2.6: Logic Symbol for SL1R1W RAM

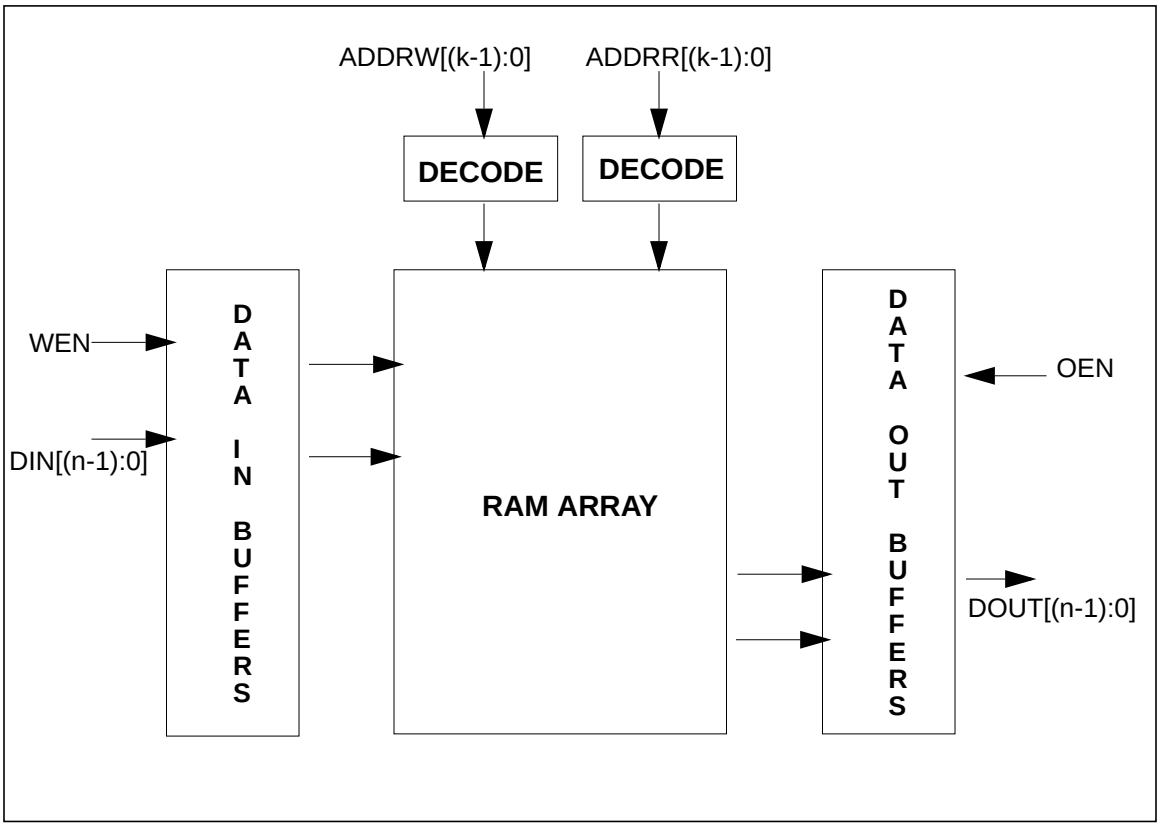


Figure 2.7: Block Diagram for SL1R1W RAM

I/O Pin Description and Truth Table

Table 2.5: SL1R1W RAM I/O Pin Description

Name	I/O	I/O Cap. (pF)	Description
WEN	I	2 * iv input cap.	Left, right read/write control
OEN	I	1 * iv input cap.	Left, right tri-state control
DIN(n-1)...DIN0	I	1 * architecture type	Left, right data input
ADDRW(k-1)...ADDRW0 ADDRR(k-1)...ADDRR0	I	2 * iv input cap.	Left, right address input
DOUT	O	7 * architecture type * output cap.	Left, right output

Table 2.6: SL1R1W RAM Truth Table

OE	WE	Mode
X	L	Write
L	H	Read
L	X	Read
H	X	Output = high impedance

Configuration and AC Parameters

Word: 8, 16, 24, 32, 40, 48, 56, 64, 72, 80, 88, 96, 104, 112, 120, 128, 144, 160, 176, 192, 208, 224, 240, 256, 288, 320, 352, 384, 416, 480, 512, 576, 640, 704, 768, 832, 896, 960, 1024

Bit : 4, 5, 6, 7..... 69, 70, 71, 72

Type : 1 = 4 - 72, 2 = 4- 36, 4 = 4 -18, 8 = 4 - 9

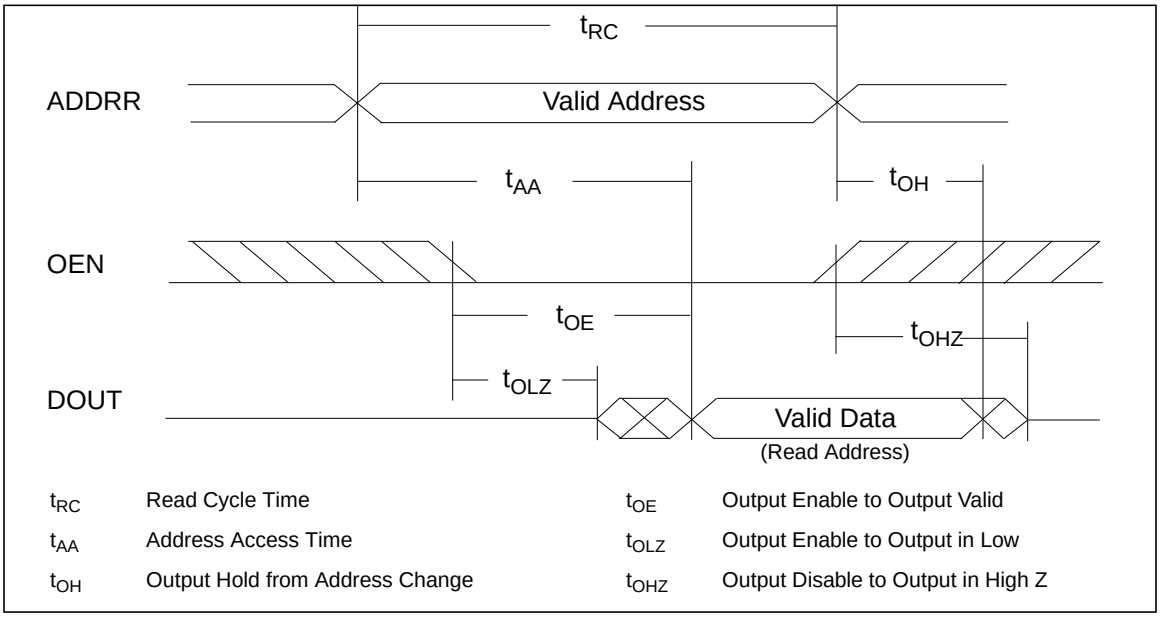
Table 2.7: SL1R1W RAM Read Cycle

Parameters	Symbol
Read Cycle time	t_{RC}
Address Access time	t_{AA}
Output Enable to Output Low-Z	t_{OLZ}
Output Enable to Output High-Z	t_{OHZ}
Output Enable time	t_{OE}

Table 2.8: SL1R1W RAM Write Cycle

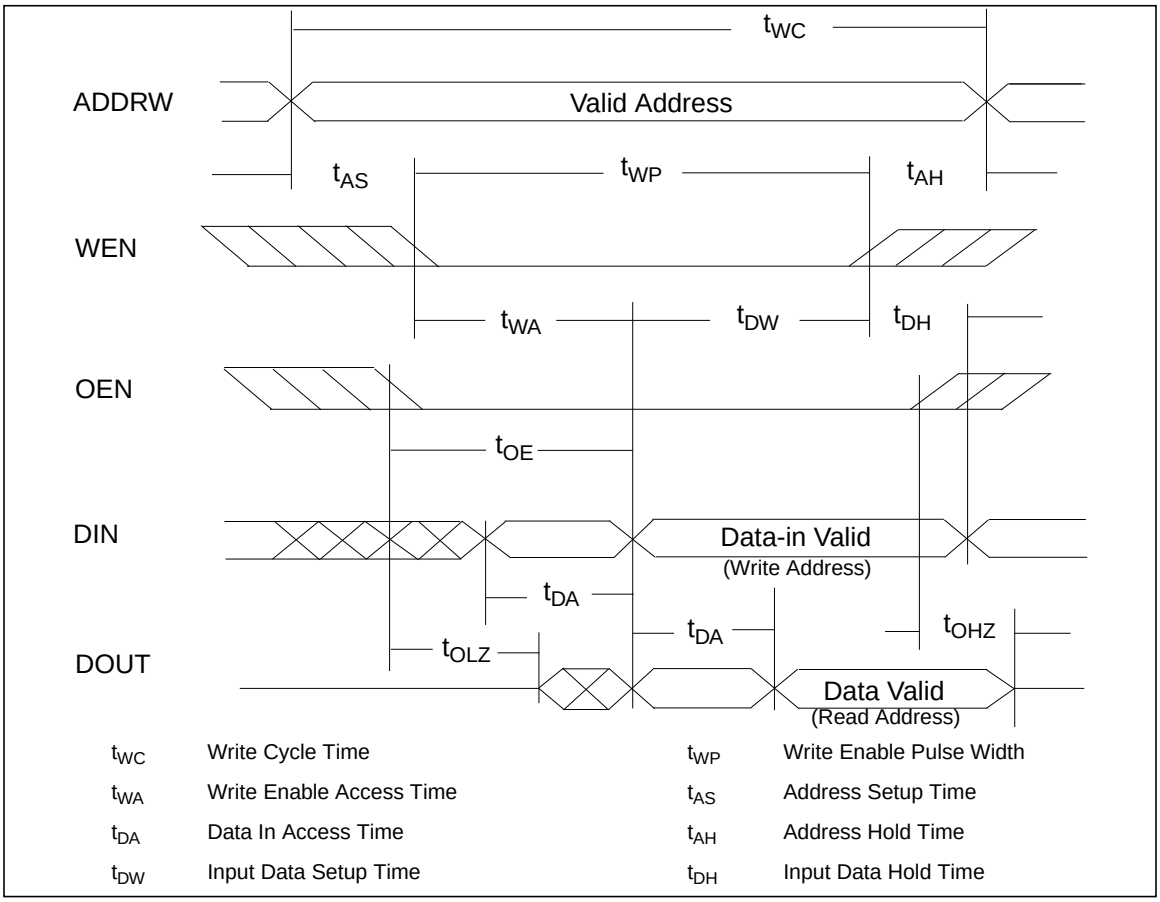
Parameters	Symbol
Write Cycle time	t_{WC}
Write Enable Access time	t_{WA}
Data-in Access time	t_{DA}
Write Pulse Width	t_{WP}
Address Setup time	t_{AS}
Address Hold time	t_{AH}
Data Setup time	t_{DW}
Data Hold time	t_{DH}

Timing Diagrams



t_{RC}	Read Cycle Time	t_{OE}	Output Enable to Output Valid
t_{AA}	Address Access Time	t_{OLZ}	Output Enable to Output in Low
t_{OH}	Output Hold from Address Change	t_{OHZ}	Output Disable to Output in High Z

Figure 2.8: SL1R1W RAM Read Cycle



t_{WC}	Write Cycle Time	t_{WP}	Write Enable Pulse Width
t_{WA}	Write Enable Access Time	t_{AS}	Address Setup Time
t_{DA}	Data In Access Time	t_{AH}	Address Hold Time
t_{DW}	Input Data Setup Time	t_{DH}	Input Data Hold Time

Figure 2.9: SL1R1W RAM Write Cycle

Architecture

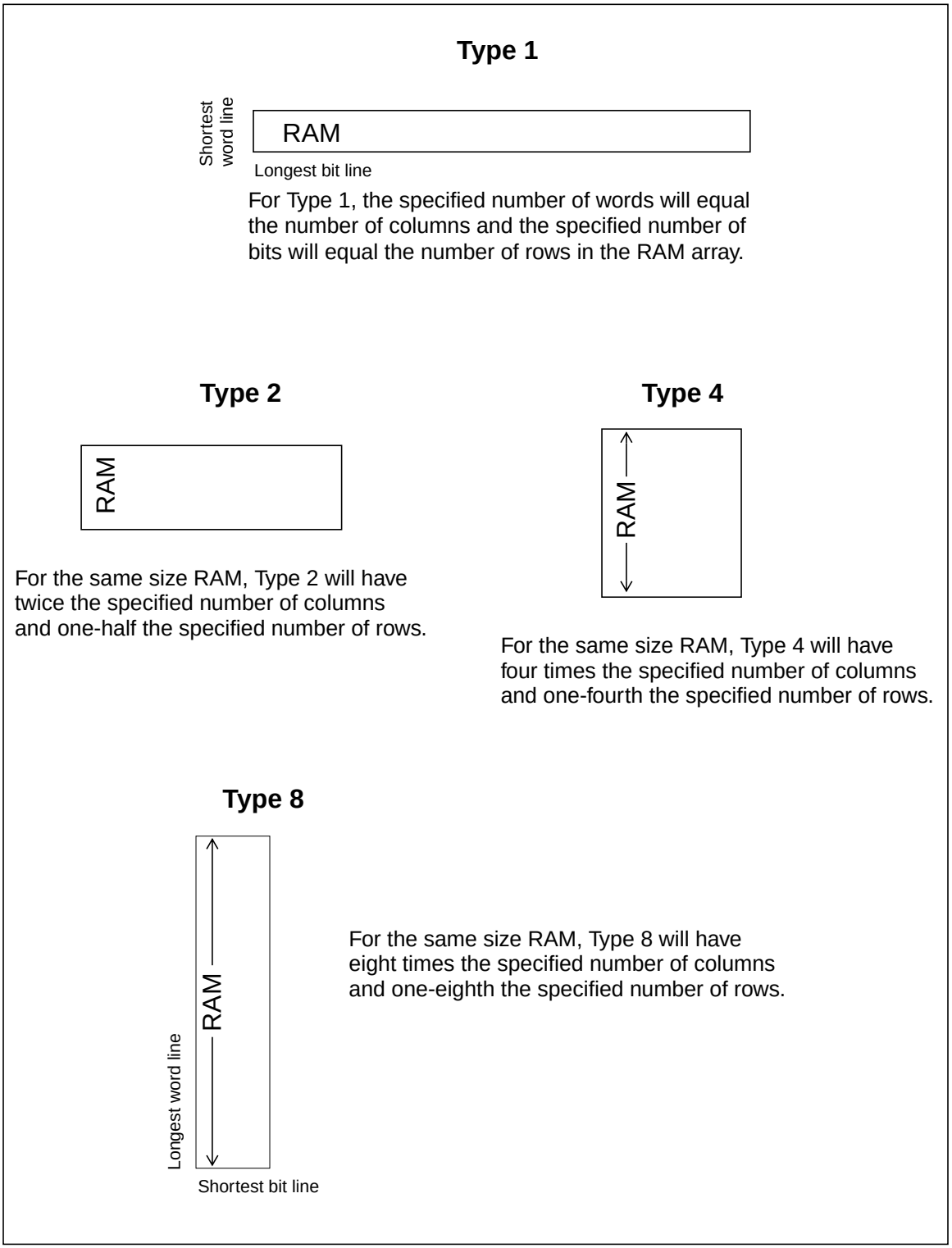


Figure 2.10: SL1R1W RAM Architecture Options

Chapter 3: Metallized Memories

3.1 5.0V ROM Specifications

Description

This is a high-speed, low power ROM (SROM) with fully static and asynchronous operation and 1 read address port and 1 data output port. The number of words and word width can be configured with the MEMGEN memory compiler. ROM code is contact layer programmable.

Three ROM architectures (Types 1, 2, 4) support variable cell aspect ratios consistent with word/bit configuration limitations.

Features

- Zero standby power
- High speed
- Contact programmable ROM code
- Asynchronous and fully static operation
- Parameter-driven compiler
- Up to 36K bit block
- Variable word depth
- Variable word width
- Available architectures

  Type 1, Type 2, Type 4

Logic Symbol and Block Diagram

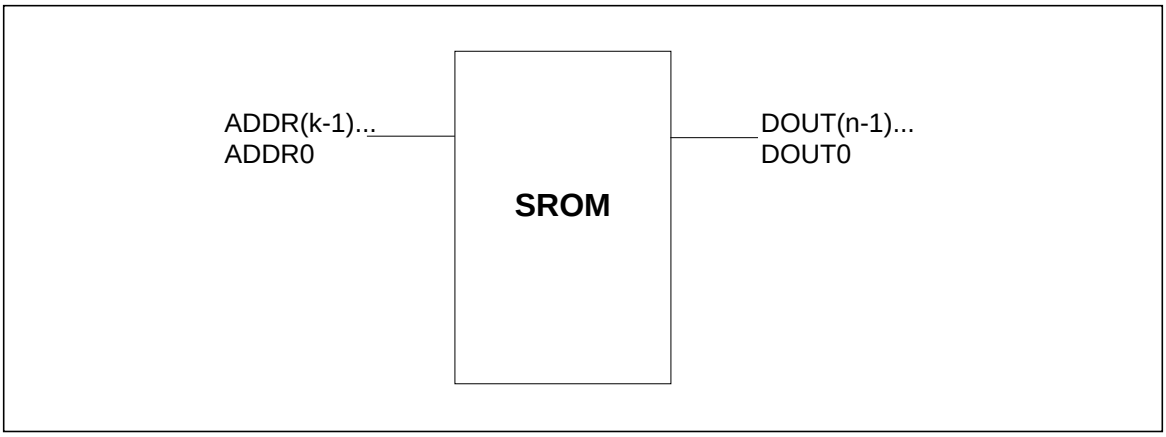


Figure 3.1: Logic Symbol for 5.0V SROM

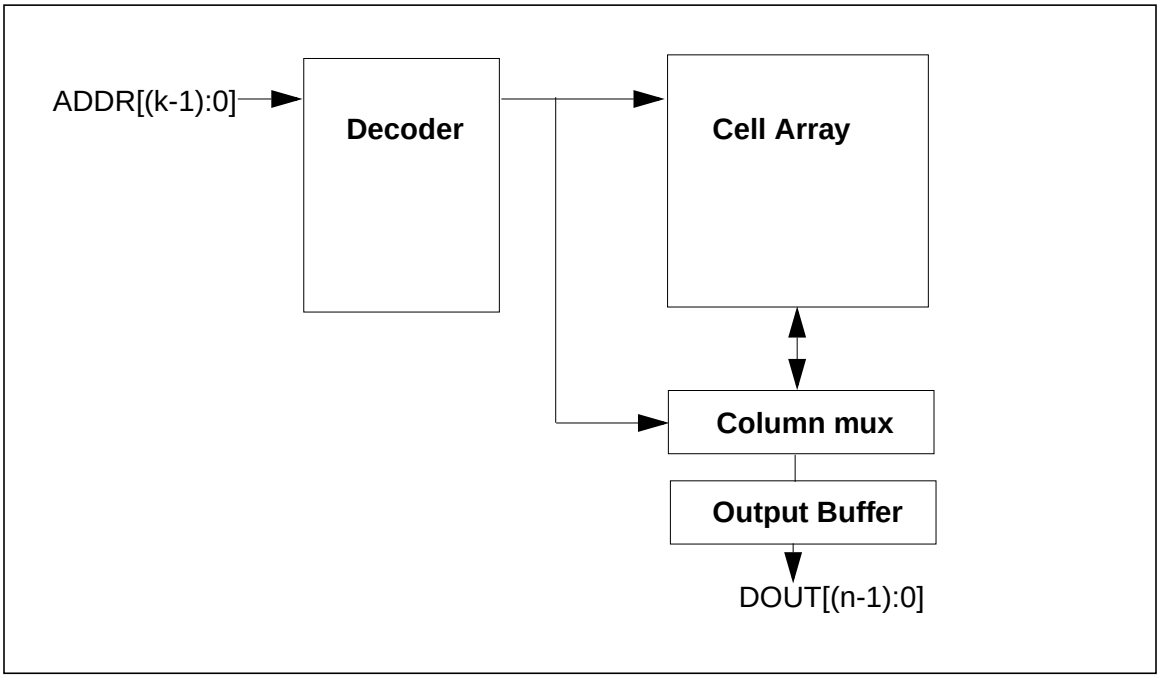


Figure 3.2: Block Diagram for 5.0V SROM

Table 3.1: 5.0V SROM I/O Pin Description

Name	I/O	Description
ADDR(k-1)...ADDR0	I	Read Address
DOU(n-1)...DOUT0	O	Output Data

Configuration and AC Parameters

Word: 8, 16, 24, 32, 40, 48, 56, 64, 80, 88, 96, 104, 112, 120, 128, 136, 144, 152, 160,168, 176,184, 192, 200, 208, 216, 224, 232, 240, 248, 256

Bit: 4, 5, 6, 7.....142, 142, 143, 144

Type : 1 = 4 - 144, 2 = 4- 72, 4 = 4 - 36

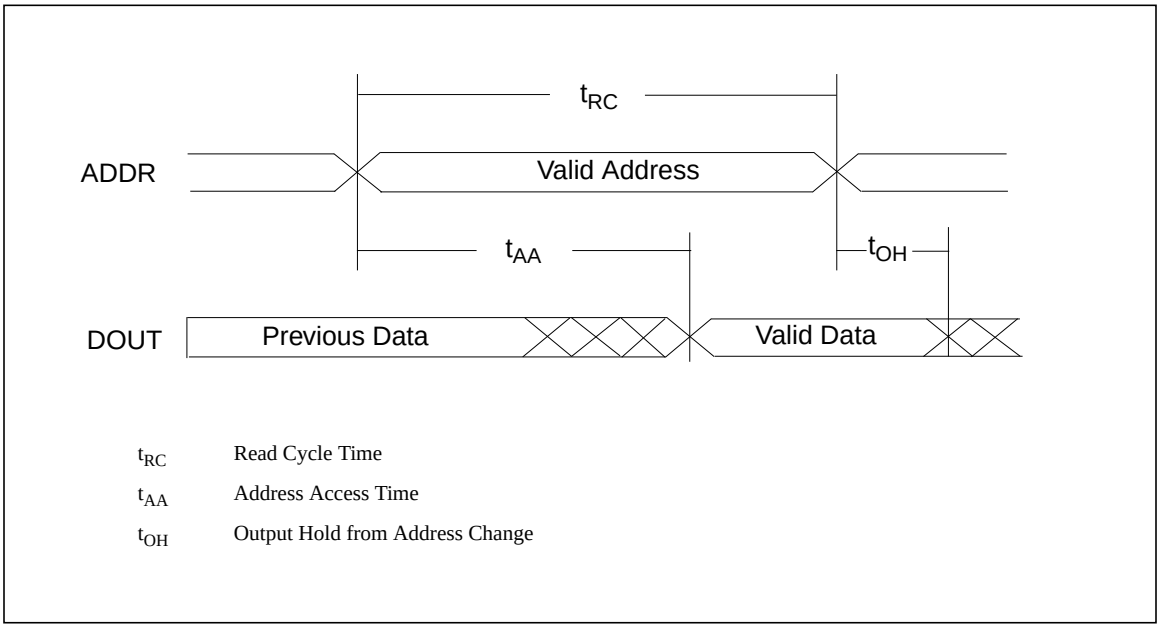
Table 3.2: 5.0V SROM Read Cycle

Parameters	Symbol
Read Cycle time	t_{RC}
Address Access time	t_{AA}
Address Output Data hold time	t_{OH}

Table 3.3: 5.0V SROM Read Cycle

Parameters	Symbol
Read Cycle time	t_{RC}
Address Access time	t_{AA}
Address Output Data hold time	t_{OH}

Timing Diagram

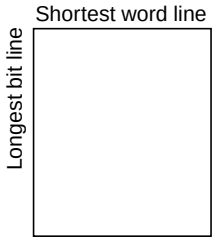


t_{RC}	Read Cycle Time
t_{AA}	Address Access Time
t_{OH}	Output Hold from Address Change

Figure 3.3: 5.0V SROM Read Cycle

Architecture

Type 1

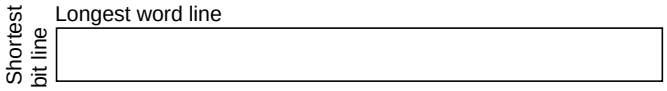


For Type 1, the specified number of words will equal the number of rows and the specified number of bits will equal the number of columns in the ROM array.

Type 2

For the same size ROM, Type 2 will have one-half the specified number of rows and twice the specified number of columns.

Type 4



For the same size ROM, Type 4 will have one-fourth the specified number of rows and four times the specified number of columns.

Figure 3.4: 5.0V SROM Architecture Options

3.2 3.3V ROM Specifications

Description

This is a low power ROM with synchronous operation. The 3.3V ROM has 1 read address port and 1 data output port and one Read Enable pin. The number of words and word width can be configured with the MEMGEN memory compiler. ROM code is contact layer programmable.

Three ROM architectures (Types 1, 2, 4) support variable cell aspect ratios consistent with word/bit configuration limitations.

Features

- Zero standby power
- High speed
- Contact programmable ROM code
- Synchronous operation
- Parameter-driven compiler
- Up to 36K bit block
- Variable word depth

  8.....256
- Variable word width

  4.....144
- Available architectures

  Type 1, Type 2, Type 4

Logic Symbol and Block Diagram

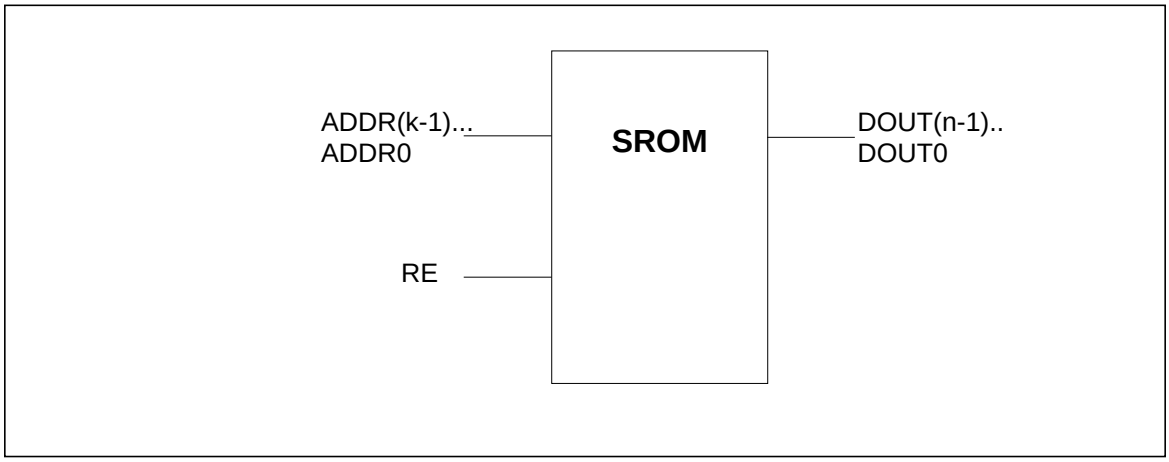


Figure 3.5: Logic Symbol for 3.3V SROM

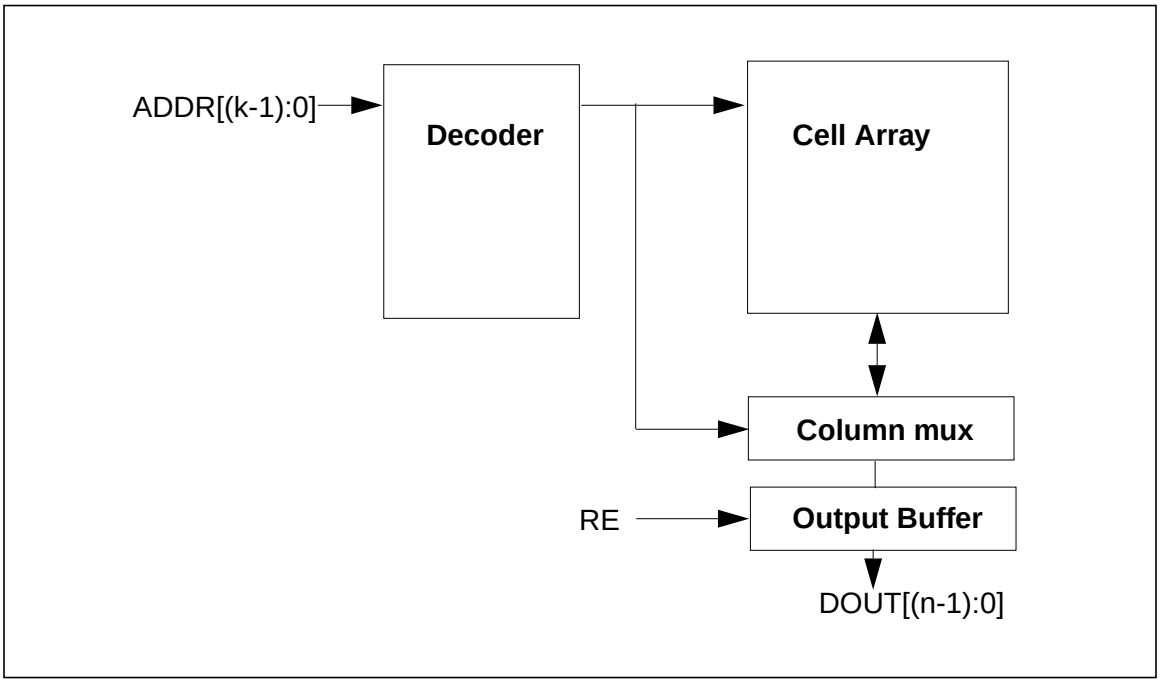


Figure 3.6: Block Diagram for 3.3V SROM

I/O Pin Description

Table 3.4: 3.3V SROM I/O Pin Description

Name	I/O	Description
ADDR(k-1)...ADDR0	I	Read Address
DOUT(n-1)...DOUT0	O	Output Data
RE	I	Read Enable

Configuration and AC Parameters

Word: 8, 16, 24, 32, 40, 48, 56, 64, 80, 88, 96, 104, 112, 120, 128, 136, 144, 152, 160,168, 176,184, 192, 200, 208, 216, 224, 232, 240, 248, 256

Bit : 4, 5, 6, 7.....142, 142, 143, 144

Type : 1 = 4 - 144, 2 = 4- 72, 4 = 4 - 36

Table 3.5: 3.3V SROM Read Cycle

Parameters	Symbol
Read Cycle time	t_{RC}
Address Access time	t_{AA}
Read Output Hold time	t_{OH}
Address Setup time	t_{AS}
Address Hold time	t_{AH}
Read Enable to Output Valid	t_{RE}

Table 3.6: 3.3V SROM Read Cycle

Parameters	Symbol
Read Cycle time	t_{RC}
Address Access time	t_{AA}
Read Output Hold time	t_{OH}
Address Setup time	t_{AS}
Address Hold time	t_{AH}
Read Enable to Output Valid	t_{RE}

Timing Diagram

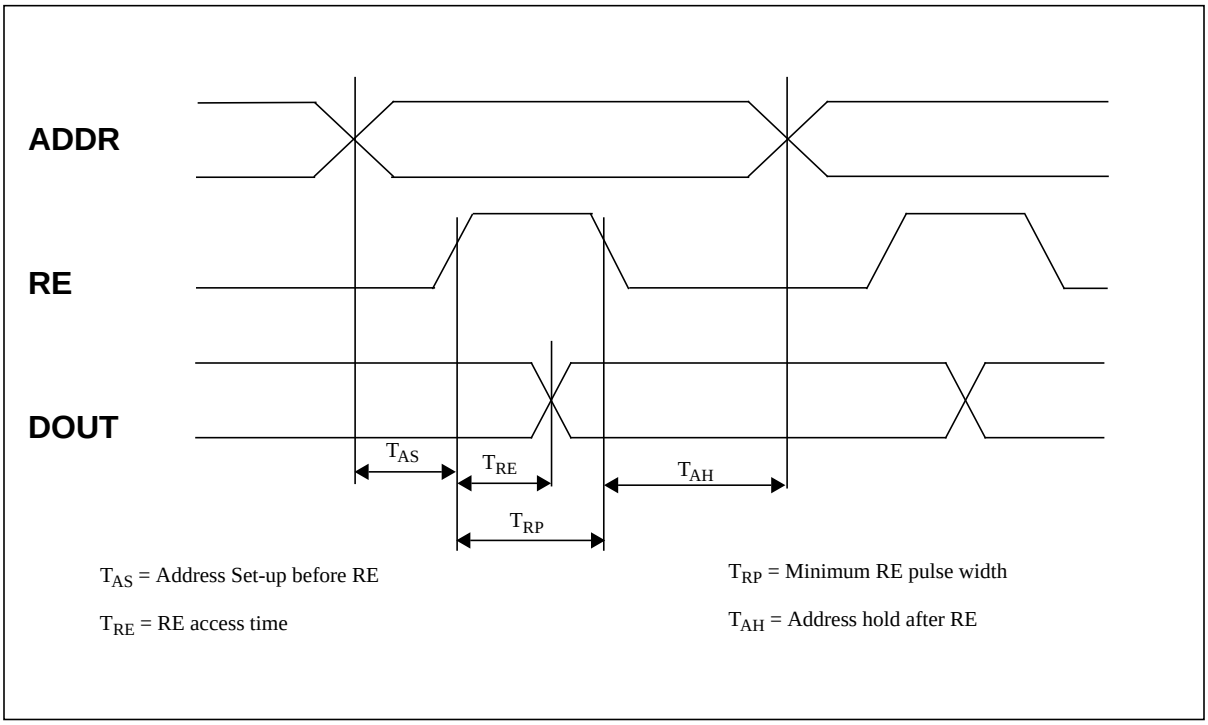
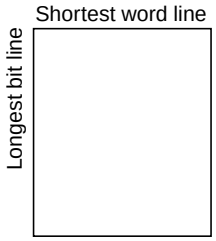


Figure 3.7: SROM RE Access Cycle (VDD = 3.3V)

Architecture

Type 1

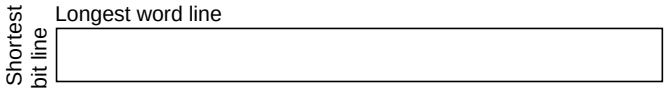


For Type 1, the specified number of words will equal the number of rows and the specified number of bits will equal the number of columns in the ROM array.

Type 2

For the same size ROM, Type 2 will have one-half the specified number of rows and twice the specified number of columns.

Type 4



For the same size ROM, Type 4 will have one-fourth the specified number of rows and four times the specified number of columns.

Figure 3.8: 3.3V SROM Architecture Options

Diffusion Memories

3.3 CADROM Specifications

Description

This is a diffusion programmable ROM (CADROM) with fully static and asynchronous operation and 1 read address port and 1 data output port. The number of words and word width can be configured with the MEMGEN memory compiler. ROM code is diffusion layer programmable.

Each data output has one OEN (output enable) pin to control it.

Features

- Zero standby power
- Diffusion programmable ROM code
- Asynchronous and fully static operation
- Parameter-driven compiler
- Up to 256K bit block
- Variable word depth
- Variable word width
- Available architectures

  Type 8

Logic Symbol and Block Diagram

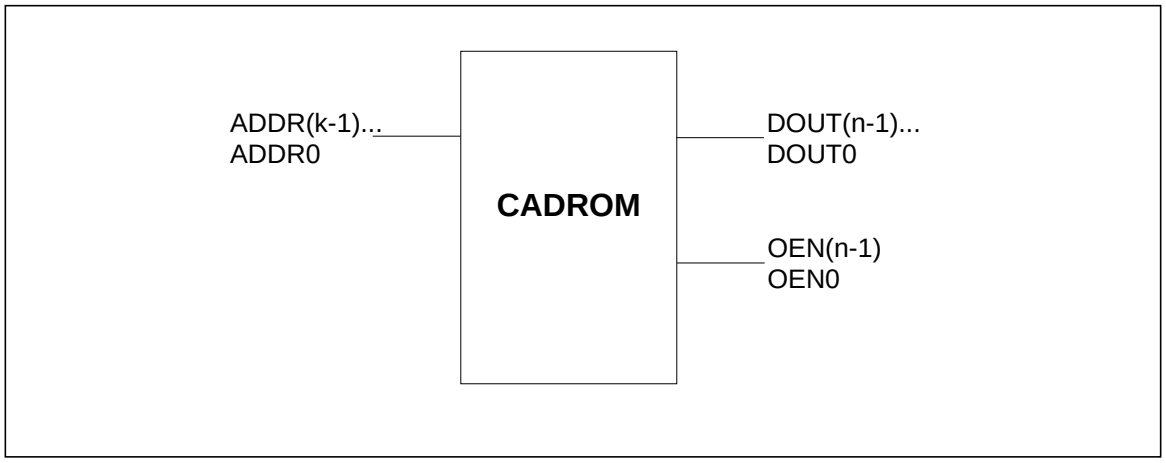


Figure 3.9: Logic Symbol for CADROM

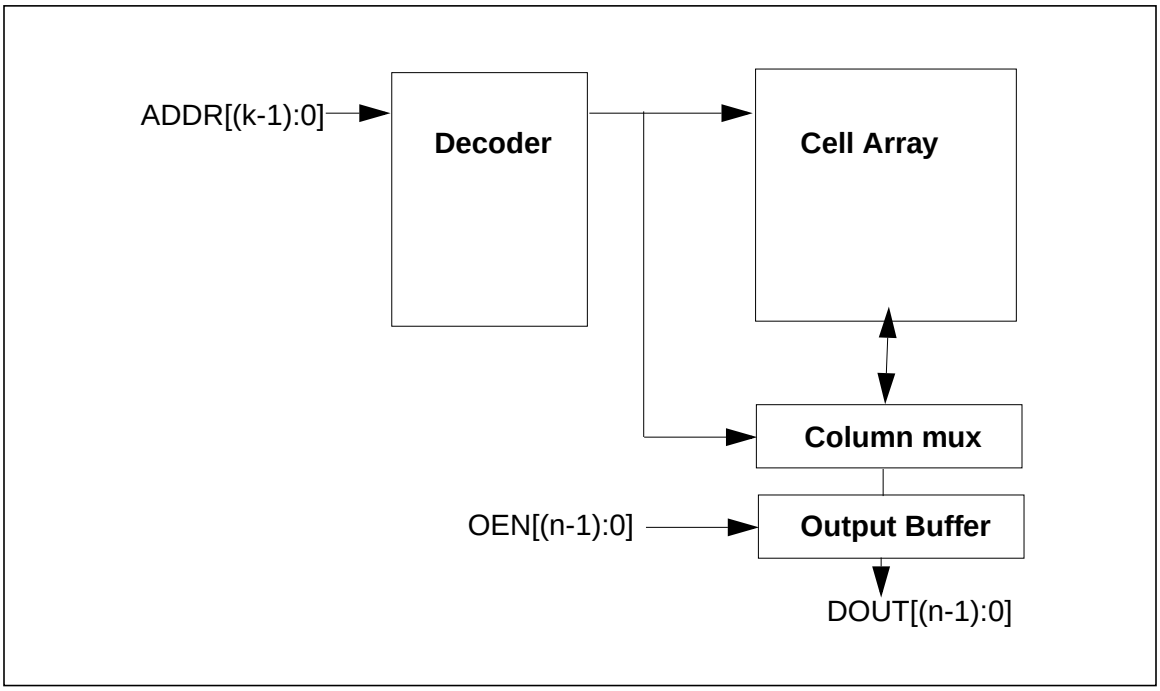


Figure 3.10: Block Diagram for CADROM

I/O Pin Description

Table 3.7: CADROM I/O Pin Description

Name	I/O	Description
ADDR(k-1)...ADDR0	I	Read Address
DOU(n-1)...DOUT0	O	Output Data
OEN(n-1)...OEN0	I	Output Enable, low active

Configuration and AC Parameters

Word: 32, 64, 96, 128, 160, 192.....4096 (increments of 32)

Bit : 2, 3, 4, 5.....64

Type : 8

Timing Diagram

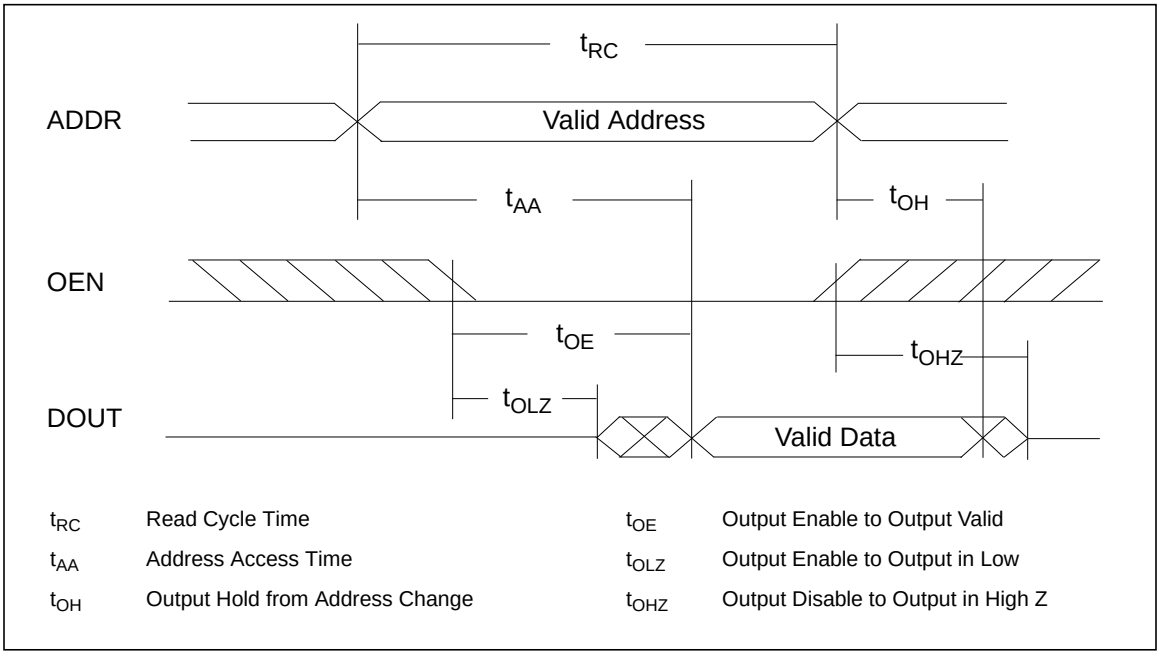


Figure 3.11: CADROM Read Cycle

Chapter 4: Full Custom Memories

Full Custom Memories, Version B

4.1 Synchronous High Density Single-Port RAM Specifications (CS1RWB)

Description

Full custom high-speed, high-density, six-transistor, single-port RAM (CS1RWB) for 0.5µm and 0.35µm technologies features synchronous operation with asynchronous output enable. The number of words and word width can be configured with the MEMGEN embedded memory compiler. The design has 1 read/write address port, 1 input data port and 1 output data port. Control pins include a separate CEN (cell enable), OEN (output enable), CK(clock) and WEN (write enable) .

Features

- Synchronous Read/Write operation
- Variable size single-port RAM with 1 read/write address port, 1 input and output data port
- Zero standby power
- 3-state output buffers
- Parameter-driven compiler
- High density: 576K bits
- Variable word depth: 32,64.....8K
- Variable word width: 2.....72
- Asynchronous output enable

I/O Pin Description

Table 4.1: CS1RWB RAM Pin Description

Name	I/O	Description
ADR(m-1:0)	I	Address port of m bits; latched at the falling edge of CK.
DI(n-1:0)	I	Data Input port of n bits; latched at the falling edge of CK.
WEN	I	Write Enable, active Low; latched at the falling edge of CK.
OEN	I	Output Enable, active Low.
CEN	I	Cell Enable, active Low.
CK	I	Clock Input
DOUT(n-1:0)	O	Data Output port of n bits wide . Outputs available at the falling edge of CK.

Configuration

Type 16 (standard)

Word: 128, 256, 512, 1024, 2048, 4096, 8192

Bit: 2 ... 72

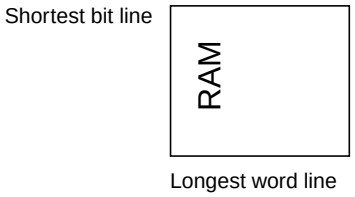
Type 4 (available on request)

Word: 32, 64, 128, 256, 512, 1024, 2048

Bit: 2 ... 72

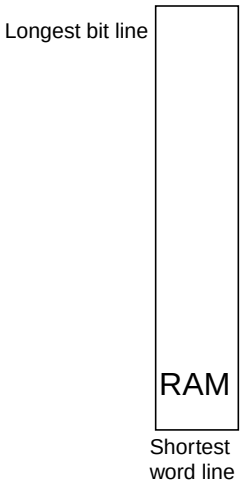
Architecture

Type 16 = 2 - 72 bits (standard)



For Type 16, the specified number of words will equal sixteen times the number of rows and the specified number of bits will equal one sixteenth of the number of columns.

Type 4 = 2 -72 bits -Type 4 (optional).



For Type 4, the specified number of words will equal four times the number of rows and the specified number of bits will equal one quarter of the number of columns in the RAM array.

Figure 4.1: Synchronous High-Density Single-Port RAM (CS1RWB) Architecture Options

Logic Symbol

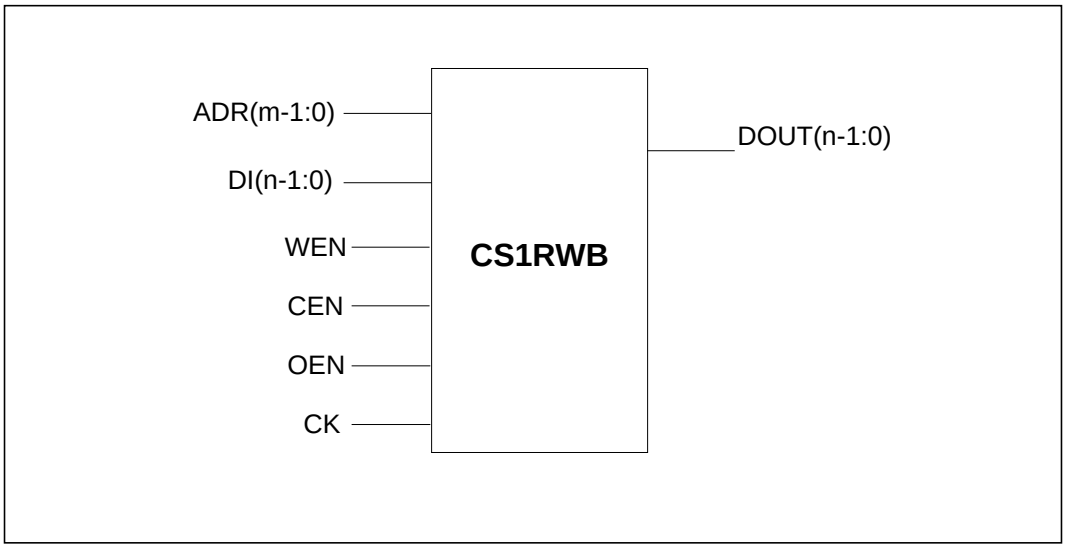


Figure 4.2: Logic Symbol for CS1RWB RAM

Timing Diagrams

Read Cycle

Outputs are valid for access time (t_{KNQ}) after the clock goes LOW; they remain latched until more data are read or written.

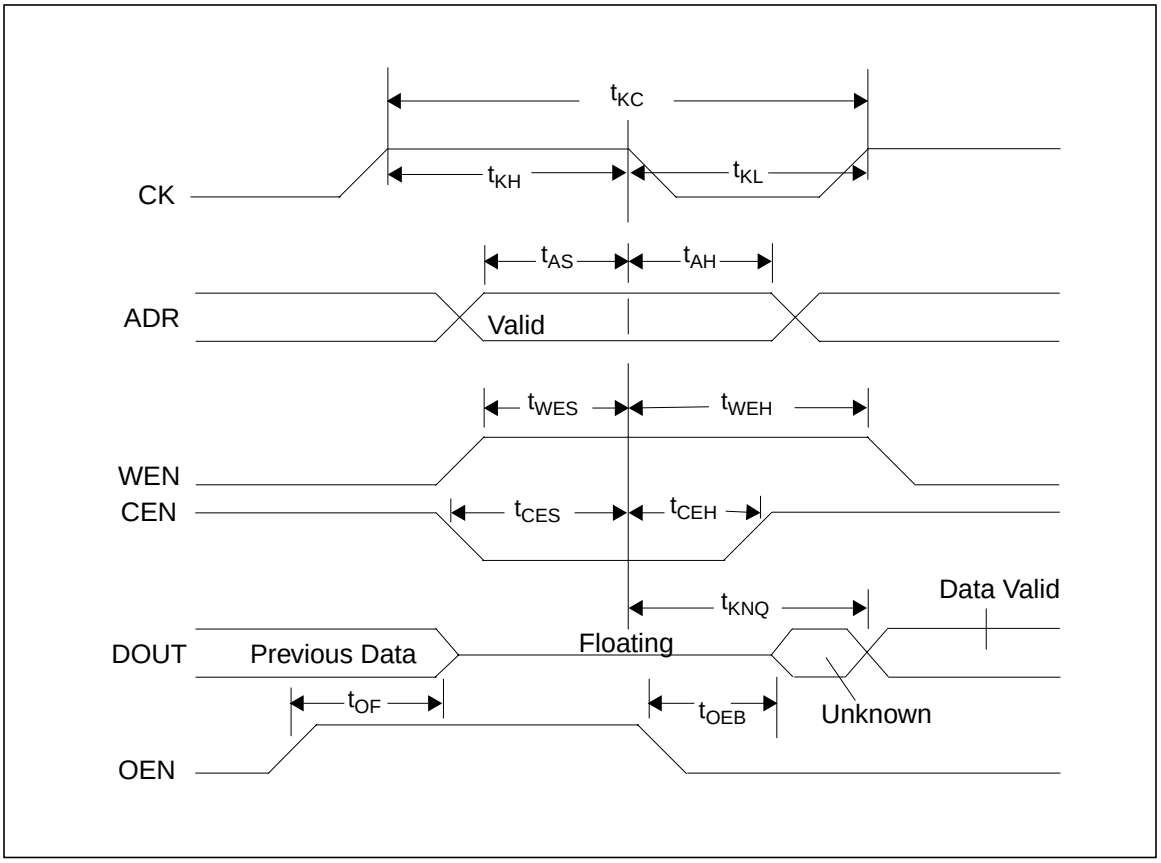


Figure 4.3: CS1RWB RAM Read Cycle

Write Cycle

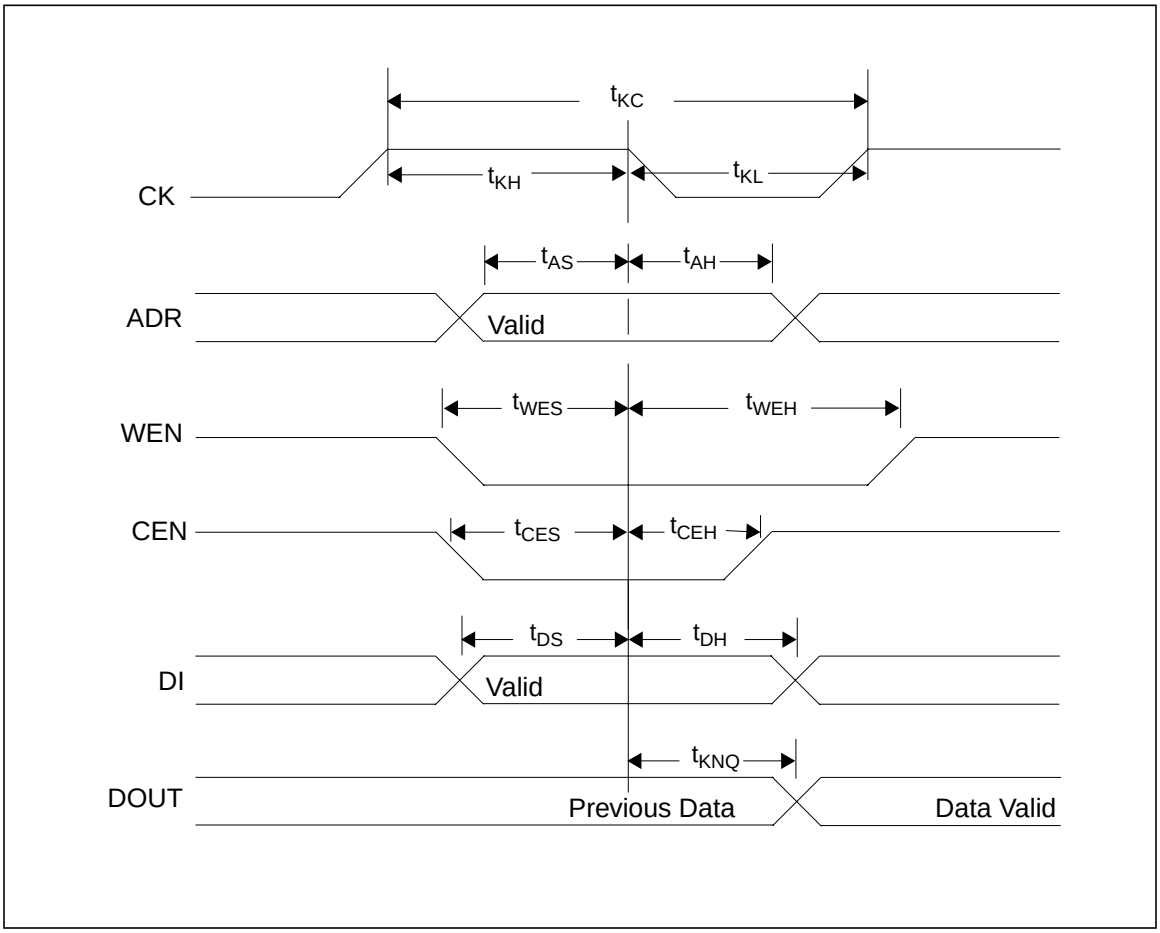


Figure 4.4: CS1RWB RAM Write Cycle

Block Diagram

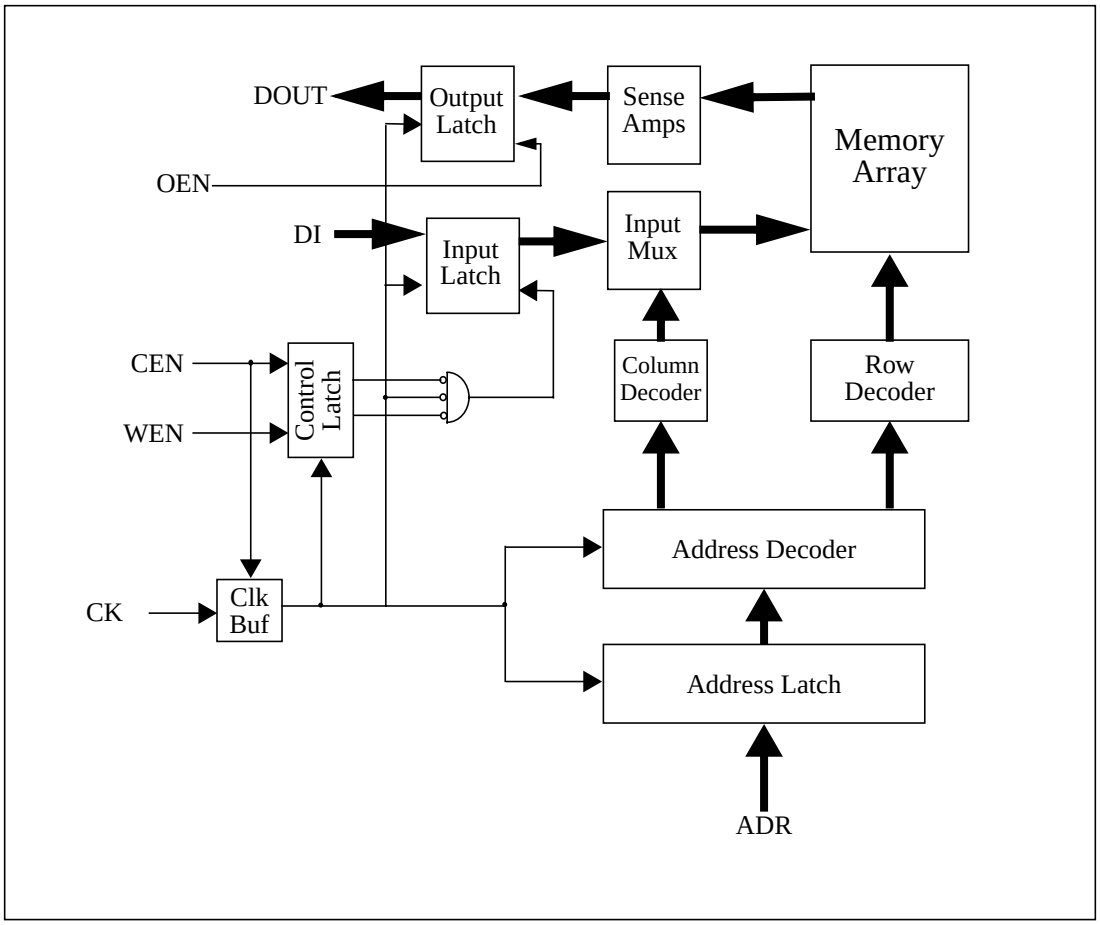


Figure 4.5: Block Diagram for CS1RWB RAM

4.2 Synchronous High-Density Dual-Port RAM Specifications (CS2RWB)

Description

Full custom high-speed, high-density, eight-transistor, dual-port RAM (CS2RWB) for 0.5µm and 0.35µm technologies. It features synchronous operation with asynchronous output enable. The number of words and word width can be configured with the MEMGEN embedded memory compiler. The design has 2 read/write address ports, 2 input data ports and 2 output data ports. Control pins include a separate CEAN, CEBN(cell enable), OEAN, OEBN (output enable), CKA, CKB(clock) and WEAN, WEBN(write enable) for each port.

Features

- Synchronous Read/Write operation
- Variable size dual-port RAM with 2 read/write address ports, 2 input and 2 output data ports
- Zero standby power
- 3-state output buffers
- Parameter-driven compiler
- High density: 576K bits
- Variable word depth: 64.....8K
- Variable word width: 2.....72
- Asynchronous output enable

I/O Pin Description

Table 4.2: CS2RWB RAM Pin Description

Name	I/O	Description
AADR(m-1:0)	I	A port Address of m bits; latched at the falling edge of CKA
DIA(n-1:0)	I	A port Data Inputs of n bits; latched at the falling edge of CKA.
WEAN	I	A port Write Enable, active Low; latched at the falling edge of CKA.
OEAN	I	A port Output Enable, active Low.
CEAN	I	A port Cell Enable, active Low
CKA	I	A port Clock Input
BADR(m-1:0)	I	B port Address of m bits; latched at the falling edge of CKB.
DIB(n-1:0)	I	B port Data Inputs of n bits; latched at the falling edge of CKB.
WEBN	I	B port Write Enable, active Low; latched at the falling edge of CKB.
OEBN	I	B port Output Enable, active Low.
CEBN	I	B port Cell Enable, active Low.
CKB	I	B port Clock Input.
DOA(n-1:0)	O	A port Data Outputs of n bits wide
DOB(n-1:0)	O	B port Data Outputs of n bits wide

Configuration

Type 16 (standard)

Word: 256, 512, 1024, 2048, 4096, 8192

Bit: 2 ... 72

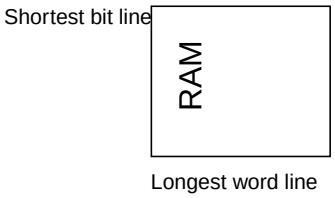
Type 4 (optional)

Word: 64, 128, 256, 512, 1024, 2048

Bit: 2 ... 72

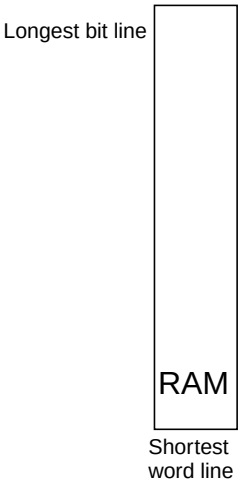
Architecture

Type 16 = 2 - 72 bits (standard)



For Type 16, the specified number of words will equal sixteen times the number of rows and the specified number of bits will equal one sixteenth of the number of columns.

Type 4 = 2 -72 bits -Type 4 (optional).



For Type 4, the specified number of words will equal four times the number of rows and the specified number of bits will equal one quarter of the number of columns in the RAM array.

Figure 4.6: Synchronous High Density Dual Port RAM (CS2RWB) Architecture Options

Logic Symbol

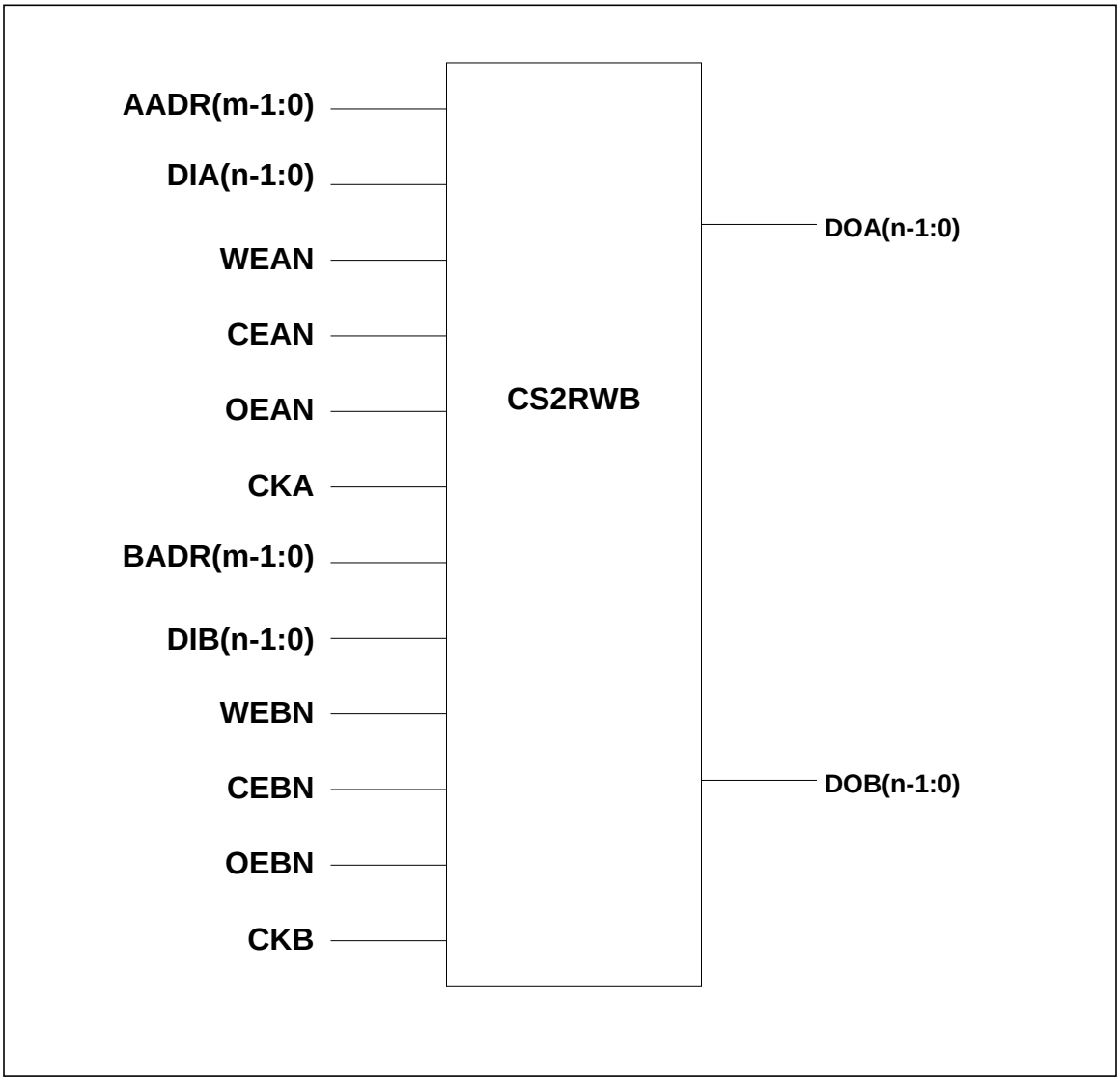


Figure 4.7: Logic Symbol for CS2RWB RAM

Timing Diagrams

Read Cycle

Outputs are valid for access time (t_{KNQ}) after the clock goes LOW; they remain latched until more data are read or written.

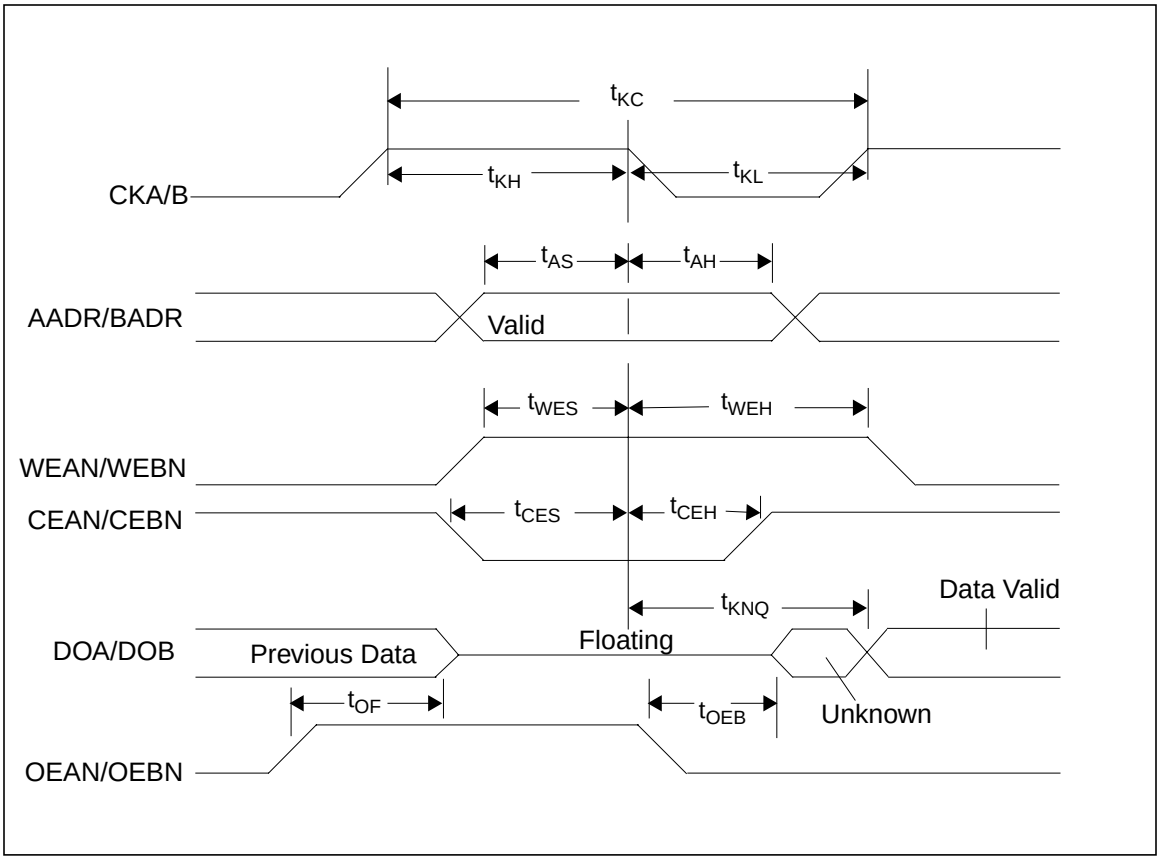


Figure 4.8: CS2RWB RAM Read Cycle

Write Cycle

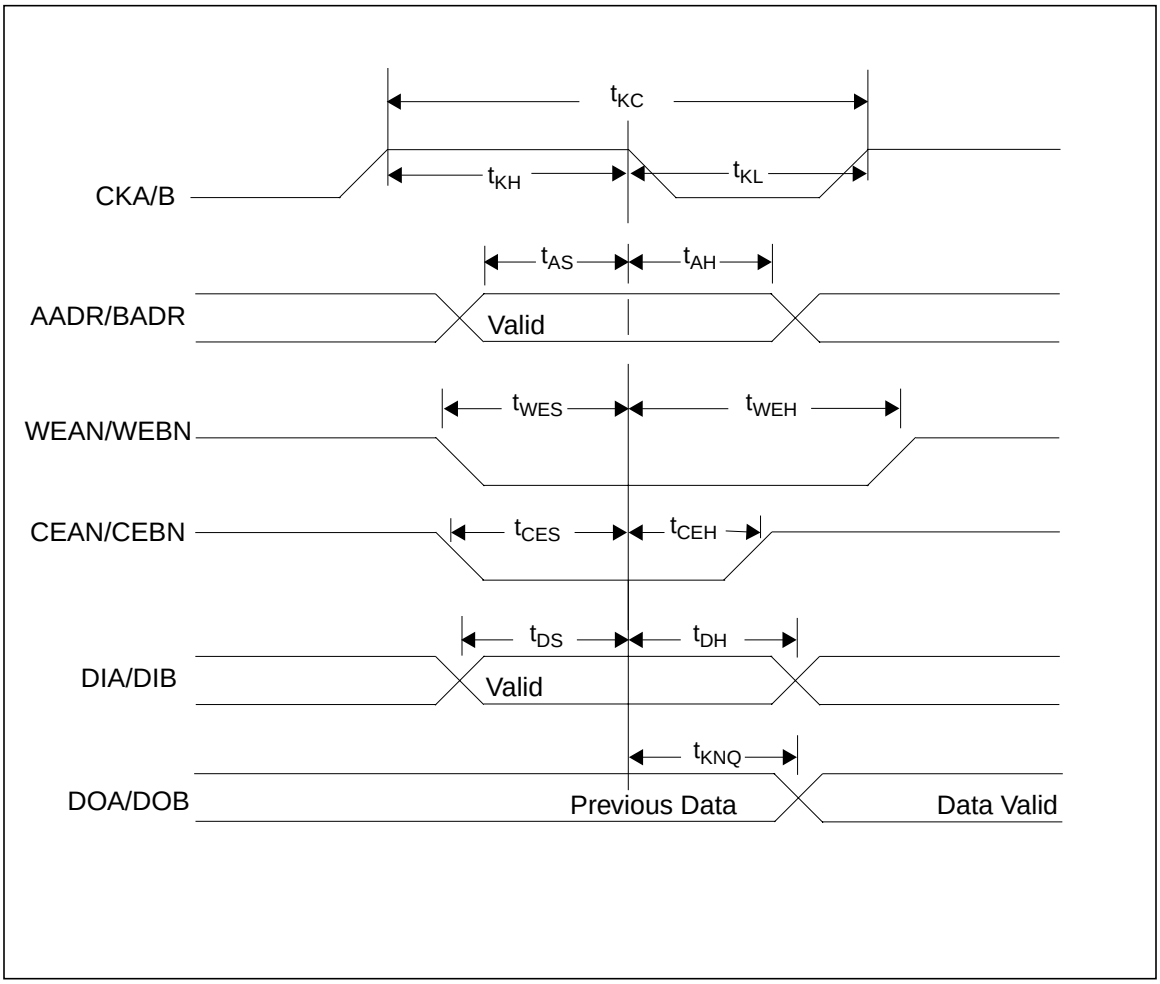


Figure 4.9: CS2RWB RAM Write Cycle

Block Diagram

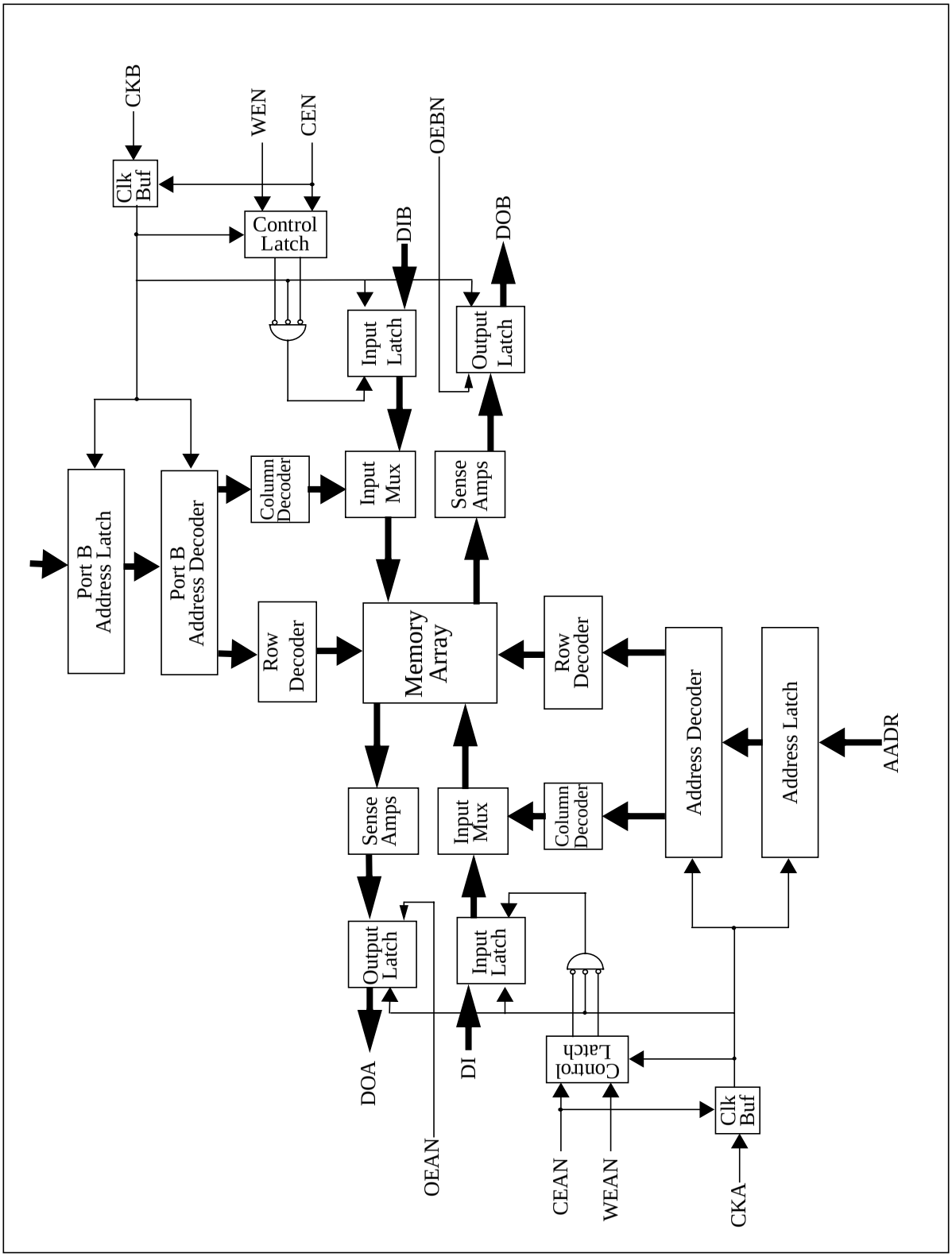


Figure 4.10: Block Diagram for CS2RWB RAM

Full Custom Memories, Version D

4.3 Synchronous High Density Single-Port SRAM Specifications (CS1RWD)

Description

Full custom high-speed, high-density, six-transistor, single-port RAM (CS1RWD) for 0.25µm technology. It features synchronous operation with asynchronous output enable. The number of words and word width can be configured with the MEMGEN embedded memory compiler. The design has 1 read/write address port, 1 input data port, and 1 output data port. Control pins include a separate CEN(cell enable), GOEN(global output enable), CK (clock) and GWEN (global write enable) .

Features

- Synchronous Read/Write Operation
- Positive Edge Triggered
- 1 Read/Write Address Port
- 1 I/P and 1 O/P Data Port
- Completely Static Appearance:
    - Low Voltage Data Retention to 1.2V
    - Operation Down to 0 Hz
    - Zero Standby Current
    - Automatic Power Down
- 3-State or Totem-Pole Output Buffer
- Maximum Memory Size
    - 576K Bits Total
    - 72 Bit Word Width Maximum
    - 8,192 Word Depth (Type 16)—Standard
    - 2,048 Word Depth (Type 4)—Optional
- Asynchronous Output Enable
- Ability to Compile to Variable Word Depth
- Ability to Compile to Variable Word Width
- Ability to Perform Bit-wise Masked Read and Write
- User Selectable Write Feed Through Mode

Functional Description

The memory supports standby mode to reduce power during non-operation. The standby mode is active when CEN is high. During this mode, both read and write are disabled, the data previously stored in the memory is retained, and any 3-state outputs are disabled. The Test Mode, TMN, and Shift Mode, SMN, override the standby mode.

Write operation is enabled when the GWEN, WEN(n -1:0), and CEN signals are low. The data on the input data bus DI(n -1:0) is written into the memory location specified by address ADR(m -1:0).

Read operation is enabled when GWEN and WEN(n -1:0) are high and CEN is low. The data appears on the output data bus DOUT(n - 1:0) as read from the specified address ADR(m - 1:0).

Where applicable, the output data DOUT(n - 1:0) will go to high-impedance state when the output enables GOEN or OEN(n - 1:0) are high, or CEN is high.

Note: In the above description, n is the number of inputs or outputs, and m is the number of addresses where 2^m equals the number of addressable words.

Table 4.3: CS1RWD Mode Table

GWEN	WEN (n-1:0)	CEN	TMN	TGWEN	TCEN	SMN	MODE
L	L	L	H	X	X	H	Write
H	H	L	H	X	X	H	Read
L	H	L	H	X	X	H	No-op
H	L	L	H	X	X	H	No-op
X	X	H	H	X	X	H	Standby
X	X	X	L	L	L	H	Test write
X	X	X	L	H	L	H	Test read
X	X	X	L	X	H	H	Test No-op
X	X	X	H	X	X	L	Shift

Other Features

- Output Buffers

The SRAM leaf cells include a selection of output drivers. Two types of output buffers are available: 3-state and totem-pole. The 3-state output buffers have two drive strengths. One drive strength is suitable to drive 1.0pF loads at F_{MAX}, while the other drive strength is suitable to drive 0.5pF loads at F_{MAX}. The totem-pole output buffers have a drive strength suitable to drive 0.25pF loads at F_{MAX}.

- Testability

The design is able to support limited scan and testability features, with a minimal amount of overhead built in. Multiplexers are added to the address, global write enable, and component enable inputs to facilitate driving the memory array from external shift registers. The data input and data output signals include scannable registers.

The following pins are added to each port to support these features:

1) Test mode, TMN, forces the input multiplexers to accept inputs from the alternate source. Assertion of test mode deactivates the functions of all local write enables, the component enable, and the standby mode.
2) Test address inputs TADR (m - 1:0) are the alternate address source. TGWEN and TCEN are the alternate global write enable and component enable sources, respectively.
3) Shift mode, SMN, disables read and write, and it causes the scan registers to shift.
4) Shift in and shift out, SI and SO, supply the input data and produce the output data from the scan register chain, which consists of the data input and data output scan registers.

- Scan Chain

The length of the internal scan chain is two times the word width of the memory. The internal serial scan chain starts with the DI[MSB] to the DOUT [MSB] and ends with the DI [LSB] to the DOUT [LSB].

The following diagram illustrates the internal scan chain circuit order for a 2-bit wide memory (when the device is in shift mode (when SMN is low)):

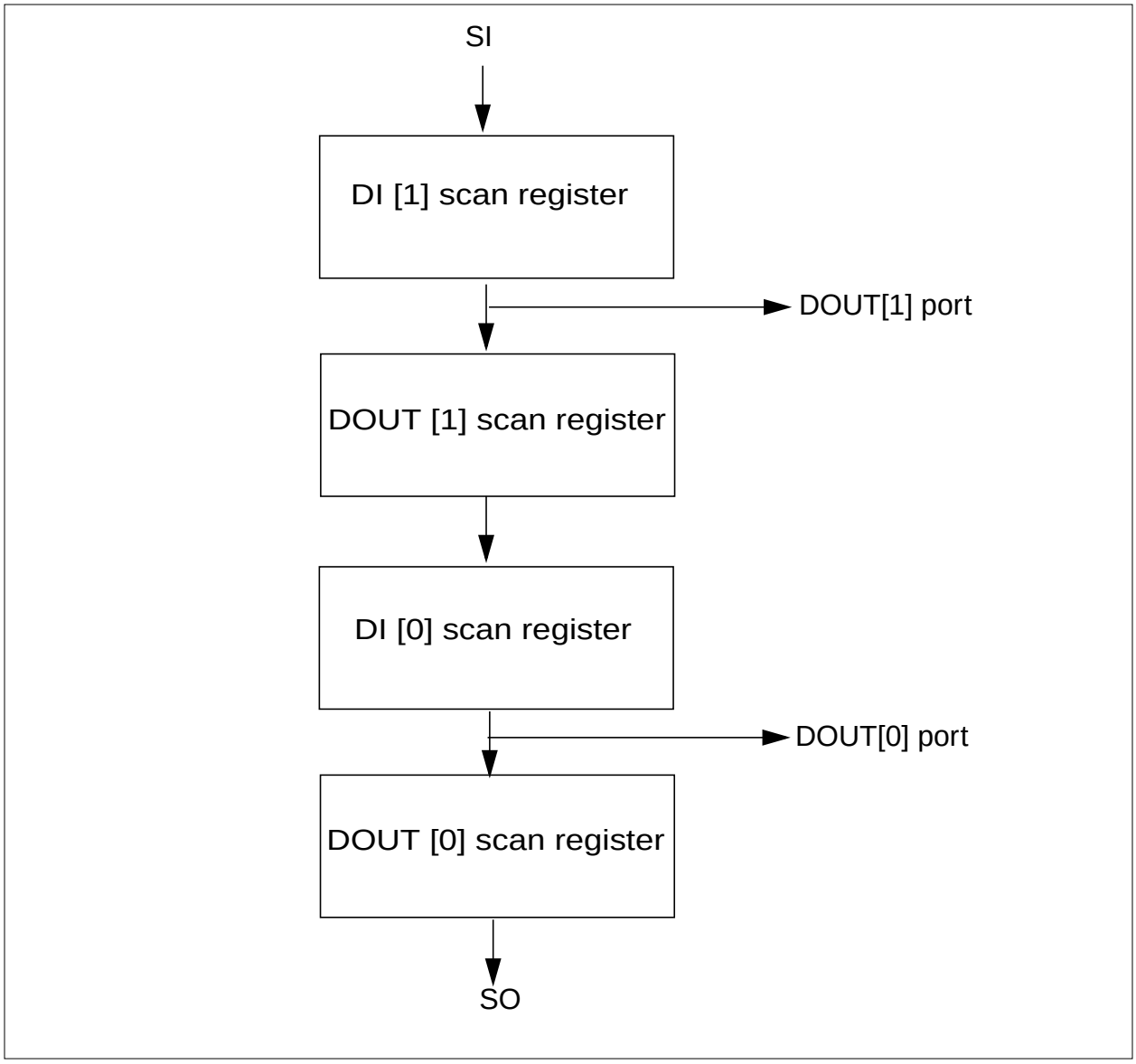


Figure 4.11: Internal Scan Chain Circuit Order

Based on the repetitive sequence of serial data shifting from an input scan register to an outpput scan register, valid input scan data is shifted in and latched at every other clock cycle (the in-between clock cycles contain arbitrary data). Likewise, for the sequential shift of output scan data, the valid output data is at every other clock cycle.

I/O Pin Description

Table 4.4: CS1RWD RAM Pin Description

Name	I/O	Description
ADR(m -1:0)	I	Address bits; latched at the rising edge of CK when TMN is high.
TADR(m -1:0)	I	External test Address bits, latched at the rising edge of CK when TMN is low.
TMN	I	Test Mode, active low, selects TADR, TGWEN, and TCEN sources.
SMN	I	Shift Mode, active low, enables scanning data for DI and DOUT, and disables reads and writes.
SI	I	Shift In, data input for shift register chain.
DI (n -1:0)	I	Data In bits, latched at the rising edge of CK.
GWEN	I	Global Write Enable Active Low, latched at the rising edge of CK.
TGWEN	I	Test Global Write Enable Active Low, latched at the rising edge of CK, alternate GWEN source.
WEN (n -1:0)	I	Local Write Enable for each bit, Active Low for Write and High for Read.
OEN (n -1:0)	I	Local Output Enable for each bit, Active Low
GOEN	I	Global Output Enable Active Low
CEN	I	SRAM Component Enable, Active Low
TCEN	I	SRAM Component Enable, Active Low, alternate CEN source
CK	I	Clock Input
WFTN	I	Write Feed Through Enable, active low, overides local WEN functionality. This is a static mode pin.
DOUT (n -1:0)	O	Data Output Ports, always available, updated following the rising edge of CK.
SO	O	Shift Out, data output from shift register chain

Configuration

Type 16 (standard)

Word: 128, 256, 384, 512, (increments of 128)... 8192

Bit: 1 ... 72

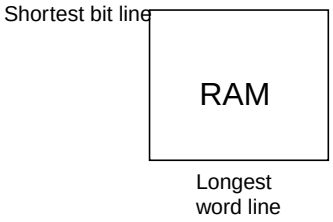
Type 4 (optional)

Word: 32, 64, 96, 128, (increments of 32) ...2048

Bit: 1 ... 72

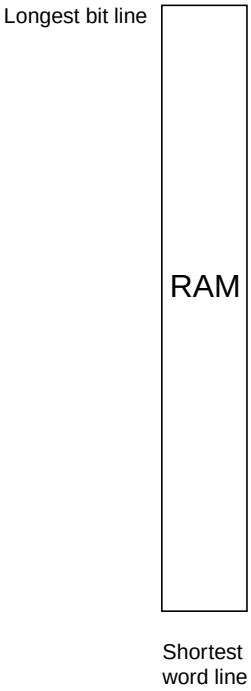
Architecture

Type 16 = 1- 72 bits (standard)



For Type 16, the specified number of words will equal sixteen times the number of rows and the specified number of bits will equal one sixteenth of the number of columns.

Type 4 = 1-72 bits (optional)



For Type 4, the specified number of words will equal four times the number of rows and the specified number of bits will equal one quarter of the number of columns in the RAM array.

Figure 4.12: Synchronous High-Density Single-Port RAM (CS1RWD) Architectures

Logic Symbol

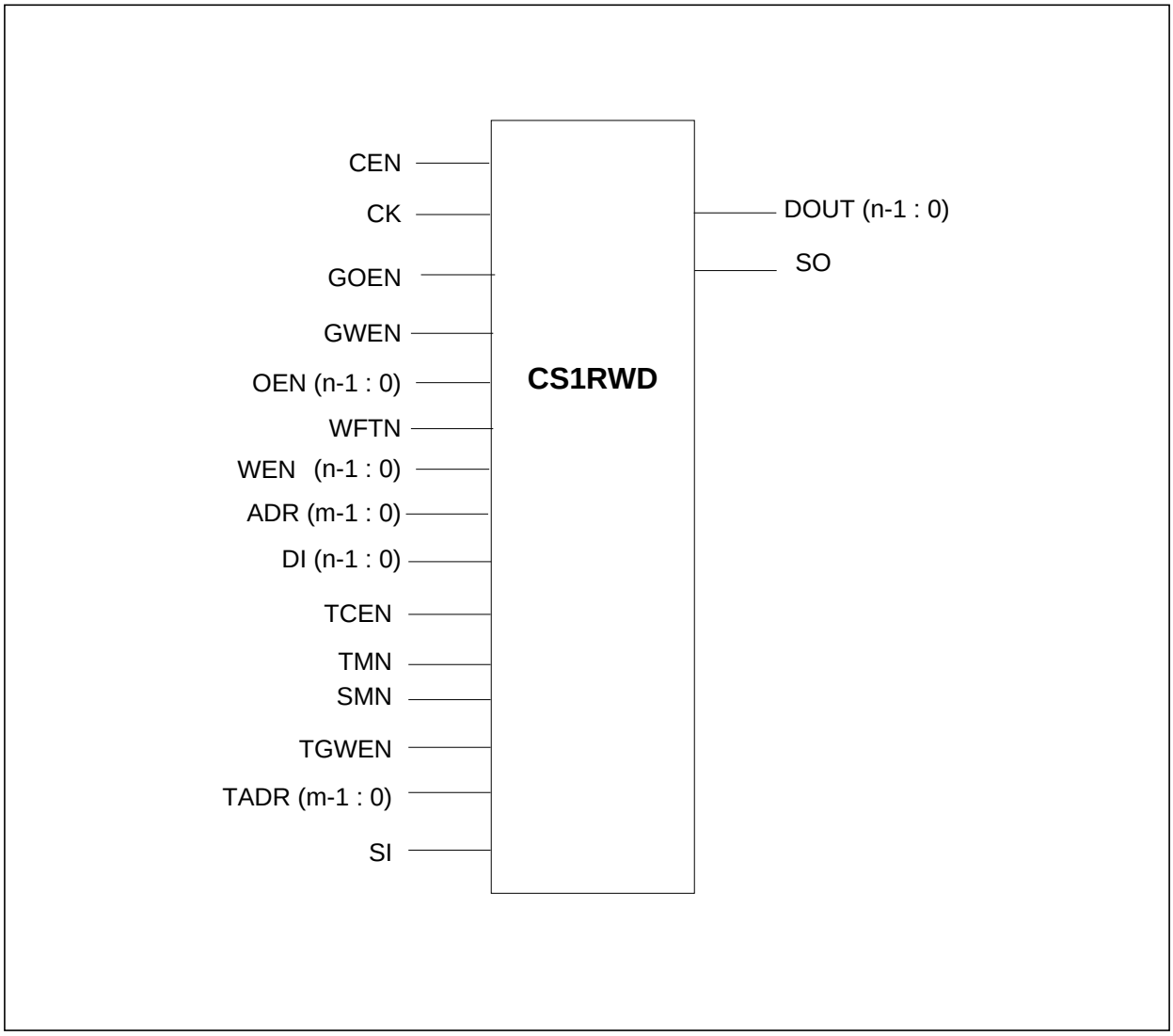


Figure 4.13: Logic Symbol for CS1RWD RAM

Timing Diagrams

Read Cycle

Outputs are valid for access time (t_{KNQ}) after the clock goes HIGH; they remain latched until more data are read or written.

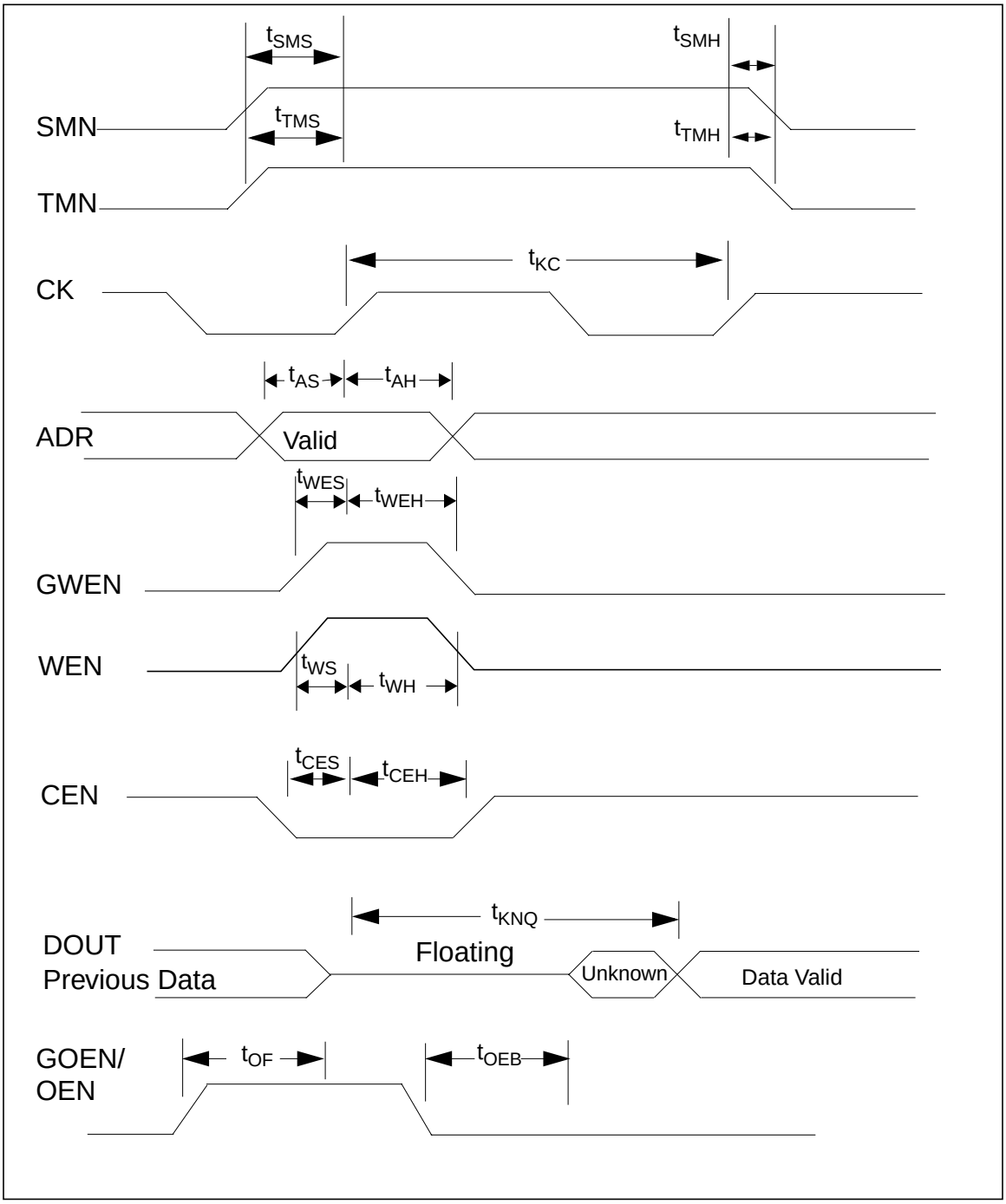


Figure 4.14: CS1RWD RAM Read Cycle

Write Cycle

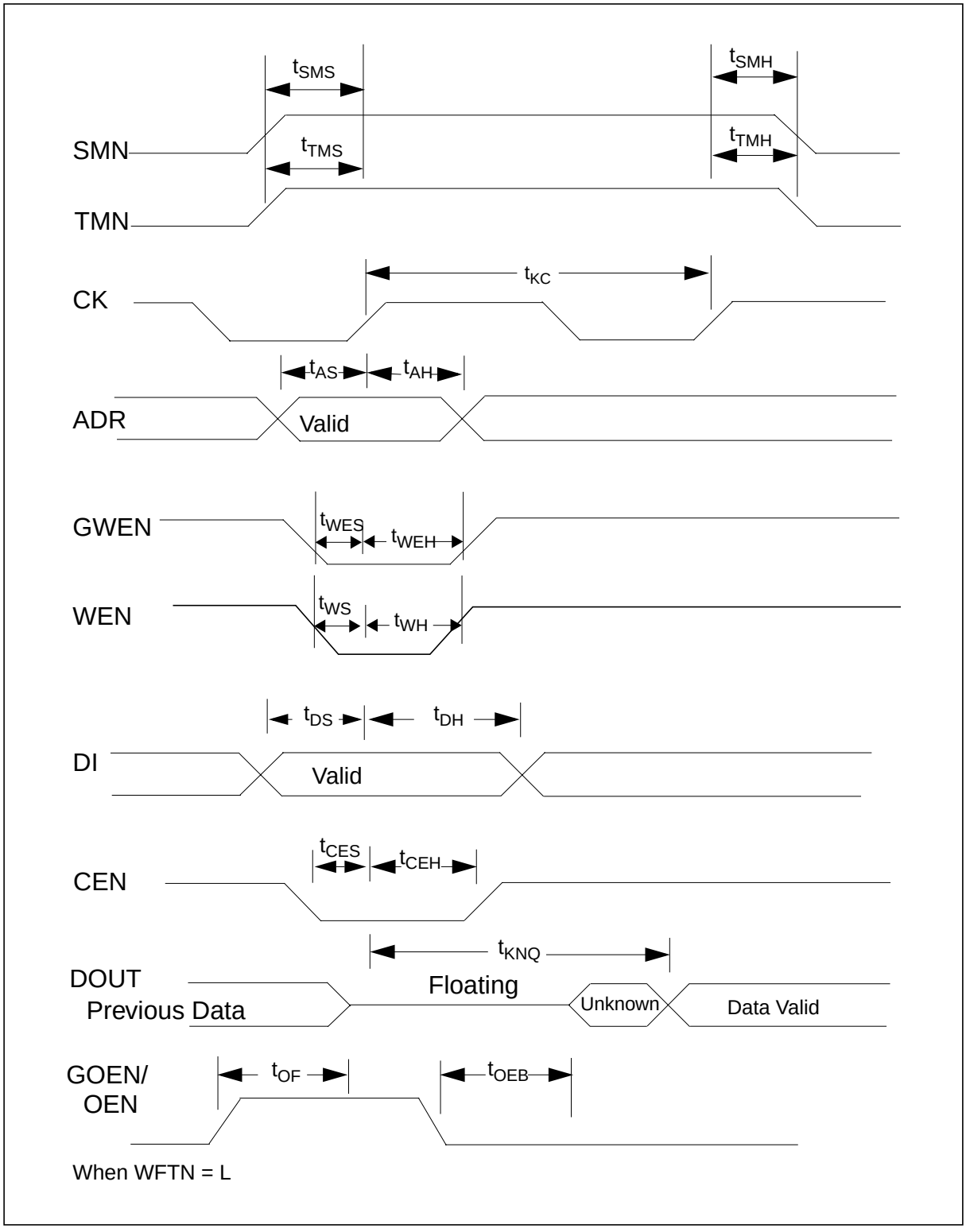


Figure 4.15: CS1RWD RAM Write Cycle

Block Diagram

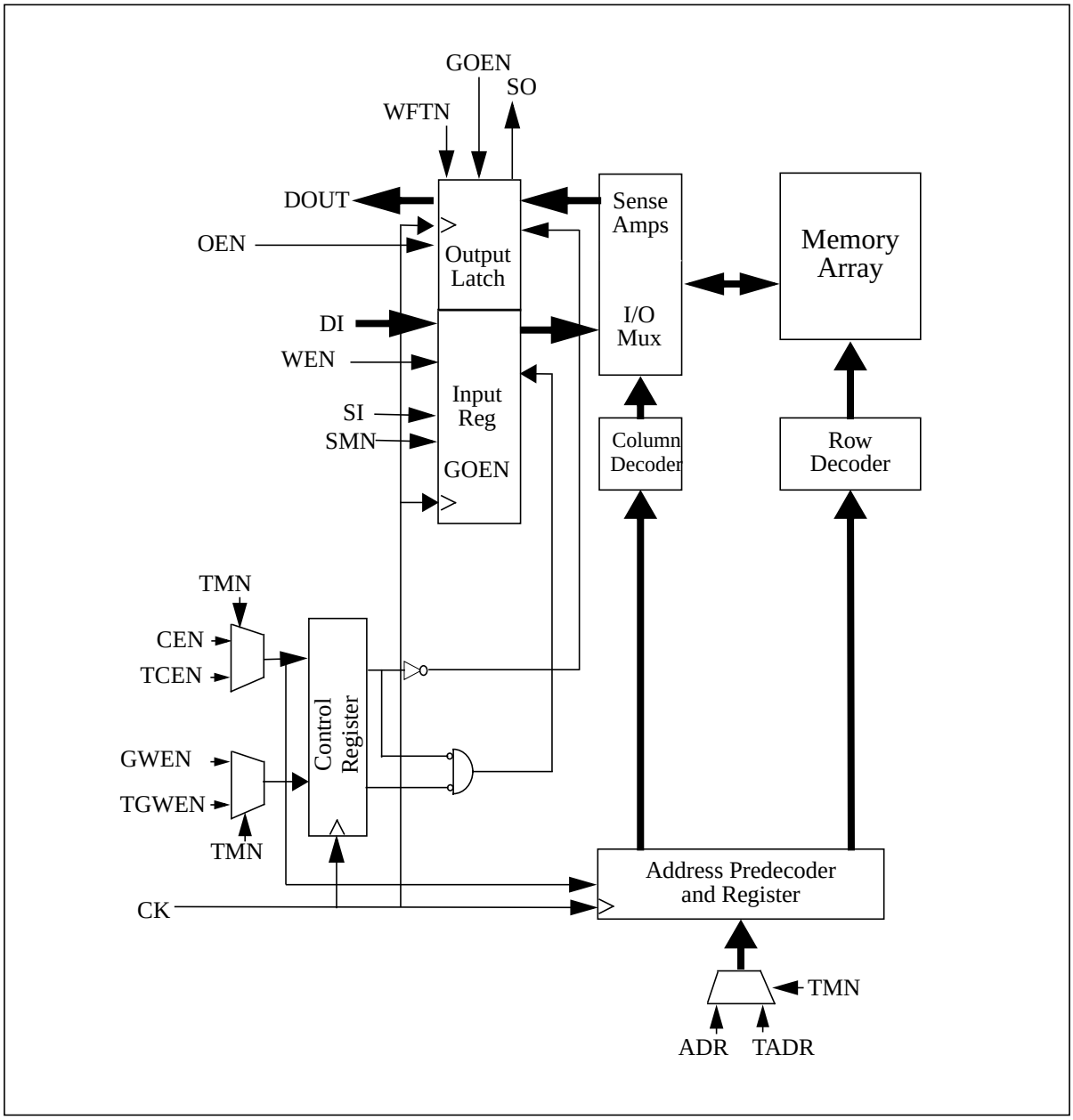


Figure 4.16: Block Diagram for CS1RWD RAM

4.4 Synchronous High-Density Dual-Port RAM Specifications (CS2RWD)

Description

Full custom high-speed, high-density, eight-transistor, dual-port RAM (CS2RWD) for 0.25µm tecnology features synchronous operation with asynchronous output enable. The number of words and word width can be configured with the MEMGEN embedded memory compiler. The design has 2 read/write address ports, 2 input data ports and 2 output data ports. Control pins include a separate CEAN, CEBN (cell enable), GOEAN, GOEBN (global output enable), CKA, CKB (clock) and GWEAN,GWEBN (write enable) for each port.

Features

- Synchronous Read/Write operation
- Positive Edge Triggered
- 2 Read/Write Address Port
- 2 I/P and 2 O/P Data Port
- Completely Static Appearance:
    - Low Voltage Data Retention to 1.2V
    - Operation Down to 0 Hz
    - Zero Standby Current
    - Automatic Power Down
- 3-state or totem-pole Output Buffer
- Maximum Memory Size
    - 576K Bits Total
    - 72 Bit Word Width Maximum
    - 8,192 Word Depth (Type 16) —Standard
    - 2,048 Word Depth (Type 4) —Optional
- Asynchronous Output Enable
- Ability to Compile to Variable Word Depth
- Ability to Compile to Variable Word Width
- Ability to Perform Bit-wise Masked Read and Write
- User Selectable Write Feed Through Mode
- Port A size equals Port B size
- No write through from Port A to Port B

Functional Description and Additional Features

See the sections beginning at “Functional Description” on page 4-17. Information within these sections are to be interpreted under a per port basis with respect to the CS2RWD dual-port RAM.

I/O Pin Description

Table 4.5: CS2RWD RAM Pin Description

Name	I/O	Description
AADR (m -1:0)	I	Port-A Address bits; latched at the rising edge of CKA when TMAN is high.
TAADR (m -1:0)	I	Port-A External test Address bits, latched at the rising edge of CKA when TMAN is low.
TMAN	I	Port-A Test Mode; active low, selects TAADR, TGWEAN, and TCEAN sources.
SMAN	I	Port-A Shift Mode, active low, enables scanning data for DIA and DOA, and disables reads and writes for Port-A.
SIA	I	Port-A Shift In, data input for Port-A shift register chain.
DIA (n -1:0)	I	Port-A Data In bits; latched at the rising edge of CKA.
WEAN(n -1:0)	I	Local Port-A Write Enable for each bit, active Low for Write, and High for Read.
GWEAN	I	Global Port-A Write Enable Active Low, latched at the rising edge of CKA.
TGWEAN	I	Port-A Test Global Write Enable Active Low, latched at the rising edge of CKA, alternate GWEAN source.
OEAN (n -1:0)	I	Local Port-A Output Enable for each bit, Active Low.
GOEAN	I	Global Port-A Output Enable, Active Low.
CEAN	I	Port-A Cell Enable, Active Low.
TCEAN	I	Port-A Test Component Enable Active Low, alternate CEAN source.
CKA	I	Port-A Clock Input.
WFTAN	I	Port-A Write Feed Through Enable, active low, overrides local WEAN functionality. This is a static mode pin.
DOA (n -1:0)	O	Data Output Port-A, always available, updated following the rising edge of CK.
SOA	O	Port-A Shift Out, data output from shift register chain.

Table 4.6: CS2RWD RAM Pin Description Continued

Name	I/O	Description
BADR (m -1:0)	I	Port-B Address bits; latched at the rising edge of CKA.
TBADR (m -1:0)	I	Port-B External test Address bits, latched at the rising edge of CKA when TMAN is low.
TMBN	I	Port-B Shift Mode; active low, selects TAADR, TGWEBN, and TCEBN sources.
SMBN	I	Port-B Shift Mode, active low, enables scanning data for DIA and DOA, and disables reads and writes for Port-B.
SIB	I	Port-B Shift In, data input for Port-B shift register chain.
DIB (n -1:0)	I	Port-B Data In bits; latched at the rising edge of CKA.
WEBN(n -1:0)	I	Local Port-B Write Enable for each bit, active Low for Write, and High for Read.
GWEBN	I	Global Port-B Write Enable Active Low, latched at the rising edge of CKA.
TGWEBN	I	Port-B Test Global Write Enable Active Low, latched at the rising edge of CKA, alternate GWEAN source.
OEBN (n -1:0)	I	Local Port-B Output Enable for each bit, Active Low.
GOEBN	I	Global Port-B Output Enable, Active Low.
CEBN	I	Port-B Cell Enable, Active Low.
TCEBN	I	Port-B Test Component Enable Active Low, alternate CEAN source.
CKB	I	Port-B Clock Input.
WFTBN	I	Port-B Write Feed Through Enable, active low, overrides local WEAN functionality. This is a static mode pin.
DOB (n -1:0)	O	Data Output Port-B, updated following the rising edge of CKB.
SOB	O	Port-B Shift Out, data output from shift register chain for Port-B.

Configuration

Type 16 (standard)

Word: 128, 256, 384, (increments of 128) ...8192

Bit: 1 ... 72

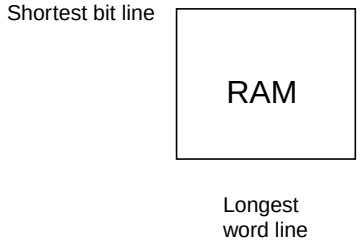
Type 4 (optional)

Word: 32, 64, 96 (increments of 32) ...2048

Bit: 1 ... 72

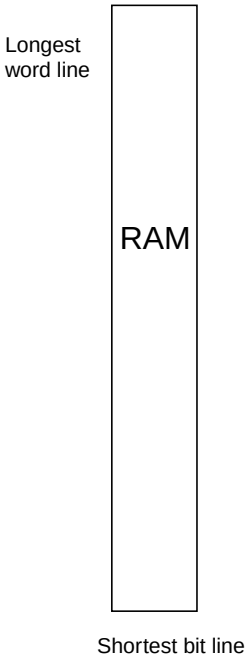
Architecture

Type 16 = 1- 72 bits (standard)



For Type 16, the specified number of words will equal sixteen times the number of rows and the specified number of bits will equal one sixteenth of the number of columns.

Type 4 = 1-72 bits (optional)



For Type 4, the specified number of words will equal four times the number of rows and the specified number of bits will equal one quarter of the number of columns in the RAM array.

Figure 4.17: Synchronous High-Density Dual-Port RAM (CS2RWD) Architectures

Logic Symbol

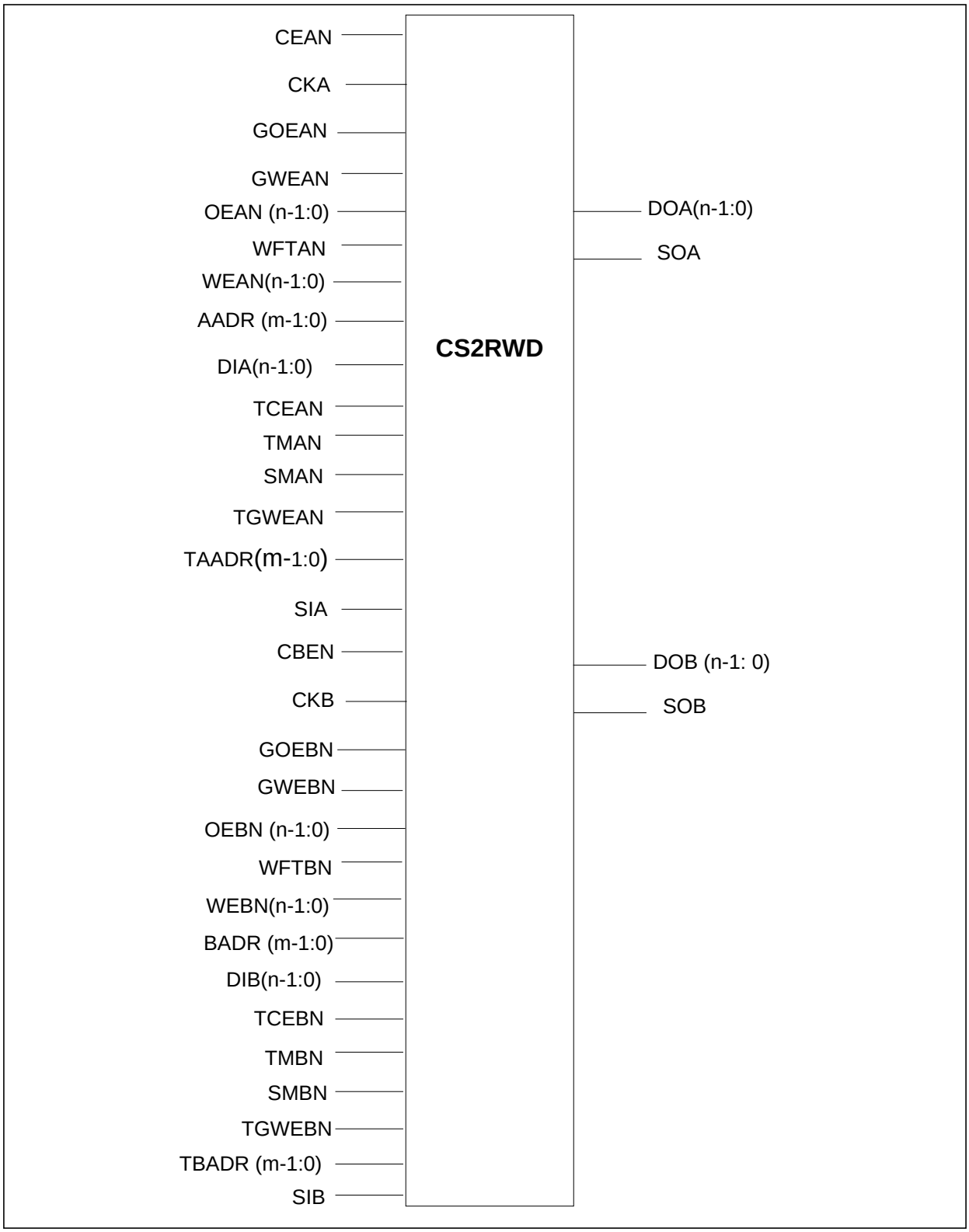


Figure 4.18: Logic Symbol for CS2RWD RAM

Timing Diagrams

Read Cycle

Outputs are valid for access time (t_{KNQ}) after the clock goes HIGH; they remain latched until more data is read or written.

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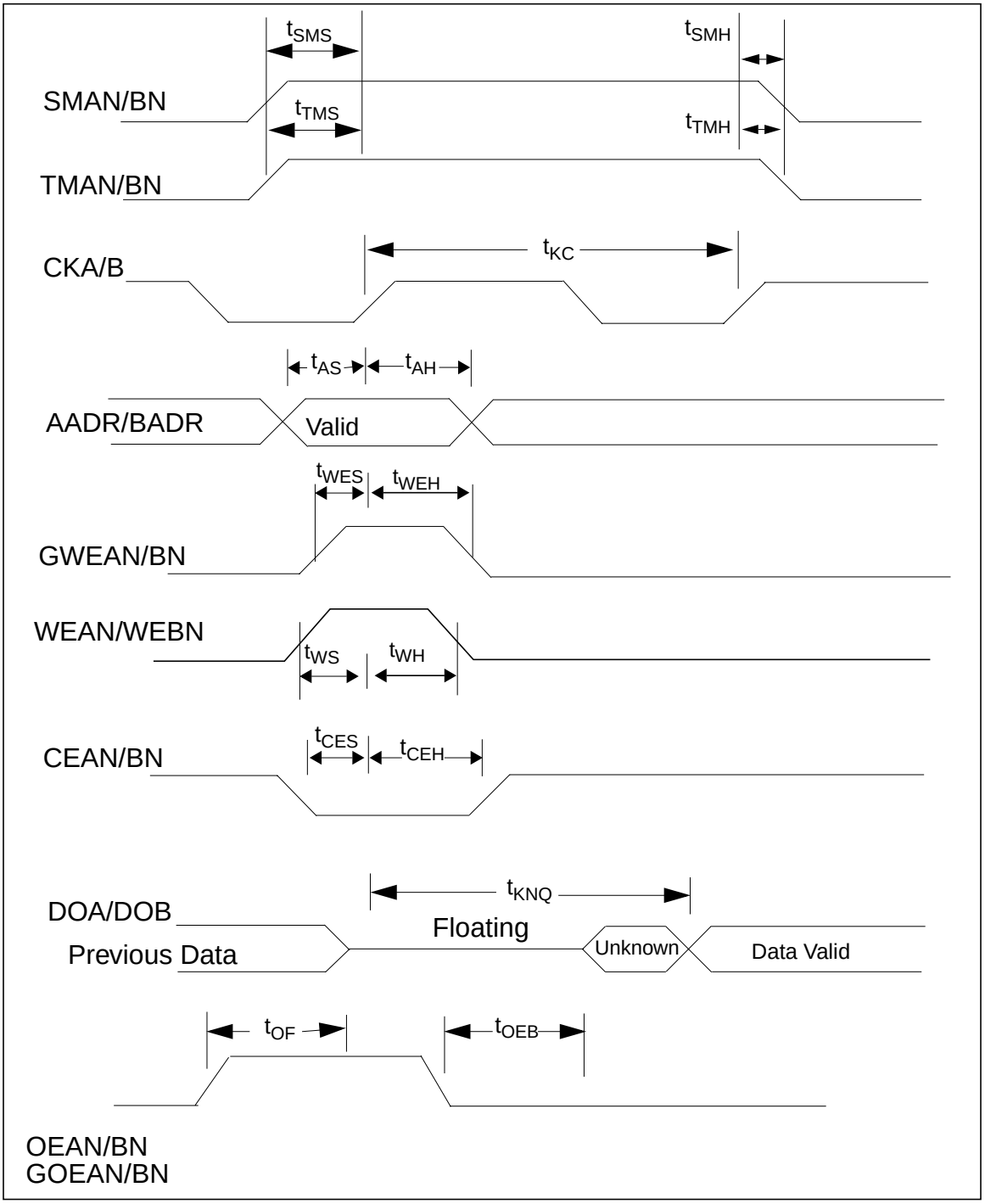

Figure 4.19: CS2RWD RAM Read Cycle

Write Cycle

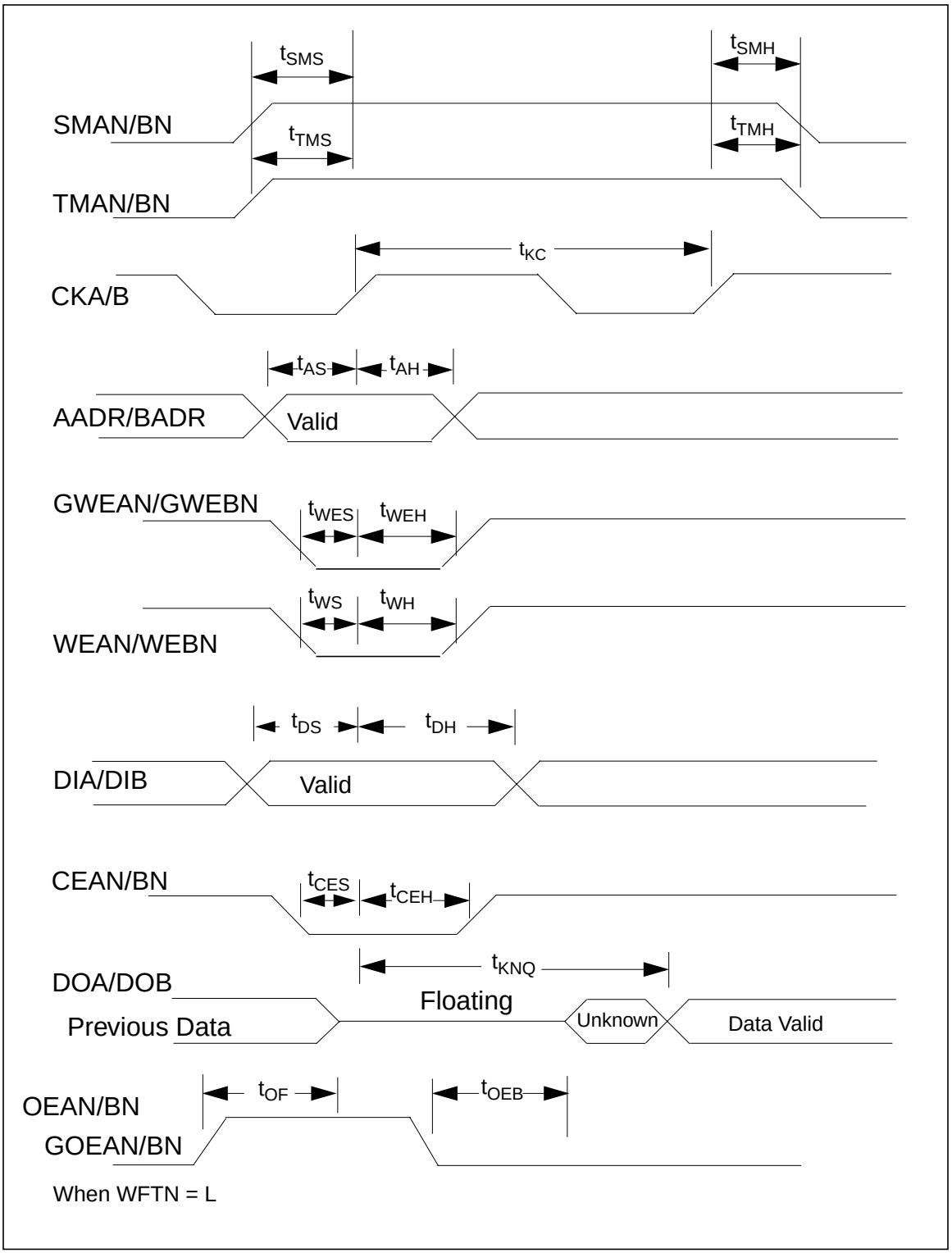

Figure 4.20: CS2RWD RAM Write Cycle

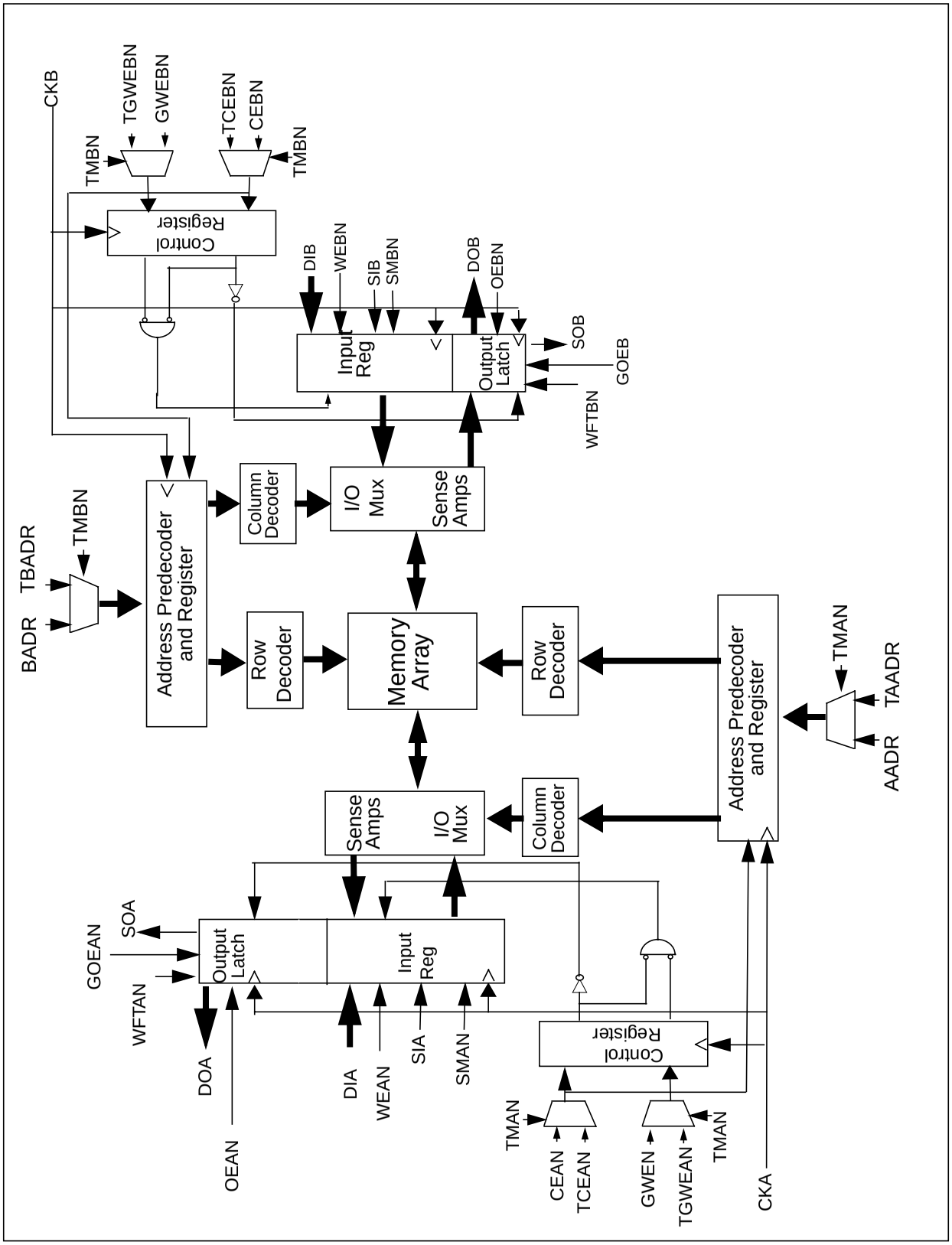

Figure 4.21: Block Diagram for CS2RWD RAM