ASPEC Technology, Inc.

0.35 Micron

Gate Array Products

HDA® 10000
(TSMC Polycide SPQM 3.3V Process)

3.3V
Macrocell Databook

October 1997

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Chapter 1: Introduction to the 3.3V Process, 3.3V 0.35μm Products

This databook provides basic technical information on the 3.3V HDA10000 product line, including masterslice statistics, macrocell data sheets, input and output DC characteristics, cell name conventions and Application Notes on Power and Ground rules and Clock Skew Management.

1.1 Product Description

HDA10000, based on an advanced array architecture, supports a triple layer metal HCMOS process. The high gate-density of this architecture results in lower on-chip noise, higher chip level performance, and lower component cost. HDA10000 is well-suited for cost-sensitive applications that also demand high circuit performance.

HDA10000 libraries support a de-facto standard set of macrocells. Power buffer and “Multiple Drive” versions of each macrocell are available for handling heavily loaded nets.

1.2 CAE Support

HDA10000 supports popular design platforms and environments such as Verilog, Viewlogic, Mentor, and Synopsys for front-end logic design capture and simulation, and Cadence Gate Ensemble and SVR GARDS for back-end place-and-route. For higher simulation accuracy, HDA10000 uses the ADVER™ delay calculator. Macrocells are characterized using a 4 x 4 delay matrix in which the input slope and output fanout are independently varied. Signal interconnect delay is based on RC Tree analysis.

1.3 Libraries

HDA10000 libraries include the following design elements:

(a) 3.3V internal macrocells
(b) 3.3V internal - 3.3V interface and 3.3V internal - 5.0V tolerant I/O cells
(c) Megacells
(d) Compiled cells
(e) Macrofunctions
(f) Megafunctions
(g) Compiled functions

1.3.1 Macrocells

Macrocells are lowest level of logic functions e.g., NAND, NOR, FLIP-FLOP, etc., used for logic design. There are 309 internal macrocells and over 700 I/O cells in the standard library. Macrocells are available in 3.3V drive strengths and have many levels of representation -- logic symbol, logic model, timing model, transistor schematic, SPICE netlist, physical layout, and place-and-route model.

1.3.2 Megacells

Megacells are large logic functions, such as RAMs and ROMs, which have the same number of levels of representation as macrocells. Improved silicon area efficiency and device performance are the main reasons for using megacells. Megacells are offered in array-cell and full custom implementations.

1.3.3 Compiled Cells

Compiled cells are generated by parameter-driven compiler programs. MEMGEN™ generates single-port and dual-port RAMs and ROMs. FIFO Builder™ and Multiplier Builder™ programs generate RAM-based FIFO and multiplier netlists.

1.3.4 Macrofunctions

Macrofunctions are netlists of logic function which have the complexity of a standard MSI integrated circuits. Macrocells are the logic building blocks. There are forty-three 7400 (TTL) compatible functions in the library.

1.3.5 Megafunctions

Megafunctions are also netlists of logic function, but with the higher logic complexity of a standard LSI circuit. Multipliers, barrel shifters, and 82XX Intel functions, etc., are supported in this library.

1.3.6 Compiled Functions

Compiled functions are generated by parameter-driven programs that use the macrocell library for basic building blocks.

1.4 Special Pad Descriptions

VDD5 - 5V Power Cell

VDDO, VSSO - Output driver VDD/VSS cells

VDDI, VSSI - Core VDD/VSS cells

VDDP, VSSP - Input and pre-driver VDD/VSS cells

VDDOI, VSSOI - Core and output VDD/VSS cells

VDDOP, VSSOP - Output driver, input and pre-driver VDD/VSS cells

VDDPI. VSSPI - Input, pre-driver and core VDD/VSS cells

VDDOPI, VSSOPI - Output, input, pre-driver and core VDD/VSS cells

CORNER - Corner cell

IO_SPACER - Spacer cell

PADCON - PAD connect for 3V I/O

PWRCON - Pad connect for power cell

PADCON5V -Pad connect for 5V tolerant I/O

1.5 VDD and VSS Rules and Guidelines

There are three types of VDD and VSS in this product family, each with its related bus and pad cells.

1. Core Logic

   VSSI, VDDI

2. Input Buffers

   VSSP, VDDP

3. Output Buffers

   VSSO, VDDO

The number of VSS and VDD pads required for a specific design depends on the following factors:

Number of input and output buffers

Number of simultaneous switching inputs

Number of simultaneous switching outputs

Number of used gates and number of simultaneous switching gates

Operating frequency of the design

1.5.1 Output Buffer VDDO Bus and VSSO Guidelines

For SSO:

Notation: n = package inductance in nH

i = sum of sso current in mA that 1 VSSO/VDDO pad supports

I = Total sso current for the design

# of VSSO pad = I / i (Round up to the next highest integer)

For n <= 15nH i = -2.4n + 84

For n >= 15nH i = -1.2n + 66

ie n=12nH and Total SSO current for the design (I) is 250mA

i = -2.4(12) + 84

= 55.2ma

# of VSSO pad = 250mA / 55.2 mA

= 4.5

Round up to the next highest integer

VSSO for SSO in the design is 5

of VDDO pad is the same as # VSSO pad

For non SSO:

Notation: n = package inductance in nH

i = sum of sso current in mA that 1 VSSO/VDDO pad supports

I = Total sso current for the design

# of VSSO pad = I / i (Round up to the next highest integer)

For n <= 15nH i = -3.6n + 126

For n >= 15nH i = -1.8n + 99

ie n=12nH and Total SSO current for the design (I) is 350mA

i = -3.6(12) + 126

= 82.8ma

# of VSSO pad = 350mA / 82.8 mA

= 4.2

Round up to the next highest integer

VSSO for SSO in the design is 5

of VDDO pad is the same as # VSSO pad

1.5.2 Core Logic VSS Bus and VSSI Pad Allocation Guidelines

The purpose of these guidelines is to ensure that VDD/VSS bounce due to simultaneous gate switching is kept to a minimum. Voltage bounce on the power bus could have a negative impact on gate switching speed, and in an extreme case could even affect the functionality of the macrocells, e.g., flip-flops and latches. Because of variations in package inductance, the number of VDD/VSS pads required for a specific design is a function of the operating frequency of the chip, i.e., designs operating at high frequency should use more VDD/VSS pads.

- VDD Bus width and pad requirement is the same as VSS.
- VDD/VSS Bus and Pads should be distributed evenly in the core and on all sides of the chip.
- At least one (1) VSSI pad should be used on each side of the chip.
- The total number of VDDI pads required is the same as VSSI.

The number of VSSI pads required for a design can be calculated from the following expression:

Notation: G = Total number of used gates in thousands
S = % of simultaneous switch gates
F = Switching frequence in MHz

# of VSSI pad = I / i (Round up to the next highest integer)
# of VSSI PAD = G * S * F * 1.8e-5
ie G = 100K S = 30% F = 50MHz

# of VSSI PAD = 100 * 30 * 50 * 1.8e-5
= 2.7
Round up to the next highest integer
VSSI in the design is 3

of VDDI pad is the same as # VSSI pad

1.6 Propagation Delays

Interconnect wire-length, temperature and supply voltage are the chief factors affecting propagation delay.

1.6.1Wire Length Loading Estimation

Loading due to interconnect wire-length can be estimated with the following expression. The result is given in terms of number of equivalent standard loads.

$$C_{WL} = C_{fo} \times (0.049 \times \sqrt{A} + 0.48) + 0.079 \times \sqrt{A} + 0.33$$

where C_{fo} = number of fan-outs in standard load
A = area of block size in mm^2
C_{WL} = number of equivalent standard loads due to interconnect

e.g., C_{fo} = 7 (standard loads)
A = 25 mm^2
C_{WL} = 5.8 (standard load)

1.6.2 Temperature and Supply Voltage

Fig. 1.1 describes propagation delay correction factor (K_T) as a function of on-chip junction temperature (T_j), and voltage delay correction factor (K_V) as a function of supply voltage (V_{DD}). As a result of increasing CMOS power dissipation, ambient and junction temperature are generally not the same. The temperature of the die inside the package (junction temperature, T_j), is calculated using chip power dissipation and the Thermal Resistance to Ambient (θ_{ja}) temperature of the package. Information on package thermal performance can be obtained from ASPEC Application Engineers.

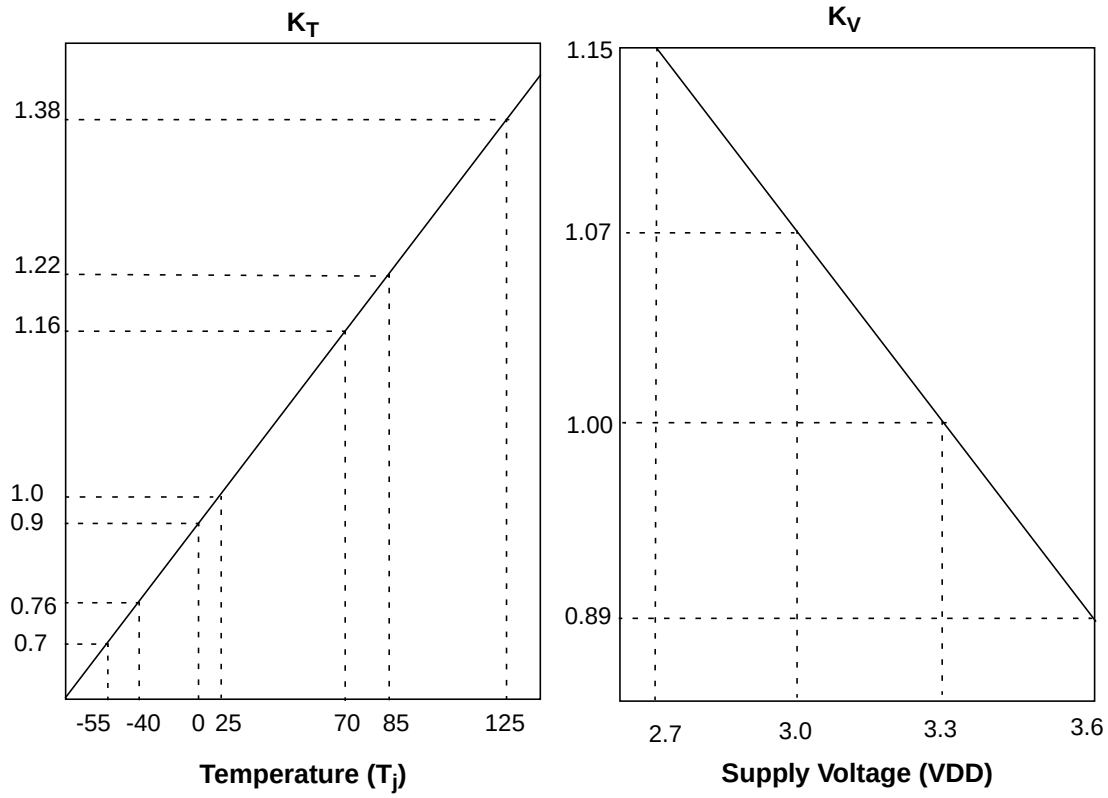


Figure 1.1: Effect of Temperature and Supply Voltage on Propagation Delay

Figure 1.2:

1.6.3 Propagation Delay

A circuit should be designed to operate properly within a given specification level, either commercial, industrial or military. It is recommended that circuits be simulated for Best Case, Nominal Case and Worst Case conditions at each specification level. The following expressions also allow for the effect of process variation on circuit performance.

Worst Case:

$$_{WC} = K_{PWC} \times K_T \times K_V \times t_{nom} = K_{WC} \times t_{nom}$$

Best Case:

$$T_{BC} = K_{PBC} \times K_T \times K_V \times t_{nom} = K_{BC} \times t_{nom}$$

T_{WC}	=	Worst case propagation delay
T_{BC}	=	Best case propagation delay
t_{nom}	=	nominal propagation delay (T_j = 25^{o}C, V_{DD} =3.3V and typical process parameters)
K_{PWC}	=	Worst case process correction factor
K_{PBC}	=	Best case process correction factor

1.7 Packages

For package options for HDA10000 gate arrays, please consult your foundry representative.

1.8 Dedicated Corner VSS/VDD Pads

The corner pads shown in Fig. 1.2 are well-suited for double bonding purposes. Pad 1 and Pad 2 can be bonded to the same package pin.

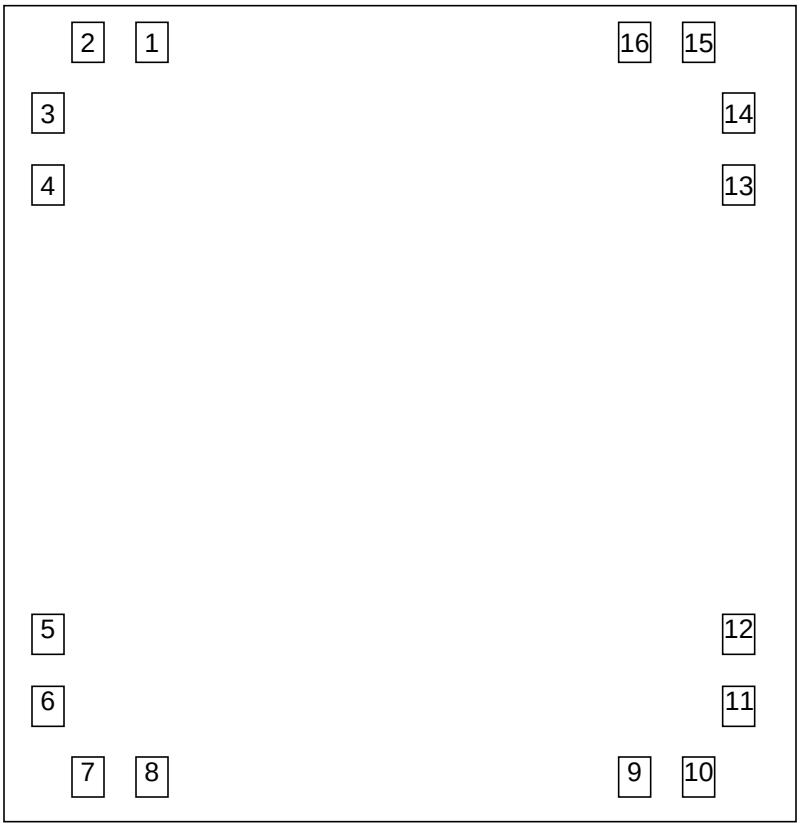


Fig. 1.2: VDD/VSS Corner Pads

Chapter 2.0 DC Characteristics

2.1 VDD = 3.3V (range: 3.0V-3.6V), junction temperature range -55 to +125°C.

Table 2.1: DC CHARACTERISTICS AT VDD = 3.3v

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage					
	CMOS				$0.3V_{DD}$	V
	CMOS Schmitt Trigger				$0.3V_{DD}$	V
	TTL				0.8	V
	TTL Schmitt Trigger				0.8	V
V_{IH}	Input High Voltage					
	CMOS		$0.7V_{DD}$			V
	CMOS Schmitt Trigger		$0.7V_{DD}$			V
	TTL		2.0			V
	TTL Schmitt Trigger		2.0			V
I_{IH}	Input High Current	$V_{IN}=V_{DD}$	-10		10	µA
	Input with pull-down	$V_{IN}=V_{DD}$	10		180	µA
I_{IL}	Input Low Current	$V_{IN}=V_{SS}$	-10		10	µA
	Input with pull-down	$V_{IN}=V_{SS}$	-180		-10	µA
V_{OH}	Output High Voltage					
	Type B1	I_{OH}= -1mA	2.4			V
	Type B2	I_{OH}= -2mA	2.4			V
	Type B4	I_{OH}= -4mA	2.4			V
	Type B8	I_{OH}= -8mA	2.4			V
	Type B12	I_{OH}= -12mA	2.4			V
	Type B16	I_{OH}= -16mA	2.4			V
	Type B20	I_{OH}= -20mA	2.4			V
	Type B24	I_{OH}= -24mA	2.4			V
V_{OL}	Output Low Voltage					
	Type B1	I_{OL}= 1mA			0.4	V
	Type B2	I_{OL}= 2mA			0.4	V
	Type B4	I_{OL}= 4mA			0.4	V
	Type B8	I_{OL}= 8mA			0.4	V
	Type B12	I_{OL}= 12mA			0.4	V
	Type B16	I_{OL}= 16mA			0.4	V
	Type B20	I_{OL}= 20mA			0.4	V
	Type B24	I_{OL}= 24mA			0.4	V
I_{OZ}	3-State Output Leakage Current	$V_{OH}=V_{SS}$ or V_{DD}	-10		10	µA
I_{DD}	Quiescent Supply Current	$V_{IN}=V_{SS}$ or V_{DD}			100[1]	µA

1. Depends on customer design

2.2 Absolute Maximum Ratings

Table 2.4: Maximum Ratings

	Symbol	Parameter	Rating	Unit
Absolute Maximum Ratings	V_{DD}	DC Supply Voltage	-0.3 to 7.0	V
	V_{IN}	DC Input Voltage	-0.3 to VDD +0.3	V
	I_{IN}	DC Input Current	$\pm$ 10	mA
	T_{STG}	Storage Temperature	-40 to +125	^{o}C
Recommended Operating Conditions	V_{DD}	DC Supply Voltage	3.0 - 3.6V	V
	T_A	Commercial Temperature	0 to 70	^{o}C
	T_A	Industrial Temperature	-40 to 85	^{o}C
	T_A	Military Temperature	-55 to 125	^{o}C

Chapter 3.0 3.3V Internal Macrocells

This chapter contains datasheets for 3.3V simple logic cells, multiplexers, decoders, adders, latches and flip-flops. Maximum fanout loading is given for each cell. This figure is the recommended standard load, including wire capacitance.

Tables 3.1 through 3.6 list 3.3V internal macrocells alphabetically by type, with size, input loading, description and the page number where the datasheet may be found.

Table 3.1: Simple Logic Cells

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
AD2D2	2	A,B = 1,1	2 Input AND 2X Drive	3-20
AD2D4	3	A,B, = 1,1	2 Input AND 4X Drive	3-20
AD2D6	4	A,B, = 1,1	2 Input AND 6X Drive	3-20
AD3	2	A,B,C = 1,1,1	3 Input AND 1X Drive	3-22
AD3D3	3	A,B,C = 1,1,1	3 Input AND 3X Drive	3-22
AD3D5	4	A,B,C = 1,1,1	3 Input AND 5X Drive	3-22
AD3D8	7	A,B,C = 2,2,2	3 Input AND 8X Drive	3-22
AD4D2	3	A,B,C,D = 1,1,1,1	4 Input AND 2X Drive	3-26
AD4D4	4	A,B,C,D = 1,1,1,1	4 Input AND 4X Drive	3-26
AD4D6	5	A,B,C,D = 2,2,2,2	4 Input AND 6X Drive	3-26
AD5	3	A,B,C,D,E = 1,1,1,1,1	5 Input AND 1X Drive	3-30
AD5D3	4	A,B,C,D,E = 1,1,1,1,1	5 Input AND 3X Drive	3-30
AD5D6	8	A,B,C,D,E = 2,2,2,2,2	5 Input AND 6X Drive	3-30
AO21	2	A,B,C = 1,1,1	2-AND into 2-NOR 1X Drive	3-34
AO21D2	3	A,B,C = 2,2,2	2-AND into 2-NOR 2X Drive	3-34
AO21D4	4	A,B,C = 1,1,1	2-AND into 2-NOR 4X Drive	3-34
AO21D6	5	A,B,C = 1,1,1	2-AND into 2-NOR 6X Drive	3-34
AO21I	2	A,B,C = 1,1,1	2-AND into 2-OR 1X Drive	3-38
AO21ID3	3	A,B,C = 1,1,1	2-AND into 2-OR 3X Drive	3-38
AO21ID5	4	A,B,C = 1,1,1	2-AND into 2-OR 5X Drive	3-38
AO21ID8	7	A,B,C = 1,1,1	2-AND into 2-OR 8X Drive	3-38
AO211	2	A,B,C,D = 1,1,1,1	2-AND into 3-NOR 1X Drive	3-42
AO211D2	4	A,B,C,D = 2,2,2,2	2-AND into 3-NOR 2X Drive	3-42
AO211D3	4	A,B,C,D = 1,1,1,1	2-AND into 3-NOR 3X Drive	3-42
AO211D7	6	A,B,C,D = 1,1,1,1	2-AND into 3-NOR 7X Drive	3-42
AO22	2	A,B,C,D = 1,1,1,1	2 2-AND into 2-NOR 1X Drive	3-46
AO22D2	4	A,B,C,D = 2,2,2,2	2 2-AND into 2-NOR 2X Drive	3-46
AO22D3	4	A,B,C,D = 1,1,1,1	2 2-AND into 2-NOR 3X Drive	3-46

Table 3.1: Simple Logic Cells (Continued)

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
AO22D7	6	A,B,C,D = 1,1,1,1	2 2-AND into 2-NOR 7X Drive	3-46
AO22A	3	A,B,C,D = 1,1,1,1	2-AND and 2-invert-AND into 2-NOR 1X Drive	3-50
AO22D2A	5	A,B,C,D = 2,2,1,1	2-AND and 2-invert-AND into2-NOR 2X Drive	3-50
AO222	3	A,B,C,D,E,F = 1,1,1,1,1,1	3 2-AND into 3-NOR 1X Drive	3-52
AO222D3	5	A,B,C,D,E,F = 1,1,1,1,1,1	3 2-AND into 3-NOR with 3X Drive	3-52
AO222D7	7	A,B,C,D,E,F = 1,1,1,1,1,1	3 2-AND into 3-NOR with 7X Drive	3-52
AO222A	3	A,B,C,D,E,F = 1,1,1,1,1,1	Inverting 2-of-3 majority 1X Drive	3-56
AO33	3	A,B,C,D,E,F = 1,1,1,1,1,1	2 3-AND into 2-NOR 1X Drive	3-58
AO33D2	5	A,B,C,D,E,F = 1,1,1,1,1,1	2 3-AND into 2-NOR 2X Drive	3-58
AO33D3	5	A,B,C,D,E,F = 1,1,1,1,1,1	2 3-AND into 2-NOR 3X Drive	3-58
AO33D7	7	A,B,C,D,E,F = 1,1,1,1,1,1	2 3-AND into 2-NOR 7X Drive	3-58
AO333	5	A,B,C,D,E,F,G,H,I = 1,1,1,1,1,1,1,1,1	3 3-AND into 3-NOR 1X Drive	3-62
AO333D2	6	A,B,C,D,E,F,G,H,I = 1,1,1,1,1,1,1,1,1	3 3-AND into 3-NOR 2X Drive	3-62
DL1D2	4	A = 1	1 ns non-inverting delay cell, 2X Drive	3-66
DL1D4	5	A = 1	1 ns non-inverting delay cell, 4X Drive	3-66
DL2D2	7	A = 1	2 ns non-inverting delay cell, 2X Drive	3-68
DL2D4	8	A = 1	2 ns non-inverting delay cell, 4X Drive	3-68
DL5D2	14	A = 1	5 ns non-inverting delay cell, 2X Drive	3-70

Table 3.1: Simple Logic Cells (Continued)

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
DL5D4	15	A = 1	5 ns non-inverting delay cell, 4X Drive	3-70
IV	1	A = 1	Inverter 1X Drive	3-72
IVD2	1	A = 2	Inverter 2X Drive	3-72
IVD3	2	A = 3	Inverter 3X Drive	3-72
IVD4	2	A = 4	Inverter 4X Drive	3-72
IVD6	3	A = 6	Inverter 6X Drive	3-74
IVD8	4	A = 8	Inverter 8X Drive	3-74
IVD12	6	A = 12	Inverter 12X Drive	3-76
IVD16	8	A = 16	Inverter 16X Drive	3-76
IVA	1	A = 1.5	Inverter with 2X P, 1X N Transistors	3-78
IVD2A	2	A = 3	Inverter with 4X P, 2X N Transistors	3-78
IVD3A	3	A = 4.5	Inverter with 6X P, 3X N Transistors	3-78
IVD4A	4	A = 6	Inverter with 8X P, 4X N Transistors	3-78
IVD8A	8	A = 8	Inverter with 16X P, 8X N Transistors	3-80
IVD12A	12	A = 18	Inverter with 24X P, 12X N Transistors	3-80
IVCD11A	2	A = 2.5	Buffer with 1X Inverting and 1X Non-inverting Outputs	3-82
IVCD22A	3	A = 3.5	Buffer with 2X inverting and 2X Non-inverting Outputs	3-82
IVCD44A	5	A = 5.5	Buffer with 4X Inverting and 4X Non-inverting Outputs	3-82
IVCD88A	9	A = 10	Buffer with 8X Inverting and 8X Non-inverting Outputs	3-82
IVT	3	A,E = 1,1.5	Inverting 3-State Buffer, Enable High, 1X Drive	3-84
IVTD2	4	A,E = 1,2	Inverting 3-State Buffer, Enable High, 2X Drive	3-84

Table 3.1: Simple Logic Cells (Continued)

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
IVTD5	5	A,E = 1,2	Inverting 3-State Buffer, Enable High, 5X Drive	3-84
IVTD9	7	A,E = 1,2	Inverting 3-State Buffe, Enable High, 9X Drive	3-84
ND2	1	A,B = 1,1	2 Input NAND 1X Drive	3-88
ND2D2	2	A,B = 2,2	2 Input NAND 2X Drive	3-88
ND2D5	4	A,B = 1,1	2 Input NAND 5X Drive	3-88
ND2D7	5	A,B = 1,1	2 Input NAND 7X Drive	3-88
ND3	2	A,B,C = 1,1,1	3 Input NAND 1X Drive	3-92
ND3D2	3	A,B,C = 2,2,2	3 Input NAND 2X Drive	3-92
ND3D4	4	A,B,C = 1,1,1	3 Input NAND 4X Drive	3-92
ND3D6	5	A,B,C = 1,1,1	3 Input NAND 6X Drive	3-92
ND4	2	A,B,C,D = 1,1,1,1	4 Input NAND 1X Drive	3-96
ND4D2	4	A,B,C,D = 2,2,2,2	4 Input NAND 2X Drive	3-96
ND4D5	5	A,B,C,D = 1,1,1,1	4 Input NAND 5X Drive	3-96
ND4D7	6	A,B,C,D = 1,1,1,1	4 Input NAND 7X Drive	3-96
ND5	3	A,B,C,D,E = 1,1,1,1,1	5 Input NAND 1X Drive	3-100
ND5D2	5	A,B,C,D,E = 2,2,2,2,2	5 Input NAND 2X Drive	3-100
ND5D4	5	A,B,C,D,E = 1,1,1,1,1	5 Input NAND 4X Drive	3-100
ND5D6	6	A,B,C,D,E = 1,1,1,1,1	5 Input NAND 6X Drive	3-100
ND6	5	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NAND 1X Drive	3-104
ND6D2	5	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NAND 2X Drive	3-104
ND6D4	6	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NAND 4x Drive	3-104
ND6D8	9	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NAND 8x Drive	3-104
ND8	6	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NAND 1X Drive	3-108
ND8D2	6	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NAND 2X Drive	3-108

Table 3.1: Simple Logic Cells (Continued)

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
ND8D4	7	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NAND 4X Drive	3-108
ND8D8	10	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NAND 8X Drive	3-108
NID8	5	A = 2	Non-Inverting Buffer 8X Drive	3-114
NID12	7	A = 2	Non-Inverting Buffer 12X Drive	3-114
NID16	9	A = 2	Non-Inverting Buffer 16X Drive	3-114
NIT	2	A,E = 1,1.5	Non-Inverting Tri-State Buffer, Enable High, 1X Drive	3-116
NITD2	3	A,E = 1,2	Non-Inverting Tri-State Buffer, Enable High, 2X Drive	3-116
NITD5	5	A = 2	Non-Inverting Tri-State Buffer, Enable High, 5X Drive	3-116
NITD9	7	A = 2	Non-Inverting Tri-State Buffer, Enable High, 9X Drive	3-116
NR2	1	A,B = 1,1	2 Input NOR 1X Drive	3-120
NR2D2	2	A,B = 2,2	2 Input NOR 2X Drive	3-120
NR2D3	3	A,B = 1,1	2 Input NOR 3X Drive	3-120
NR2D7	5	A,B = 1,1	2 Input NOR 7X Drive	3-120
NR3	2	A,B,C = 1,1,1	3 Input NOR 1X Drive	3-124
NR3D2	3	A,B,C = 2,2,2	3 Input NOR 2X Drive	3-124
NR3D3	4	A,B,C = 1,1,1	3 Input NOR 3X Drive	3-124
NR3D7	6	A,B,C = 1,1,1	3 Input NOR 7X Drive	3-124
NR4	2	A,B,C,D = 1,1,1,1	4 Input NOR 1X Drive	3-128
NR4D2	4	A,B,C,D = 1,1,1,1	4 Input NOR 2X Drive	3-128
NR4D4	5	A,B,C,D = 1,1,1,1	4 Input NOR 4X Drive	3-128
NR4D6	6	A,B,C,D = 1,1,1,1	4 Input NOR 6X Drive	3-128
NR5	4	A,B,C,D,E = 1,1,1,1,1	5 Input NOR 1X Drive	3-132
NR5D2	5	A,B,C,D,E = 1,1,1,1,1	5 Input NOR 2X Drive	3-132
NR5D4	6	A,B,C,D,E = 1,1,1,1,1	5 Input NOR 5X Drive	3-132
NR5D6	7	A,B,C,D,E = 1,1,1,1,1	5 Input NOR 7X Drive	3-132

Table 3.1: Simple Logic Cells (Continued)

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
NR6	5	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NOR 1X Drive	3-136
NR6D2	6	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NOR 2x Drive	3-136
NR8	6	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NOR 1X Drive	3-140
NR8D2	7	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NOR 2X Drive	3-140
OA21	2	A,B,C = 1,1,1	2-OR into 2-NAND 1X Drive	3-144
OA21D2	3	A,B,C, = 2,2,2	2-OR into 2-NAND 2X Drive	3-144
OA21D4	4	A,B,C = 1,1,1	2-OR into 2-NAND 4X Drive	3-144
OA21D6	5	A,B,C = 1,1,1	2-OR into 2-NAND 6X Drive	3-144
OA21I	2	A,B,C = 1,1,1	2-OR into 2-AND 1X Drive	3-148
OA21ID3	3	A,B,C = 1,1,1	2-OR into 2-AND 3X Drive	3-148
OA21ID5	4	A,B,C = 1,1,1	2-OR into 2-AND 5X Drive	3-148
OA21ID8	7	A,B,C, = 2,2,2	2-OR into 2-AND 8X Drive	3-148
OA211	2	A,B,C,D = 1,1,1,1	2-OR into 3-NAND 1X Drive	3-152
OA211D2	4	A,B,C,D = 2,2,2,2	2-OR into 3-NAND 2X Drive	3-152
OA211D3	4	A,B,C,D = 1,1,1,1	2-OR into 3-NAND 3X Drive	3-152
OA211D7	6	A,B,C,D = 1,1,1,1	2-OR into 3-NAND 7X Drive	3-152
OA22	2	A,B,C = 1,1,1	2 2-OR into 2-NAND 1X Drive	3-156
OA22D2	4	A,B,C,D = 2,2,2,2	2 2-OR into 2-NAND 2X Drive	3-156
OA22D3	4	A,B,C,D = 1,1,1,1	2 2-OR into 2-NAND 3X Drive	3-156
OA22D7	6	A,B,C,D = 1,1,1,1	2 2-OR into 2-NAND 7X Drive	3-156
OA22A	3	A,B,C,D = 1,1,1,1	2 2-OR and 12-invert-OR into 2-NAND 1X Drive	3-160
OA22D2A	4	A,B,C,D = 2,2,1,1	2-OR and 2-invert-OR into 2-NAND 2X Drive	3-160
OR2D2	2	A,B = 1,1	2 Input OR 2X Drive	3-162
OR2D4	3	A,B = 1,1	2 Input OR 4X Drive	3-162
OR2D8	6	A,B = 2,2	2 Input OR 8X Drive	3-162

Table 3.1: Simple Logic Cells (Continued)

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
OR3	2	A,B,C = 1,1,1	3 Input OR 1X Drive	3-164
OR3D3	3	A,B,C = 1,1,1	3 Input OR 3X Drive	3-164
OR3D6	6	A,B,C = 2,2,2	3 Input OR 6X Drive	3-164
OR3D8	7	A,B,C = 2,2,2	3 Input OR 8X Drive	3-164
OR4	3	A,B,C,D = 1,1,1,1	4 Input OR 1X Drive	3-168
OR4D2	4	A,B,C,D = 1,1,1,1	4 Input OR 2X Drive	3-168
OR4D5	6	A,B,C,D = 1,1,1,1	4 Input OR 5X Drive	3-168
OR4D7	7	A,B,C,D = 1,1,1,1	4 Input OR 7X Drive	3-168
OR5	4	A,B,C,D,E = 1,1,1,1,	5 Input OR 1X Drive	3-172
OR5D2	5	A,B,C,D,E = 1,1,1,1,	5 Input OR 2X Drive	3-172
XN2	3	A,B = 1,2	2 Input Exclusive NOR 1X Drive	3-174
XN2D2	4	A,B = 1,2	2 Input Exclusive NOR 2X Drive	3-174
XN2D3	4	A,B = 1,2	2 Input Exclusive NOR 3X Drive	3-174
XN2D5	5	A,B = 1,2	2 Input Exclusive NOR 5X Drive	3-174
XN3	5	A,B,C = 2,1,2	3 Input Exclusive NOR 1X Drive	3-178
XN3D3	6	A,B,C = 2,1,2	3 Input Exclusive NOR 3X Drive	3-178
XO2	3	A,B = 1,2	2 Input Exclusive OR 1X Drive	3-180
XO2D2	4	A,B = 1,2	2 Input Exclusive OR 2X Drive	3-180
XO2D3	4	A,B = 1,2	2 Input Exclusive OR 3X Drive	3-180
XO2D5	5	A,B = 1,2	2 Input Exclusive OR 5X Drive	3-180
XO3	5	A,B,C = 2,1,2	3 Input Exclusive OR 1X Drive	3-184
XO3D3	6	A,B,C = 2,1,2	3 Input Exclusive OR 3X Drive	3-184

Table 3.2: Multiplexers and Decoders

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
DC4	7	S0,S1 = 3,3	2 > 4 Non-Inverting Decoder 1X Drive	3-186
DC4D2	9	S0,S1 = 3,3	2 > 4 Non-Inverting Decoder 2X Drive	3-186
DC4D4	13	S0,S1 = 3,3	2 > 4 Non-Inverting Decoder 4X Drive	3-186
DC4I	5	S0,S1 = 3,3	2 > 4 Inverting Decoder 1X Drive	3-190
DC4ID2	9	S0,S1 = 3,3	2 > 4 Inverting Decoder 2X Drive	3-190
DC4ID4	13	S0,S1 = 3,3	2 > 4 Inverting Decoder 4X Drive	3-190
MX2	3	D0,D1,S = 1,1,2	2 > 1 Non-Inverting Mux 1X Drive	3-194
MX2D3	4	D0,D1,S = 1,1,2	2 > 1 Non-Inverting Mux 3X Drive	3-194
MX2X4	11	D00,D10,D01,D11,D02, D12,D03,D13,S = 1,1,1,1,1,1,1,1,1	4-Bit 2 > 1 Non-Inverting Mux 1X Drive	3-196
MX2D2X4	13	D00,D10,D01,D11,D02, D12,D03,D13,S = 1,1,1,1,1,1,1,1,4	4-Bit 2 > 1 Non-Inverting Mux 2X Drive	3-196
MX2I	2	D0,D1,S = 3,3,2	2 > 1 Inverting Mux 1X Drive	3-202
MX2ID2	3	D0,D1,S = 4,4,2	2 > 1 Inverting Mux 2X Drive	3-202
MX2ID3	3	D0,D1,S = 5,5,2	2 > 1 Inverting Mux 3X Drive	3-202
MX2IX4	7	D00,D10,D01,D11,D02, D12,D03,D13,S = 3,3,3,3,3,3,3,3,1	4-Bit 2 > 1 Inverting Mux 1X Drive	3-206
MX2ID2X4	9	D00,D10,D01,D11,D02, D12,D03,D13,S = 4,4,4,4,4,4,4,4,1	4-Bit 2 > 1 Inverting Mux 2X Drive	3-206
MX2IA	2	D0,D1,S,SN = 3,3,1,1	2 > 1 Inverting Mux 1X Drive, separate S and SN inputs	3-212
MX2ID2A	2	D0,D1,S, SN = 4,4,1,1	2 > 1 Inverting Mux 2X Drive, separate S and SN inputs	3-212
MX2ID4A	3	D0,D1,S = 6,6,1,1	2 > 1 Inverting Mux 4X Drive, separate S and SN inputs	3-212

Table 3.2: Multiplexers and Decoders

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
MX3I	4	D0,D1,D2,S0,S1 = 3,3,1,2,2	3 > 1 Inverting Mux 1X Drive	3-216
MX3ID2	4	D0,D1,D2,S0,S1 = 6,6,4,2,2	3 > 1 Inverting Mux 2X Drive	3-216
MX3ID4	6	D0,D1,D2,S0,S1 = 3,3,6,,2,2	3 > 1 Inverting Mux 4X Drive	3-216
MX4	6	D0,D1,D2,D3,S0,S1 = 3,3,3,3,3,2	4 > 1 Non-inverting Mux 1X Drive	3-220
MX4D2	6	D0,D1,D2,D3,S0,S1 = 3,3,3,3,3,2	4 > 1 Non-inverting Mux 2X Drive	3-220
MX8	12	D0,D1,D2,D3,D4,D5,D6, D7,S0,S1,S2 = 3,3,3,3,3,3,3,3,1,3,2	8 > 1 Non-inverting Mux 1X Drive	3-224
MX8D2	12	D0,D1,D2,D3,D4,D5,D6, D7,D8,S0,S1,S2 = 3,3,3,3,3,3,3,3,1,3,2	8 > 1 Non-inverting Mux 2X Drive	3-224

Table 3.3: Adders

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
FA	7	CI,A,B = 2,1,2	Full Adder 1X Drive	3-288
FAD2	8	CI,A,B = 2,1,2	Full Adder 2X Drive	3-288
FAD4	10	CI,A,B = 2,1,2	Full Adder 4X Drive	3-288
FAD6	12	CI,A,B = 2,1,2	Full Adder 6X Drive	3-288
HA	5	A,B = 2,3	Half Adder 1X Drive	3-294
HAD2	6	A,B = 2,3	Half Adder 2X Drive	3-294
HAD4	8	A,B = 2,3	Half Adder 4X Drive	3-294

Table 3.4: Miscellaneous Cells

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
Busholder	0	2	Busholder	3-472

Table 3. 5: Latches

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
LD1	4	D,G = 3,1	D-Latch Active High Gate, 1X Drive	3-230
LD1D2	5	D,G = 3,1	D-Latch Active High Gate, 2X Drive	3-230
LD1D2Q	4	D,G = 3,1	D-Latch Active High Gate, Q Output Only, 2X Drive	3-234
LD1D4Q	5	D,G = 3,1	D-Latch Active High Gate, Q Output Only, 4X Drive	3-234
LD1A	5	D,G,E = 3,1,1.5	D-Latch Active High Gate, 3-State, 1X Drive	3-236
LD1B	4	D,WR,WRN,RD = 3,1,1,1.5	D-Latch, 3-State, with separate WR, WRN, commonly known as RAM1	3-238
LD1S	7	D,G,SI,SG = 1,2,1,2	D-Latch Active High Gate with Scan, 1X Drive	3-342
LD1SD2	8	D,G,SI,SG = 1,2,1,2	D-Latch Active High Gate with Scan, 2x Drive	3-242
LD1X4	13	D0,D1,D2,D3,G = 3,3,3,3,1	4-Bit D-Latch Active High Gate, 1X Drive	3-248
LD2	5	D,G,RN = 3,1,1	D-Latch Active High Gate with Reset, 1X Drive	3-252
LD2Q	4	D,G,RN = 3,1,1	D-Latch Active High Gate with Reset, Q Output Only, 1X Drive	3-254
LD2D3Q	5	D,G,RN = 3,1,1	D-Latch Active High Gate with Reset, Q Output Only, 3X Drive	3-254
LD4	6	D,G,RN,SN = 3,1,1,2	D-Latch Active High Gate with Set, Reset, 1X Drive	3-258
LD4D2Q	6	D,G,RN,SN = 3,1,1,2	D-Latch Active High Gate with Set, Reset, Q Output Only, 2X Drive	3-262
LD4D4Q	7	D,G,RN,SN = 3,1,1,2	D-Latch Active High Gate with Set, Reset, Q Output Only, 4X Drive	3-262
LD5	4	D,GN = 3,1	D-Latch Active Low Gate, 1X Drive	3-266
LD5D2	5	D,GN = 3,1	D-Latch Active Low Gate, 2X Drive	3-266
LD5D2Q	4	D,GN = 3,1	D-Latch Active Low Gate, Q Output Only, 2X Drive	3-270
LD5D4Q	5	D,GN = 3,1	D-Latch Active Low Gate, Q Output Only, 4X Drive	3-270

Table 3. 5: Latches

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
LD5X4	13	D0,D1,D2,D3,G = 3,3,3,3,1	4-Bit D-Latch Active Low Gate, 1X Drive	3-272
LD6	5	D,GN,RN = 3,1,1	D-Latch Active Low Gate with Reset,1X Drive	3-276
LD6D2	6	D,GN,RN = 3,1,1	D-Latch Active Low Gate with Reset, 2X Drive	3-276
LD6Q	4	D,GN,RN = 3,1,1	D-Latch Active Low Gate with Reset, Q Output Only, 1X Drive	3-280
LD6D3Q	5	D,GN,RN = 3,1,1	D-Latch Active Low Gate with Reset, Q Output Only, 3X Drive	3-280
LS1	4	SN1,SN2,SN,RN,RN1, RN2 = 1,1,1,1,1,1	SR Latch with separate Gate inputs, 1X Drive	3-284
LS1D3	8	SN1,SN2,SN,RN,RN1, RN2 = 1,1,1,1,1,1	SR Latch with separate Gate inputs, 3X Drive	3-284

Table 3.6: Flip-Flops

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
FD1	6	D,CK = 3,1	D Flip-Flop, Positive Edge Trigger,1X Drive	3-298
FD1D2	7	D,CK = 3,1	D Flip-Flop, Positive Edge Trigger, 2X Drive	3-298
FD1D2Q	6	D,CK = 3,1	D Flip-Flop, Positive Edge Trigger, Q Output Only, 2X Drive	3-300
FD1D4Q	7	D,CK = 3,1	D Flip-Flop, Positive Edge Trigger, Q Output Only, 4X Drive	3-300
FD1S	9	D,TI,TE,CK = 1,1,2,1	D Flip-Flop with Scan, Positive Edge Trigger, 1X Drive	3-302
FD1SD2	10	D,TI,TE,CK = 1,1,2,1	D Flip-Flop with Scan, Positive Edge Trigger, 2X Drive	3-302
FD1SD2Q	9	D,TI,TE,CK = 1,1,2,1	D Flip-Flop with Scan, Positive Edge Trigger, Q Output Only, 2X Drive	3-306
FD1SD4Q	10	D,TI,TE,CK = 1,1,2,1	D Flip-Flop with Scan, Positive Edge Trigger, Q Output Only, 4X Drive	3-306
FD1X4	21	D0,D1,D2,D3,CK = 3,3,3,3,1	4-Bit D Flip-Flop, Positive Edge Trigger, 1X Drive	3-308
FD1D2X4Q	24	D0,D1,D2,D3,CK = 3,3,3,3,1	4-Bit D Flip-Flop, Positive Edge Trigger, Q Output Only, 2X Drive	3-312
FD1D4X4Q	28	D0,D1,D2,D3,CK = 3,3,3,3,1	4-Bit D Flip-Flop, Positive Edge Trigger, Q Output Only, 4X Drive	3-312
FD2	7	D,CK,RN = 3,1,2	D Flip-Flop with Reset, Positive Edge Trigger, 1X Drive	3-316
FD2D2	8	D,CK,RN = 3,1,2	D Flip-Flop with Reset, Positive Edge Trigger, 2X Drive	3-316
FD2D2Q	7	D,CK,RN = 3,1,2	D Flip-Flop with Reset, Positive Edge Trigger, Q Output Only, 2X Drive	3-320
FD2D4Q	8	D,CK,RN = 3,1,2	D Flip-Flop with Reset, Positive Edge Trigger, Q Output Only, 4X Drive	3-320
FD2S	10	D,TI,TE,CK,RN = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Positive Edge Trigger, 1X Drive	3-322
FD2SD2	11	D,TI,TE,CK,RN = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Positive Edge Trigger, 2X Drive	3-322

Table 3.6: Flip-Flops (Continued)

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
FD2SD2Q	10	D,CK,RN, TI, TE = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Positive Edge Trigger, Q Output Only, 2X Drive	3-326
FD2SD4Q	11	D,CK,RN, TI, TE = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Positive Edge Trigger, Q Output Only, 4X Drive	3-326
FD2X4	25	D0,D1,D2,D3,CK,RN = 3,3,3,3,3,8	4-Bit D Flip-Flop with Reset, Positive Edge Trigger, 1X Drive	3-330
FD2D2X4Q	28	D0,D1,D2,D3,CK,RN = 3,3,3,3,1,8	4-Bit D Flip-Flop with Reset, Positive Edge Trigger, Q Output Only, 2X Drive	3-334
FD2D4X4Q	32	D0,D1,D2,D3,CK,RN = 3,3,3,3,1,8	4-Bit D Flip-Flop with Reset, Positive Edge Trigger, Q Output Only, 4X Drive	3-334
FD3	7	D,CK,SN = 3,1,2	D Flip-Flop with Set, Positive Edge TriggerTrigger, 1X Drive	3-340
FD3D2	8	D,CK,SN = 3,1,2	D Flip-Flop with Set, Positive Edge Trigger, 2X Drive	3-340
FD3S	10	D,TI,TE,CK,SN = 1,1,2,1,2	D Flip-Flop with Set, Scan, Positive Edge Trigger, 1X Drive	3-344
FD3SD2	11	D,TI,TE,CK,SN = 1,1,2,1,2	D Flip-Flop with Set, Scan, Positive Edge Trigger, 2X Drive	3-344
FD4	8	D,CK,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset, Positive Edge Trigger, 1X Drive	3-348
FD4D2	9	D,CK,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset, Positive Edge Trigger, 2X Drive	3-348
FD4D2Q	8	D,CK,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset, Positive Edge Trigger, Q Output Only, 2X Drive	3-352
FD4D4Q	9	D,CK,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset, Positive Edge Trigger, Q Output Only, 4X Drive	3-352
FD4S	11	D,TI,TE,CK,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, 1X Drive	3-356
FD4SD2	12	D,TI,TE,CK,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, 2X Drive	3-356

Table 3.6: Flip-Flops (Continued)

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
FD4SD2Q	11	D,TI,TE,CK,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, Q Output On ly, 2X Drive	3-362
FD4SD4Q	12	D,TI,TE,CK,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, Q Output On ly, 4X Drive	3-362
FD4D2X4Q	32	DO,D1,D2,D3,CK,RN, SN = 3,3,3,3,1,8,8	4-Bit D Flip-Flop with Set and Reset, Positive Edge Trigger, Q Output Only, 2X Drive	3-366
FD4D4X4Q	36	DO,D1,D2,D3,CK,RN, SN = 3,3,3,3,1,8,8	4-Bit D Flip-Flop with Set and Reset, Positive Edge Trigger, Q Output Only, 4X Drive	3-366
FD5	6	D,CKN = 3,1	D Flip-Flop, Negative Edge Trigger,1X Drive	3-372
FD5D2	7	D,CKN = 3,1	D Flip-Flop, Negative Edge Trigger,2X Drive	3-372
FD5D2Q	6	D,CKN = 3,1	D Flip-Flop, Negative Edge Trigger, Q Output Only, 2X Drive	3-376
FD5D4Q	7	D,CKN = 3,1	D Flip-Flop, Negative Edge Trigger, Q Output Only, 4X Drive	3-376
FD5SD2Q	9	D,CKN,TI,TE = 1,1,1,2	D Flip-Flop, Scan, Negative Edge Trigger, Q Output Only, 2X Drive	3-378
FD5SD4Q	10	D,CKN,TI,TE = 1,1,1,2	D Flip-Flop, Scan, Negative Edge Trigger, Q Output Only, 4X Drive	3-378
FD5X4	21	D0, D1, D2, D3, CKN = 3, 3, 3, 3, 1	4-Bit Flip-Flop with Negative Edge Trigger	3-382
FD5D2X4Q	24	D0, D1, D2, D3, CKN = 3,3,3,3,1	4-Bit Flip-Flop with Negative Edge Trigger, Q Output Only, 2X Drive	3-386
FD5D4X4Q	28	D0, D1, D2, D3, CKN = 3,3,3,3,1	4-Bit Flip-Flop with Negative Edge Trigger, Q Output Only, 4X Drive	3-386
FD6	7	D,CKN,RN = 3,1,2	D Flip-Flop with Reset, Negative Edge Trigger,1X Drive	3-390
FD6D2	8	D,CKN,RN = 3,1,2	D Flip-Flop with Reset, Negative EdgeTrigger, 2X Drive	3-390
FD6D2Q	7	D,CKN,RN = 3,1,2	D Flip-Flop with Reset, Negative EdgeTrigger, Q Output Only, 2X Drive	3-394
FD6D4Q	8	D,CKN,RN = 3,1,2	D Flip-Flop with Reset, Negative EdgeTrigger, Q Output Only, 4X Drive	3-394

Table 3.6: Flip-Flops (Continued)

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
FD6SD2Q	10	D,CKN,RN,TI,TE = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Negative Edge Trigger, Q Output Only, 2X Drive	3-398
FD6SD4Q	11	D,CKN,RN,TI,TE = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Negative Edge Trigger, Q Output Only, 4X Drive	3-398
FD6D2X4Q	28	D0, D1, D2, D3, CKN, RN = 3,3,3,3,1, 8	4-Bit D Flip-Flop with Reset, Negative Edge Trigger, Q Output Only, 2X Drive	3-402
FD6D4X4Q	32	D0, D1, D2, D3, CKN, RN = 3,3,3,3,1, 8	4-Bit D Flip-Flop with Reset, Negative Edge Trigger, Q Output Only, 4X Drive	3-402
FD7	7	D,CKN,SN = 3,1,2	D Flip-Flop with Set, Negative Edge Trigger, 1X Drive	3-408
FD7D2	8	D,CKN,SN = 3,1,2	D Flip-Flop with Set, Negative Edge Trigger, 2X Drive	3-408
FD8	8	D,CKN,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset,Negative Edge Trigger, 1X Drive	3-412
FD8D2	9	D,CKN,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset, Negative Edge Trigger, 2X Drive	3-412
FD8D2Q	8	D,CKN,RN,SN = 3,1,2, 2	D Flip-Flop with Set and Reset, Negative Edge Trigger, Q Output Only, 2X Drive	3-416
FD8D4Q	9	D,CKN,RN,SN = 3,1,2, 2	D Flip-Flop with Set and Reset, Negative Edge Trigger, Q Output Only, 4X Drive	3-416
FD8SD2Q	11	D,TI,TE,CKN,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set and Reset, Scan, Negative Edge Trigger, Q Output Only, 2X Drive	3-420
FD8SD4Q	12	D,TI,TE,CKN,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set and Reset, Scan, Negative Edge Trigger, Q Output Only, 4X Drive	3-420
FD8D2X4Q	32	D0, D1, D2, D3, CKN, RN , SN = 3, 3, 3 ,3, 1, 8, 8	4-Bit D Flip-Flop with Set and Reset, Negative Edge Trigger, Q Output Only, 2X Drive	3-424
FD8D4X4Q	36	D0, D1, D2, D3, CKN, RN , SN = 3, 3, 3 ,3, 1, 8, 8	4-Bit D Flip-Flop with Set and Reset, Negative Edge Trigger, Q Output Only, 4X Drive	3-424
FG1	7	D,E,CK = 3,1,1	D Flip-Flop with CK Enable, Positive Edge Trigger, 1X Drive	3-430

Table 3.6: Flip-Flops (Continued)

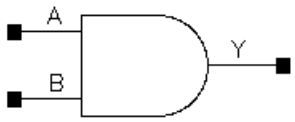
Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
FG1X4	22	D0,D1,D2,D3,E,CK = 3,3,3,3,1,1	4-Bit D Flip-Flop with CK Enable, Positive Edge Trigger, 1X Drive	3-432
FG2	8	D,E,CK RN = 3,1,1,2	D Flip-Flop with Reset, CK Enable, Positive Edge Trigger, 1X Drive	3-436
FG2X4	26	D0,D1,D2,D3,E,CK,RN = 3,3,3,3,1,1,8	4-Bit D Flip-Flop with Reset, CK Enable, Positive Edge Trigger, 1X Drive	3-438
FJ1	9	J,K,CK = 1,1,1	JK Flip-Flop, Positive Edge Trigger, 1X Drive	3-442
FJ1D2	10	J,K,CK = 1,1,1	JK Flip-Flop, Positive Edge Trigger, 2X Drive	3-442
FJ1S	11	J,K,CK,TI,TE = 1,1,1,1,2	JK Flip-Flop with Scan, Positive Edge Trigger, 1X Drive	3-446
FJ1SD2	12	J,K,CK,TI,TE = 1,1,1,1,2	JK Flip-Flop with Scan, Positive Edge Trigger, 2X Drive	3-446
FJ2	10	J,K,CK,RN = 1,1,1,2	JK Flip-Flop with Reset, Positive Edge Trigger, 1X Drive	3-450
FJ2D2	11	J,K,CK,RN = 1,1,1,2	JK Flip-Flop with Reset, Positive Edge Trigger, 2X Drive	3-450
FJ2S	12	J,K,CK,TI,TE,RN = 1,1,1,1,2,2	JK Flip-Flop with Scan, Reset, Positive Edge Trigger, 1X Drive	3-454
FJ2SD2	13	J,K,CK,TI,TE,RN = 1,1,1,1,2,2	JK Flip-Flop with Reset, Scan, Positive Edge Trigger, 2X Drive	3-454
FJ4	11	J,K,CK,SN,RN = 1,1,1,2,2	JK Flip-Flop with Set, Reset, Positive Edge Trigger, 1X Drive	3-458
FJ4D2	12	J,K,CK,SN,RN = 1,1,11,2,2	JK Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, 1X Drive	3-458
FJ4S	13	J,K,CK,TI,TE,SN,RN = 1,1,1,1,2,2,2	JK Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, 1X Drive	3-462
FJ4SD2	14	J,K,CK,TI,TE,SN,RN = 1,1,1,1,2,2,2	JK Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, 2X Drive	3-462
FT2	7	CK,RN = 1,2	Toggle Flip-Flop with Reset, Positive Edge Trigger, 1X Drive	3-468
FT2D2	8	CK,RN = 1,2	Toggle Flip-Flop with Reset, Positive Edge Trigger, 2X Drive	3-468

Datasheets for HDA10000 3.3V Macrocells (5.0V Device) are on pages 3-20 to 3-472

Inputs: A, B
Output: Y
Input Loading (SL):
- AD2D2: All: 1
- AD2D4: All: 1
- AD2D6: All: 1

Maximum Fanout (Rec. SL):
- AD2D2: 56
- AD2D4: 112
- AD2D6: 168

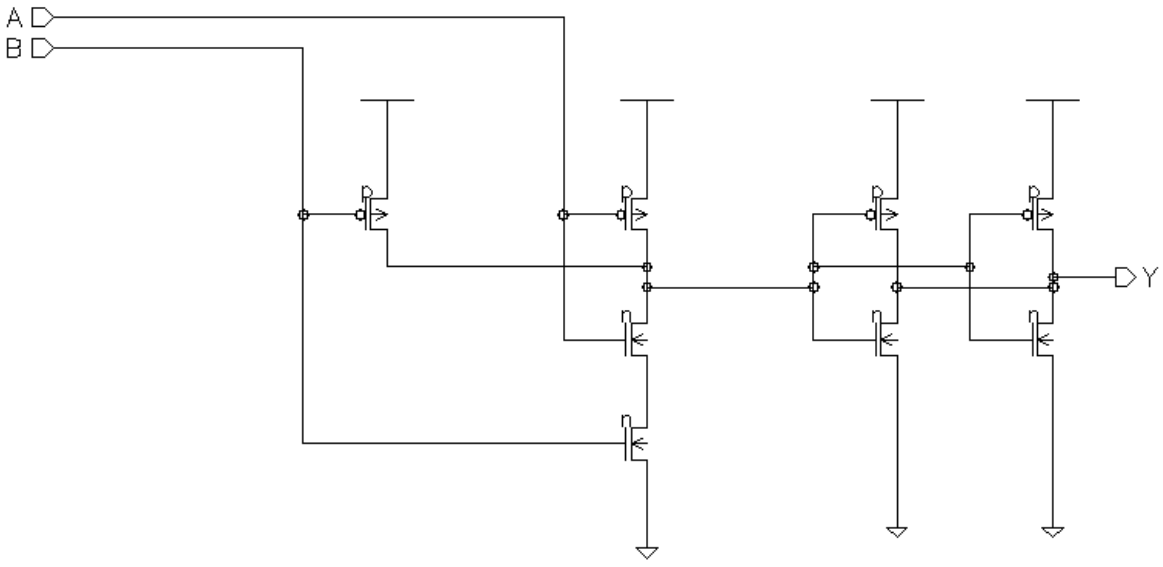
Gate Count:
- AD2D2: 2
- AD2D4: 3
- AD2D6: 4



Symbol

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table



Schematic

AD2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.23	0.18 + 0.023*SL	0.19 + 0.019*SL	0.20 + 0.019*SL
	tPHL	0.32	0.29 + 0.014*SL	0.30 + 0.010*SL	0.34 + 0.008*SL
	tR	0.19	0.10 + 0.042*SL	0.10 + 0.044*SL	0.08 + 0.045*SL
	tF	0.15	0.11 + 0.016*SL	0.11 + 0.016*SL	0.11 + 0.017*SL
B to Y	tPLH	0.19	0.14 + 0.023*SL	0.15 + 0.020*SL	0.16 + 0.019*SL
	tPHL	0.37	0.34 + 0.015*SL	0.35 + 0.010*SL	0.39 + 0.008*SL
	tR	0.20	0.12 + 0.042*SL	0.11 + 0.043*SL	0.07 + 0.045*SL
	tF	0.16	0.13 + 0.017*SL	0.13 + 0.016*SL	0.12 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

AD2D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.29	0.27 + 0.014*SL	0.28 + 0.010*SL	0.29 + 0.010*SL
	tPHL	0.38	0.36 + 0.007*SL	0.36 + 0.007*SL	0.40 + 0.005*SL
	tR	0.17	0.13 + 0.019*SL	0.12 + 0.022*SL	0.12 + 0.022*SL
	tF	0.16	0.15 + 0.005*SL	0.14 + 0.008*SL	0.15 + 0.008*SL
B to Y	tPLH	0.25	0.22 + 0.014*SL	0.23 + 0.010*SL	0.25 + 0.009*SL
	tPHL	0.41	0.39 + 0.012*SL	0.41 + 0.007*SL	0.45 + 0.005*SL
	tR	0.18	0.14 + 0.021*SL	0.13 + 0.021*SL	0.13 + 0.022*SL
	tF	0.17	0.16 + 0.008*SL	0.16 + 0.009*SL	0.18 + 0.007*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

AD2D6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

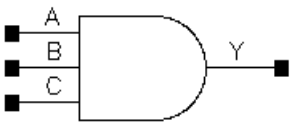
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.37	0.35 + 0.008*SL	0.35 + 0.007*SL	0.37 + 0.007*SL
	tPHL	0.44	0.43 + 0.007*SL	0.44 + 0.005*SL	0.46 + 0.004*SL
	tR	0.19	0.17 + 0.011*SL	0.16 + 0.014*SL	0.15 + 0.014*SL
	tF	0.20	0.19 + 0.003*SL	0.18 + 0.006*SL	0.21 + 0.005*SL
B to Y	tPLH	0.31	0.30 + 0.008*SL	0.30 + 0.007*SL	0.32 + 0.006*SL
	tPHL	0.47	0.46 + 0.007*SL	0.46 + 0.006*SL	0.49 + 0.004*SL
	tR	0.19	0.15 + 0.022*SL	0.17 + 0.013*SL	0.14 + 0.015*SL
	tF	0.21	0.22 + -0.002*SL	0.19 + 0.005*SL	0.20 + 0.005*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

Inputs: A, B, C
Output: Y
Input Loading (SL):
- AD3: All : 1
- AD3D3: All: 1
- AD3D5: All: 1
- AD3D8: All: 2

Maximum Fanout (Rec. SL):
- AD3: 28
- AD3D3: 84
- AD3D5: 140
- AD3D8: 224

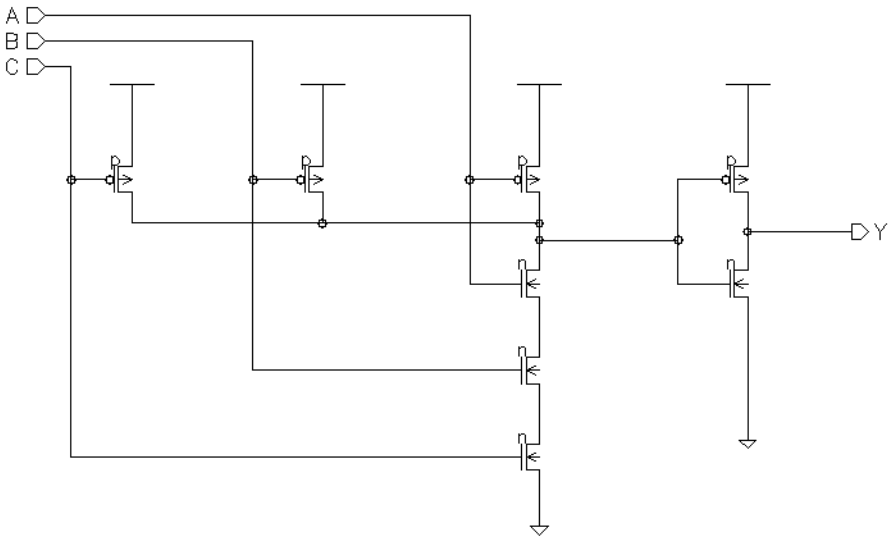
Gate Count:
- AD3 : 2
- AD3D3 : 3
- AD3D5 : 4
- AD3D8 : 7



Symbol

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Truth Table



Schematic

AD3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.29	0.21 + 0.040*SL	0.21 + 0.038*SL	0.22 + 0.037*SL
	t_{PHL}	0.29	0.24 + 0.025*SL	0.26 + 0.017*SL	0.29 + 0.016*SL
	t_R	0.29	0.12 + 0.081*SL	0.11 + 0.086*SL	0.07 + 0.088*SL
	t_F	0.16	0.09 + 0.035*SL	0.11 + 0.031*SL	0.06 + 0.033*SL
B to Y	t_{PLH}	0.28	0.19 + 0.044*SL	0.21 + 0.038*SL	0.22 + 0.037*SL
	t_{PHL}	0.34	0.29 + 0.026*SL	0.32 + 0.017*SL	0.34 + 0.016*SL
	t_R	0.28	0.11 + 0.089*SL	0.11 + 0.086*SL	0.07 + 0.088*SL
	t_F	0.18	0.12 + 0.029*SL	0.12 + 0.030*SL	0.06 + 0.033*SL
C to Y	t_{PLH}	0.25	0.16 + 0.042*SL	0.18 + 0.038*SL	0.18 + 0.037*SL
	t_{PHL}	0.38	0.33 + 0.025*SL	0.35 + 0.018*SL	0.38 + 0.016*SL
	t_R	0.29	0.13 + 0.083*SL	0.12 + 0.086*SL	0.07 + 0.088*SL
	t_F	0.20	0.15 + 0.023*SL	0.13 + 0.030*SL	0.08 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AD3D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.35	0.31 + 0.018*SL	0.33 + 0.014*SL	0.35 + 0.013*SL
	t_{PHL}	0.35	0.32 + 0.013*SL	0.34 + 0.008*SL	0.37 + 0.006*SL
	t_R	0.20	0.15 + 0.026*SL	0.14 + 0.029*SL	0.14 + 0.029*SL
	t_F	0.16	0.14 + 0.012*SL	0.14 + 0.010*SL	0.14 + 0.010*SL
B to Y	t_{PLH}	0.33	0.30 + 0.018*SL	0.31 + 0.014*SL	0.33 + 0.013*SL
	t_{PHL}	0.38	0.36 + 0.009*SL	0.36 + 0.009*SL	0.41 + 0.006*SL
	t_R	0.21	0.13 + 0.039*SL	0.17 + 0.027*SL	0.14 + 0.029*SL
	t_F	0.17	0.15 + 0.010*SL	0.15 + 0.010*SL	0.14 + 0.010*SL
C to Y	t_{PLH}	0.28	0.25 + 0.017*SL	0.26 + 0.014*SL	0.28 + 0.013*SL
	t_{PHL}	0.41	0.38 + 0.014*SL	0.40 + 0.009*SL	0.45 + 0.006*SL
	t_R	0.20	0.14 + 0.029*SL	0.15 + 0.028*SL	0.13 + 0.029*SL
	t_F	0.18	0.16 + 0.012*SL	0.16 + 0.010*SL	0.17 + 0.010*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AD3D5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.44	0.42 + 0.012*SL	0.43 + 0.009*SL	0.45 + 0.008*SL
	tPHL	0.40	0.38 + 0.012*SL	0.40 + 0.006*SL	0.43 + 0.004*SL
	tR	0.22	0.19 + 0.014*SL	0.19 + 0.016*SL	0.17 + 0.017*SL
	tF	0.19	0.16 + 0.013*SL	0.18 + 0.006*SL	0.19 + 0.006*SL
B to Y	tPLH	0.41	0.39 + 0.012*SL	0.40 + 0.009*SL	0.42 + 0.008*SL
	tPHL	0.44	0.42 + 0.008*SL	0.43 + 0.006*SL	0.47 + 0.004*SL
	tR	0.23	0.19 + 0.015*SL	0.19 + 0.016*SL	0.18 + 0.017*SL
	tF	0.19	0.17 + 0.008*SL	0.17 + 0.007*SL	0.20 + 0.006*SL
C to Y	tPLH	0.37	0.35 + 0.011*SL	0.35 + 0.009*SL	0.37 + 0.008*SL
	tPHL	0.46	0.45 + 0.008*SL	0.45 + 0.006*SL	0.49 + 0.005*SL
	tR	0.23	0.19 + 0.017*SL	0.19 + 0.016*SL	0.18 + 0.017*SL
	tF	0.21	0.22 + -0.003*SL	0.19 + 0.007*SL	0.19 + 0.006*SL

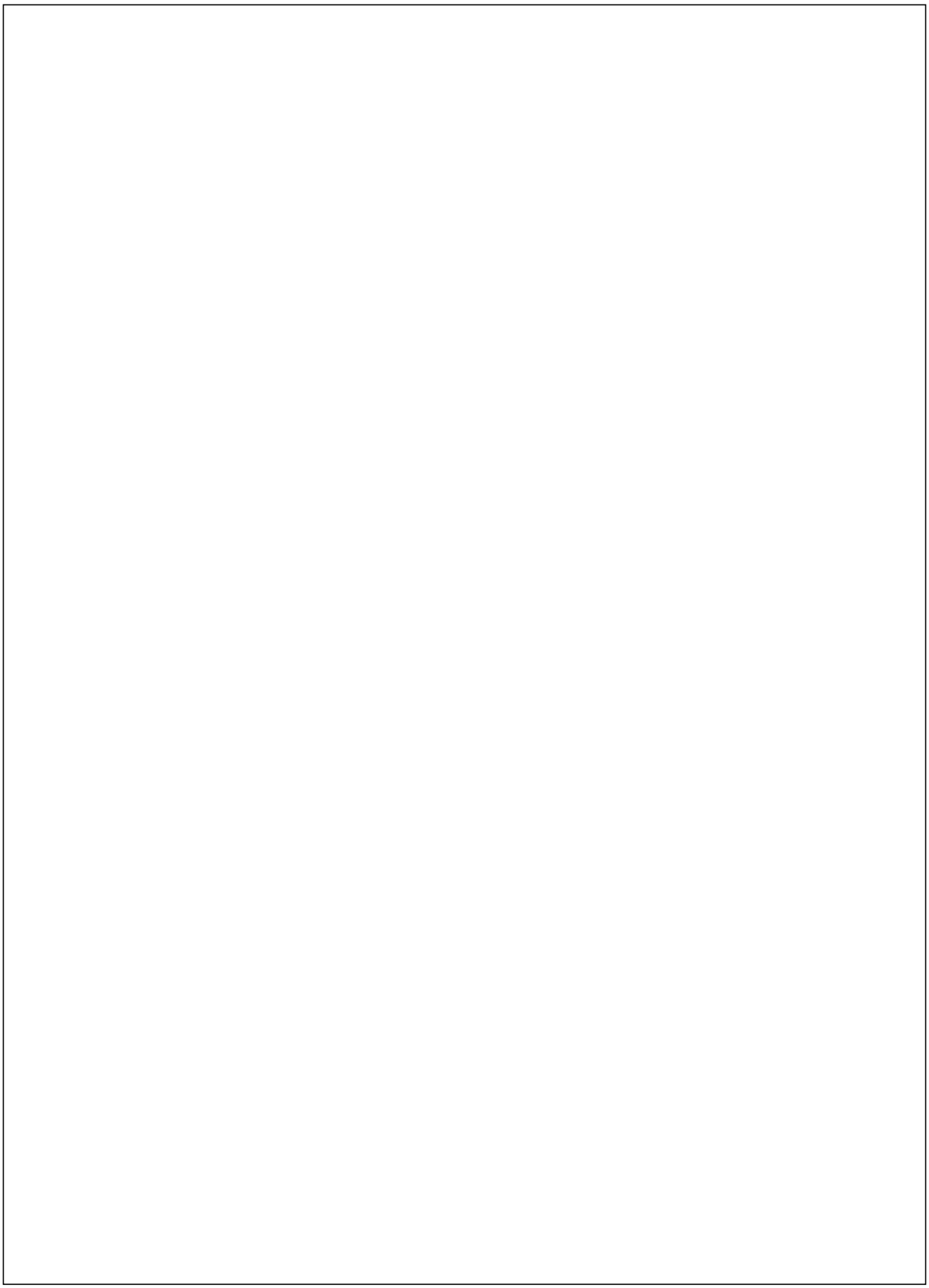
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AD3D8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.41	0.39 + 0.008*SL	0.40 + 0.006*SL	0.41 + 0.005*SL
	tPHL	0.36	0.36 + 0.003*SL	0.35 + 0.004*SL	0.38 + 0.003*SL
	tR	0.19	0.17 + 0.013*SL	0.17 + 0.010*SL	0.16 + 0.011*SL
	tF	0.16	0.15 + 0.004*SL	0.15 + 0.005*SL	0.18 + 0.003*SL
B to Y	tPLH	0.38	0.36 + 0.008*SL	0.37 + 0.006*SL	0.38 + 0.005*SL
	tPHL	0.39	0.39 + 0.003*SL	0.38 + 0.005*SL	0.41 + 0.003*SL
	tR	0.20	0.17 + 0.014*SL	0.18 + 0.011*SL	0.20 + 0.010*SL
	tF	0.17	0.16 + 0.006*SL	0.16 + 0.005*SL	0.18 + 0.004*SL
C to Y	tPLH	0.34	0.32 + 0.007*SL	0.32 + 0.006*SL	0.34 + 0.005*SL
	tPHL	0.43	0.41 + 0.008*SL	0.42 + 0.004*SL	0.44 + 0.003*SL
	tR	0.20	0.19 + 0.007*SL	0.18 + 0.011*SL	0.18 + 0.010*SL
	tF	0.19	0.19 + 0.002*SL	0.18 + 0.004*SL	0.19 + 0.004*SL

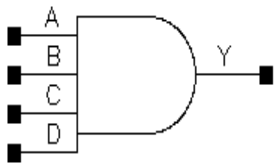
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D
Output: Y
Input Loading (SL):
- AD4D2: All: 1
- AD4D4: All: 1
- AD4D6: All: 2

Maximum Fanout (Rec. SL):
- AD4D2: 56
- AD4D4: 112
- AD4D6: 168

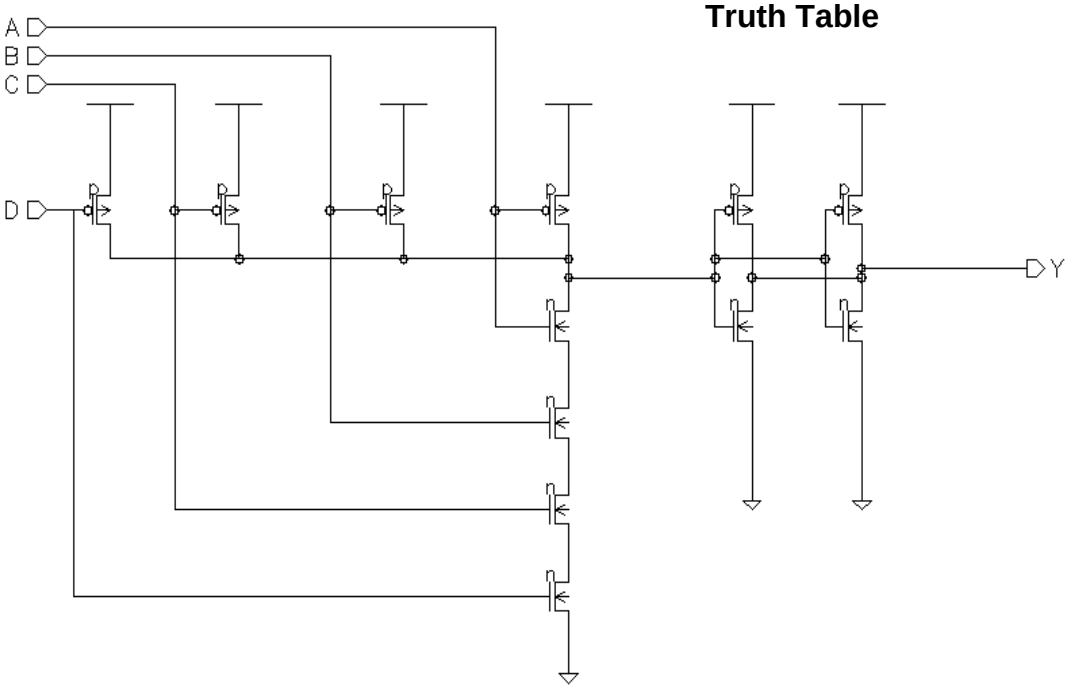
Gate Count:
- AD4D2: 3
- AD4D4: 4
- AD4D6: 7



Symbol

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Truth Table



Schematic

AD4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.38	0.33 + 0.025*SL	0.34 + 0.021*SL	0.38 + 0.019*SL
	t_{PHL}	0.31	0.28 + 0.016*SL	0.30 + 0.011*SL	0.34 + 0.009*SL
	t_R	0.24	0.15 + 0.042*SL	0.15 + 0.043*SL	0.12 + 0.045*SL
	t_F	0.16	0.13 + 0.012*SL	0.12 + 0.017*SL	0.13 + 0.016*SL
B to Y	t_{PLH}	0.38	0.34 + 0.024*SL	0.35 + 0.020*SL	0.37 + 0.019*SL
	t_{PHL}	0.36	0.33 + 0.015*SL	0.34 + 0.011*SL	0.38 + 0.009*SL
	t_R	0.25	0.18 + 0.036*SL	0.15 + 0.043*SL	0.12 + 0.045*SL
	t_F	0.17	0.15 + 0.014*SL	0.14 + 0.016*SL	0.13 + 0.016*SL
C to Y	t_{PLH}	0.36	0.31 + 0.025*SL	0.33 + 0.020*SL	0.35 + 0.019*SL
	t_{PHL}	0.39	0.35 + 0.016*SL	0.37 + 0.011*SL	0.42 + 0.009*SL
	t_R	0.24	0.16 + 0.040*SL	0.15 + 0.043*SL	0.13 + 0.045*SL
	t_F	0.18	0.15 + 0.017*SL	0.15 + 0.015*SL	0.14 + 0.016*SL
D to Y	t_{PLH}	0.34	0.29 + 0.025*SL	0.31 + 0.020*SL	0.33 + 0.019*SL
	t_{PHL}	0.41	0.37 + 0.021*SL	0.40 + 0.011*SL	0.45 + 0.009*SL
	t_R	0.25	0.18 + 0.034*SL	0.16 + 0.043*SL	0.13 + 0.044*SL
	t_F	0.19	0.14 + 0.029*SL	0.18 + 0.015*SL	0.15 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AD4D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.49	0.45 + 0.017*SL	0.47 + 0.011*SL	0.49 + 0.010*SL
	tPHL	0.37	0.35 + 0.010*SL	0.36 + 0.007*SL	0.40 + 0.005*SL
	tR	0.25	0.21 + 0.021*SL	0.20 + 0.021*SL	0.19 + 0.022*SL
	tF	0.17	0.15 + 0.011*SL	0.16 + 0.008*SL	0.16 + 0.008*SL
B to Y	tPLH	0.48	0.45 + 0.016*SL	0.46 + 0.011*SL	0.49 + 0.010*SL
	tPHL	0.41	0.39 + 0.011*SL	0.40 + 0.007*SL	0.44 + 0.005*SL
	tR	0.25	0.21 + 0.021*SL	0.21 + 0.021*SL	0.19 + 0.022*SL
	tF	0.19	0.16 + 0.012*SL	0.18 + 0.008*SL	0.19 + 0.007*SL
C to Y	tPLH	0.45	0.42 + 0.015*SL	0.43 + 0.011*SL	0.46 + 0.010*SL
	tPHL	0.44	0.42 + 0.011*SL	0.43 + 0.007*SL	0.47 + 0.005*SL
	tR	0.25	0.22 + 0.013*SL	0.20 + 0.021*SL	0.19 + 0.022*SL
	tF	0.20	0.18 + 0.007*SL	0.18 + 0.008*SL	0.19 + 0.007*SL
D to Y	tPLH	0.43	0.40 + 0.014*SL	0.41 + 0.011*SL	0.43 + 0.010*SL
	tPHL	0.46	0.44 + 0.010*SL	0.45 + 0.008*SL	0.49 + 0.005*SL
	tR	0.25	0.20 + 0.025*SL	0.22 + 0.020*SL	0.19 + 0.022*SL
	tF	0.21	0.18 + 0.013*SL	0.20 + 0.008*SL	0.20 + 0.008*SL

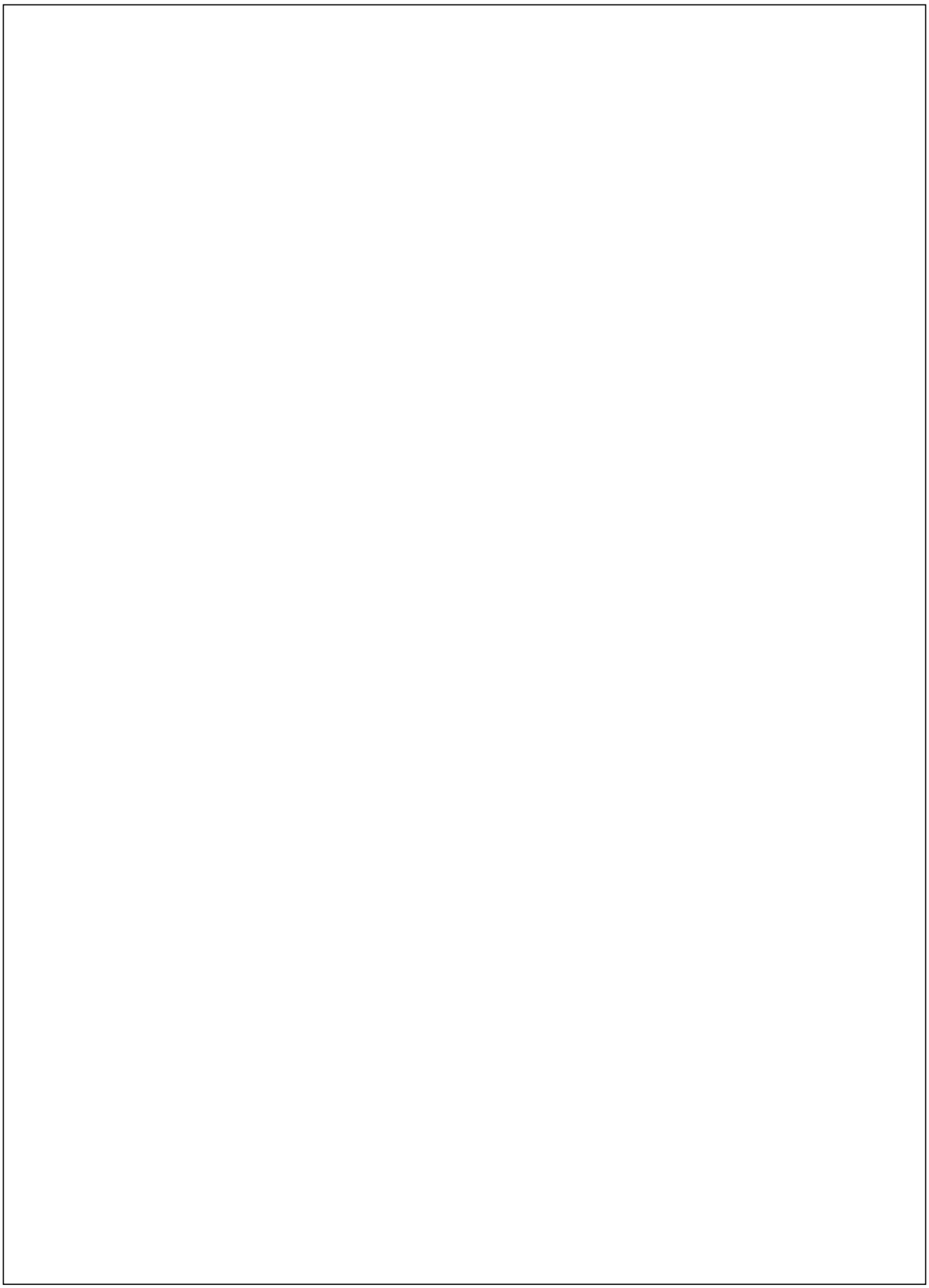
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AD4D6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.45	0.43 + 0.010*SL	0.44 + 0.008*SL	0.46 + 0.007*SL
	tPHL	0.33	0.32 + 0.007*SL	0.32 + 0.005*SL	0.35 + 0.004*SL
	tR	0.22	0.20 + 0.011*SL	0.19 + 0.014*SL	0.18 + 0.014*SL
	tF	0.15	0.15 + 0.001*SL	0.13 + 0.006*SL	0.17 + 0.005*SL
B to Y	tPLH	0.44	0.42 + 0.009*SL	0.43 + 0.008*SL	0.45 + 0.007*SL
	tPHL	0.36	0.35 + 0.007*SL	0.36 + 0.005*SL	0.39 + 0.004*SL
	tR	0.23	0.20 + 0.014*SL	0.20 + 0.013*SL	0.19 + 0.014*SL
	tF	0.16	0.16 + 0.003*SL	0.15 + 0.006*SL	0.17 + 0.005*SL
C to Y	tPLH	0.42	0.39 + 0.012*SL	0.40 + 0.008*SL	0.43 + 0.007*SL
	tPHL	0.39	0.38 + 0.005*SL	0.38 + 0.006*SL	0.41 + 0.004*SL
	tR	0.24	0.22 + 0.009*SL	0.21 + 0.013*SL	0.19 + 0.014*SL
	tF	0.17	0.16 + 0.007*SL	0.16 + 0.006*SL	0.18 + 0.005*SL
D to Y	tPLH	0.39	0.37 + 0.011*SL	0.38 + 0.008*SL	0.40 + 0.007*SL
	tPHL	0.42	0.40 + 0.010*SL	0.41 + 0.005*SL	0.44 + 0.004*SL
	tR	0.22	0.18 + 0.018*SL	0.20 + 0.014*SL	0.18 + 0.014*SL
	tF	0.19	0.18 + 0.006*SL	0.18 + 0.005*SL	0.19 + 0.005*SL

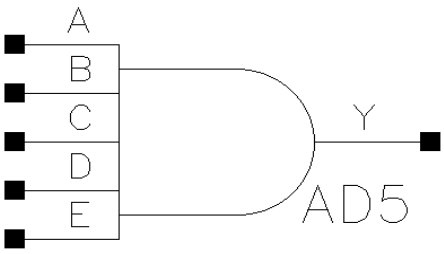
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D,E
Output: Y
Input Loading (SL):
- AD5: All: 1
- AD5D3: All: 1
- AD5D6: All: 2

Maximum Fanout (Rec. SL):
- AD5: 28
- AD5D3: 72
- AD5D6: 144

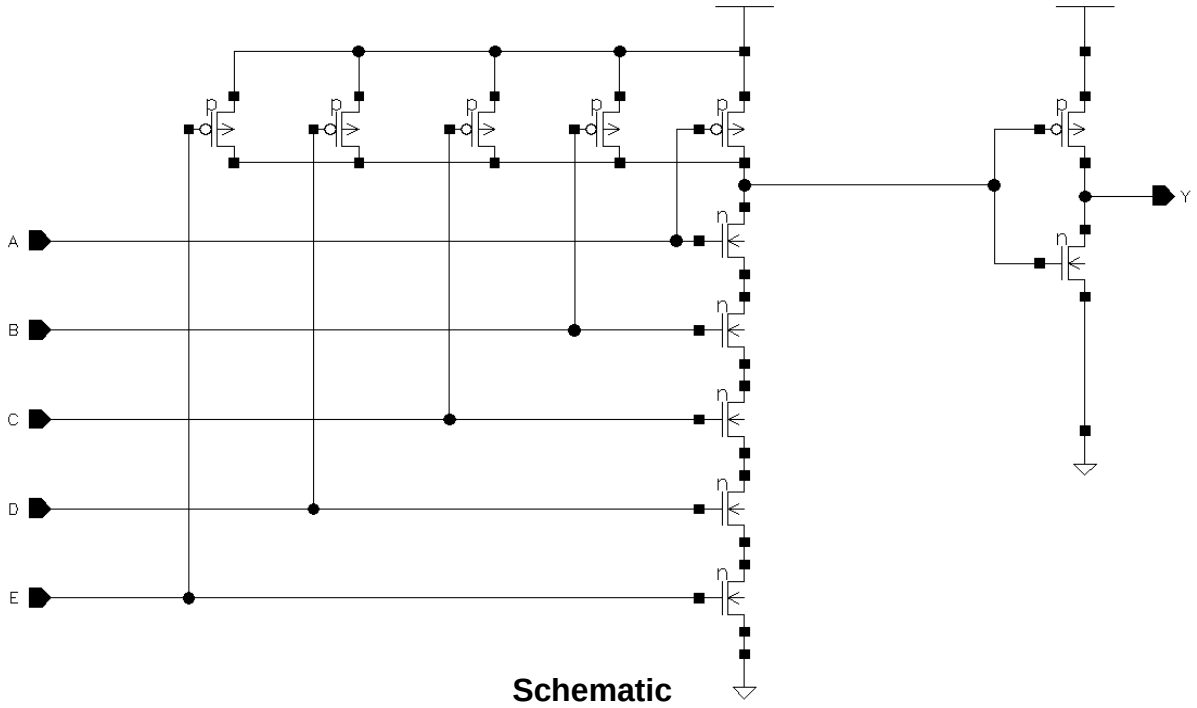
Gate Count:
- AD5: 3
- AD5D3: 4
- AD5D6: 8



Symbol

A	B	C	D	E	Y
0	x	x	x	x	0
x	0	x	x	x	0
x	x	0	x	x	0
x	x	x	0	x	0
1	1	1	1	1	1

Truth Table



Schematic

AD5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.42	0.32 + 0.048*SL	0.35 + 0.039*SL	0.38 + 0.037*SL
	t_{PHL}	0.30	0.24 + 0.027*SL	0.27 + 0.018*SL	0.30 + 0.016*SL
	t_R	0.31	0.14 + 0.088*SL	0.14 + 0.086*SL	0.11 + 0.087*SL
	t_F	0.17	0.10 + 0.037*SL	0.12 + 0.030*SL	0.07 + 0.033*SL
B to Y	t_{PLH}	0.44	0.34 + 0.047*SL	0.37 + 0.039*SL	0.40 + 0.038*SL
	t_{PHL}	0.34	0.28 + 0.029*SL	0.32 + 0.018*SL	0.34 + 0.016*SL
	t_R	0.32	0.16 + 0.084*SL	0.15 + 0.086*SL	0.12 + 0.087*SL
	t_F	0.18	0.11 + 0.035*SL	0.13 + 0.030*SL	0.08 + 0.033*SL
C to Y	t_{PLH}	0.44	0.34 + 0.046*SL	0.36 + 0.039*SL	0.40 + 0.037*SL
	t_{PHL}	0.38	0.32 + 0.029*SL	0.35 + 0.018*SL	0.39 + 0.016*SL
	t_R	0.33	0.16 + 0.087*SL	0.17 + 0.085*SL	0.12 + 0.087*SL
	t_F	0.19	0.11 + 0.041*SL	0.15 + 0.029*SL	0.09 + 0.033*SL
D to Y	t_{PLH}	0.43	0.34 + 0.046*SL	0.36 + 0.039*SL	0.39 + 0.037*SL
	t_{PHL}	0.40	0.34 + 0.031*SL	0.38 + 0.018*SL	0.42 + 0.016*SL
	t_R	0.33	0.17 + 0.083*SL	0.16 + 0.085*SL	0.12 + 0.087*SL
	t_F	0.21	0.14 + 0.037*SL	0.16 + 0.029*SL	0.09 + 0.032*SL
E to Y	t_{PLH}	0.41	0.31 + 0.047*SL	0.34 + 0.039*SL	0.36 + 0.037*SL
	t_{PHL}	0.41	0.35 + 0.033*SL	0.39 + 0.019*SL	0.44 + 0.016*SL
	t_R	0.34	0.16 + 0.085*SL	0.17 + 0.085*SL	0.12 + 0.087*SL
	t_F	0.23	0.15 + 0.039*SL	0.18 + 0.029*SL	0.12 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

AD5D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.52	0.48 + 0.019*SL	0.49 + 0.015*SL	0.52 + 0.013*SL
	tPHL	0.35	0.33 + 0.009*SL	0.33 + 0.008*SL	0.38 + 0.006*SL
	tR	0.27	0.23 + 0.021*SL	0.20 + 0.029*SL	0.20 + 0.029*SL
	tF	0.16	0.14 + 0.011*SL	0.14 + 0.010*SL	0.14 + 0.010*SL
B to Y	tPLH	0.53	0.49 + 0.020*SL	0.51 + 0.015*SL	0.54 + 0.013*SL
	tPHL	0.38	0.35 + 0.012*SL	0.36 + 0.009*SL	0.42 + 0.006*SL
	tR	0.27	0.23 + 0.021*SL	0.21 + 0.029*SL	0.21 + 0.029*SL
	tF	0.17	0.15 + 0.014*SL	0.16 + 0.011*SL	0.17 + 0.010*SL
C to Y	tPLH	0.52	0.48 + 0.019*SL	0.50 + 0.015*SL	0.53 + 0.013*SL
	tPHL	0.41	0.38 + 0.014*SL	0.40 + 0.009*SL	0.45 + 0.006*SL
	tR	0.28	0.23 + 0.024*SL	0.22 + 0.028*SL	0.20 + 0.029*SL
	tF	0.19	0.16 + 0.014*SL	0.17 + 0.010*SL	0.17 + 0.010*SL
D to Y	tPLH	0.51	0.47 + 0.020*SL	0.49 + 0.015*SL	0.52 + 0.013*SL
	tPHL	0.43	0.40 + 0.016*SL	0.42 + 0.009*SL	0.47 + 0.006*SL
	tR	0.27	0.24 + 0.019*SL	0.21 + 0.029*SL	0.20 + 0.029*SL
	tF	0.21	0.18 + 0.013*SL	0.19 + 0.010*SL	0.19 + 0.010*SL
E to Y	tPLH	0.49	0.45 + 0.019*SL	0.46 + 0.015*SL	0.49 + 0.013*SL
	tPHL	0.45	0.42 + 0.015*SL	0.44 + 0.009*SL	0.49 + 0.007*SL
	tR	0.28	0.24 + 0.020*SL	0.21 + 0.028*SL	0.21 + 0.029*SL
	tF	0.22	0.20 + 0.009*SL	0.20 + 0.010*SL	0.20 + 0.010*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

AD5D6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

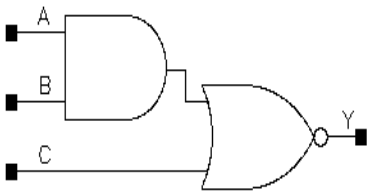
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.54	0.51 + 0.013*SL	0.53 + 0.008*SL	0.55 + 0.007*SL
	t_{PHL}	0.34	0.33 + 0.003*SL	0.33 + 0.005*SL	0.35 + 0.004*SL
	t_R	0.26	0.24 + 0.013*SL	0.24 + 0.013*SL	0.20 + 0.015*SL
	t_F	0.16	0.16 + -0.003*SL	0.14 + 0.006*SL	0.14 + 0.006*SL
B to Y	t_{PLH}	0.55	0.52 + 0.011*SL	0.53 + 0.008*SL	0.55 + 0.007*SL
	t_{PHL}	0.36	0.35 + 0.006*SL	0.35 + 0.006*SL	0.39 + 0.004*SL
	t_R	0.27	0.25 + 0.010*SL	0.24 + 0.014*SL	0.24 + 0.014*SL
	t_F	0.16	0.15 + 0.004*SL	0.15 + 0.007*SL	0.19 + 0.004*SL
C to Y	t_{PLH}	0.54	0.52 + 0.010*SL	0.53 + 0.008*SL	0.55 + 0.007*SL
	t_{PHL}	0.39	0.38 + 0.008*SL	0.38 + 0.006*SL	0.42 + 0.004*SL
	t_R	0.27	0.25 + 0.012*SL	0.24 + 0.014*SL	0.24 + 0.014*SL
	t_F	0.18	0.14 + 0.016*SL	0.18 + 0.005*SL	0.17 + 0.005*SL
D to Y	t_{PLH}	0.53	0.51 + 0.010*SL	0.51 + 0.008*SL	0.54 + 0.007*SL
	t_{PHL}	0.42	0.40 + 0.009*SL	0.41 + 0.006*SL	0.45 + 0.004*SL
	t_R	0.27	0.25 + 0.011*SL	0.24 + 0.014*SL	0.22 + 0.015*SL
	t_F	0.20	0.18 + 0.012*SL	0.20 + 0.005*SL	0.20 + 0.005*SL
E to Y	t_{PLH}	0.51	0.49 + 0.011*SL	0.50 + 0.008*SL	0.52 + 0.007*SL
	t_{PHL}	0.43	0.42 + 0.007*SL	0.42 + 0.006*SL	0.46 + 0.004*SL
	t_R	0.27	0.25 + 0.008*SL	0.23 + 0.014*SL	0.23 + 0.014*SL
	t_F	0.22	0.21 + 0.005*SL	0.21 + 0.005*SL	0.21 + 0.005*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: A, B, C
Output: Y
Input Loading(SL):
- AO21: All : 1
- AO21D2: All : 2
- AO21D4: All : 1
- AO21D6: All : 1

Maximum Fanout (Rec. SL):
- AO21: 14
- AO21D2: 28
- AO21D4: 112
- AO21D6: 168

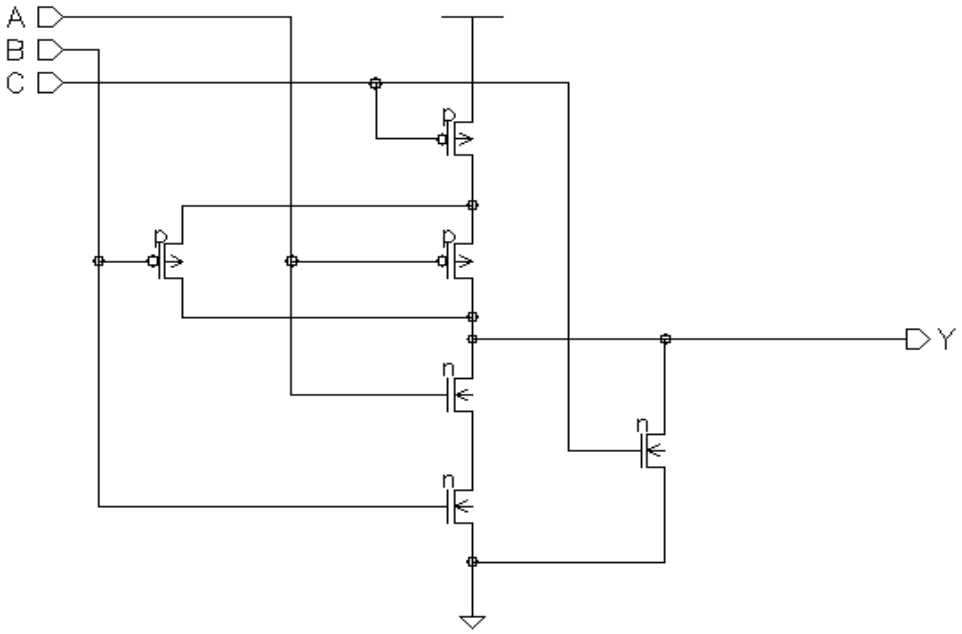
Gate Count:
- AO21 : 2
- AO21D2 : 3
- AO21D4: 4
- AO21D6: 5



Symbol

A	B	C	Y
x	x	1	0
0	x	0	1
x	0	0	1
1	1	x	0

Truth Table



Schematic

AO21 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.44	0.29 + 0.076*SL	0.30 + 0.072*SL	0.27 + 0.073*SL
	t_{PHL}	0.11	0.01 + 0.052*SL	0.07 + 0.030*SL	0.16 + 0.026*SL
	t_R	0.64	0.34 + 0.153*SL	0.29 + 0.170*SL	0.21 + 0.174*SL
	t_F	0.38	0.27 + 0.051*SL	0.27 + 0.053*SL	0.20 + 0.056*SL
B to Y	t_{PLH}	0.50	0.36 + 0.071*SL	0.36 + 0.072*SL	0.33 + 0.073*SL
	t_{PHL}	0.07	-0.02 + 0.044*SL	0.03 + 0.029*SL	0.08 + 0.026*SL
	t_R	0.73	0.42 + 0.151*SL	0.37 + 0.170*SL	0.29 + 0.174*SL
	t_F	0.35	0.25 + 0.051*SL	0.24 + 0.053*SL	0.16 + 0.057*SL
C to Y	t_{PLH}	0.48	0.34 + 0.071*SL	0.34 + 0.072*SL	0.31 + 0.073*SL
	t_{PHL}	0.08	0.01 + 0.035*SL	0.05 + 0.022*SL	0.15 + 0.017*SL
	t_R	0.71	0.39 + 0.156*SL	0.35 + 0.171*SL	0.29 + 0.174*SL
	t_F	0.38	0.32 + 0.032*SL	0.33 + 0.028*SL	0.27 + 0.031*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

AO21D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.36	0.28 + 0.041*SL	0.29 + 0.036*SL	0.29 + 0.036*SL
	t_{PHL}	0.06	-0.00 + 0.032*SL	0.04 + 0.019*SL	0.14 + 0.014*SL
	t_R	0.49	0.34 + 0.079*SL	0.33 + 0.081*SL	0.24 + 0.086*SL
	t_F	0.32	0.25 + 0.034*SL	0.27 + 0.027*SL	0.26 + 0.028*SL
B to Y	t_{PLH}	0.43	0.36 + 0.036*SL	0.36 + 0.035*SL	0.34 + 0.036*SL
	t_{PHL}	0.03	-0.02 + 0.025*SL	0.00 + 0.017*SL	0.07 + 0.014*SL
	t_R	0.57	0.41 + 0.081*SL	0.41 + 0.082*SL	0.33 + 0.086*SL
	t_F	0.30	0.25 + 0.027*SL	0.25 + 0.026*SL	0.21 + 0.028*SL
C to Y	t_{PLH}	0.41	0.34 + 0.035*SL	0.34 + 0.035*SL	0.33 + 0.036*SL
	t_{PHL}	0.04	-0.00 + 0.022*SL	0.02 + 0.014*SL	0.11 + 0.009*SL
	t_R	0.54	0.38 + 0.080*SL	0.38 + 0.083*SL	0.32 + 0.086*SL
	t_F	0.35	0.33 + 0.013*SL	0.32 + 0.014*SL	0.32 + 0.014*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

AO21D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.53	0.51 + 0.011*SL	0.51 + 0.010*SL	0.52 + 0.010*SL
	tPHL	0.28	0.26 + 0.010*SL	0.27 + 0.006*SL	0.30 + 0.005*SL
	tR	0.14	0.10 + 0.018*SL	0.09 + 0.022*SL	0.08 + 0.022*SL
	tF	0.13	0.12 + 0.007*SL	0.11 + 0.009*SL	0.11 + 0.008*SL
B to Y	tPLH	0.61	0.59 + 0.011*SL	0.59 + 0.010*SL	0.60 + 0.009*SL
	tPHL	0.26	0.24 + 0.010*SL	0.25 + 0.007*SL	0.28 + 0.005*SL
	tR	0.14	0.09 + 0.025*SL	0.10 + 0.021*SL	0.08 + 0.022*SL
	tF	0.13	0.11 + 0.008*SL	0.11 + 0.009*SL	0.13 + 0.008*SL
C to Y	tPLH	0.59	0.57 + 0.010*SL	0.57 + 0.010*SL	0.57 + 0.009*SL
	tPHL	0.28	0.26 + 0.009*SL	0.27 + 0.006*SL	0.30 + 0.005*SL
	tR	0.14	0.10 + 0.022*SL	0.10 + 0.021*SL	0.08 + 0.022*SL
	tF	0.13	0.11 + 0.008*SL	0.11 + 0.009*SL	0.11 + 0.008*SL

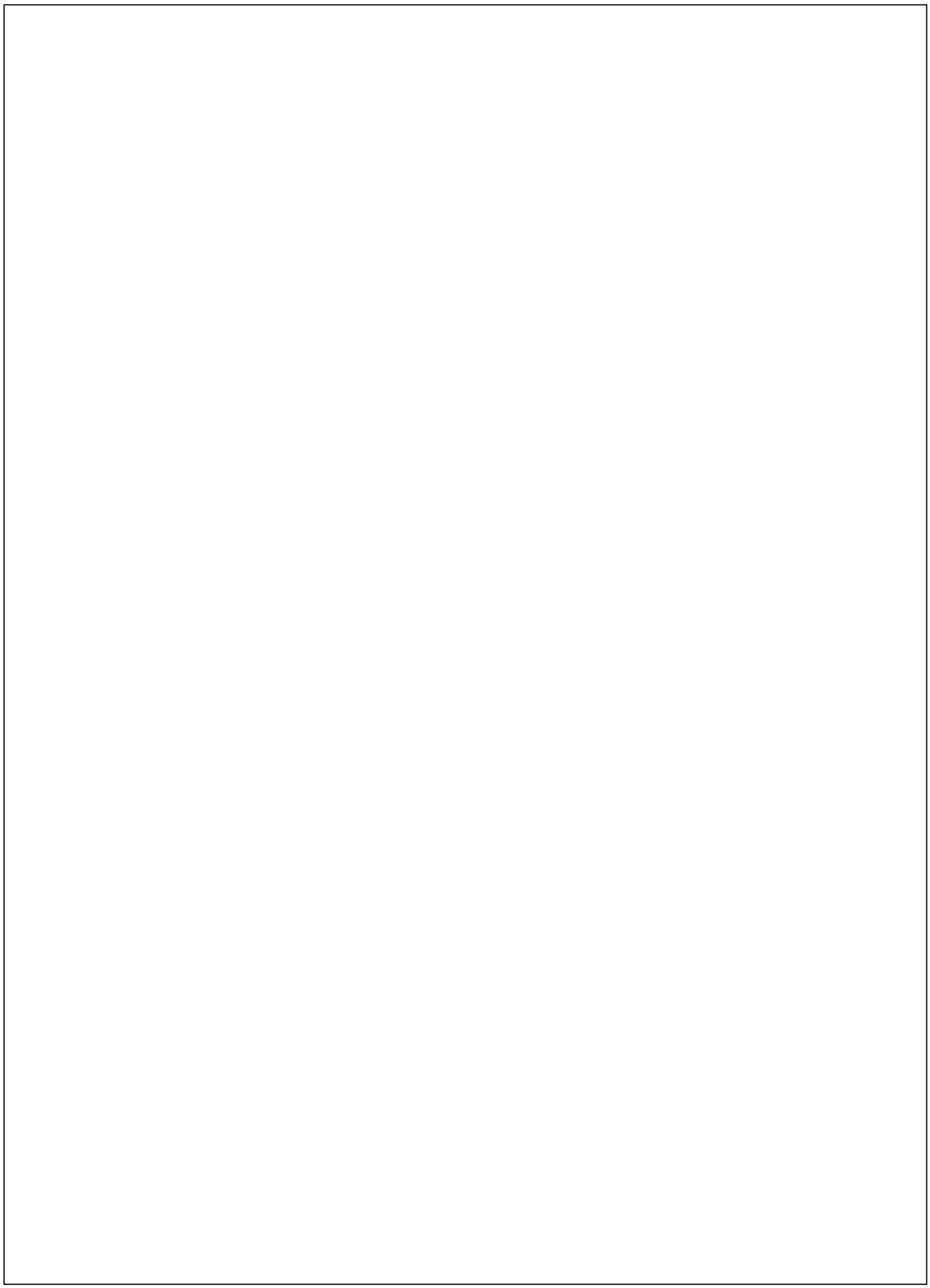
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO21D6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.57	0.56 + 0.008*SL	0.56 + 0.007*SL	0.57 + 0.006*SL
	tPHL	0.33	0.32 + 0.006*SL	0.32 + 0.005*SL	0.35 + 0.004*SL
	tR	0.13	0.10 + 0.016*SL	0.11 + 0.015*SL	0.11 + 0.014*SL
	tF	0.16	0.15 + 0.004*SL	0.15 + 0.006*SL	0.17 + 0.005*SL
B to Y	tPLH	0.65	0.64 + 0.007*SL	0.64 + 0.007*SL	0.64 + 0.007*SL
	tPHL	0.31	0.30 + 0.007*SL	0.30 + 0.005*SL	0.34 + 0.004*SL
	tR	0.14	0.09 + 0.021*SL	0.12 + 0.014*SL	0.09 + 0.015*SL
	tF	0.16	0.15 + 0.003*SL	0.14 + 0.007*SL	0.18 + 0.005*SL
C to Y	tPLH	0.63	0.61 + 0.008*SL	0.61 + 0.007*SL	0.63 + 0.006*SL
	tPHL	0.33	0.32 + 0.006*SL	0.33 + 0.005*SL	0.35 + 0.004*SL
	tR	0.14	0.10 + 0.021*SL	0.12 + 0.014*SL	0.10 + 0.014*SL
	tF	0.16	0.14 + 0.008*SL	0.15 + 0.006*SL	0.17 + 0.005*SL

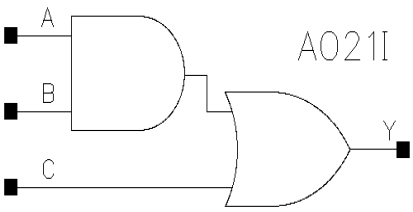
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C
Output: Y
Input Loading(SL):
- AO21I: All: 1
- AO21ID3: All: 1
- AO2ID5: All: 1
- AO21ID8: All: 2

Maximum Fanout (Rec. SL):
- AO21I: 28
- AO21ID3: 84
- AO2ID5: 120
- AO21ID8: 224

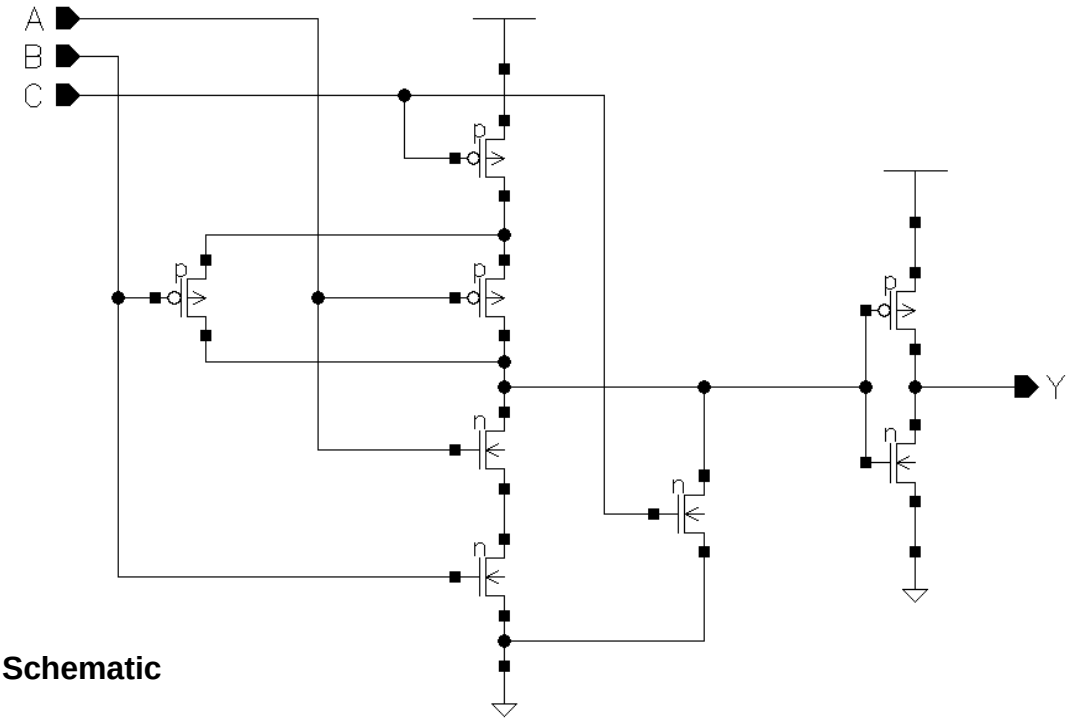
Gate Count:
- AO21I: 2
- AO21ID3: 3
- AO2ID5: 4
- AO21ID8: 7



Symbol

A	B	C	Y
x	x	1	1
0	x	0	0
x	0	0	0
1	1	x	1

Truth Table



Schematic

AO21I Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.20	0.12 + 0.040*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
	tPHL	0.41	0.36 + 0.028*SL	0.39 + 0.018*SL	0.43 + 0.016*SL
	tR	0.27	0.12 + 0.078*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
	tF	0.20	0.12 + 0.042*SL	0.15 + 0.030*SL	0.10 + 0.033*SL
B to Y	tPLH	0.19	0.11 + 0.039*SL	0.11 + 0.038*SL	0.11 + 0.038*SL
	tPHL	0.48	0.42 + 0.031*SL	0.45 + 0.019*SL	0.51 + 0.016*SL
	tR	0.27	0.11 + 0.083*SL	0.09 + 0.086*SL	0.06 + 0.088*SL
	tF	0.22	0.15 + 0.033*SL	0.16 + 0.030*SL	0.12 + 0.032*SL
C to Y	tPLH	0.20	0.12 + 0.039*SL	0.13 + 0.037*SL	0.11 + 0.038*SL
	tPHL	0.46	0.40 + 0.030*SL	0.43 + 0.019*SL	0.49 + 0.016*SL
	tR	0.27	0.11 + 0.079*SL	0.09 + 0.086*SL	0.06 + 0.088*SL
	tF	0.21	0.14 + 0.037*SL	0.16 + 0.030*SL	0.12 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO21ID3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.25	0.22 + 0.017*SL	0.23 + 0.013*SL	0.24 + 0.012*SL
	tPHL	0.49	0.47 + 0.014*SL	0.48 + 0.009*SL	0.53 + 0.007*SL
	tR	0.18	0.12 + 0.027*SL	0.12 + 0.028*SL	0.10 + 0.029*SL
	tF	0.21	0.18 + 0.015*SL	0.19 + 0.011*SL	0.19 + 0.011*SL
B to Y	tPLH	0.21	0.18 + 0.014*SL	0.19 + 0.013*SL	0.21 + 0.012*SL
	tPHL	0.55	0.52 + 0.017*SL	0.54 + 0.010*SL	0.59 + 0.007*SL
	tR	0.18	0.13 + 0.025*SL	0.12 + 0.028*SL	0.10 + 0.029*SL
	tF	0.22	0.20 + 0.010*SL	0.20 + 0.012*SL	0.22 + 0.011*SL
C to Y	tPLH	0.22	0.18 + 0.016*SL	0.19 + 0.013*SL	0.21 + 0.012*SL
	tPHL	0.52	0.49 + 0.019*SL	0.51 + 0.010*SL	0.57 + 0.007*SL
	tR	0.17	0.10 + 0.034*SL	0.12 + 0.027*SL	0.09 + 0.029*SL
	tF	0.24	0.21 + 0.012*SL	0.22 + 0.011*SL	0.22 + 0.010*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO21ID5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.33	0.31 + 0.010*SL	0.32 + 0.008*SL	0.33 + 0.008*SL
	tPHL	0.60	0.58 + 0.010*SL	0.59 + 0.007*SL	0.63 + 0.005*SL
	tR	0.18	0.14 + 0.020*SL	0.15 + 0.017*SL	0.13 + 0.017*SL
	tF	0.26	0.26 + 0.004*SL	0.25 + 0.007*SL	0.26 + 0.007*SL
B to Y	tPLH	0.28	0.25 + 0.012*SL	0.26 + 0.009*SL	0.28 + 0.008*SL
	tPHL	0.65	0.63 + 0.012*SL	0.64 + 0.007*SL	0.68 + 0.006*SL
	tR	0.18	0.15 + 0.012*SL	0.14 + 0.017*SL	0.14 + 0.017*SL
	tF	0.29	0.26 + 0.013*SL	0.28 + 0.007*SL	0.29 + 0.006*SL
C to Y	tPLH	0.27	0.25 + 0.011*SL	0.26 + 0.008*SL	0.27 + 0.008*SL
	tPHL	0.63	0.60 + 0.013*SL	0.62 + 0.008*SL	0.66 + 0.005*SL
	tR	0.16	0.13 + 0.018*SL	0.13 + 0.016*SL	0.11 + 0.017*SL
	tF	0.28	0.25 + 0.014*SL	0.27 + 0.007*SL	0.29 + 0.006*SL

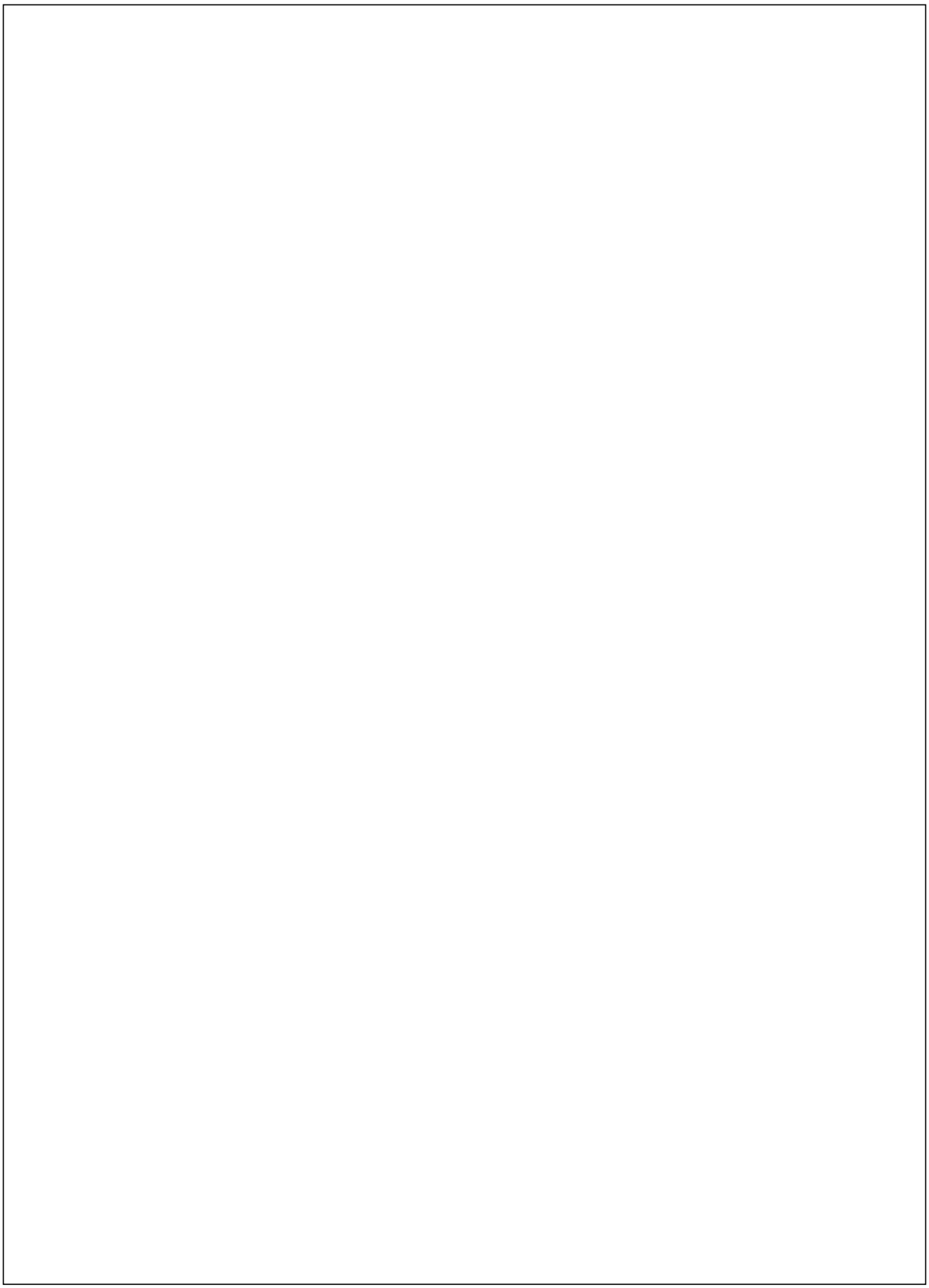
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO21ID8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.30	0.29 + 0.007*SL	0.29 + 0.006*SL	0.30 + 0.005*SL
	tPHL	0.55	0.53 + 0.007*SL	0.54 + 0.005*SL	0.57 + 0.004*SL
	tR	0.16	0.14 + 0.007*SL	0.13 + 0.011*SL	0.13 + 0.011*SL
	tF	0.22	0.22 + 0.004*SL	0.21 + 0.005*SL	0.24 + 0.004*SL
B to Y	tPLH	0.25	0.23 + 0.009*SL	0.24 + 0.006*SL	0.26 + 0.005*SL
	tPHL	0.60	0.58 + 0.006*SL	0.59 + 0.005*SL	0.61 + 0.004*SL
	tR	0.16	0.13 + 0.013*SL	0.14 + 0.011*SL	0.14 + 0.011*SL
	tF	0.25	0.24 + 0.004*SL	0.24 + 0.005*SL	0.25 + 0.004*SL
C to Y	tPLH	0.23	0.22 + 0.006*SL	0.22 + 0.005*SL	0.23 + 0.005*SL
	tPHL	0.58	0.57 + 0.006*SL	0.57 + 0.005*SL	0.60 + 0.004*SL
	tR	0.14	0.13 + 0.006*SL	0.12 + 0.011*SL	0.13 + 0.011*SL
	tF	0.25	0.24 + 0.004*SL	0.24 + 0.005*SL	0.26 + 0.004*SL

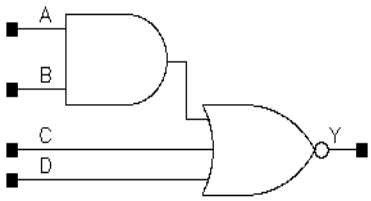
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D
Output: Y
Input Loading(SL):
- AO211: All : 1
- AO211D2: All : 2
- AO211D3: All: 1
- AO211D7: All: 1

Maximum Fanout (Rec. SL):
- AO211: 9
- AO211D2: 18
- AO211D3: 84
- AO211D7: 196

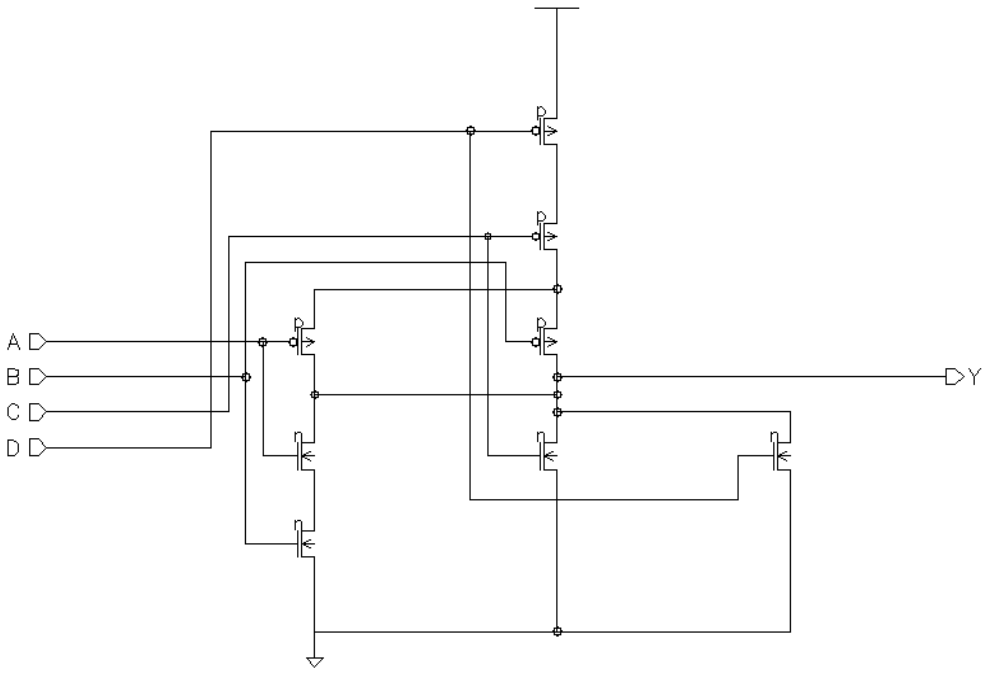
Gate Count:
- AO211: 2
- AO211D2: 4
- AO211D3: 4
- AO211D7: 6



Symbol

A	B	C	D	Y
1	1	x	x	0
x	x	1	x	0
x	x	x	1	0
x	0	0	0	1
0	x	0	0	1

Truth Table



Schematic

AO211 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.56	0.35 + 0.102*SL	0.35 + 0.105*SL	0.31 + 0.106*SL
	tPHL	0.12	0.01 + 0.051*SL	0.08 + 0.030*SL	0.16 + 0.026*SL
	tR	0.94	0.47 + 0.235*SL	0.43 + 0.248*SL	0.38 + 0.251*SL
	tF	0.38	0.27 + 0.052*SL	0.27 + 0.053*SL	0.21 + 0.056*SL
B to Y	tPLH	0.64	0.44 + 0.100*SL	0.43 + 0.104*SL	0.39 + 0.106*SL
	tPHL	0.08	-0.01 + 0.042*SL	0.03 + 0.029*SL	0.09 + 0.026*SL
	tR	1.06	0.58 + 0.237*SL	0.55 + 0.248*SL	0.50 + 0.251*SL
	tF	0.36	0.25 + 0.052*SL	0.25 + 0.053*SL	0.17 + 0.057*SL
C to Y	tPLH	0.67	0.46 + 0.104*SL	0.45 + 0.105*SL	0.43 + 0.106*SL
	tPHL	0.09	0.01 + 0.036*SL	0.06 + 0.022*SL	0.16 + 0.017*SL
	tR	1.06	0.58 + 0.239*SL	0.55 + 0.248*SL	0.51 + 0.251*SL
	tF	0.38	0.32 + 0.031*SL	0.32 + 0.029*SL	0.28 + 0.032*SL
D to Y	tPLH	0.65	0.45 + 0.102*SL	0.44 + 0.105*SL	0.41 + 0.106*SL
	tPHL	0.09	0.02 + 0.037*SL	0.06 + 0.022*SL	0.16 + 0.017*SL
	tR	1.05	0.57 + 0.238*SL	0.54 + 0.249*SL	0.51 + 0.251*SL
	tF	0.41	0.34 + 0.035*SL	0.36 + 0.029*SL	0.30 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO211D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.46	0.35 + 0.054*SL	0.36 + 0.053*SL	0.33 + 0.054*SL
	tPHL	0.07	0.01 + 0.030*SL	0.04 + 0.019*SL	0.14 + 0.014*SL
	tR	0.73	0.50 + 0.118*SL	0.47 + 0.127*SL	0.41 + 0.129*SL
	tF	0.33	0.27 + 0.031*SL	0.28 + 0.027*SL	0.27 + 0.028*SL
B to Y	tPLH	0.55	0.45 + 0.051*SL	0.45 + 0.052*SL	0.42 + 0.054*SL
	tPHL	0.04	-0.01 + 0.024*SL	0.01 + 0.017*SL	0.07 + 0.014*SL
	tR	0.85	0.61 + 0.120*SL	0.59 + 0.127*SL	0.54 + 0.130*SL
	tF	0.31	0.24 + 0.032*SL	0.26 + 0.026*SL	0.21 + 0.028*SL
C to Y	tPLH	0.58	0.47 + 0.053*SL	0.47 + 0.054*SL	0.45 + 0.054*SL
	tPHL	0.05	0.01 + 0.021*SL	0.03 + 0.014*SL	0.11 + 0.009*SL
	tR	0.85	0.61 + 0.120*SL	0.59 + 0.127*SL	0.55 + 0.129*SL
	tF	0.35	0.31 + 0.016*SL	0.32 + 0.015*SL	0.32 + 0.015*SL
D to Y	tPLH	0.56	0.46 + 0.053*SL	0.45 + 0.053*SL	0.44 + 0.054*SL
	tPHL	0.05	0.01 + 0.022*SL	0.03 + 0.014*SL	0.12 + 0.009*SL
	tR	0.84	0.59 + 0.124*SL	0.58 + 0.127*SL	0.54 + 0.129*SL
	tF	0.37	0.34 + 0.018*SL	0.35 + 0.014*SL	0.34 + 0.014*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO211D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.61	0.59 + 0.013*SL	0.59 + 0.013*SL	0.59 + 0.013*SL
	tPHL	0.27	0.25 + 0.010*SL	0.25 + 0.007*SL	0.28 + 0.006*SL
	tR	0.15	0.09 + 0.029*SL	0.09 + 0.028*SL	0.06 + 0.030*SL
	tF	0.12	0.10 + 0.011*SL	0.10 + 0.011*SL	0.09 + 0.011*SL
B to Y	tPLH	0.71	0.67 + 0.015*SL	0.68 + 0.013*SL	0.69 + 0.013*SL
	tPHL	0.24	0.23 + 0.008*SL	0.23 + 0.007*SL	0.26 + 0.006*SL
	tR	0.16	0.09 + 0.033*SL	0.11 + 0.028*SL	0.07 + 0.030*SL
	tF	0.13	0.11 + 0.009*SL	0.11 + 0.010*SL	0.09 + 0.011*SL
C to Y	tPLH	0.72	0.69 + 0.014*SL	0.69 + 0.013*SL	0.71 + 0.012*SL
	tPHL	0.26	0.24 + 0.011*SL	0.25 + 0.007*SL	0.28 + 0.006*SL
	tR	0.16	0.10 + 0.030*SL	0.11 + 0.028*SL	0.07 + 0.030*SL
	tF	0.12	0.09 + 0.012*SL	0.10 + 0.011*SL	0.10 + 0.011*SL
D to Y	tPLH	0.71	0.68 + 0.014*SL	0.68 + 0.013*SL	0.69 + 0.012*SL
	tPHL	0.27	0.25 + 0.011*SL	0.26 + 0.007*SL	0.28 + 0.006*SL
	tR	0.16	0.11 + 0.030*SL	0.11 + 0.028*SL	0.08 + 0.030*SL
	tF	0.12	0.10 + 0.009*SL	0.09 + 0.011*SL	0.11 + 0.011*SL

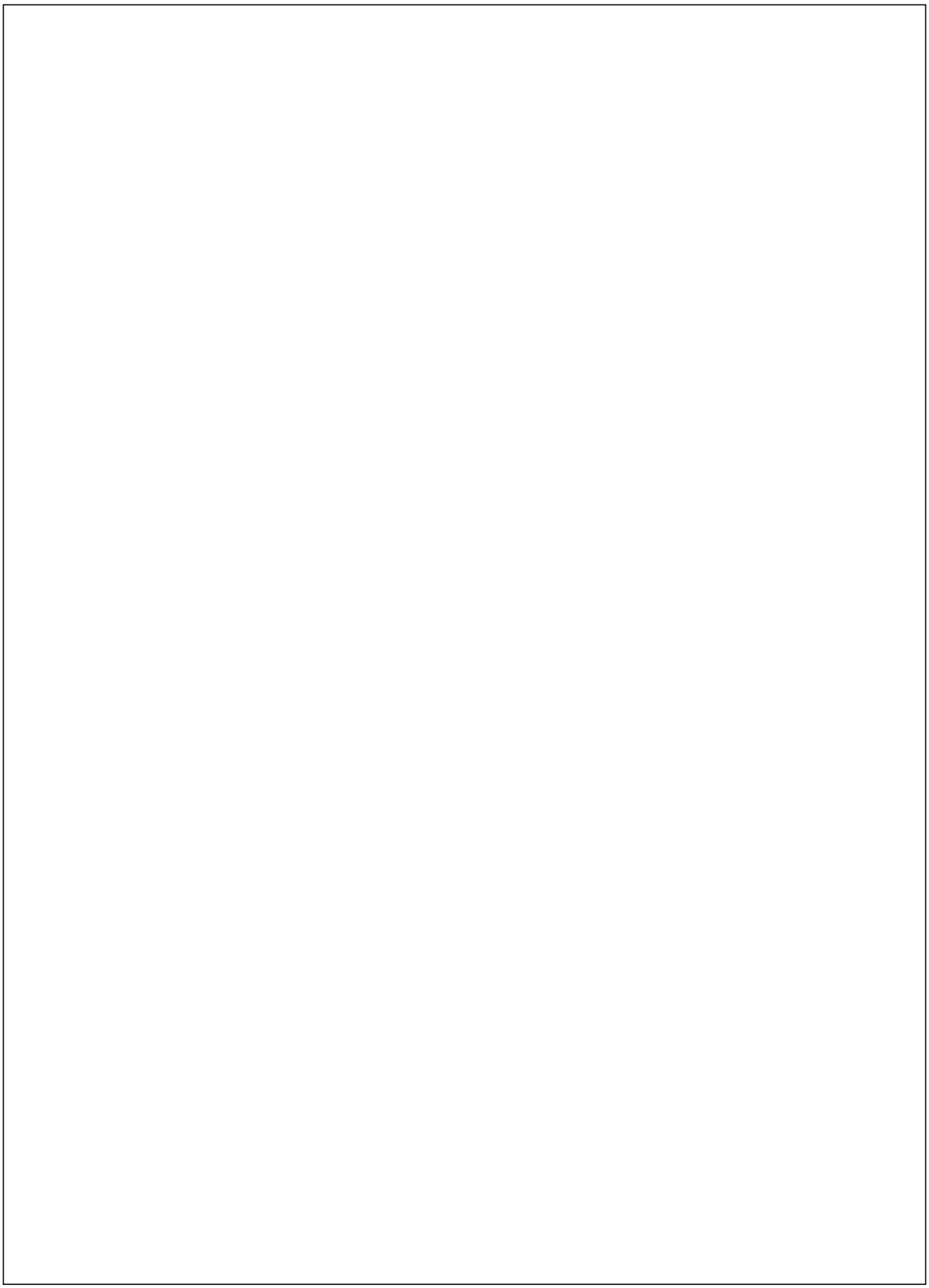
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO211D7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.71	0.69 + 0.007*SL	0.70 + 0.006*SL	0.71 + 0.005*SL
	tPHL	0.37	0.36 + 0.006*SL	0.36 + 0.005*SL	0.39 + 0.003*SL
	tR	0.15	0.11 + 0.017*SL	0.13 + 0.012*SL	0.14 + 0.012*SL
	tF	0.19	0.17 + 0.006*SL	0.18 + 0.005*SL	0.18 + 0.005*SL
B to Y	tPLH	0.81	0.79 + 0.007*SL	0.80 + 0.006*SL	0.81 + 0.005*SL
	tPHL	0.35	0.34 + 0.008*SL	0.35 + 0.005*SL	0.38 + 0.003*SL
	tR	0.15	0.12 + 0.014*SL	0.13 + 0.013*SL	0.16 + 0.011*SL
	tF	0.19	0.18 + 0.004*SL	0.18 + 0.005*SL	0.21 + 0.004*SL
C to Y	tPLH	0.82	0.81 + 0.007*SL	0.81 + 0.006*SL	0.82 + 0.006*SL
	tPHL	0.37	0.35 + 0.007*SL	0.36 + 0.005*SL	0.38 + 0.004*SL
	tR	0.15	0.13 + 0.013*SL	0.13 + 0.011*SL	0.11 + 0.013*SL
	tF	0.19	0.18 + 0.004*SL	0.18 + 0.004*SL	0.17 + 0.005*SL
D to Y	tPLH	0.81	0.80 + 0.009*SL	0.80 + 0.006*SL	0.81 + 0.005*SL
	tPHL	0.38	0.37 + 0.006*SL	0.37 + 0.005*SL	0.40 + 0.003*SL
	tR	0.15	0.12 + 0.014*SL	0.13 + 0.011*SL	0.11 + 0.012*SL
	tF	0.19	0.18 + 0.002*SL	0.17 + 0.005*SL	0.19 + 0.004*SL

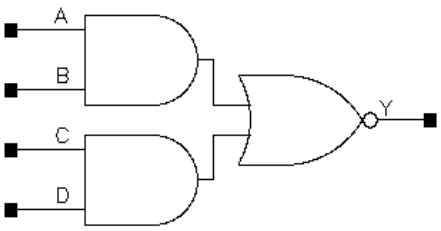
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D
Output: Y
Input Loading(SL):
- AO22: All : 1
- AO22D2: All : 2
- AO22D3: All : 1
- AO22D7: All : 1

Maximum Fanout (Rec. SL):
- AO22: 14
- AO22D2: 28
- AO22D3: 84
- AO22D7: 196

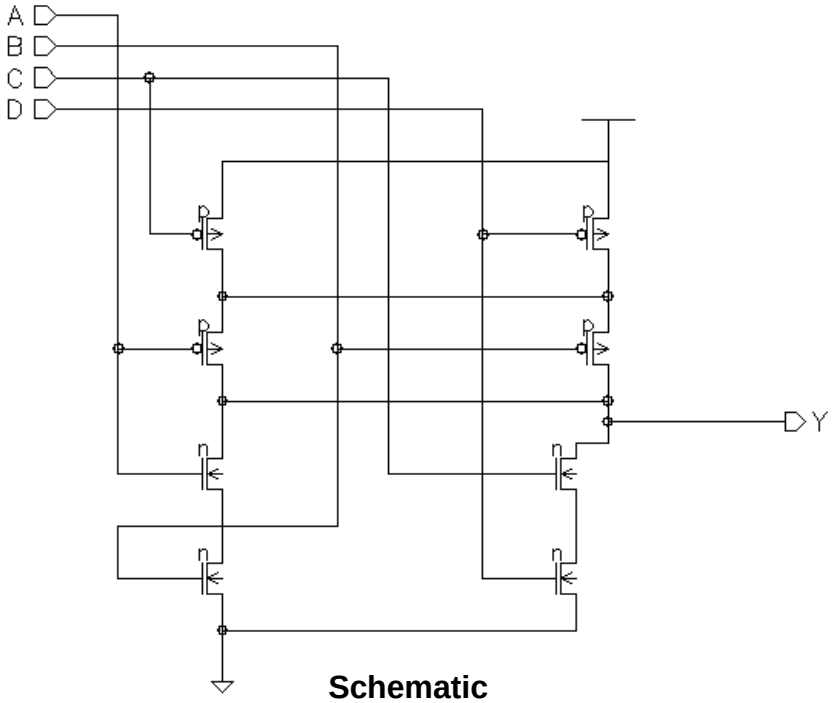
Gate Count:
- AO22: 2
- AO22D2: 4
- AO22D3: 5
- AO22D7: 7



Symbol

A	B	C	D	Y
1	1	x	x	0
x	x	1	1	0
0	x	0	x	1
0	x	x	0	1
x	0	x	0	1
x	0	0	x	1

Truth Table



Schematic

AO22 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.49	0.35 + 0.070*SL	0.35 + 0.069*SL	0.33 + 0.071*SL
	tPHL	0.13	0.03 + 0.048*SL	0.09 + 0.030*SL	0.17 + 0.026*SL
	tR	0.70	0.41 + 0.145*SL	0.36 + 0.161*SL	0.28 + 0.165*SL
	tF	0.42	0.33 + 0.046*SL	0.31 + 0.053*SL	0.24 + 0.056*SL
B to Y	tPLH	0.55	0.41 + 0.068*SL	0.41 + 0.069*SL	0.38 + 0.070*SL
	tPHL	0.09	0.01 + 0.040*SL	0.04 + 0.029*SL	0.09 + 0.026*SL
	tR	0.77	0.47 + 0.151*SL	0.44 + 0.161*SL	0.36 + 0.165*SL
	tF	0.39	0.31 + 0.042*SL	0.27 + 0.053*SL	0.20 + 0.057*SL
C to Y	tPLH	0.47	0.33 + 0.071*SL	0.33 + 0.071*SL	0.32 + 0.072*SL
	tPHL	0.17	0.09 + 0.043*SL	0.13 + 0.029*SL	0.19 + 0.026*SL
	tR	0.70	0.40 + 0.152*SL	0.36 + 0.164*SL	0.29 + 0.168*SL
	tF	0.49	0.39 + 0.048*SL	0.38 + 0.052*SL	0.29 + 0.056*SL
D to Y	tPLH	0.52	0.39 + 0.068*SL	0.38 + 0.070*SL	0.36 + 0.071*SL
	tPHL	0.12	0.04 + 0.038*SL	0.08 + 0.028*SL	0.12 + 0.026*SL
	tR	0.77	0.46 + 0.153*SL	0.44 + 0.162*SL	0.36 + 0.165*SL
	tF	0.45	0.36 + 0.044*SL	0.33 + 0.053*SL	0.25 + 0.057*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO22D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.42	0.35 + 0.038*SL	0.35 + 0.036*SL	0.35 + 0.036*SL
	tPHL	0.08	0.03 + 0.028*SL	0.06 + 0.018*SL	0.14 + 0.014*SL
	tR	0.57	0.42 + 0.078*SL	0.40 + 0.083*SL	0.33 + 0.086*SL
	tF	0.38	0.33 + 0.026*SL	0.33 + 0.026*SL	0.29 + 0.028*SL
B to Y	tPLH	0.49	0.42 + 0.036*SL	0.42 + 0.035*SL	0.40 + 0.036*SL
	tPHL	0.05	-0.00 + 0.023*SL	0.02 + 0.016*SL	0.08 + 0.014*SL
	tR	0.64	0.50 + 0.072*SL	0.47 + 0.082*SL	0.41 + 0.085*SL
	tF	0.35	0.30 + 0.028*SL	0.30 + 0.026*SL	0.25 + 0.028*SL
C to Y	tPLH	0.41	0.33 + 0.036*SL	0.33 + 0.036*SL	0.32 + 0.036*SL
	tPHL	0.13	0.08 + 0.024*SL	0.10 + 0.017*SL	0.17 + 0.014*SL
	tR	0.56	0.40 + 0.079*SL	0.39 + 0.082*SL	0.33 + 0.086*SL
	tF	0.45	0.39 + 0.027*SL	0.40 + 0.026*SL	0.36 + 0.028*SL
D to Y	tPLH	0.47	0.40 + 0.035*SL	0.39 + 0.035*SL	0.38 + 0.036*SL
	tPHL	0.08	0.04 + 0.021*SL	0.05 + 0.016*SL	0.10 + 0.014*SL
	tR	0.64	0.49 + 0.075*SL	0.47 + 0.082*SL	0.41 + 0.085*SL
	tF	0.41	0.37 + 0.020*SL	0.36 + 0.026*SL	0.30 + 0.028*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO22D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.58	0.55 + 0.015*SL	0.56 + 0.013*SL	0.57 + 0.012*SL
	tPHL	0.30	0.28 + 0.009*SL	0.29 + 0.008*SL	0.32 + 0.006*SL
	tR	0.15	0.10 + 0.025*SL	0.09 + 0.029*SL	0.06 + 0.030*SL
	tF	0.12	0.10 + 0.009*SL	0.10 + 0.012*SL	0.12 + 0.011*SL
B to Y	tPLH	0.65	0.62 + 0.014*SL	0.63 + 0.013*SL	0.63 + 0.013*SL
	tPHL	0.27	0.24 + 0.012*SL	0.26 + 0.007*SL	0.28 + 0.006*SL
	tR	0.15	0.08 + 0.031*SL	0.09 + 0.028*SL	0.07 + 0.030*SL
	tF	0.12	0.10 + 0.012*SL	0.10 + 0.011*SL	0.09 + 0.012*SL
C to Y	tPLH	0.57	0.54 + 0.014*SL	0.54 + 0.013*SL	0.55 + 0.012*SL
	tPHL	0.35	0.33 + 0.010*SL	0.34 + 0.008*SL	0.38 + 0.006*SL
	tR	0.15	0.10 + 0.027*SL	0.10 + 0.028*SL	0.07 + 0.030*SL
	tF	0.12	0.09 + 0.016*SL	0.11 + 0.011*SL	0.11 + 0.011*SL
D to Y	tPLH	0.63	0.60 + 0.014*SL	0.61 + 0.012*SL	0.61 + 0.013*SL
	tPHL	0.32	0.30 + 0.008*SL	0.30 + 0.008*SL	0.33 + 0.006*SL
	tR	0.15	0.09 + 0.030*SL	0.10 + 0.028*SL	0.06 + 0.030*SL
	tF	0.12	0.11 + 0.009*SL	0.10 + 0.011*SL	0.11 + 0.011*SL

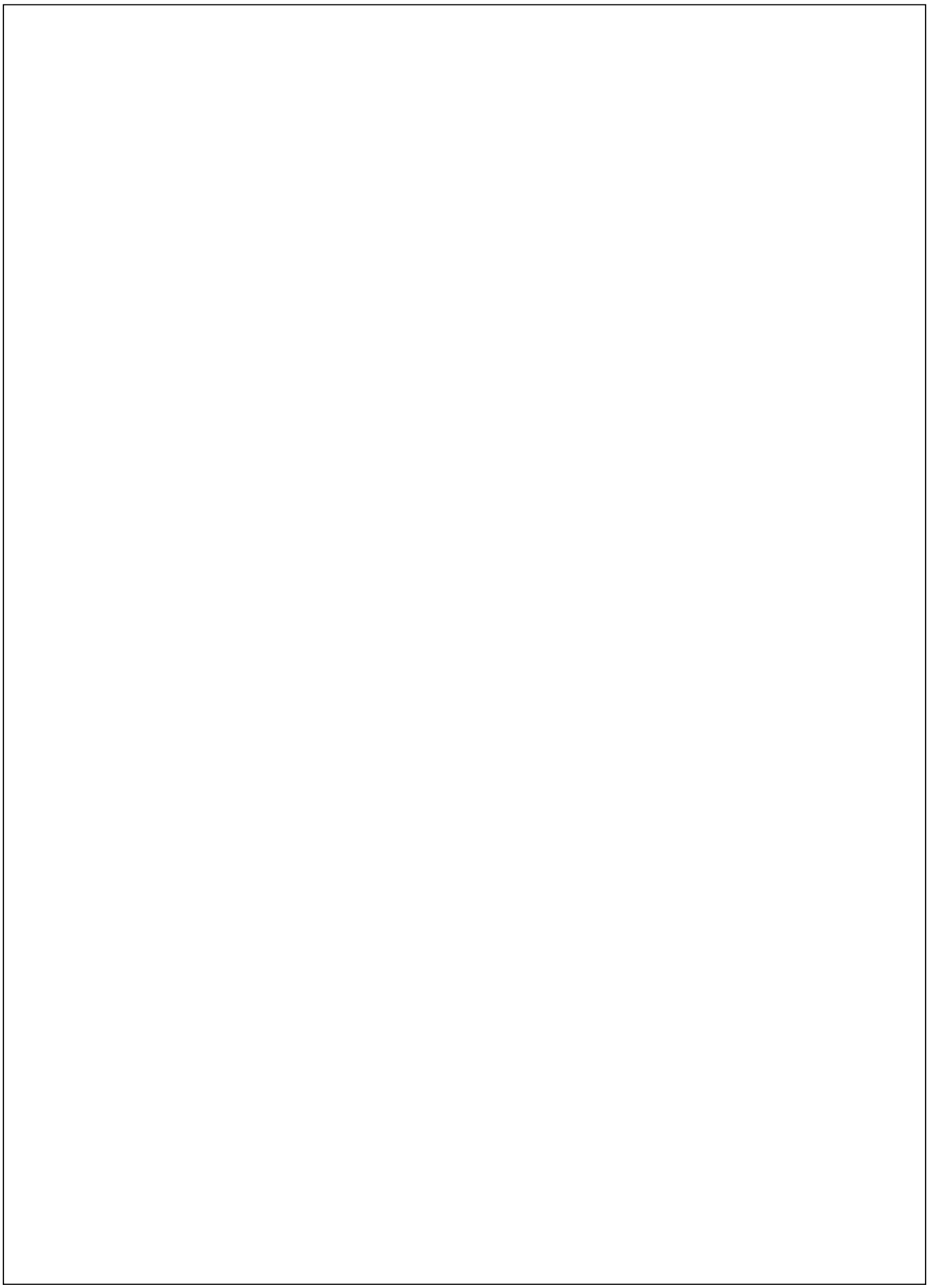
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

AO22D7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.67	0.66 + 0.007*SL	0.66 + 0.006*SL	0.67 + 0.005*SL
	tPHL	0.40	0.39 + 0.007*SL	0.40 + 0.005*SL	0.42 + 0.004*SL
	tR	0.14	0.11 + 0.014*SL	0.12 + 0.012*SL	0.12 + 0.012*SL
	tF	0.19	0.18 + 0.004*SL	0.18 + 0.005*SL	0.19 + 0.004*SL
B to Y	tPLH	0.74	0.73 + 0.008*SL	0.73 + 0.006*SL	0.74 + 0.005*SL
	tPHL	0.38	0.36 + 0.009*SL	0.38 + 0.005*SL	0.40 + 0.004*SL
	tR	0.15	0.12 + 0.010*SL	0.12 + 0.012*SL	0.11 + 0.012*SL
	tF	0.19	0.19 + 0.002*SL	0.18 + 0.005*SL	0.20 + 0.004*SL
C to Y	tPLH	0.65	0.64 + 0.006*SL	0.64 + 0.006*SL	0.65 + 0.006*SL
	tPHL	0.46	0.44 + 0.008*SL	0.45 + 0.005*SL	0.48 + 0.004*SL
	tR	0.14	0.11 + 0.015*SL	0.12 + 0.012*SL	0.13 + 0.012*SL
	tF	0.20	0.20 + 0.002*SL	0.19 + 0.004*SL	0.18 + 0.005*SL
D to Y	tPLH	0.72	0.71 + 0.007*SL	0.71 + 0.006*SL	0.72 + 0.006*SL
	tPHL	0.43	0.42 + 0.007*SL	0.42 + 0.005*SL	0.45 + 0.003*SL
	tR	0.14	0.12 + 0.013*SL	0.12 + 0.012*SL	0.10 + 0.012*SL
	tF	0.20	0.20 + 0.001*SL	0.19 + 0.005*SL	0.19 + 0.005*SL

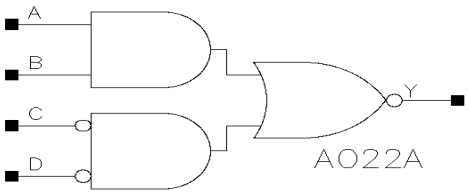
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D
Output: Y
Input Loading (SL):
- AO22A: All : 1
- AO22D2A: A,B : 2
  C,D : 1

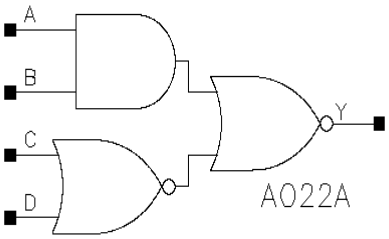
Maximum Fanout (Rec. SL):
- AO22A: 14
- AO22D2A: 28

Gate Count:
- AO22A: 3
- AO22D2A: 5

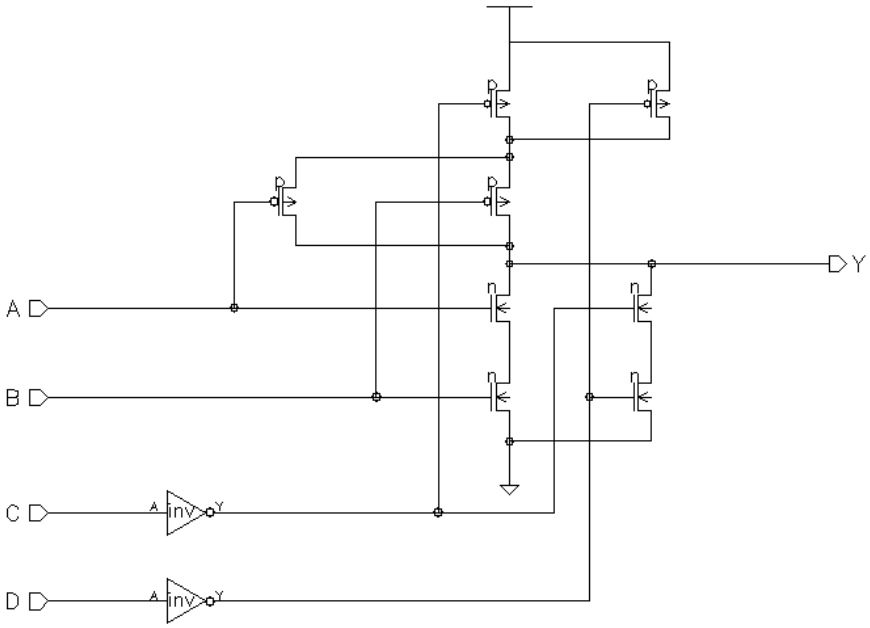


A	B	C	D	Y
1	1	x	x	0
0	x	1	x	1
0	x	x	1	1
x	0	1	x	1
x	0	x	1	1
x	x	0	0	0

Truth Table



Symbols



Schematic

AO22A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.37	0.25 + 0.061*SL	0.27 + 0.053*SL	0.26 + 0.054*SL
	tPHL	0.12	0.02 + 0.049*SL	0.08 + 0.030*SL	0.16 + 0.025*SL
	tR	0.51	0.30 + 0.107*SL	0.26 + 0.120*SL	0.16 + 0.125*SL
	tF	0.37	0.27 + 0.051*SL	0.27 + 0.051*SL	0.20 + 0.055*SL
B to Y	tPLH	0.42	0.32 + 0.054*SL	0.32 + 0.052*SL	0.30 + 0.053*SL
	tPHL	0.08	-0.01 + 0.043*SL	0.03 + 0.028*SL	0.08 + 0.025*SL
	tR	0.57	0.35 + 0.112*SL	0.33 + 0.120*SL	0.22 + 0.125*SL
	tF	0.35	0.25 + 0.051*SL	0.25 + 0.051*SL	0.16 + 0.055*SL
C to Y	tPLH	0.35	0.21 + 0.072*SL	0.21 + 0.072*SL	0.22 + 0.072*SL
	tPHL	0.37	0.32 + 0.029*SL	0.32 + 0.026*SL	0.33 + 0.026*SL
	tR	0.63	0.31 + 0.161*SL	0.29 + 0.167*SL	0.28 + 0.167*SL
	tF	0.31	0.21 + 0.051*SL	0.19 + 0.056*SL	0.16 + 0.058*SL
D to Y	tPLH	0.40	0.25 + 0.073*SL	0.26 + 0.072*SL	0.26 + 0.072*SL
	tPHL	0.37	0.31 + 0.030*SL	0.32 + 0.027*SL	0.33 + 0.026*SL
	tR	0.71	0.38 + 0.162*SL	0.37 + 0.167*SL	0.36 + 0.167*SL
	tF	0.31	0.20 + 0.054*SL	0.19 + 0.057*SL	0.16 + 0.058*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

AO22D2A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

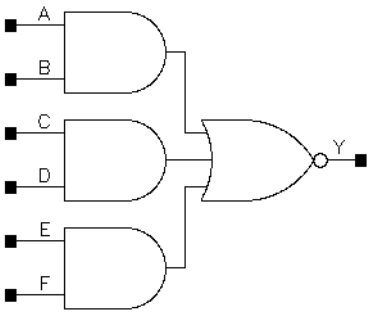
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.31	0.24 + 0.036*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	tPHL	0.07	0.01 + 0.030*SL	0.04 + 0.018*SL	0.14 + 0.014*SL
	tR	0.41	0.28 + 0.066*SL	0.29 + 0.061*SL	0.22 + 0.065*SL
	tF	0.33	0.27 + 0.028*SL	0.28 + 0.027*SL	0.26 + 0.027*SL
B to Y	tPLH	0.37	0.31 + 0.030*SL	0.32 + 0.027*SL	0.32 + 0.027*SL
	tPHL	0.03	-0.02 + 0.025*SL	0.01 + 0.016*SL	0.07 + 0.014*SL
	tR	0.48	0.36 + 0.060*SL	0.36 + 0.060*SL	0.28 + 0.064*SL
	tF	0.31	0.26 + 0.026*SL	0.26 + 0.026*SL	0.21 + 0.028*SL
C to Y	tPLH	0.32	0.25 + 0.037*SL	0.25 + 0.037*SL	0.25 + 0.037*SL
	tPHL	0.40	0.36 + 0.018*SL	0.37 + 0.015*SL	0.39 + 0.014*SL
	tR	0.48	0.32 + 0.081*SL	0.30 + 0.086*SL	0.29 + 0.086*SL
	tF	0.30	0.24 + 0.029*SL	0.24 + 0.029*SL	0.20 + 0.031*SL
D to Y	tPLH	0.38	0.30 + 0.039*SL	0.30 + 0.038*SL	0.31 + 0.038*SL
	tPHL	0.40	0.36 + 0.015*SL	0.37 + 0.015*SL	0.39 + 0.014*SL
	tR	0.58	0.42 + 0.081*SL	0.40 + 0.088*SL	0.39 + 0.089*SL
	tF	0.28	0.23 + 0.029*SL	0.22 + 0.030*SL	0.20 + 0.031*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

Inputs: A, B, C, D, E, F
Output: Y
Input Loading (SL):
- AO222: All : 1
- AO222D3: All : 1
- AO222D7: All: 1

Maximum Fanout (Rec. SL):
- AO222: 9
- AO222D3: 84
- AO222D7: 196

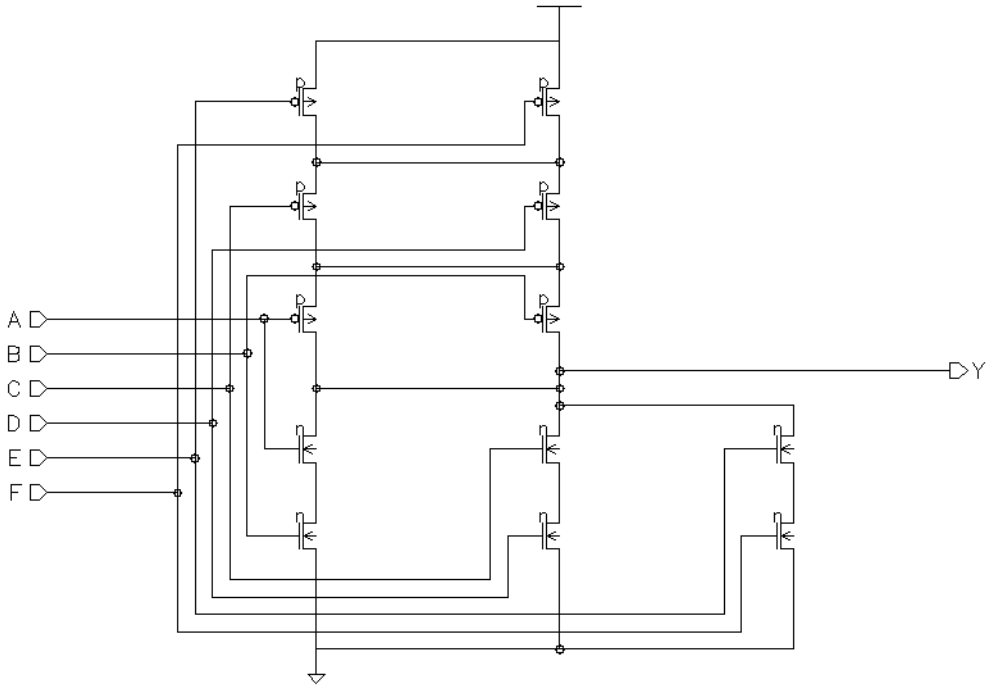
Gate Count:
- AO222: 3
- AO222D3: 5
- AO222D7: 7



Symbol

A	B	C	D	E	F	Y
1	1	x	x	x	x	0
x	x	1	1	x	x	0
x	x	x	x	1	1	0
		other	states			1

Truth Table



Schematic

AO222 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.72	0.52 + 0.103*SL	0.51 + 0.106*SL	0.48 + 0.107*SL
	tPHL	0.15	0.06 + 0.045*SL	0.11 + 0.030*SL	0.18 + 0.026*SL
	tR	1.19	0.71 + 0.243*SL	0.68 + 0.251*SL	0.66 + 0.253*SL
	tF	0.47	0.38 + 0.050*SL	0.37 + 0.053*SL	0.30 + 0.056*SL
B to Y	tPLH	0.81	0.60 + 0.102*SL	0.59 + 0.105*SL	0.56 + 0.107*SL
	tPHL	0.10	0.03 + 0.038*SL	0.06 + 0.028*SL	0.11 + 0.026*SL
	tR	1.31	0.82 + 0.245*SL	0.80 + 0.252*SL	0.78 + 0.253*SL
	tF	0.44	0.35 + 0.045*SL	0.33 + 0.053*SL	0.25 + 0.057*SL
C to Y	tPLH	0.76	0.55 + 0.106*SL	0.55 + 0.108*SL	0.53 + 0.108*SL
	tPHL	0.19	0.11 + 0.042*SL	0.14 + 0.029*SL	0.21 + 0.026*SL
	tR	1.22	0.73 + 0.245*SL	0.70 + 0.253*SL	0.67 + 0.255*SL
	tF	0.54	0.45 + 0.046*SL	0.43 + 0.052*SL	0.34 + 0.056*SL
D to Y	tPLH	0.84	0.63 + 0.104*SL	0.62 + 0.106*SL	0.61 + 0.107*SL
	tPHL	0.14	0.06 + 0.037*SL	0.09 + 0.028*SL	0.13 + 0.026*SL
	tR	1.32	0.84 + 0.243*SL	0.81 + 0.251*SL	0.78 + 0.253*SL
	tF	0.50	0.40 + 0.047*SL	0.38 + 0.053*SL	0.30 + 0.057*SL
E to Y	tPLH	0.77	0.56 + 0.108*SL	0.55 + 0.109*SL	0.55 + 0.109*SL
	tPHL	0.21	0.12 + 0.043*SL	0.16 + 0.029*SL	0.22 + 0.026*SL
	tR	1.21	0.71 + 0.247*SL	0.69 + 0.254*SL	0.67 + 0.255*SL
	tF	0.59	0.50 + 0.046*SL	0.49 + 0.052*SL	0.40 + 0.056*SL
F to Y	tPLH	0.85	0.64 + 0.106*SL	0.63 + 0.107*SL	0.62 + 0.107*SL
	tPHL	0.15	0.07 + 0.038*SL	0.10 + 0.029*SL	0.15 + 0.026*SL
	tR	1.31	0.82 + 0.245*SL	0.80 + 0.252*SL	0.78 + 0.253*SL
	tF	0.55	0.46 + 0.044*SL	0.43 + 0.053*SL	0.35 + 0.057*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO222D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.79	0.76 + 0.015*SL	0.76 + 0.013*SL	0.77 + 0.012*SL
	t_{PHL}	0.34	0.32 + 0.008*SL	0.32 + 0.008*SL	0.36 + 0.006*SL
	t_R	0.16	0.11 + 0.027*SL	0.10 + 0.028*SL	0.08 + 0.030*SL
	t_F	0.13	0.11 + 0.010*SL	0.11 + 0.011*SL	0.11 + 0.011*SL
B to Y	t_{PLH}	0.87	0.84 + 0.014*SL	0.85 + 0.013*SL	0.85 + 0.013*SL
	t_{PHL}	0.31	0.29 + 0.007*SL	0.29 + 0.007*SL	0.32 + 0.006*SL
	t_R	0.17	0.11 + 0.031*SL	0.11 + 0.028*SL	0.09 + 0.029*SL
	t_F	0.13	0.11 + 0.009*SL	0.10 + 0.011*SL	0.12 + 0.011*SL
C to Y	t_{PLH}	0.82	0.80 + 0.013*SL	0.80 + 0.013*SL	0.81 + 0.012*SL
	t_{PHL}	0.39	0.37 + 0.011*SL	0.38 + 0.007*SL	0.41 + 0.006*SL
	t_R	0.16	0.11 + 0.027*SL	0.10 + 0.028*SL	0.08 + 0.030*SL
	t_F	0.13	0.10 + 0.015*SL	0.11 + 0.011*SL	0.10 + 0.011*SL
D to Y	t_{PLH}	0.90	0.88 + 0.014*SL	0.88 + 0.013*SL	0.89 + 0.013*SL
	t_{PHL}	0.35	0.32 + 0.011*SL	0.34 + 0.008*SL	0.37 + 0.006*SL
	t_R	0.17	0.11 + 0.031*SL	0.12 + 0.028*SL	0.09 + 0.029*SL
	t_F	0.13	0.10 + 0.014*SL	0.11 + 0.011*SL	0.12 + 0.010*SL
E to Y	t_{PLH}	0.83	0.80 + 0.014*SL	0.81 + 0.013*SL	0.81 + 0.013*SL
	t_{PHL}	0.42	0.40 + 0.009*SL	0.41 + 0.007*SL	0.44 + 0.006*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.028*SL	0.07 + 0.030*SL
	t_F	0.13	0.11 + 0.011*SL	0.11 + 0.011*SL	0.10 + 0.011*SL
F to Y	t_{PLH}	0.91	0.88 + 0.014*SL	0.89 + 0.013*SL	0.90 + 0.012*SL
	t_{PHL}	0.37	0.35 + 0.010*SL	0.36 + 0.008*SL	0.40 + 0.006*SL
	t_R	0.16	0.11 + 0.026*SL	0.10 + 0.029*SL	0.09 + 0.029*SL
	t_F	0.13	0.10 + 0.013*SL	0.11 + 0.011*SL	0.10 + 0.011*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

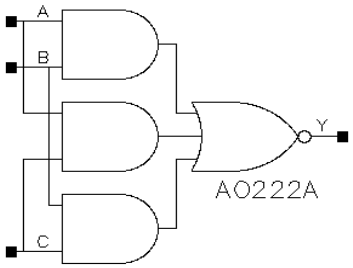
AO222D7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.90	0.89 + 0.007*SL	0.89 + 0.006*SL	0.90 + 0.005*SL
	tPHL	0.45	0.43 + 0.008*SL	0.44 + 0.005*SL	0.47 + 0.004*SL
	tR	0.16	0.13 + 0.011*SL	0.13 + 0.012*SL	0.13 + 0.012*SL
	tF	0.20	0.19 + 0.006*SL	0.19 + 0.005*SL	0.20 + 0.004*SL
B to Y	tPLH	0.99	0.98 + 0.008*SL	0.98 + 0.006*SL	0.99 + 0.006*SL
	tPHL	0.42	0.41 + 0.006*SL	0.41 + 0.005*SL	0.43 + 0.004*SL
	tR	0.17	0.14 + 0.015*SL	0.15 + 0.011*SL	0.13 + 0.012*SL
	tF	0.20	0.18 + 0.010*SL	0.19 + 0.004*SL	0.19 + 0.004*SL
C to Y	tPLH	0.94	0.92 + 0.009*SL	0.93 + 0.006*SL	0.94 + 0.005*SL
	tPHL	0.51	0.50 + 0.005*SL	0.50 + 0.005*SL	0.53 + 0.003*SL
	tR	0.17	0.14 + 0.010*SL	0.14 + 0.012*SL	0.14 + 0.012*SL
	tF	0.19	0.17 + 0.009*SL	0.18 + 0.005*SL	0.21 + 0.004*SL
D to Y	tPLH	1.03	1.01 + 0.009*SL	1.02 + 0.006*SL	1.03 + 0.005*SL
	tPHL	0.46	0.44 + 0.007*SL	0.45 + 0.005*SL	0.47 + 0.004*SL
	tR	0.16	0.13 + 0.016*SL	0.14 + 0.012*SL	0.14 + 0.012*SL
	tF	0.20	0.20 + 0.003*SL	0.19 + 0.005*SL	0.20 + 0.004*SL
E to Y	tPLH	0.94	0.93 + 0.008*SL	0.93 + 0.006*SL	0.94 + 0.006*SL
	tPHL	0.54	0.51 + 0.010*SL	0.53 + 0.005*SL	0.55 + 0.004*SL
	tR	0.16	0.13 + 0.012*SL	0.13 + 0.012*SL	0.12 + 0.012*SL
	tF	0.20	0.20 + 0.003*SL	0.19 + 0.004*SL	0.18 + 0.005*SL
F to Y	tPLH	1.03	1.02 + 0.007*SL	1.02 + 0.006*SL	1.03 + 0.006*SL
	tPHL	0.48	0.47 + 0.006*SL	0.48 + 0.005*SL	0.51 + 0.004*SL
	tR	0.17	0.15 + 0.007*SL	0.14 + 0.012*SL	0.12 + 0.012*SL
	tF	0.20	0.19 + 0.005*SL	0.19 + 0.005*SL	0.21 + 0.004*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

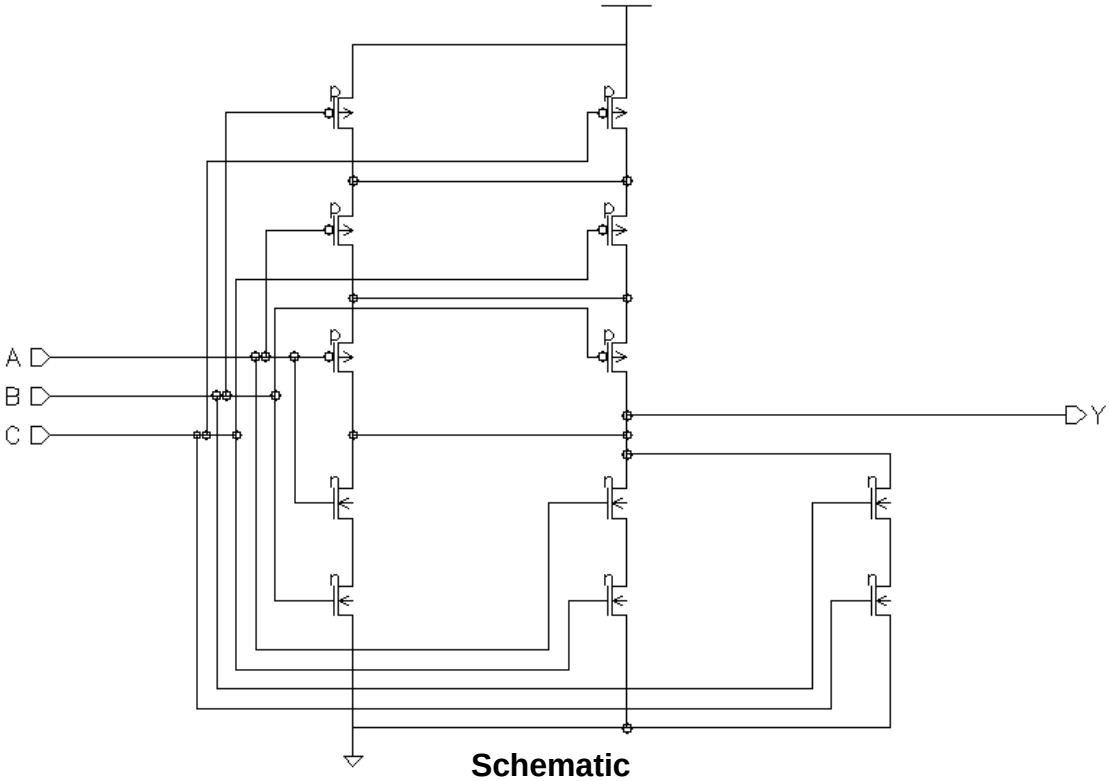
Inputs: A, B, C
Output: Y
Input Loading (SL): All : 2
Maximum Fanout (Rec. SL): 9
Gate Count: 3



Symbol

A	B	C	Y
1	1	x	0
1	x	1	0
x	1	1	0
0	0	x	1
0	x	0	1
x	0	0	1

Truth Table



Schematic

AO222A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

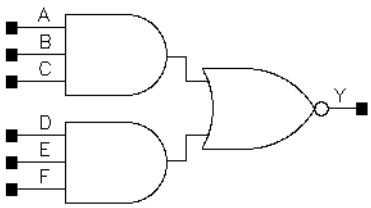
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.60	0.43 + 0.087*SL	0.43 + 0.088*SL	0.42 + 0.088*SL
	t_{PHL}	0.14	0.04 + 0.046*SL	0.09 + 0.030*SL	0.18 + 0.026*SL
	t_R	0.91	0.52 + 0.194*SL	0.49 + 0.204*SL	0.45 + 0.206*SL
	t_F	0.46	0.36 + 0.050*SL	0.36 + 0.053*SL	0.29 + 0.057*SL
B to Y	t_{PLH}	0.67	0.50 + 0.085*SL	0.49 + 0.088*SL	0.48 + 0.089*SL
	t_{PHL}	0.09	0.01 + 0.039*SL	0.04 + 0.029*SL	0.10 + 0.026*SL
	t_R	0.97	0.58 + 0.197*SL	0.56 + 0.205*SL	0.52 + 0.207*SL
	t_F	0.44	0.35 + 0.046*SL	0.32 + 0.054*SL	0.25 + 0.057*SL
C to Y	t_{PLH}	0.66	0.49 + 0.085*SL	0.49 + 0.087*SL	0.47 + 0.088*SL
	t_{PHL}	0.13	0.05 + 0.038*SL	0.08 + 0.028*SL	0.13 + 0.026*SL
	t_R	0.99	0.60 + 0.196*SL	0.57 + 0.205*SL	0.52 + 0.207*SL
	t_F	0.46	0.37 + 0.042*SL	0.34 + 0.053*SL	0.25 + 0.057*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: A, B, C, D, E, F
Output: Y
Input Loading (SL):
- AO33: All : 1
- AO33D2: All: 1
- AO33D3: All: 1
- AO33D7: All: 1

Maximum Fanout (Rec. SL):
- AO33: 14
- AO33D2: 28
- AO33D3: 84
- AO33D7: 196

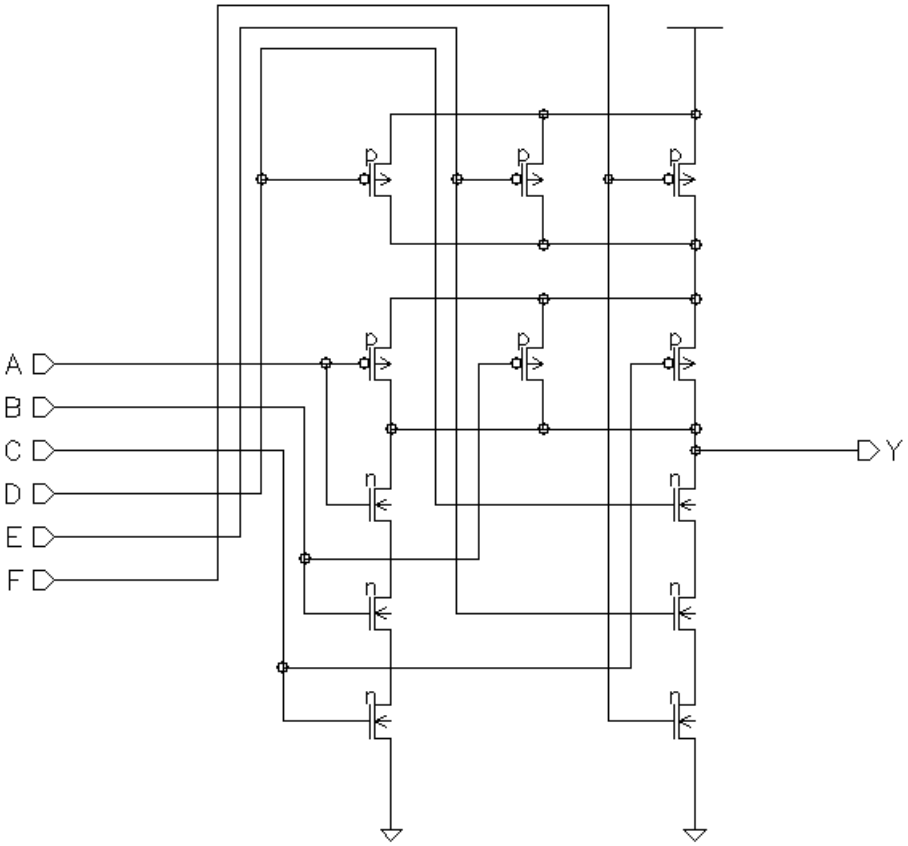
Gate Count:
- AO33: 3
- AO33D2: 5
- AO33D3: 5
- AO33D7: 7



Symbol

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	1	0
other states						1

Truth Table



Schematic

AO33 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.54	0.39 + 0.072*SL	0.40 + 0.070*SL	0.39 + 0.071*SL
	tPHL	0.21	0.11 + 0.053*SL	0.15 + 0.039*SL	0.20 + 0.037*SL
	tR	0.82	0.52 + 0.148*SL	0.48 + 0.162*SL	0.41 + 0.165*SL
	tF	0.61	0.46 + 0.073*SL	0.44 + 0.080*SL	0.33 + 0.085*SL
B to Y	tPLH	0.60	0.46 + 0.070*SL	0.46 + 0.070*SL	0.44 + 0.071*SL
	tPHL	0.18	0.08 + 0.048*SL	0.11 + 0.039*SL	0.15 + 0.037*SL
	tR	0.90	0.60 + 0.149*SL	0.56 + 0.162*SL	0.49 + 0.165*SL
	tF	0.58	0.44 + 0.069*SL	0.40 + 0.081*SL	0.31 + 0.085*SL
C to Y	tPLH	0.65	0.51 + 0.068*SL	0.51 + 0.070*SL	0.49 + 0.071*SL
	tPHL	0.14	0.05 + 0.044*SL	0.07 + 0.038*SL	0.10 + 0.037*SL
	tR	0.98	0.68 + 0.148*SL	0.64 + 0.162*SL	0.57 + 0.165*SL
	tF	0.55	0.41 + 0.069*SL	0.37 + 0.082*SL	0.29 + 0.086*SL
D to Y	tPLH	0.55	0.40 + 0.073*SL	0.41 + 0.072*SL	0.41 + 0.072*SL
	tPHL	0.28	0.19 + 0.048*SL	0.21 + 0.039*SL	0.25 + 0.037*SL
	tR	0.81	0.51 + 0.154*SL	0.47 + 0.165*SL	0.42 + 0.168*SL
	tF	0.71	0.57 + 0.069*SL	0.54 + 0.079*SL	0.42 + 0.085*SL
E to Y	tPLH	0.61	0.46 + 0.072*SL	0.46 + 0.072*SL	0.46 + 0.072*SL
	tPHL	0.24	0.15 + 0.045*SL	0.17 + 0.038*SL	0.20 + 0.037*SL
	tR	0.90	0.59 + 0.153*SL	0.55 + 0.165*SL	0.50 + 0.168*SL
	tF	0.67	0.54 + 0.067*SL	0.50 + 0.080*SL	0.40 + 0.085*SL
F to Y	tPLH	0.65	0.51 + 0.069*SL	0.51 + 0.070*SL	0.50 + 0.071*SL
	tPHL	0.20	0.11 + 0.045*SL	0.13 + 0.038*SL	0.15 + 0.037*SL
	tR	0.97	0.66 + 0.154*SL	0.63 + 0.162*SL	0.57 + 0.165*SL
	tF	0.64	0.50 + 0.072*SL	0.47 + 0.081*SL	0.39 + 0.086*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO33D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.69	0.65 + 0.021*SL	0.66 + 0.019*SL	0.65 + 0.019*SL
	tPHL	0.36	0.33 + 0.013*SL	0.34 + 0.009*SL	0.37 + 0.008*SL
	tR	0.18	0.10 + 0.041*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	tF	0.11	0.07 + 0.019*SL	0.08 + 0.016*SL	0.06 + 0.017*SL
B to Y	tPLH	0.76	0.71 + 0.022*SL	0.72 + 0.019*SL	0.72 + 0.019*SL
	tPHL	0.33	0.30 + 0.013*SL	0.31 + 0.010*SL	0.34 + 0.008*SL
	tR	0.18	0.09 + 0.044*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	tF	0.11	0.08 + 0.014*SL	0.07 + 0.017*SL	0.06 + 0.017*SL
C to Y	tPLH	0.81	0.77 + 0.022*SL	0.78 + 0.019*SL	0.77 + 0.019*SL
	tPHL	0.29	0.27 + 0.012*SL	0.27 + 0.010*SL	0.30 + 0.008*SL
	tR	0.19	0.11 + 0.040*SL	0.10 + 0.044*SL	0.07 + 0.045*SL
	tF	0.11	0.08 + 0.016*SL	0.07 + 0.017*SL	0.06 + 0.017*SL
D to Y	tPLH	0.70	0.66 + 0.021*SL	0.67 + 0.019*SL	0.67 + 0.019*SL
	tPHL	0.44	0.42 + 0.012*SL	0.43 + 0.009*SL	0.44 + 0.008*SL
	tR	0.18	0.10 + 0.043*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	tF	0.12	0.09 + 0.015*SL	0.08 + 0.016*SL	0.06 + 0.017*SL
E to Y	tPLH	0.76	0.72 + 0.020*SL	0.72 + 0.019*SL	0.72 + 0.019*SL
	tPHL	0.40	0.37 + 0.014*SL	0.39 + 0.009*SL	0.41 + 0.008*SL
	tR	0.19	0.11 + 0.038*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	tF	0.11	0.07 + 0.022*SL	0.09 + 0.016*SL	0.06 + 0.017*SL
F to Y	tPLH	0.81	0.77 + 0.022*SL	0.78 + 0.019*SL	0.79 + 0.019*SL
	tPHL	0.36	0.33 + 0.015*SL	0.35 + 0.009*SL	0.37 + 0.008*SL
	tR	0.18	0.10 + 0.041*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	tF	0.12	0.07 + 0.022*SL	0.09 + 0.016*SL	0.06 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO33D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.64	0.62 + 0.014*SL	0.62 + 0.013*SL	0.62 + 0.013*SL
	tPHL	0.43	0.41 + 0.010*SL	0.41 + 0.007*SL	0.44 + 0.006*SL
	tR	0.15	0.09 + 0.030*SL	0.10 + 0.028*SL	0.07 + 0.030*SL
	tF	0.14	0.11 + 0.013*SL	0.12 + 0.011*SL	0.11 + 0.011*SL
B to Y	tPLH	0.71	0.68 + 0.013*SL	0.68 + 0.013*SL	0.69 + 0.013*SL
	tPHL	0.41	0.39 + 0.011*SL	0.40 + 0.008*SL	0.43 + 0.006*SL
	tR	0.15	0.10 + 0.029*SL	0.10 + 0.028*SL	0.07 + 0.030*SL
	tF	0.13	0.10 + 0.014*SL	0.12 + 0.011*SL	0.11 + 0.011*SL
C to Y	tPLH	0.74	0.71 + 0.015*SL	0.72 + 0.013*SL	0.72 + 0.013*SL
	tPHL	0.37	0.35 + 0.009*SL	0.36 + 0.008*SL	0.39 + 0.006*SL
	tR	0.15	0.10 + 0.028*SL	0.10 + 0.029*SL	0.07 + 0.030*SL
	tF	0.14	0.11 + 0.013*SL	0.12 + 0.011*SL	0.12 + 0.011*SL
D to Y	tPLH	0.65	0.62 + 0.014*SL	0.62 + 0.013*SL	0.63 + 0.012*SL
	tPHL	0.52	0.50 + 0.010*SL	0.50 + 0.008*SL	0.54 + 0.006*SL
	tR	0.16	0.10 + 0.030*SL	0.11 + 0.028*SL	0.06 + 0.030*SL
	tF	0.13	0.12 + 0.009*SL	0.11 + 0.011*SL	0.13 + 0.010*SL
E to Y	tPLH	0.70	0.68 + 0.014*SL	0.68 + 0.013*SL	0.69 + 0.012*SL
	tPHL	0.49	0.47 + 0.012*SL	0.48 + 0.008*SL	0.51 + 0.006*SL
	tR	0.16	0.11 + 0.025*SL	0.10 + 0.028*SL	0.07 + 0.030*SL
	tF	0.13	0.10 + 0.015*SL	0.12 + 0.011*SL	0.12 + 0.011*SL
F to Y	tPLH	0.75	0.72 + 0.014*SL	0.72 + 0.013*SL	0.73 + 0.013*SL
	tPHL	0.44	0.42 + 0.009*SL	0.43 + 0.008*SL	0.47 + 0.006*SL
	tR	0.15	0.10 + 0.027*SL	0.10 + 0.028*SL	0.07 + 0.030*SL
	tF	0.14	0.12 + 0.007*SL	0.11 + 0.011*SL	0.13 + 0.010*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

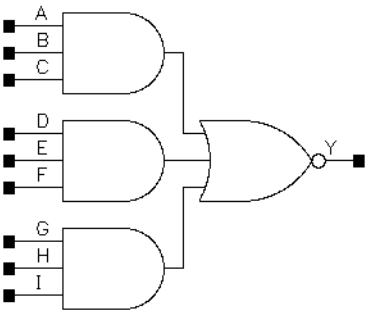
AO33D7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.74	0.73 + 0.007*SL	0.73 + 0.006*SL	0.75 + 0.005*SL
	tPHL	0.54	0.53 + 0.006*SL	0.53 + 0.005*SL	0.56 + 0.004*SL
	tR	0.15	0.12 + 0.011*SL	0.12 + 0.012*SL	0.13 + 0.012*SL
	tF	0.21	0.20 + 0.006*SL	0.21 + 0.004*SL	0.19 + 0.005*SL
B to Y	tPLH	0.81	0.79 + 0.006*SL	0.79 + 0.006*SL	0.80 + 0.006*SL
	tPHL	0.53	0.52 + 0.005*SL	0.52 + 0.005*SL	0.55 + 0.003*SL
	tR	0.15	0.12 + 0.015*SL	0.13 + 0.012*SL	0.14 + 0.012*SL
	tF	0.20	0.19 + 0.006*SL	0.19 + 0.005*SL	0.21 + 0.004*SL
C to Y	tPLH	0.85	0.83 + 0.007*SL	0.83 + 0.006*SL	0.85 + 0.006*SL
	tPHL	0.49	0.48 + 0.005*SL	0.48 + 0.005*SL	0.51 + 0.003*SL
	tR	0.16	0.14 + 0.011*SL	0.14 + 0.011*SL	0.13 + 0.012*SL
	tF	0.21	0.20 + 0.005*SL	0.20 + 0.005*SL	0.21 + 0.004*SL
D to Y	tPLH	0.74	0.73 + 0.005*SL	0.73 + 0.006*SL	0.74 + 0.006*SL
	tPHL	0.63	0.61 + 0.008*SL	0.62 + 0.005*SL	0.65 + 0.004*SL
	tR	0.15	0.12 + 0.014*SL	0.13 + 0.012*SL	0.12 + 0.012*SL
	tF	0.21	0.21 + 0.001*SL	0.19 + 0.005*SL	0.20 + 0.005*SL
E to Y	tPLH	0.81	0.79 + 0.009*SL	0.80 + 0.006*SL	0.81 + 0.005*SL
	tPHL	0.61	0.60 + 0.003*SL	0.60 + 0.005*SL	0.62 + 0.004*SL
	tR	0.15	0.13 + 0.014*SL	0.13 + 0.011*SL	0.12 + 0.012*SL
	tF	0.21	0.20 + 0.005*SL	0.20 + 0.004*SL	0.19 + 0.005*SL
F to Y	tPLH	0.85	0.84 + 0.007*SL	0.84 + 0.006*SL	0.85 + 0.006*SL
	tPHL	0.56	0.54 + 0.008*SL	0.55 + 0.005*SL	0.58 + 0.004*SL
	tR	0.15	0.13 + 0.013*SL	0.13 + 0.011*SL	0.11 + 0.013*SL
	tF	0.22	0.21 + 0.003*SL	0.21 + 0.004*SL	0.19 + 0.005*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

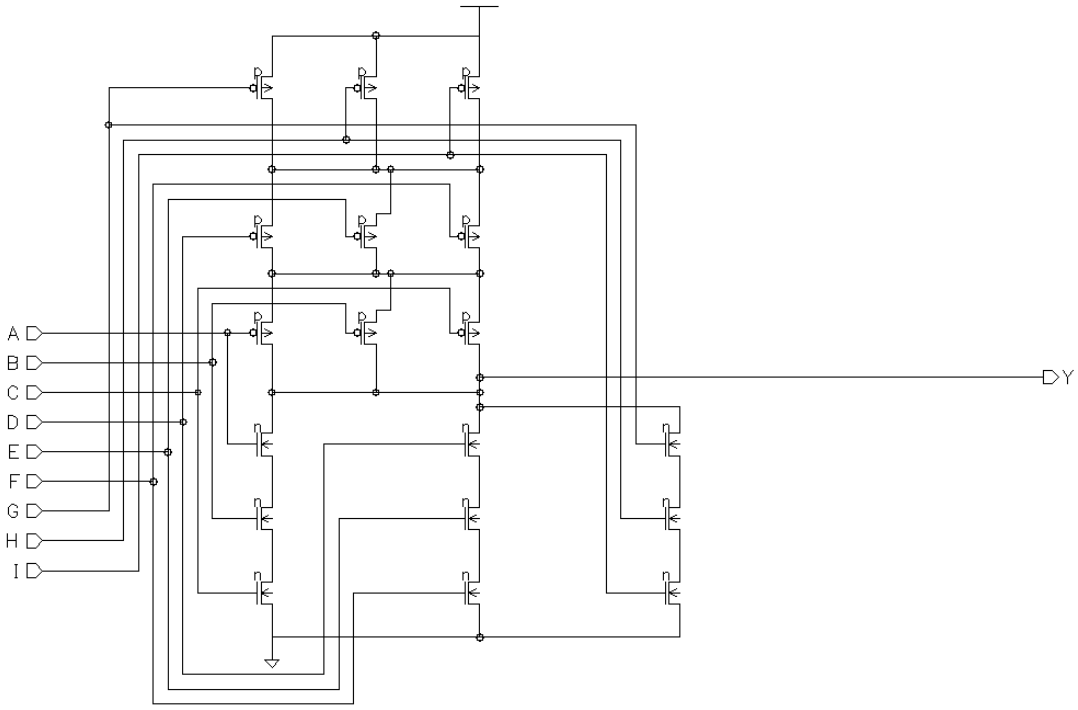
Inputs: A, B, C, D, E, F, G, H, I
Output: Y
Input Loading (SL): All : 1
Maximum Fanout (Rec. SL):
AO333: 9
AO333D2: 18
Gate Count:
AO333: 5
AO333D2: 6



Symbol

A	B	C	D	E	F	G	H	I	Y
1	1	1	x	x	x	x	x	x	0
x	x	x	1	1	1	x	x	x	0
x	x	x	x	x	x	1	1	1	0
other states									1

Truth Table



Schematic

AO333 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.87	0.66 + 0.105*SL	0.66 + 0.105*SL	0.65 + 0.106*SL
	t_{PHL}	0.25	0.15 + 0.050*SL	0.19 + 0.039*SL	0.23 + 0.037*SL
	t_R	1.49	1.02 + 0.238*SL	0.99 + 0.246*SL	0.98 + 0.247*SL
	t_F	0.75	0.60 + 0.075*SL	0.58 + 0.080*SL	0.48 + 0.086*SL
B to Y	t_{PLH}	0.95	0.74 + 0.104*SL	0.74 + 0.105*SL	0.72 + 0.106*SL
	t_{PHL}	0.22	0.12 + 0.046*SL	0.15 + 0.039*SL	0.18 + 0.037*SL
	t_R	1.61	1.13 + 0.240*SL	1.11 + 0.247*SL	1.10 + 0.247*SL
	t_F	0.72	0.58 + 0.071*SL	0.54 + 0.082*SL	0.45 + 0.086*SL
C to Y	t_{PLH}	1.03	0.82 + 0.103*SL	0.81 + 0.104*SL	0.80 + 0.105*SL
	t_{PHL}	0.18	0.09 + 0.043*SL	0.11 + 0.038*SL	0.13 + 0.037*SL
	t_R	1.73	1.25 + 0.239*SL	1.23 + 0.246*SL	1.21 + 0.247*SL
	t_F	0.69	0.54 + 0.073*SL	0.51 + 0.083*SL	0.44 + 0.086*SL
D to Y	t_{PLH}	0.96	0.75 + 0.108*SL	0.75 + 0.107*SL	0.75 + 0.107*SL
	t_{PHL}	0.32	0.22 + 0.048*SL	0.25 + 0.039*SL	0.28 + 0.037*SL
	t_R	1.52	1.04 + 0.241*SL	1.02 + 0.247*SL	0.99 + 0.249*SL
	t_F	0.84	0.70 + 0.073*SL	0.68 + 0.080*SL	0.56 + 0.085*SL
E to Y	t_{PLH}	1.04	0.83 + 0.107*SL	0.83 + 0.107*SL	0.83 + 0.107*SL
	t_{PHL}	0.28	0.19 + 0.044*SL	0.21 + 0.038*SL	0.23 + 0.037*SL
	t_R	1.64	1.15 + 0.243*SL	1.14 + 0.247*SL	1.11 + 0.249*SL
	t_F	0.81	0.67 + 0.070*SL	0.64 + 0.081*SL	0.54 + 0.086*SL
F to Y	t_{PLH}	1.11	0.90 + 0.105*SL	0.90 + 0.106*SL	0.90 + 0.106*SL
	t_{PHL}	0.23	0.15 + 0.043*SL	0.16 + 0.038*SL	0.19 + 0.037*SL
	t_R	1.74	1.26 + 0.241*SL	1.25 + 0.245*SL	1.22 + 0.246*SL
	t_F	0.78	0.64 + 0.072*SL	0.61 + 0.082*SL	0.53 + 0.086*SL
G to Y	t_{PLH}	1.00	0.78 + 0.109*SL	0.79 + 0.108*SL	0.80 + 0.107*SL
	t_{PHL}	0.35	0.26 + 0.047*SL	0.28 + 0.039*SL	0.32 + 0.037*SL
	t_R	1.52	1.03 + 0.243*SL	1.02 + 0.248*SL	1.00 + 0.249*SL
	t_F	0.95	0.81 + 0.070*SL	0.78 + 0.079*SL	0.67 + 0.085*SL
H to Y	t_{PLH}	1.09	0.87 + 0.108*SL	0.87 + 0.107*SL	0.88 + 0.107*SL
	t_{PHL}	0.31	0.22 + 0.045*SL	0.24 + 0.039*SL	0.28 + 0.037*SL
	t_R	1.63	1.15 + 0.244*SL	1.13 + 0.248*SL	1.11 + 0.249*SL
	t_F	0.92	0.78 + 0.068*SL	0.74 + 0.080*SL	0.65 + 0.085*SL
I to Y	t_{PLH}	1.15	0.94 + 0.107*SL	0.94 + 0.106*SL	0.95 + 0.106*SL
	t_{PHL}	0.25	0.16 + 0.046*SL	0.18 + 0.039*SL	0.22 + 0.037*SL
	t_R	1.73	1.25 + 0.241*SL	1.24 + 0.246*SL	1.22 + 0.246*SL
	t_F	0.88	0.73 + 0.073*SL	0.71 + 0.082*SL	0.63 + 0.085*SL

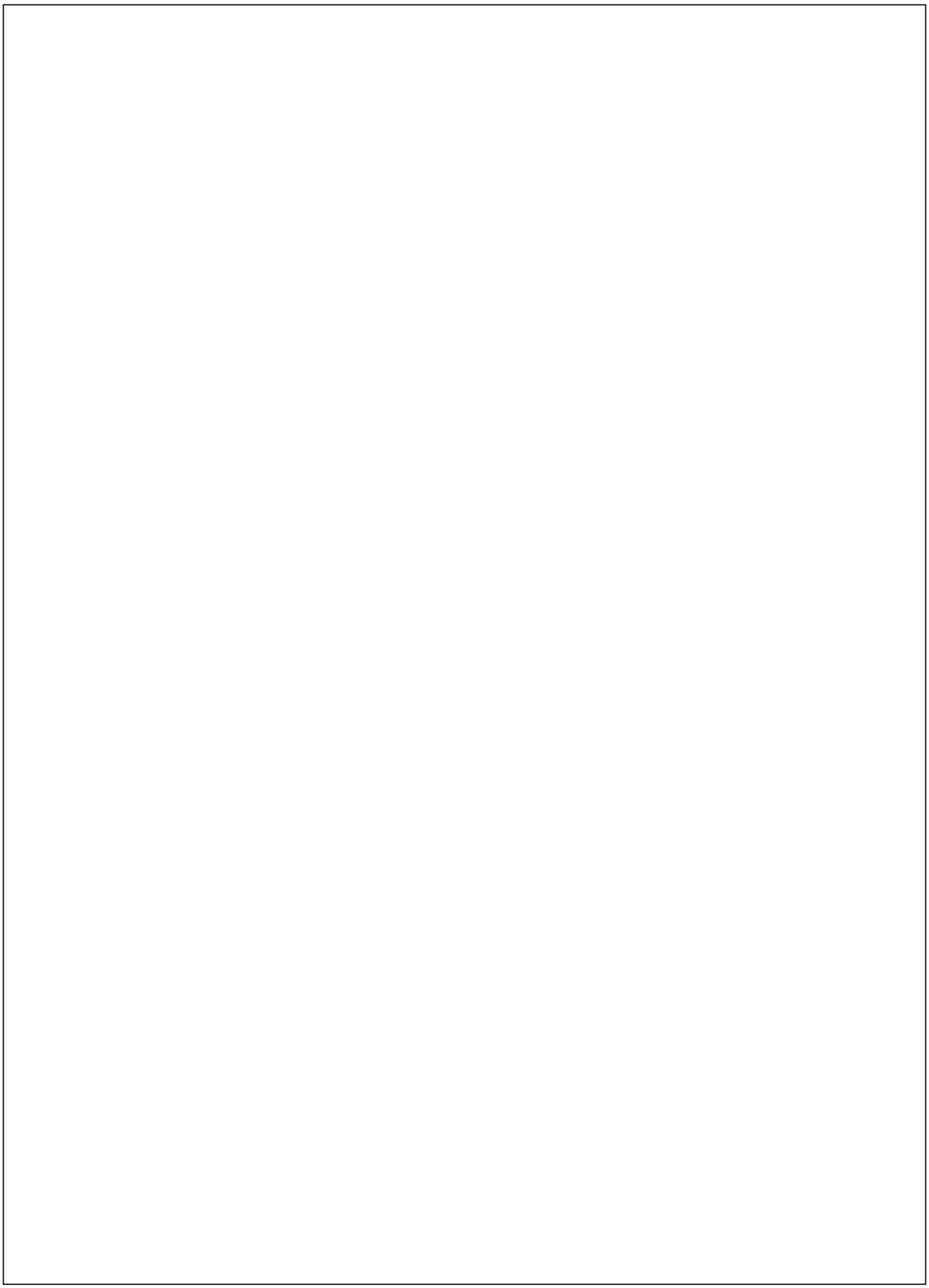
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

AO333D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.89	0.84 + 0.022*SL	0.85 + 0.019*SL	0.86 + 0.018*SL
	t_{PHL}	0.48	0.46 + 0.011*SL	0.46 + 0.010*SL	0.50 + 0.008*SL
	t_R	0.19	0.11 + 0.042*SL	0.11 + 0.040*SL	0.07 + 0.043*SL
	t_F	0.13	0.10 + 0.013*SL	0.10 + 0.016*SL	0.10 + 0.016*SL
B to Y	t_{PLH}	0.96	0.93 + 0.017*SL	0.92 + 0.019*SL	0.94 + 0.018*SL
	t_{PHL}	0.45	0.42 + 0.014*SL	0.43 + 0.010*SL	0.46 + 0.008*SL
	t_R	0.19	0.13 + 0.035*SL	0.11 + 0.041*SL	0.08 + 0.043*SL
	t_F	0.12	0.09 + 0.016*SL	0.09 + 0.016*SL	0.10 + 0.016*SL
C to Y	t_{PLH}	1.03	0.99 + 0.019*SL	0.99 + 0.019*SL	1.00 + 0.018*SL
	t_{PHL}	0.41	0.38 + 0.013*SL	0.39 + 0.010*SL	0.42 + 0.008*SL
	t_R	0.19	0.12 + 0.037*SL	0.10 + 0.041*SL	0.08 + 0.042*SL
	t_F	0.13	0.10 + 0.016*SL	0.10 + 0.015*SL	0.09 + 0.016*SL
D to Y	t_{PLH}	0.97	0.93 + 0.020*SL	0.94 + 0.019*SL	0.95 + 0.018*SL
	t_{PHL}	0.56	0.53 + 0.016*SL	0.55 + 0.010*SL	0.58 + 0.008*SL
	t_R	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.07 + 0.043*SL
	t_F	0.14	0.09 + 0.023*SL	0.11 + 0.015*SL	0.09 + 0.016*SL
E to Y	t_{PLH}	1.05	1.01 + 0.019*SL	1.01 + 0.019*SL	1.02 + 0.018*SL
	t_{PHL}	0.53	0.50 + 0.011*SL	0.51 + 0.010*SL	0.54 + 0.008*SL
	t_R	0.19	0.11 + 0.039*SL	0.10 + 0.041*SL	0.08 + 0.042*SL
	t_F	0.13	0.11 + 0.014*SL	0.10 + 0.015*SL	0.07 + 0.016*SL
F to Y	t_{PLH}	1.11	1.07 + 0.020*SL	1.07 + 0.019*SL	1.08 + 0.018*SL
	t_{PHL}	0.48	0.46 + 0.012*SL	0.47 + 0.010*SL	0.50 + 0.008*SL
	t_R	0.19	0.11 + 0.040*SL	0.10 + 0.041*SL	0.09 + 0.042*SL
	t_F	0.13	0.10 + 0.012*SL	0.09 + 0.016*SL	0.10 + 0.015*SL
G to Y	t_{PLH}	1.01	0.97 + 0.021*SL	0.98 + 0.019*SL	0.99 + 0.018*SL
	t_{PHL}	0.61	0.57 + 0.016*SL	0.59 + 0.010*SL	0.62 + 0.008*SL
	t_R	0.18	0.09 + 0.045*SL	0.11 + 0.041*SL	0.07 + 0.043*SL
	t_F	0.14	0.10 + 0.021*SL	0.11 + 0.015*SL	0.09 + 0.016*SL
H to Y	t_{PLH}	1.09	1.05 + 0.019*SL	1.05 + 0.019*SL	1.06 + 0.018*SL
	t_{PHL}	0.58	0.55 + 0.015*SL	0.56 + 0.010*SL	0.59 + 0.008*SL
	t_R	0.19	0.12 + 0.037*SL	0.10 + 0.041*SL	0.08 + 0.042*SL
	t_F	0.14	0.10 + 0.021*SL	0.12 + 0.015*SL	0.10 + 0.016*SL
I to Y	t_{PLH}	1.15	1.11 + 0.021*SL	1.11 + 0.019*SL	1.12 + 0.018*SL
	t_{PHL}	0.52	0.50 + 0.011*SL	0.50 + 0.010*SL	0.54 + 0.008*SL
	t_R	0.19	0.11 + 0.041*SL	0.11 + 0.041*SL	0.08 + 0.043*SL
	t_F	0.14	0.12 + 0.011*SL	0.10 + 0.016*SL	0.10 + 0.016*SL

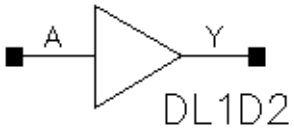
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL



Input: A
Output: Y
Input Loading (SL):
- DL1D2: A : 1
- DL1D4: A : 1

Maximum Fanout (Rec. SL):
- DL1D2: 56
- DL1D4: 112

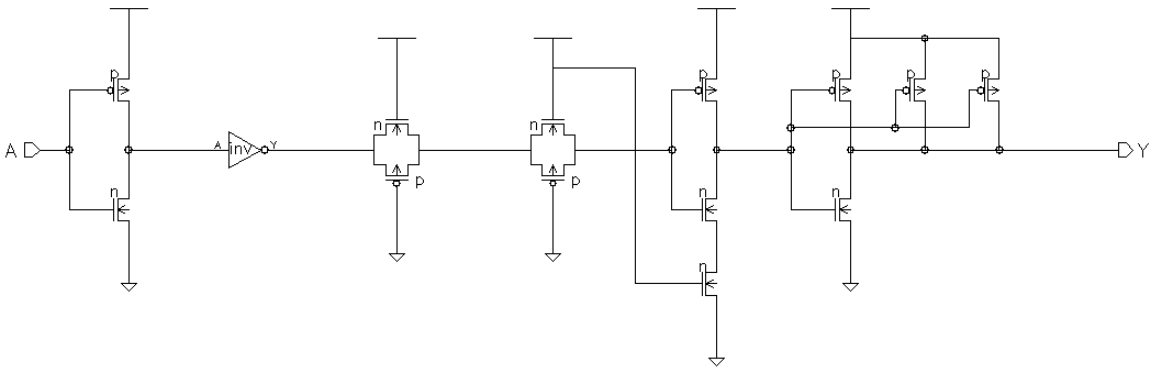
Gate Count:
- DL1D2: 4
- DL1D4: 5



Symbol

A	Y
0	0
1	1

Truth Table



Schematic

DL1D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.39	0.35 + 0.016*SL	0.36 + 0.013*SL	0.38 + 0.012*SL
	t_{PHL}	0.61	0.57 + 0.023*SL	0.59 + 0.016*SL	0.60 + 0.016*SL
	t_R	0.16	0.10 + 0.029*SL	0.11 + 0.026*SL	0.07 + 0.028*SL
	t_F	0.16	0.09 + 0.035*SL	0.10 + 0.031*SL	0.06 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

DL1D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

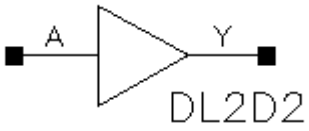
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.43	0.41 + 0.011*SL	0.42 + 0.009*SL	0.44 + 0.008*SL
	t_{PHL}	0.65	0.63 + 0.011*SL	0.63 + 0.009*SL	0.65 + 0.008*SL
	t_R	0.15	0.12 + 0.015*SL	0.11 + 0.016*SL	0.10 + 0.017*SL
	t_F	0.15	0.12 + 0.015*SL	0.12 + 0.015*SL	0.11 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Input: A
Output: Y
Input Loading (SL):
- DL2D2: A : 1
- DL2D4: A : 1

Maximum Fanout Rec. SL):
- DL2D2: 56
- DL2D4: 112

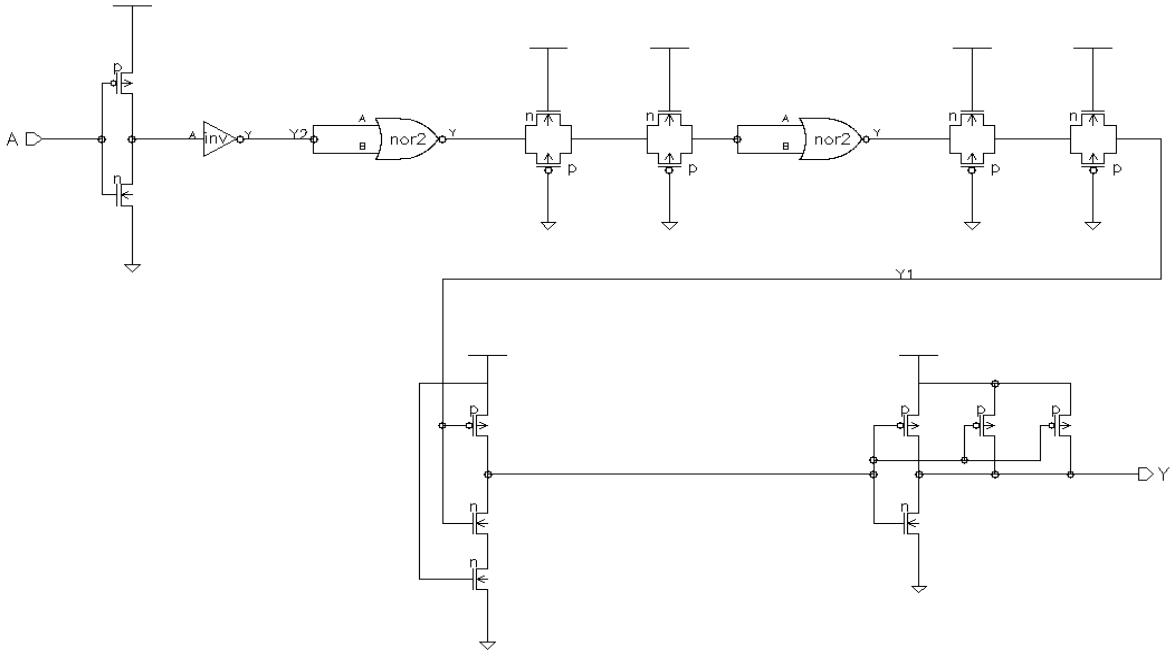
Gate Count:
- DL2D2: 7
- DL2D4: 8



Symbol

A	Y
0	0
1	1

Truth Table



Schematic

DL2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.96	0.92 + 0.017*SL	0.93 + 0.013*SL	0.96 + 0.012*SL
	t_{PHL}	1.11	1.08 + 0.018*SL	1.08 + 0.017*SL	1.10 + 0.016*SL
	t_R	0.16	0.10 + 0.034*SL	0.12 + 0.026*SL	0.07 + 0.028*SL
	t_F	0.15	0.08 + 0.036*SL	0.10 + 0.030*SL	0.06 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

DL2D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

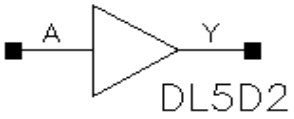
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.94	0.92 + 0.010*SL	0.92 + 0.008*SL	0.94 + 0.007*SL
	t_{PHL}	1.15	1.12 + 0.016*SL	1.14 + 0.009*SL	1.16 + 0.008*SL
	t_R	0.14	0.11 + 0.014*SL	0.10 + 0.016*SL	0.11 + 0.016*SL
	t_F	0.16	0.11 + 0.024*SL	0.14 + 0.014*SL	0.10 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Input: A
Output: Y
Input Loading (SL):
- DL5D2: All : 1
- DL5D4: All : 1

Maximum Fanout (Rec. SL):
- DL5D2: 56
- DL5D4: 112

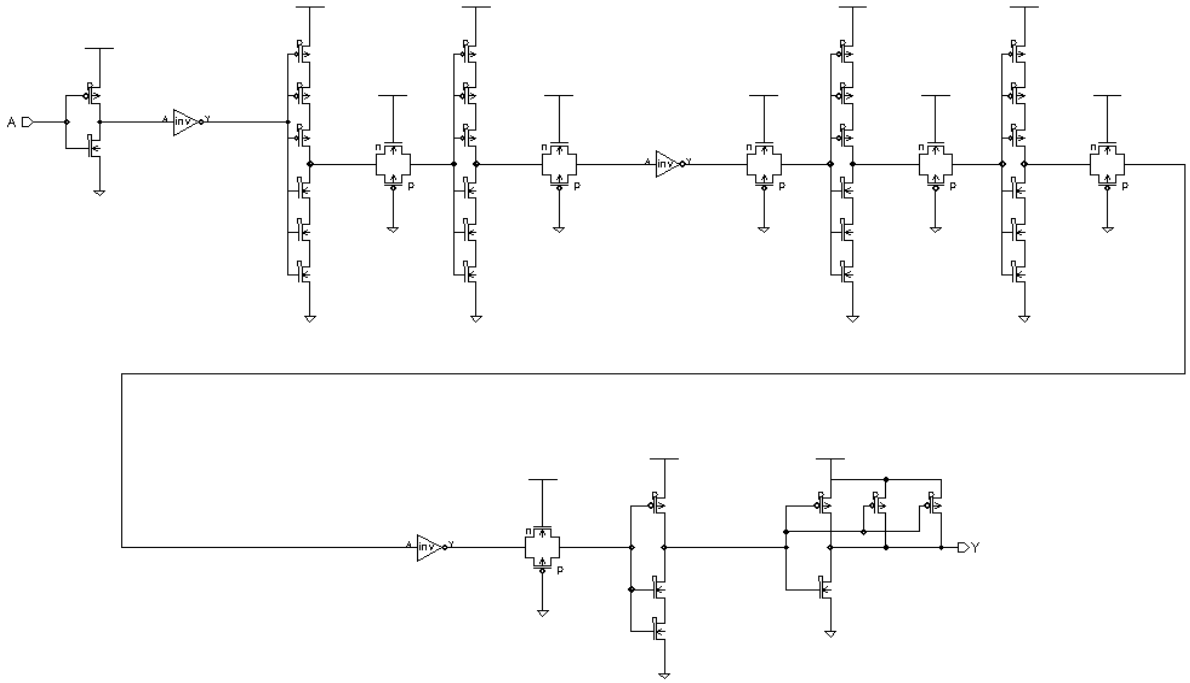
Gate Count:
- DL5D2: 14
- DL5D4: 15



Symbol

A	Y
0	0
1	1

Truth Table



Schematic

DL5D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	2.85	2.82 + 0.015*SL	2.83 + 0.013*SL	2.84 + 0.012*SL
	tPHL	3.02	2.98 + 0.021*SL	2.99 + 0.017*SL	3.01 + 0.016*SL
	tR	0.13	0.08 + 0.027*SL	0.08 + 0.027*SL	0.05 + 0.029*SL
	tF	0.15	0.09 + 0.031*SL	0.09 + 0.031*SL	0.06 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

DL5D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

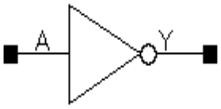
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	2.88	2.86 + 0.011*SL	2.87 + 0.008*SL	2.88 + 0.007*SL
	tPHL	3.06	3.03 + 0.013*SL	3.05 + 0.009*SL	3.06 + 0.008*SL
	tR	0.13	0.08 + 0.024*SL	0.10 + 0.015*SL	0.08 + 0.017*SL
	tF	0.15	0.11 + 0.021*SL	0.13 + 0.015*SL	0.10 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Input: A
Output: Y
Input Loading (SL):
- IV: 1
- IVD2: 2
- IVD3: 3
- IVD4: 4

Maximum Fanout (Rec. SL):
- IV: 28
- IVD2: 56
- IVD3: 84
- IVD4: 112

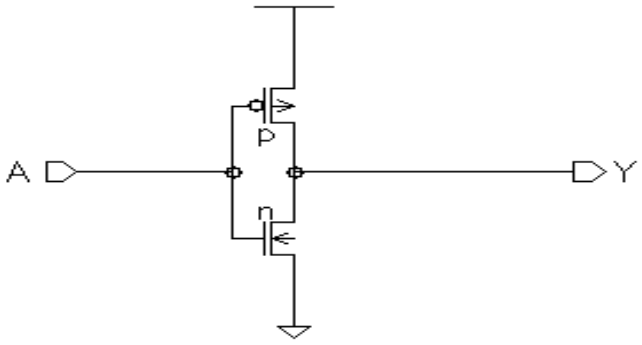
Gate Count:
- IV, IVD2: 1
- IVD3, IVD4: 2



Symbol

A	Y
0	1
1	0

Truth Table



Schematic

IV Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.32	0.23 + 0.047*SL	0.26 + 0.037*SL	0.25 + 0.037*SL
	t_{PHL}	0.06	-0.02 + 0.040*SL	0.03 + 0.022*SL	0.14 + 0.017*SL
	t_R	0.41	0.26 + 0.073*SL	0.23 + 0.082*SL	0.14 + 0.087*SL
	t_F	0.32	0.24 + 0.036*SL	0.26 + 0.029*SL	0.22 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.25	0.19 + 0.031*SL	0.22 + 0.020*SL	0.25 + 0.018*SL
	t_{PHL}	-0.01	-0.06 + 0.028*SL	-0.02 + 0.015*SL	0.08 + 0.010*SL
	t_R	0.29	0.22 + 0.039*SL	0.21 + 0.041*SL	0.16 + 0.044*SL
	t_F	0.27	0.21 + 0.026*SL	0.25 + 0.016*SL	0.26 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVD3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.23	0.19 + 0.022*SL	0.21 + 0.014*SL	0.25 + 0.012*SL
	t_{PHL}	-0.03	-0.06 + 0.017*SL	-0.04 + 0.012*SL	0.04 + 0.007*SL
	t_R	0.27	0.21 + 0.028*SL	0.22 + 0.026*SL	0.19 + 0.028*SL
	t_F	0.25	0.21 + 0.019*SL	0.24 + 0.011*SL	0.25 + 0.010*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVD4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

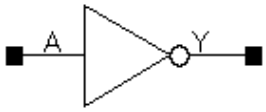
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.22	0.18 + 0.018*SL	0.20 + 0.011*SL	0.25 + 0.009*SL
	t_{PHL}	-0.03	-0.06 + 0.012*SL	-0.05 + 0.010*SL	0.02 + 0.006*SL
	t_R	0.25	0.21 + 0.020*SL	0.22 + 0.019*SL	0.19 + 0.020*SL
	t_F	0.23	0.21 + 0.012*SL	0.22 + 0.009*SL	0.26 + 0.007*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Input: A
Output: Y
Input Loading (SL):
- IVD6: 6
- IVD8: 8

Maximum Fanout (Rec. SL):
- IVD6: 168
- IVD8: 224

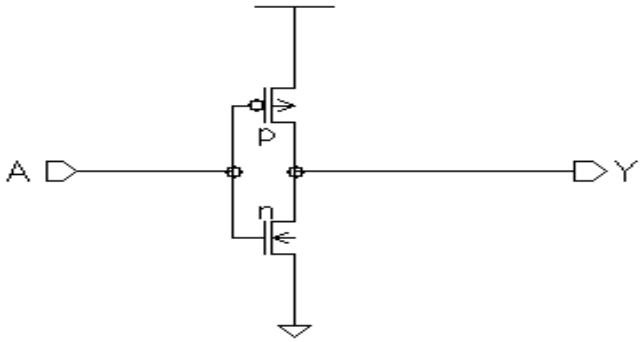
Gate Count:
- IVD6: 3
- IVD8: 4



Symbol

A	Y
0	1
1	0

Truth Table



Schematic

IVD6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.21	0.18 + 0.012*SL	0.19 + 0.009*SL	0.24 + 0.006*SL
	t_{PHL}	-0.04	-0.06 + 0.008*SL	-0.06 + 0.008*SL	-0.00 + 0.005*SL
	t_R	0.24	0.21 + 0.013*SL	0.21 + 0.013*SL	0.22 + 0.013*SL
	t_F	0.23	0.21 + 0.009*SL	0.22 + 0.007*SL	0.25 + 0.005*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVD8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

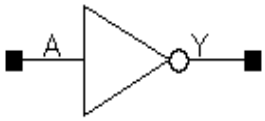
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.20	0.18 + 0.010*SL	0.19 + 0.007*SL	0.23 + 0.005*SL
	t_{PHL}	-0.05	-0.06 + 0.007*SL	-0.06 + 0.006*SL	-0.02 + 0.004*SL
	t_R	0.23	0.21 + 0.013*SL	0.21 + 0.010*SL	0.24 + 0.009*SL
	t_F	0.22	0.21 + 0.007*SL	0.21 + 0.006*SL	0.25 + 0.004*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Input: A
Outputs: Y
Input Loading (SL):
- IVD12: 12
- IVD16: 16

Maximum Fanout (Rec. SL):
- IVD12: 336
- IVD16: 448

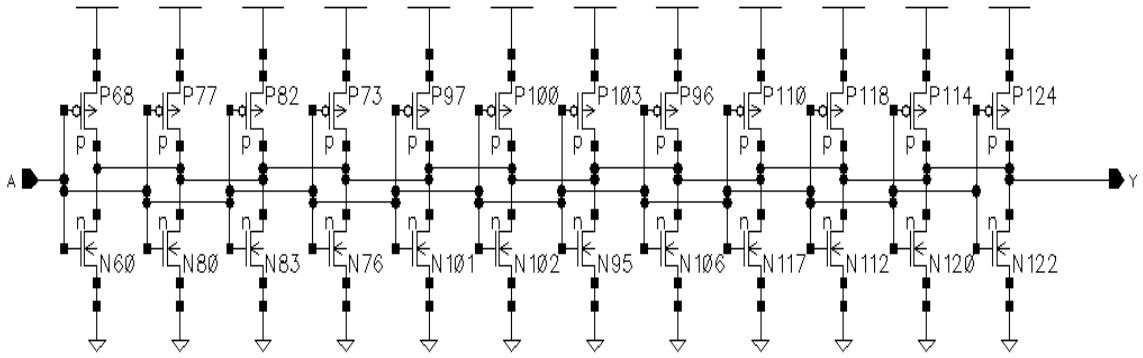
Gate Count:
- IVD12: 6
- IVD16: 8



Symbol

A	Y
0	1
1	0

Truth Table



Schematic

IVD12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.20	0.18 + 0.007*SL	0.19 + 0.005*SL	0.21 + 0.004*SL
	tPHL	-0.05	-0.07 + 0.007*SL	-0.06 + 0.004*SL	-0.03 + 0.003*SL
	tR	0.24	0.23 + 0.004*SL	0.22 + 0.006*SL	0.20 + 0.007*SL
	tF	0.22	0.20 + 0.010*SL	0.21 + 0.004*SL	0.23 + 0.003*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVD16 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

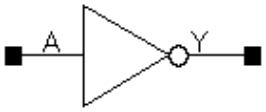
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.19	0.18 + 0.006*SL	0.19 + 0.004*SL	0.21 + 0.003*SL
	tPHL	-0.06	-0.07 + 0.006*SL	-0.06 + 0.003*SL	-0.05 + 0.003*SL
	tR	0.23	0.23 + 0.001*SL	0.22 + 0.005*SL	0.22 + 0.005*SL
	tF	0.21	0.20 + 0.009*SL	0.21 + 0.003*SL	0.22 + 0.003*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Input: A
Output: Y
Input Loading (SL):
- IVA: 1.5
- IVD2A: 3
- IVD3A: 4.5
- IVD4A: 6

Maximum Fanout (Rec. SL):
- IVA: 56
- IVD2A: 112
- IVD3A:168
- IVD4A: 224

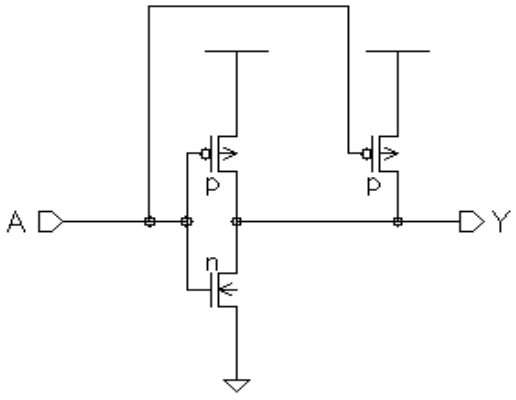
Gate Count:
- IVA:1
- IVD2A: 2
- IVD3A: 3
- IVD4A: 4



Symbol

A	Y
0	1
1	0

Truth Table



Schematic

IVA Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.20	0.13 + 0.036*SL	0.17 + 0.021*SL	0.23 + 0.019*SL
	t_{PHL}	0.10	0.03 + 0.035*SL	0.07 + 0.021*SL	0.16 + 0.017*SL
	t_R	0.34	0.26 + 0.041*SL	0.26 + 0.039*SL	0.19 + 0.043*SL
	t_F	0.32	0.25 + 0.032*SL	0.26 + 0.029*SL	0.21 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVD2A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.16	0.12 + 0.018*SL	0.14 + 0.013*SL	0.20 + 0.010*SL
	t_{PHL}	0.06	0.01 + 0.023*SL	0.04 + 0.013*SL	0.12 + 0.009*SL
	t_R	0.29	0.23 + 0.027*SL	0.26 + 0.018*SL	0.24 + 0.019*SL
	t_F	0.26	0.21 + 0.027*SL	0.24 + 0.016*SL	0.25 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVD3A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.15	0.11 + 0.016*SL	0.13 + 0.009*SL	0.18 + 0.007*SL
	t_{PHL}	0.04	0.00 + 0.018*SL	0.03 + 0.010*SL	0.09 + 0.007*SL
	t_R	0.27	0.24 + 0.018*SL	0.25 + 0.012*SL	0.25 + 0.012*SL
	t_F	0.25	0.21 + 0.019*SL	0.24 + 0.011*SL	0.25 + 0.010*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVD4A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

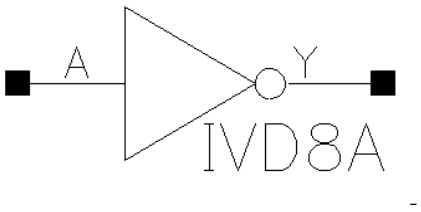
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.14	0.11 + 0.014*SL	0.13 + 0.008*SL	0.17 + 0.006*SL
	t_{PHL}	0.03	0.01 + 0.014*SL	0.02 + 0.008*SL	0.07 + 0.006*SL
	t_R	0.27	0.24 + 0.014*SL	0.25 + 0.010*SL	0.26 + 0.009*SL
	t_F	0.24	0.21 + 0.016*SL	0.23 + 0.009*SL	0.26 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Input: A
Outputs: Y
Input Loading (SL):
- IVD8A: 8
- IVD12A: 18

Maximum Fanout (Rec. SL):
- IVD8A: 448
- IVD12A: 672

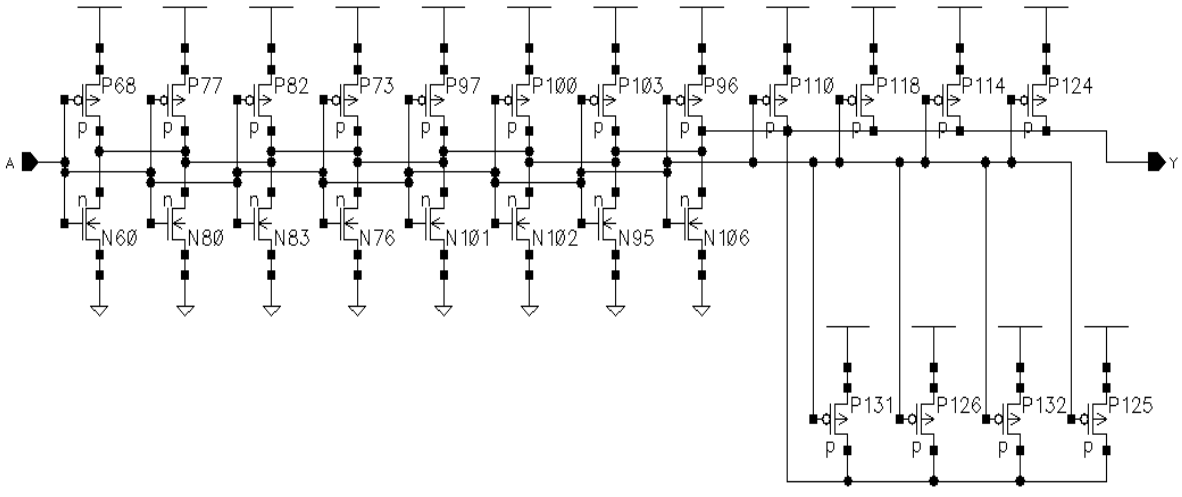
Gate Count:
- IVD8A: 8
- IVD12A: 12



Symbol

A	Y
0	1
1	0

Truth Table



Schematic

IVD8A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.12	0.11 + 0.009*SL	0.12 + 0.005*SL	0.14 + 0.003*SL
	t_{PHL}	0.02	0.01 + 0.005*SL	0.01 + 0.005*SL	0.04 + 0.004*SL
	t_R	0.25	0.24 + 0.005*SL	0.24 + 0.006*SL	0.28 + 0.004*SL
	t_F	0.23	0.22 + 0.005*SL	0.22 + 0.006*SL	0.25 + 0.004*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

IVD12A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

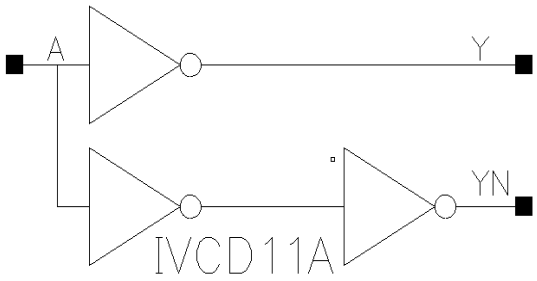
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.12	0.11 + 0.006*SL	0.12 + 0.003*SL	0.12 + 0.003*SL
	t_{PHL}	0.02	0.01 + 0.003*SL	0.01 + 0.004*SL	0.03 + 0.003*SL
	t_R	0.25	0.23 + 0.008*SL	0.24 + 0.004*SL	0.26 + 0.003*SL
	t_F	0.23	0.22 + 0.003*SL	0.22 + 0.004*SL	0.25 + 0.003*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

Input: A
Outputs: Y, YN
Input Loading (SL):
- IVCD11A: 2.5
- IVCD22A: 3.5
- IVCD44A: 5.5
- IVCD88A: 10

Maximum Fanout (Rec. SL):
- IVCD11A: 28
- IVCD22A: 56
- IVCD44A: 114
- IVCD88A: 224

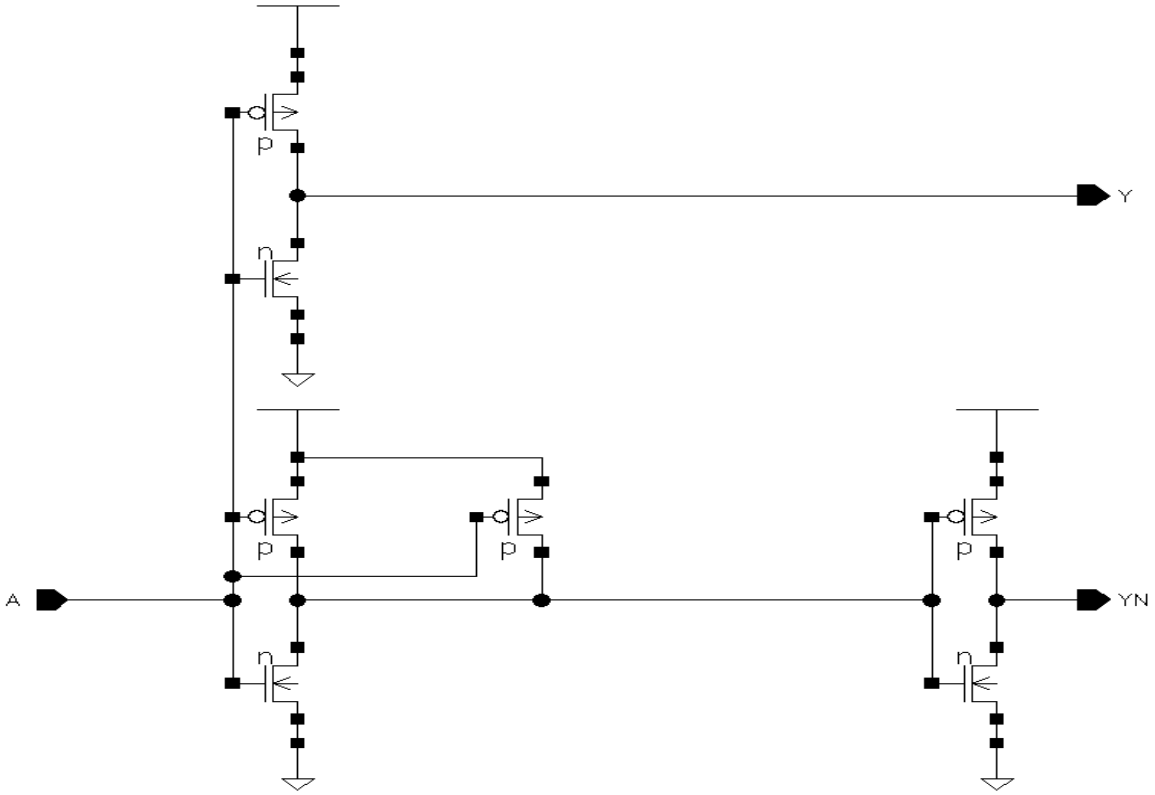
Gate Count:
- IVCD11A: 2
- IVCD22A: 3
- IVCD44A: 5
- IVCD88A: 9



Symbol

A	Y	YN
1	0	1
0	1	0

Truth Table



Schematic

IVCD11A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.29	0.20 + 0.048*SL	0.23 + 0.037*SL	0.23 + 0.037*SL
	tPHL	0.04	-0.05 + 0.043*SL	0.01 + 0.022*SL	0.13 + 0.017*SL
	tR	0.36	0.20 + 0.081*SL	0.19 + 0.083*SL	0.11 + 0.087*SL
	tF	0.29	0.22 + 0.035*SL	0.23 + 0.030*SL	0.20 + 0.032*SL
A to YN	tPLH	0.20	0.12 + 0.039*SL	0.13 + 0.037*SL	0.12 + 0.038*SL
	tPHL	0.23	0.18 + 0.023*SL	0.20 + 0.017*SL	0.21 + 0.016*SL
	tR	0.27	0.10 + 0.084*SL	0.09 + 0.087*SL	0.05 + 0.088*SL
	tF	0.15	0.10 + 0.024*SL	0.07 + 0.033*SL	0.05 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVCD22A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.25	0.19 + 0.029*SL	0.22 + 0.020*SL	0.25 + 0.018*SL
	tPHL	-0.01	-0.06 + 0.028*SL	-0.02 + 0.015*SL	0.08 + 0.010*SL
	tR	0.29	0.20 + 0.042*SL	0.20 + 0.041*SL	0.16 + 0.044*SL
	tF	0.25	0.22 + 0.018*SL	0.22 + 0.017*SL	0.25 + 0.015*SL
A to YN	tPLH	0.20	0.15 + 0.023*SL	0.17 + 0.019*SL	0.17 + 0.019*SL
	tPHL	0.23	0.21 + 0.013*SL	0.22 + 0.010*SL	0.24 + 0.008*SL
	tR	0.18	0.10 + 0.041*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	tF	0.13	0.10 + 0.017*SL	0.10 + 0.016*SL	0.08 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVCD44A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.22	0.18 + 0.017*SL	0.20 + 0.011*SL	0.24 + 0.009*SL
	tPHL	-0.03	-0.06 + 0.012*SL	-0.05 + 0.010*SL	0.02 + 0.006*SL
	tR	0.24	0.21 + 0.017*SL	0.20 + 0.020*SL	0.19 + 0.020*SL
	tF	0.23	0.21 + 0.012*SL	0.22 + 0.008*SL	0.23 + 0.008*SL
A to YN	tPLH	0.24	0.22 + 0.010*SL	0.22 + 0.009*SL	0.22 + 0.009*SL
	tPHL	0.27	0.25 + 0.009*SL	0.26 + 0.006*SL	0.29 + 0.004*SL
	tR	0.15	0.11 + 0.019*SL	0.11 + 0.019*SL	0.09 + 0.021*SL
	tF	0.12	0.11 + 0.007*SL	0.11 + 0.008*SL	0.12 + 0.007*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVCD88A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

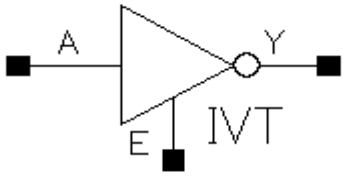
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.20	0.18 + 0.009*SL	0.19 + 0.007*SL	0.21 + 0.005*SL
	tPHL	-0.05	-0.06 + 0.008*SL	-0.06 + 0.006*SL	-0.02 + 0.004*SL
	tR	0.22	0.21 + 0.009*SL	0.20 + 0.010*SL	0.21 + 0.010*SL
	tF	0.22	0.21 + 0.004*SL	0.21 + 0.005*SL	0.23 + 0.004*SL
A to YN	tPLH	0.18	0.17 + 0.005*SL	0.17 + 0.005*SL	0.18 + 0.005*SL
	tPHL	0.38	0.37 + 0.005*SL	0.37 + 0.004*SL	0.38 + 0.003*SL
	tR	0.13	0.12 + 0.004*SL	0.10 + 0.010*SL	0.10 + 0.010*SL
	tF	0.14	0.13 + 0.005*SL	0.13 + 0.004*SL	0.15 + 0.004*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: A, E
Output: Y
Input Loading (SL):
- IVT: A : 1, E : 1.5
- IVTD2: A : 1, E : 2
- IVTD5: A : 1, E : 2
- IVTD9: A : 1, E : 2

Maximum Fanout (Rec. SL):
- IVT: 28
- IVTD2: 56
- IVTD5: 120
- IVTD9: 232

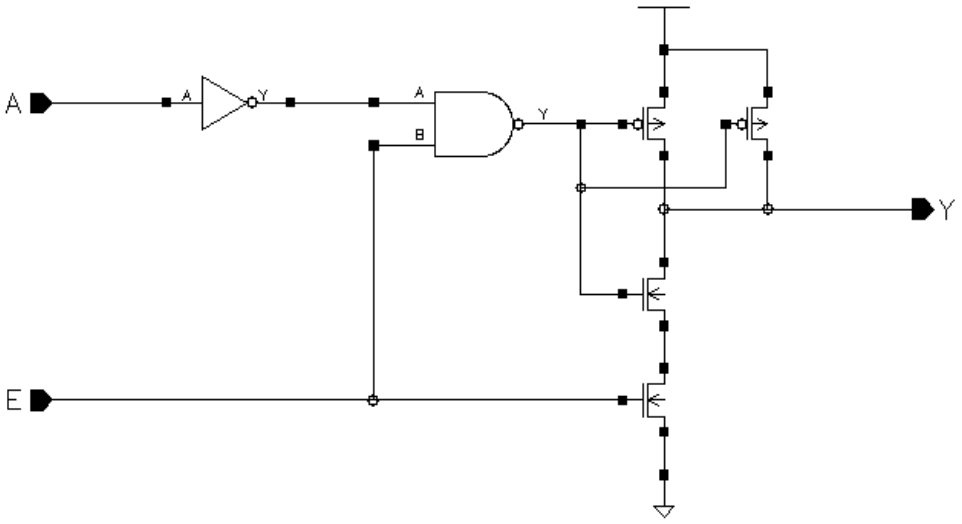
Gate Count:
- IVT : 3
- IVTD2 : 4
- IVTD5 : 5
- IVTD9 : 7



Symbol

A	E	Y
x	0	hi-z
0	1	1
1	1	0

Truth Table



Schematic

IVT Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.40	0.36 + 0.022*SL	0.37 + 0.019*SL	0.37 + 0.018*SL
	tPHL	0.22	0.16 + 0.031*SL	0.17 + 0.026*SL	0.18 + 0.026*SL
	tR	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.05 + 0.043*SL
	tF	0.20	0.09 + 0.056*SL	0.09 + 0.056*SL	0.06 + 0.057*SL
E to Y	tPLH	0.15	0.09 + 0.026*SL	0.12 + 0.019*SL	0.13 + 0.018*SL
	tPHL	0.02	-0.08 + 0.049*SL	-0.02 + 0.029*SL	0.05 + 0.026*SL
	tR	0.19	0.11 + 0.041*SL	0.11 + 0.040*SL	0.06 + 0.042*SL
	tF	0.32	0.22 + 0.054*SL	0.22 + 0.052*SL	0.16 + 0.055*SL
	tPLZ	0.40	0.40 + -0.000*SL	0.40 + -0.000*SL	0.40 + -0.000*SL
	tPHZ	0.44	0.44 + -0.000*SL	0.44 + -0.000*SL	0.44 + -0.000*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVTD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.42	0.39 + 0.014*SL	0.40 + 0.010*SL	0.42 + 0.009*SL
	tPHL	0.25	0.21 + 0.021*SL	0.23 + 0.014*SL	0.24 + 0.013*SL
	tR	0.14	0.10 + 0.020*SL	0.10 + 0.020*SL	0.08 + 0.021*SL
	tF	0.17	0.12 + 0.029*SL	0.12 + 0.029*SL	0.10 + 0.029*SL
E to Y	tPLH	0.17	0.14 + 0.014*SL	0.15 + 0.011*SL	0.18 + 0.009*SL
	tPHL	-0.04	-0.10 + 0.032*SL	-0.06 + 0.018*SL	0.03 + 0.014*SL
	tR	0.17	0.13 + 0.018*SL	0.13 + 0.019*SL	0.10 + 0.020*SL
	tF	0.26	0.18 + 0.040*SL	0.22 + 0.027*SL	0.20 + 0.028*SL
	tPLZ	0.40	0.40 + -0.000*SL	0.40 + -0.000*SL	0.40 + -0.000*SL
	tPHZ	0.52	0.53 + -0.000*SL	0.52 + -0.000*SL	0.52 + -0.000*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVTD5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.44	0.43 + 0.010*SL	0.43 + 0.009*SL	0.45 + 0.008*SL
	t_{PHL}	0.29	0.27 + 0.007*SL	0.28 + 0.005*SL	0.30 + 0.004*SL
	t_R	0.14	0.10 + 0.019*SL	0.11 + 0.016*SL	0.09 + 0.017*SL
	t_F	0.11	0.10 + 0.005*SL	0.10 + 0.006*SL	0.09 + 0.007*SL
E to Y	t_{PLH}	0.13	0.09 + 0.018*SL	0.12 + 0.010*SL	0.16 + 0.008*SL
	t_{PHL}	0.21	0.20 + 0.006*SL	0.20 + 0.006*SL	0.23 + 0.004*SL
	t_R	0.17	0.12 + 0.025*SL	0.15 + 0.015*SL	0.13 + 0.016*SL
	t_F	0.09	0.09 + 0.004*SL	0.07 + 0.008*SL	0.10 + 0.006*SL
	t_{PLZ}	0.47	0.47 + 0.001*SL	0.47 + 0.000*SL	0.48 + -0.000*SL
	t_{PHZ}	0.55	0.55 + 0.000*SL	0.55 + -0.000*SL	0.55 + -0.000*SL

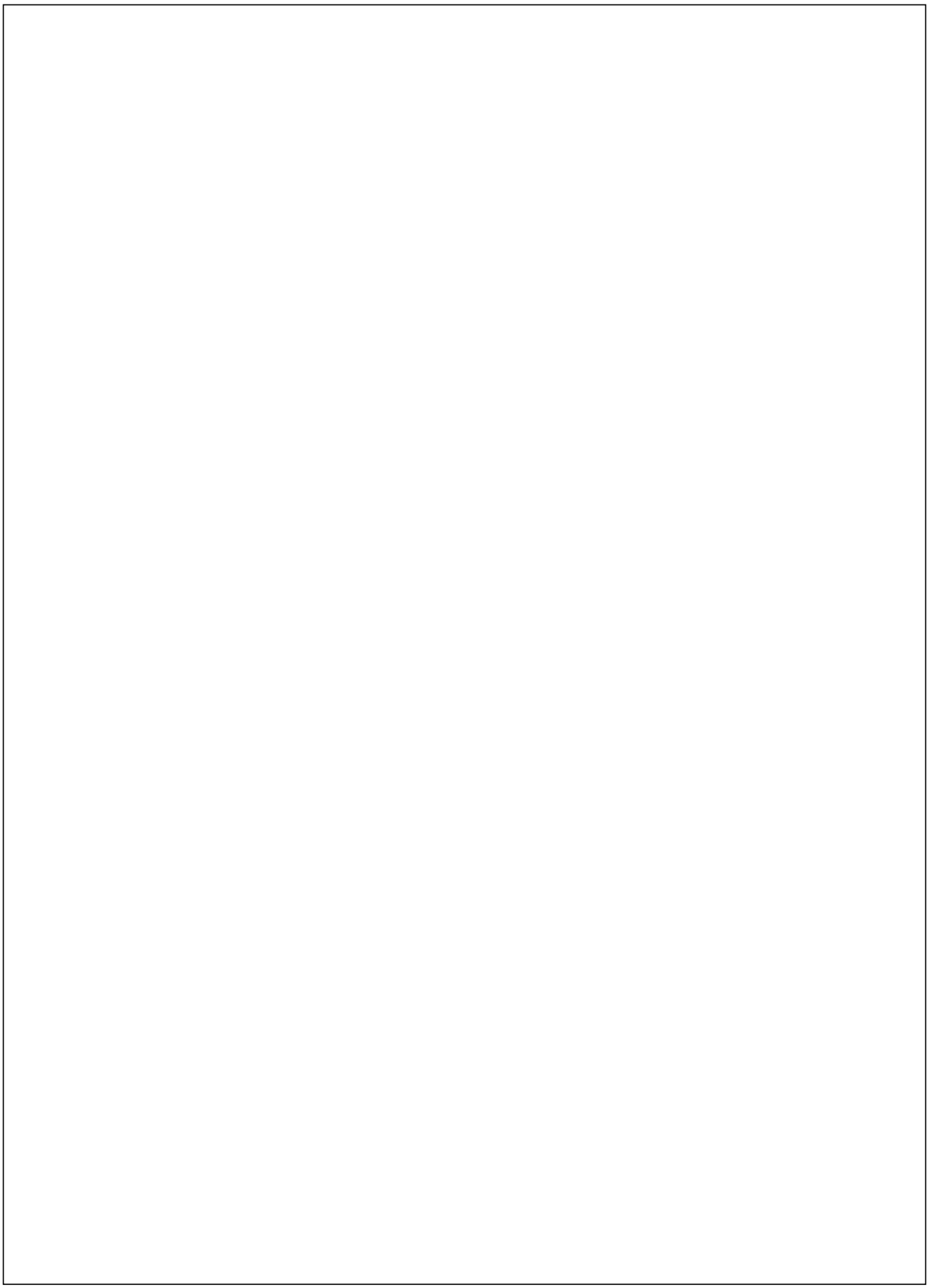
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

IVTD9 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.49	0.48 + 0.006*SL	0.48 + 0.006*SL	0.50 + 0.005*SL
	t_{PHL}	0.34	0.33 + 0.005*SL	0.33 + 0.003*SL	0.34 + 0.003*SL
	t_R	0.13	0.11 + 0.010*SL	0.10 + 0.011*SL	0.13 + 0.009*SL
	t_F	0.16	0.15 + 0.002*SL	0.15 + 0.003*SL	0.14 + 0.004*SL
E to Y	t_{PLH}	0.16	0.14 + 0.011*SL	0.15 + 0.007*SL	0.19 + 0.005*SL
	t_{PHL}	0.24	0.22 + 0.010*SL	0.24 + 0.004*SL	0.26 + 0.003*SL
	t_R	0.17	0.15 + 0.007*SL	0.15 + 0.010*SL	0.16 + 0.009*SL
	t_F	0.12	0.08 + 0.015*SL	0.12 + 0.004*SL	0.11 + 0.004*SL
	t_{PLZ}	0.54	0.54 + 0.000*SL	0.54 + 0.000*SL	0.54 + 0.000*SL
	t_{PHZ}	0.70	0.70 + 0.000*SL	0.70 + 0.000*SL	0.70 + -0.000*SL

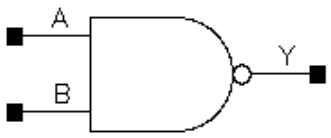
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B
Output: Y
Input Loading (SL):
- ND2 : All : 1
- ND2D2: All : 2
- ND2D5: All: 1
- ND2D7: All: 1

Maximum Fanout (Rec. SL):
- ND2 : 28
- ND2D2 : 56
- ND2D5: 140
- ND2D7: 196

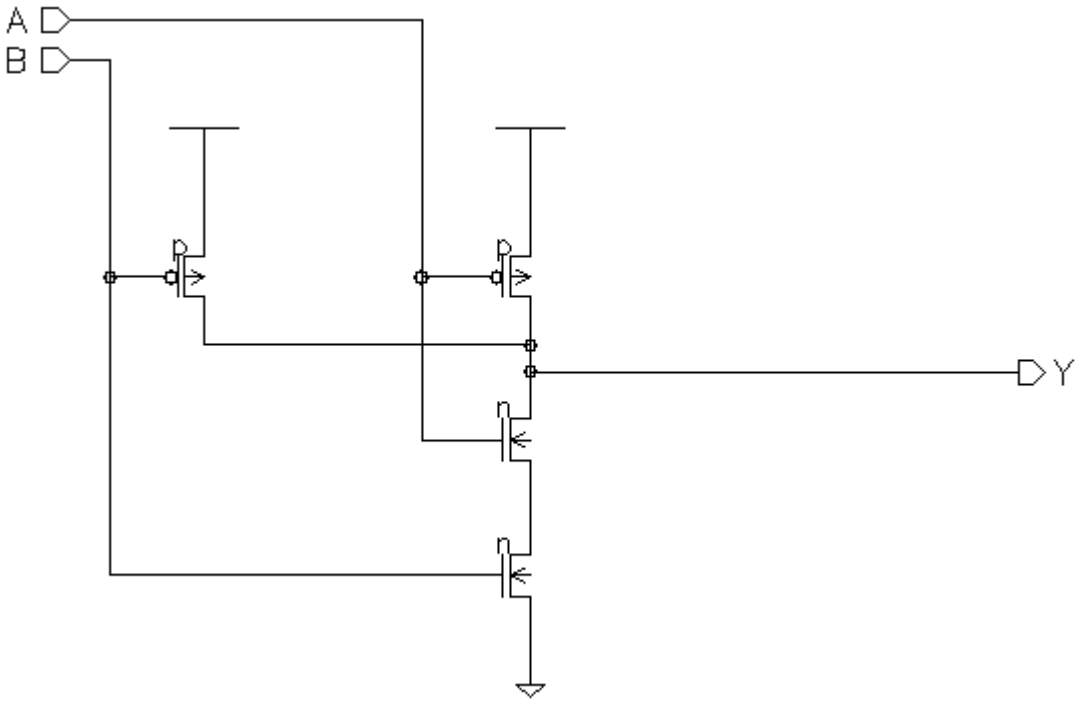
Gate Count:
- ND2 : 1
- ND2D2 : 2
- ND2D5: 4
- ND2D7: 5



Symbol

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table



Schematic

ND2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.29	0.19 + 0.050*SL	0.23 + 0.038*SL	0.24 + 0.037*SL
	t_{PHL}	0.12	0.02 + 0.049*SL	0.08 + 0.030*SL	0.16 + 0.026*SL
	t_R	0.41	0.27 + 0.075*SL	0.25 + 0.081*SL	0.13 + 0.087*SL
	t_F	0.37	0.27 + 0.050*SL	0.26 + 0.053*SL	0.19 + 0.056*SL
B to Y	t_{PLH}	0.34	0.25 + 0.044*SL	0.27 + 0.037*SL	0.27 + 0.037*SL
	t_{PHL}	0.08	-0.01 + 0.042*SL	0.04 + 0.028*SL	0.08 + 0.026*SL
	t_R	0.46	0.31 + 0.075*SL	0.29 + 0.081*SL	0.17 + 0.087*SL
	t_F	0.35	0.26 + 0.046*SL	0.24 + 0.053*SL	0.15 + 0.057*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

ND2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.24	0.17 + 0.031*SL	0.21 + 0.020*SL	0.25 + 0.018*SL
	t_{PHL}	0.07	0.01 + 0.030*SL	0.05 + 0.018*SL	0.14 + 0.014*SL
	t_R	0.34	0.27 + 0.035*SL	0.26 + 0.038*SL	0.19 + 0.041*SL
	t_F	0.32	0.25 + 0.034*SL	0.27 + 0.027*SL	0.25 + 0.028*SL
B to Y	t_{PLH}	0.29	0.24 + 0.024*SL	0.26 + 0.019*SL	0.28 + 0.018*SL
	t_{PHL}	0.03	-0.01 + 0.024*SL	0.01 + 0.016*SL	0.06 + 0.014*SL
	t_R	0.39	0.33 + 0.032*SL	0.31 + 0.038*SL	0.24 + 0.041*SL
	t_F	0.31	0.26 + 0.026*SL	0.26 + 0.025*SL	0.20 + 0.028*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

ND2D5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.42	0.40 + 0.011*SL	0.41 + 0.008*SL	0.42 + 0.007*SL
	tPHL	0.32	0.31 + 0.005*SL	0.30 + 0.006*SL	0.34 + 0.004*SL
	tR	0.13	0.09 + 0.023*SL	0.11 + 0.016*SL	0.08 + 0.018*SL
	tF	0.14	0.13 + 0.006*SL	0.13 + 0.007*SL	0.15 + 0.006*SL
B to Y	tPLH	0.48	0.46 + 0.009*SL	0.46 + 0.008*SL	0.47 + 0.008*SL
	tPHL	0.29	0.28 + 0.008*SL	0.28 + 0.006*SL	0.31 + 0.004*SL
	tR	0.13	0.09 + 0.021*SL	0.10 + 0.017*SL	0.08 + 0.018*SL
	tF	0.15	0.14 + 0.006*SL	0.13 + 0.007*SL	0.15 + 0.006*SL

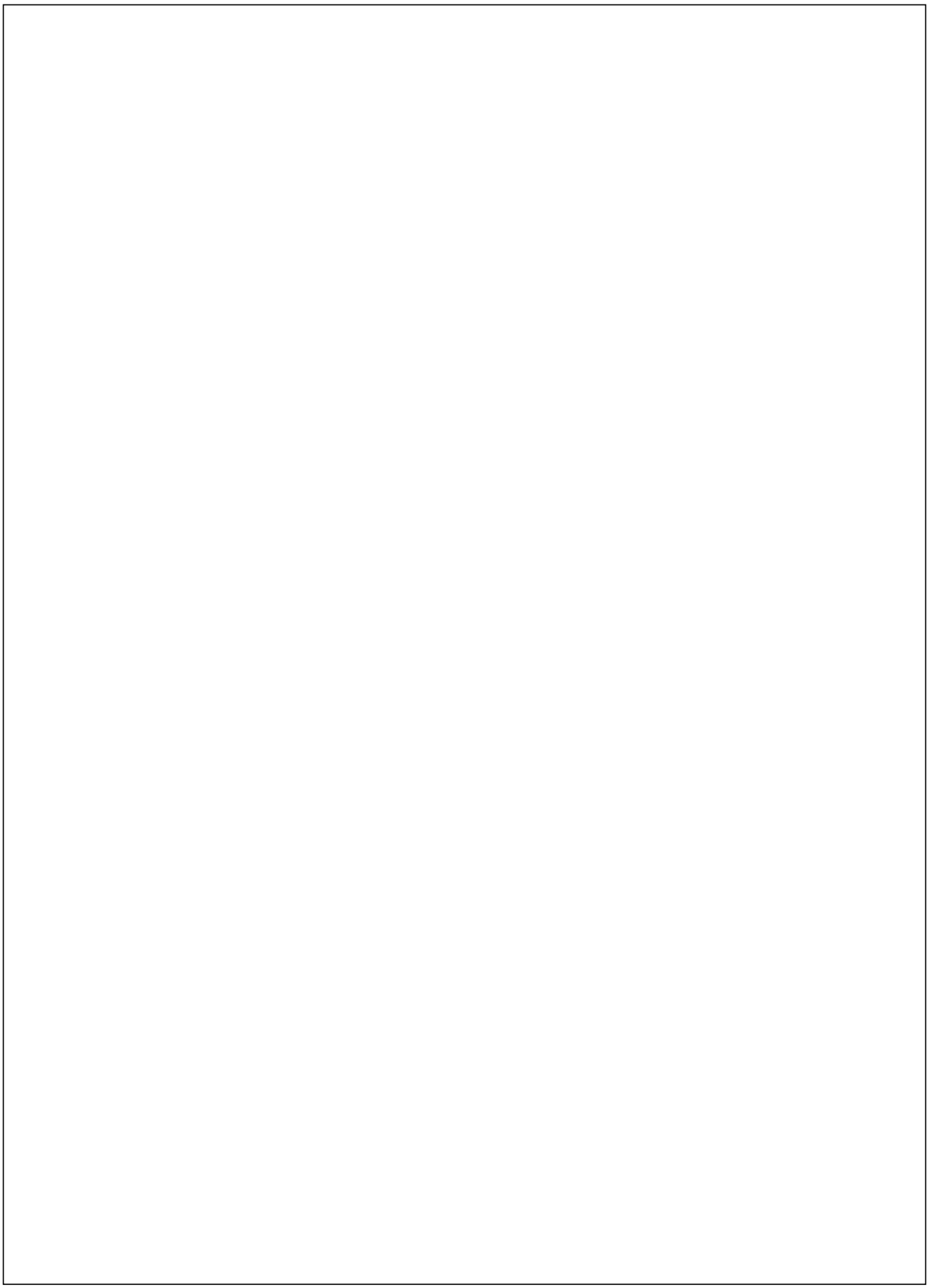
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

ND2D7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.45	0.44 + 0.008*SL	0.44 + 0.006*SL	0.46 + 0.005*SL
	tPHL	0.37	0.36 + 0.006*SL	0.36 + 0.005*SL	0.39 + 0.004*SL
	tR	0.13	0.11 + 0.013*SL	0.11 + 0.012*SL	0.11 + 0.012*SL
	tF	0.19	0.18 + 0.001*SL	0.17 + 0.006*SL	0.20 + 0.004*SL
B to Y	tPLH	0.51	0.50 + 0.007*SL	0.50 + 0.006*SL	0.51 + 0.005*SL
	tPHL	0.35	0.34 + 0.005*SL	0.34 + 0.005*SL	0.36 + 0.004*SL
	tR	0.14	0.11 + 0.013*SL	0.11 + 0.012*SL	0.12 + 0.012*SL
	tF	0.19	0.16 + 0.012*SL	0.18 + 0.005*SL	0.18 + 0.005*SL

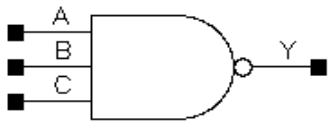
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C
Output: Y
Input Loading (SL):
- ND3 : All : 1
- ND3D2 : All : 2
- ND3D4: All: 1
- ND3D6:All: 1

Maximum Fanout (Rec. SL):
- ND3 : 18
- ND3D2 : 40
- ND3D4: 112
- ND3D6: 168

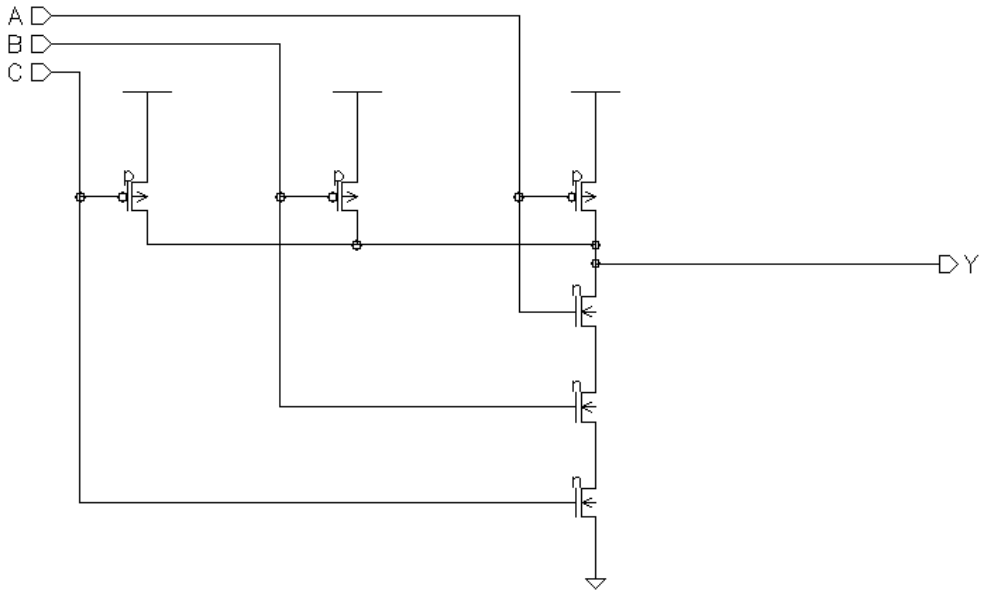
Gate Count:
- ND3 : 2
- ND3D2 : 3
- ND3D4: 4
- ND3D6: 5



Symbol

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table



Schematic

ND3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.29	0.18 + 0.052*SL	0.22 + 0.038*SL	0.24 + 0.037*SL
	t_{PHL}	0.19	0.08 + 0.054*SL	0.13 + 0.039*SL	0.17 + 0.037*SL
	t_R	0.44	0.29 + 0.073*SL	0.27 + 0.081*SL	0.15 + 0.087*SL
	t_F	0.47	0.32 + 0.074*SL	0.30 + 0.081*SL	0.20 + 0.086*SL
B to Y	t_{PLH}	0.33	0.24 + 0.047*SL	0.27 + 0.037*SL	0.27 + 0.037*SL
	t_{PHL}	0.17	0.07 + 0.050*SL	0.10 + 0.038*SL	0.13 + 0.037*SL
	t_R	0.48	0.34 + 0.072*SL	0.31 + 0.081*SL	0.19 + 0.087*SL
	t_F	0.45	0.31 + 0.070*SL	0.28 + 0.081*SL	0.18 + 0.086*SL
C to Y	t_{PLH}	0.37	0.28 + 0.042*SL	0.30 + 0.037*SL	0.29 + 0.037*SL
	t_{PHL}	0.13	0.04 + 0.045*SL	0.06 + 0.038*SL	0.07 + 0.037*SL
	t_R	0.54	0.41 + 0.068*SL	0.37 + 0.080*SL	0.24 + 0.087*SL
	t_F	0.43	0.30 + 0.068*SL	0.25 + 0.082*SL	0.16 + 0.087*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

ND3D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.23	0.16 + 0.032*SL	0.20 + 0.021*SL	0.25 + 0.018*SL
	t_{PHL}	0.14	0.07 + 0.033*SL	0.10 + 0.023*SL	0.17 + 0.019*SL
	t_R	0.36	0.30 + 0.033*SL	0.28 + 0.038*SL	0.21 + 0.041*SL
	t_F	0.39	0.30 + 0.043*SL	0.31 + 0.042*SL	0.27 + 0.044*SL
B to Y	t_{PLH}	0.28	0.23 + 0.025*SL	0.25 + 0.020*SL	0.28 + 0.018*SL
	t_{PHL}	0.11	0.06 + 0.029*SL	0.08 + 0.021*SL	0.12 + 0.019*SL
	t_R	0.42	0.36 + 0.033*SL	0.34 + 0.038*SL	0.26 + 0.042*SL
	t_F	0.39	0.32 + 0.036*SL	0.30 + 0.041*SL	0.23 + 0.045*SL
C to Y	t_{PLH}	0.32	0.27 + 0.023*SL	0.29 + 0.019*SL	0.30 + 0.018*SL
	t_{PHL}	0.08	0.03 + 0.025*SL	0.05 + 0.020*SL	0.07 + 0.019*SL
	t_R	0.47	0.41 + 0.031*SL	0.39 + 0.037*SL	0.31 + 0.041*SL
	t_F	0.37	0.30 + 0.032*SL	0.27 + 0.041*SL	0.20 + 0.045*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

ND3D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.40	0.37 + 0.013*SL	0.38 + 0.010*SL	0.39 + 0.009*SL
	tPHL	0.37	0.34 + 0.011*SL	0.36 + 0.006*SL	0.39 + 0.005*SL
	tR	0.13	0.10 + 0.016*SL	0.08 + 0.022*SL	0.08 + 0.022*SL
	tF	0.13	0.11 + 0.013*SL	0.12 + 0.009*SL	0.14 + 0.008*SL
B to Y	tPLH	0.45	0.43 + 0.012*SL	0.43 + 0.010*SL	0.44 + 0.010*SL
	tPHL	0.36	0.34 + 0.009*SL	0.35 + 0.007*SL	0.38 + 0.005*SL
	tR	0.14	0.09 + 0.027*SL	0.11 + 0.021*SL	0.07 + 0.023*SL
	tF	0.14	0.11 + 0.011*SL	0.12 + 0.009*SL	0.14 + 0.008*SL
C to Y	tPLH	0.49	0.47 + 0.011*SL	0.48 + 0.010*SL	0.48 + 0.010*SL
	tPHL	0.33	0.32 + 0.005*SL	0.31 + 0.007*SL	0.35 + 0.005*SL
	tR	0.13	0.09 + 0.021*SL	0.09 + 0.022*SL	0.08 + 0.022*SL
	tF	0.14	0.12 + 0.011*SL	0.12 + 0.009*SL	0.14 + 0.008*SL

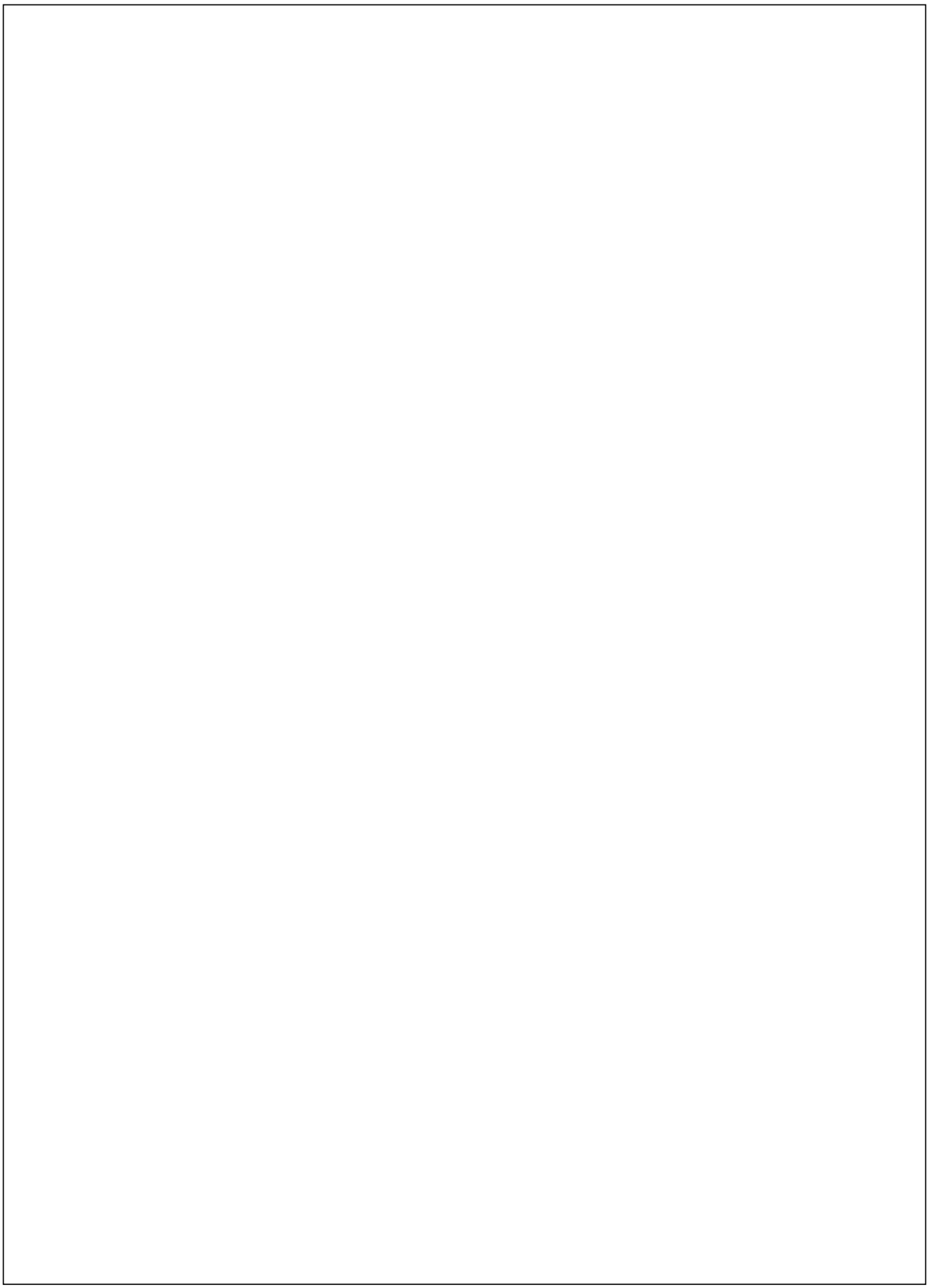
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

ND3D6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.43	0.41 + 0.008*SL	0.42 + 0.007*SL	0.43 + 0.007*SL
	tPHL	0.42	0.41 + 0.007*SL	0.42 + 0.005*SL	0.44 + 0.004*SL
	tR	0.13	0.10 + 0.015*SL	0.11 + 0.014*SL	0.09 + 0.015*SL
	tF	0.17	0.16 + 0.008*SL	0.16 + 0.005*SL	0.17 + 0.005*SL
B to Y	tPLH	0.49	0.47 + 0.008*SL	0.47 + 0.007*SL	0.49 + 0.006*SL
	tPHL	0.42	0.41 + 0.006*SL	0.41 + 0.005*SL	0.44 + 0.004*SL
	tR	0.13	0.10 + 0.020*SL	0.11 + 0.014*SL	0.10 + 0.015*SL
	tF	0.17	0.16 + 0.005*SL	0.16 + 0.006*SL	0.17 + 0.005*SL
C to Y	tPLH	0.53	0.51 + 0.011*SL	0.52 + 0.007*SL	0.53 + 0.006*SL
	tPHL	0.37	0.36 + 0.007*SL	0.36 + 0.006*SL	0.40 + 0.004*SL
	tR	0.14	0.10 + 0.019*SL	0.11 + 0.014*SL	0.10 + 0.014*SL
	tF	0.18	0.18 + 0.001*SL	0.16 + 0.006*SL	0.19 + 0.005*SL

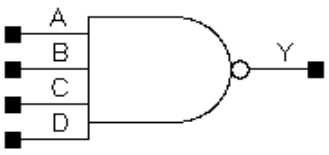
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D
Output: Y
Input Loading (SL):
- ND4: All : 1
- ND4D2: All : 2
- ND4D5: All: 1
- ND4D7: All: 1

Maximum Fanout (Rec. SL):
- ND4: 14
- ND4D2: 28
- ND4D5: 140
- ND4D7: 196

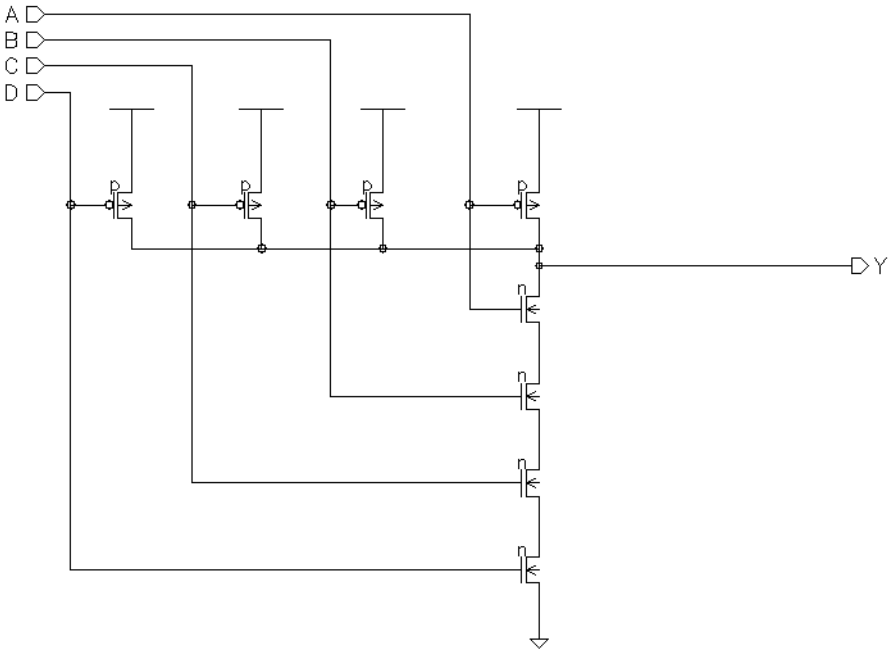
Gate Count:
- ND4 : 2
- ND4D2 : 4
- ND4D5: 5
- ND4D7: 6



Symbol

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Truth Table



Schematic

ND4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.29	0.18 + 0.053*SL	0.23 + 0.038*SL	0.25 + 0.037*SL
	t_{PHL}	0.24	0.12 + 0.061*SL	0.16 + 0.048*SL	0.17 + 0.047*SL
	t_R	0.45	0.30 + 0.074*SL	0.28 + 0.081*SL	0.17 + 0.087*SL
	t_F	0.57	0.36 + 0.103*SL	0.36 + 0.106*SL	0.24 + 0.112*SL
B to Y	t_{PLH}	0.33	0.24 + 0.048*SL	0.27 + 0.038*SL	0.27 + 0.037*SL
	t_{PHL}	0.23	0.12 + 0.057*SL	0.15 + 0.048*SL	0.16 + 0.047*SL
	t_R	0.50	0.36 + 0.070*SL	0.32 + 0.081*SL	0.21 + 0.087*SL
	t_F	0.56	0.38 + 0.094*SL	0.34 + 0.107*SL	0.23 + 0.112*SL
C to Y	t_{PLH}	0.37	0.28 + 0.044*SL	0.30 + 0.037*SL	0.30 + 0.037*SL
	t_{PHL}	0.21	0.10 + 0.052*SL	0.12 + 0.047*SL	0.12 + 0.047*SL
	t_R	0.55	0.41 + 0.069*SL	0.38 + 0.081*SL	0.25 + 0.087*SL
	t_F	0.55	0.36 + 0.093*SL	0.32 + 0.107*SL	0.22 + 0.112*SL
D to Y	t_{PLH}	0.39	0.31 + 0.042*SL	0.32 + 0.038*SL	0.32 + 0.037*SL
	t_{PHL}	0.18	0.08 + 0.051*SL	0.09 + 0.047*SL	0.09 + 0.047*SL
	t_R	0.60	0.47 + 0.066*SL	0.43 + 0.080*SL	0.30 + 0.087*SL
	t_F	0.52	0.33 + 0.096*SL	0.29 + 0.108*SL	0.22 + 0.112*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

ND4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.23	0.17 + 0.032*SL	0.20 + 0.021*SL	0.25 + 0.018*SL
	t_{PHL}	0.19	0.12 + 0.034*SL	0.14 + 0.026*SL	0.19 + 0.024*SL
	t_R	0.38	0.30 + 0.036*SL	0.30 + 0.038*SL	0.23 + 0.041*SL
	t_F	0.48	0.38 + 0.049*SL	0.37 + 0.054*SL	0.31 + 0.057*SL
B to Y	t_{PLH}	0.28	0.23 + 0.026*SL	0.25 + 0.020*SL	0.28 + 0.019*SL
	t_{PHL}	0.18	0.12 + 0.033*SL	0.14 + 0.026*SL	0.16 + 0.024*SL
	t_R	0.43	0.36 + 0.034*SL	0.35 + 0.038*SL	0.28 + 0.042*SL
	t_F	0.48	0.38 + 0.049*SL	0.37 + 0.054*SL	0.30 + 0.057*SL
C to Y	t_{PLH}	0.32	0.27 + 0.025*SL	0.29 + 0.020*SL	0.31 + 0.019*SL
	t_{PHL}	0.16	0.11 + 0.029*SL	0.12 + 0.025*SL	0.13 + 0.024*SL
	t_R	0.49	0.42 + 0.032*SL	0.41 + 0.038*SL	0.33 + 0.042*SL
	t_F	0.46	0.38 + 0.041*SL	0.34 + 0.054*SL	0.27 + 0.058*SL
D to Y	t_{PLH}	0.35	0.30 + 0.023*SL	0.31 + 0.019*SL	0.33 + 0.018*SL
	t_{PHL}	0.14	0.08 + 0.028*SL	0.09 + 0.025*SL	0.10 + 0.024*SL
	t_R	0.54	0.48 + 0.030*SL	0.46 + 0.037*SL	0.38 + 0.041*SL
	t_F	0.44	0.35 + 0.047*SL	0.32 + 0.055*SL	0.26 + 0.058*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

ND4D5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.42	0.40 + 0.009*SL	0.40 + 0.008*SL	0.41 + 0.008*SL
	tPHL	0.46	0.45 + 0.005*SL	0.45 + 0.006*SL	0.49 + 0.004*SL
	tR	0.13	0.09 + 0.018*SL	0.10 + 0.017*SL	0.08 + 0.018*SL
	tF	0.16	0.15 + 0.006*SL	0.14 + 0.007*SL	0.15 + 0.006*SL
B to Y	tPLH	0.47	0.45 + 0.009*SL	0.46 + 0.008*SL	0.47 + 0.007*SL
	tPHL	0.47	0.45 + 0.008*SL	0.46 + 0.006*SL	0.49 + 0.004*SL
	tR	0.13	0.09 + 0.020*SL	0.10 + 0.017*SL	0.09 + 0.018*SL
	tF	0.15	0.14 + 0.007*SL	0.14 + 0.008*SL	0.17 + 0.006*SL
C to Y	tPLH	0.51	0.49 + 0.009*SL	0.50 + 0.008*SL	0.50 + 0.008*SL
	tPHL	0.45	0.44 + 0.005*SL	0.44 + 0.006*SL	0.48 + 0.004*SL
	tR	0.14	0.10 + 0.020*SL	0.11 + 0.017*SL	0.09 + 0.017*SL
	tF	0.16	0.15 + 0.006*SL	0.14 + 0.007*SL	0.16 + 0.006*SL
D to Y	tPLH	0.54	0.52 + 0.010*SL	0.53 + 0.008*SL	0.54 + 0.008*SL
	tPHL	0.43	0.42 + 0.007*SL	0.42 + 0.006*SL	0.45 + 0.004*SL
	tR	0.13	0.10 + 0.016*SL	0.10 + 0.017*SL	0.10 + 0.017*SL
	tF	0.16	0.15 + 0.005*SL	0.14 + 0.007*SL	0.17 + 0.006*SL

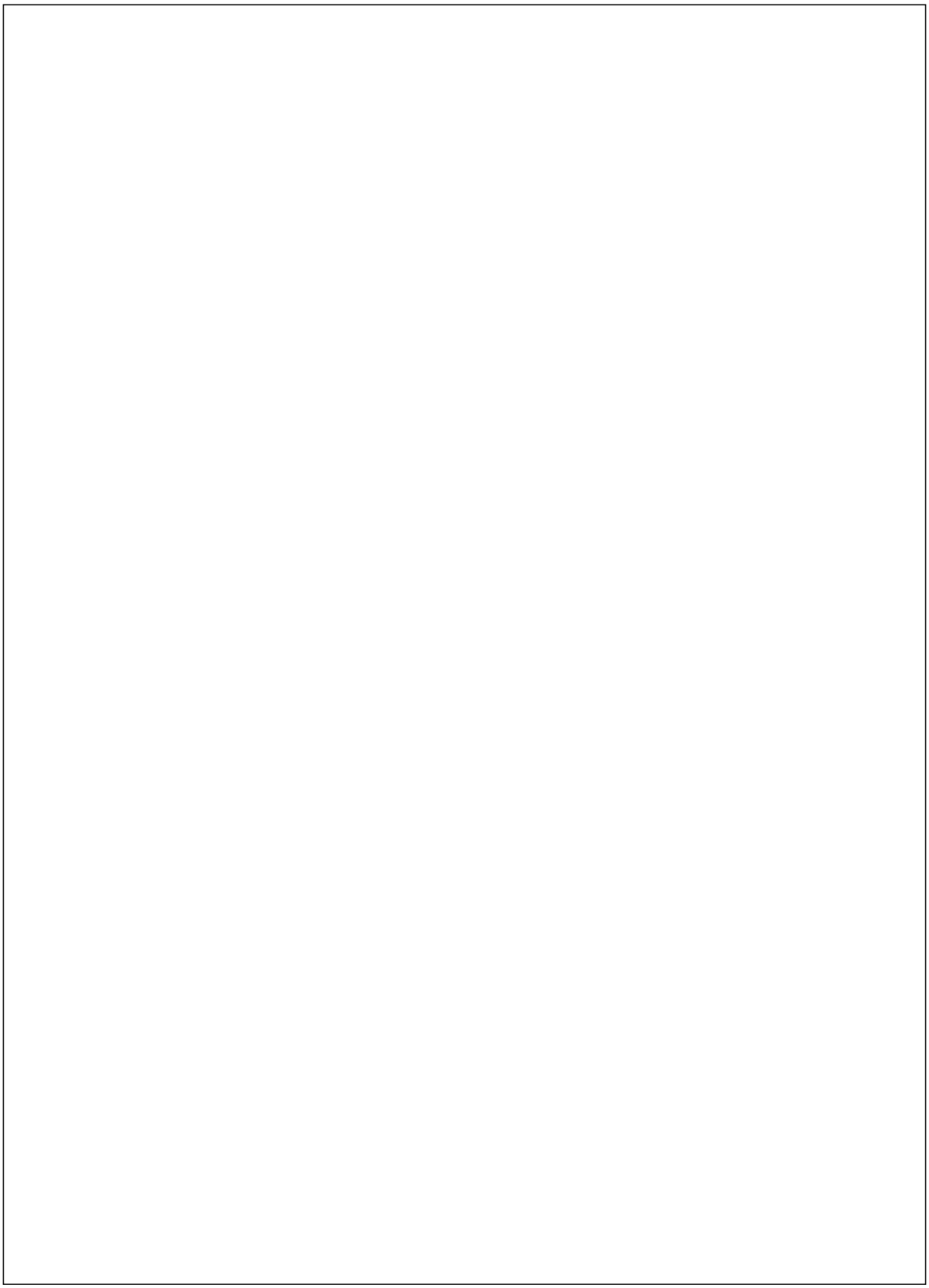
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

ND4D7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.46	0.45 + 0.006*SL	0.45 + 0.006*SL	0.46 + 0.006*SL
	tPHL	0.52	0.51 + 0.008*SL	0.52 + 0.005*SL	0.54 + 0.003*SL
	tR	0.13	0.11 + 0.014*SL	0.11 + 0.012*SL	0.11 + 0.012*SL
	tF	0.19	0.19 + 0.004*SL	0.18 + 0.005*SL	0.21 + 0.004*SL
B to Y	tPLH	0.51	0.50 + 0.007*SL	0.50 + 0.006*SL	0.51 + 0.006*SL
	tPHL	0.53	0.51 + 0.007*SL	0.52 + 0.005*SL	0.55 + 0.004*SL
	tR	0.14	0.11 + 0.016*SL	0.12 + 0.012*SL	0.11 + 0.012*SL
	tF	0.20	0.21 + -0.003*SL	0.18 + 0.005*SL	0.19 + 0.004*SL
C to Y	tPLH	0.55	0.54 + 0.007*SL	0.54 + 0.006*SL	0.55 + 0.006*SL
	tPHL	0.51	0.50 + 0.006*SL	0.51 + 0.005*SL	0.53 + 0.003*SL
	tR	0.14	0.11 + 0.014*SL	0.11 + 0.012*SL	0.11 + 0.012*SL
	tF	0.20	0.19 + 0.005*SL	0.19 + 0.005*SL	0.20 + 0.004*SL
D to Y	tPLH	0.58	0.57 + 0.005*SL	0.57 + 0.006*SL	0.59 + 0.005*SL
	tPHL	0.49	0.48 + 0.005*SL	0.48 + 0.005*SL	0.51 + 0.003*SL
	tR	0.14	0.11 + 0.015*SL	0.12 + 0.012*SL	0.11 + 0.012*SL
	tF	0.20	0.19 + 0.003*SL	0.19 + 0.005*SL	0.20 + 0.004*SL

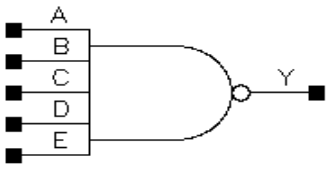
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D, E
Output: Y
Input Loading (SL):
- ND5: All : 1
- ND5D2: All: 2
- ND5D4:All: 1
- ND5D6: All: 1

Maximum Fanout (Rec. SL):
- ND5: 12
- ND5D2: 24
- ND5D4: 112
- ND5D6: 168

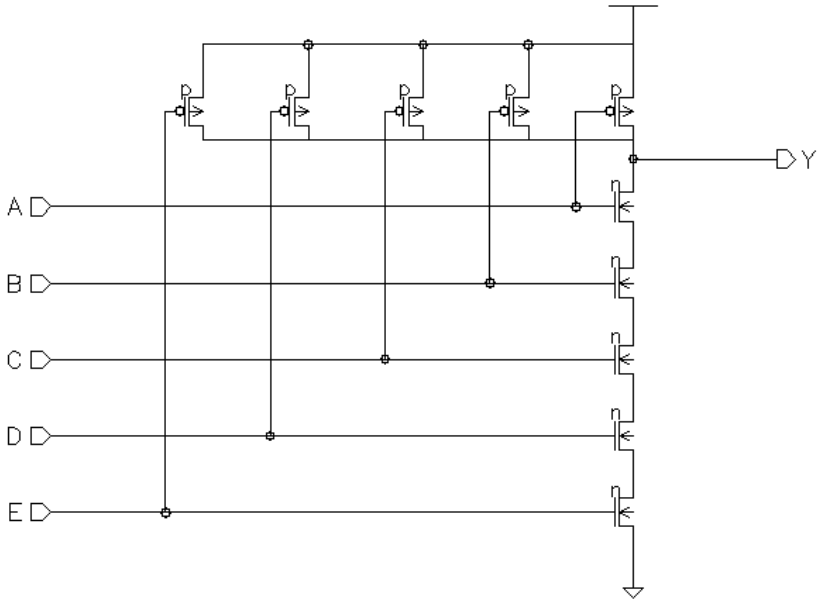
Gate Count:
- ND5: 3
- ND5D2: 5
- ND5D4: 5
- ND5D6: 6



Symbol

A	B	C	D	E	Y
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

Truth Table



Schematic

ND5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.30	0.19 + 0.053*SL	0.23 + 0.038*SL	0.25 + 0.037*SL
	tPHL	0.29	0.16 + 0.067*SL	0.19 + 0.059*SL	0.19 + 0.059*SL
	t_R	0.46	0.32 + 0.074*SL	0.29 + 0.081*SL	0.18 + 0.087*SL
	t_F	0.71	0.45 + 0.127*SL	0.43 + 0.135*SL	0.32 + 0.140*SL
B to Y	tPLH	0.34	0.24 + 0.048*SL	0.27 + 0.038*SL	0.28 + 0.037*SL
	tPHL	0.30	0.17 + 0.064*SL	0.19 + 0.059*SL	0.19 + 0.059*SL
	t_R	0.51	0.37 + 0.072*SL	0.34 + 0.081*SL	0.23 + 0.087*SL
	t_F	0.71	0.46 + 0.122*SL	0.42 + 0.135*SL	0.32 + 0.140*SL
C to Y	tPLH	0.37	0.28 + 0.045*SL	0.30 + 0.038*SL	0.31 + 0.037*SL
	tPHL	0.29	0.16 + 0.063*SL	0.18 + 0.059*SL	0.17 + 0.059*SL
	t_R	0.56	0.42 + 0.071*SL	0.39 + 0.081*SL	0.27 + 0.087*SL
	t_F	0.69	0.45 + 0.123*SL	0.41 + 0.136*SL	0.32 + 0.140*SL
D to Y	tPLH	0.39	0.31 + 0.043*SL	0.32 + 0.038*SL	0.33 + 0.037*SL
	tPHL	0.28	0.15 + 0.061*SL	0.16 + 0.059*SL	0.16 + 0.059*SL
	t_R	0.62	0.48 + 0.068*SL	0.44 + 0.081*SL	0.32 + 0.087*SL
	t_F	0.67	0.43 + 0.119*SL	0.38 + 0.137*SL	0.31 + 0.141*SL
E to Y	tPLH	0.41	0.33 + 0.043*SL	0.34 + 0.038*SL	0.35 + 0.038*SL
	tPHL	0.26	0.14 + 0.060*SL	0.14 + 0.059*SL	0.14 + 0.059*SL
	t_R	0.67	0.53 + 0.070*SL	0.50 + 0.081*SL	0.38 + 0.087*SL
	t_F	0.66	0.41 + 0.126*SL	0.37 + 0.138*SL	0.31 + 0.141*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

ND5D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.24	0.18 + 0.031*SL	0.21 + 0.021*SL	0.26 + 0.018*SL
	tPHL	0.23	0.16 + 0.039*SL	0.18 + 0.031*SL	0.20 + 0.030*SL
	t_R	0.39	0.32 + 0.034*SL	0.31 + 0.038*SL	0.25 + 0.041*SL
	t_F	0.59	0.45 + 0.068*SL	0.46 + 0.067*SL	0.38 + 0.071*SL
B to Y	tPLH	0.29	0.23 + 0.027*SL	0.25 + 0.020*SL	0.29 + 0.019*SL
	tPHL	0.24	0.17 + 0.034*SL	0.18 + 0.031*SL	0.19 + 0.030*SL
	t_R	0.44	0.37 + 0.033*SL	0.36 + 0.039*SL	0.29 + 0.042*SL
	t_F	0.60	0.47 + 0.061*SL	0.45 + 0.067*SL	0.37 + 0.071*SL
C to Y	tPLH	0.32	0.27 + 0.025*SL	0.29 + 0.020*SL	0.31 + 0.019*SL
	tPHL	0.23	0.16 + 0.036*SL	0.18 + 0.030*SL	0.18 + 0.030*SL
	t_R	0.50	0.44 + 0.032*SL	0.42 + 0.038*SL	0.34 + 0.042*SL
	t_F	0.58	0.45 + 0.066*SL	0.44 + 0.067*SL	0.36 + 0.072*SL
D to Y	tPLH	0.35	0.30 + 0.024*SL	0.31 + 0.020*SL	0.33 + 0.019*SL
	tPHL	0.22	0.15 + 0.033*SL	0.16 + 0.030*SL	0.17 + 0.030*SL
	t_R	0.55	0.48 + 0.034*SL	0.47 + 0.038*SL	0.40 + 0.042*SL
	t_F	0.56	0.44 + 0.062*SL	0.42 + 0.068*SL	0.35 + 0.072*SL
E to Y	tPLH	0.36	0.31 + 0.024*SL	0.33 + 0.019*SL	0.35 + 0.019*SL
	tPHL	0.20	0.14 + 0.030*SL	0.14 + 0.030*SL	0.15 + 0.030*SL
	t_R	0.60	0.54 + 0.032*SL	0.52 + 0.037*SL	0.45 + 0.041*SL
	t_F	0.54	0.42 + 0.064*SL	0.40 + 0.069*SL	0.34 + 0.072*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

ND5D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.40	0.38 + 0.011*SL	0.39 + 0.010*SL	0.40 + 0.009*SL
	tPHL	0.51	0.49 + 0.007*SL	0.49 + 0.007*SL	0.53 + 0.005*SL
	tR	0.13	0.09 + 0.022*SL	0.09 + 0.022*SL	0.07 + 0.022*SL
	tF	0.16	0.14 + 0.007*SL	0.14 + 0.008*SL	0.15 + 0.008*SL
B to Y	tPLH	0.46	0.44 + 0.010*SL	0.44 + 0.010*SL	0.45 + 0.009*SL
	tPHL	0.52	0.51 + 0.004*SL	0.50 + 0.007*SL	0.55 + 0.005*SL
	tR	0.13	0.11 + 0.013*SL	0.08 + 0.022*SL	0.07 + 0.023*SL
	tF	0.15	0.13 + 0.007*SL	0.13 + 0.008*SL	0.13 + 0.008*SL
C to Y	tPLH	0.49	0.47 + 0.011*SL	0.48 + 0.010*SL	0.48 + 0.009*SL
	tPHL	0.53	0.51 + 0.007*SL	0.51 + 0.007*SL	0.55 + 0.005*SL
	tR	0.14	0.10 + 0.021*SL	0.09 + 0.021*SL	0.07 + 0.022*SL
	tF	0.16	0.15 + 0.006*SL	0.14 + 0.008*SL	0.13 + 0.008*SL
D to Y	tPLH	0.52	0.50 + 0.012*SL	0.51 + 0.010*SL	0.51 + 0.009*SL
	tPHL	0.51	0.49 + 0.010*SL	0.50 + 0.007*SL	0.54 + 0.005*SL
	tR	0.14	0.10 + 0.019*SL	0.09 + 0.022*SL	0.09 + 0.022*SL
	tF	0.16	0.13 + 0.012*SL	0.14 + 0.008*SL	0.16 + 0.008*SL
E to Y	tPLH	0.54	0.52 + 0.011*SL	0.52 + 0.010*SL	0.53 + 0.009*SL
	tPHL	0.49	0.47 + 0.010*SL	0.48 + 0.006*SL	0.51 + 0.005*SL
	tR	0.14	0.10 + 0.020*SL	0.10 + 0.021*SL	0.08 + 0.022*SL
	tF	0.17	0.16 + 0.003*SL	0.15 + 0.008*SL	0.15 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

ND5D6 Switching Characteristics

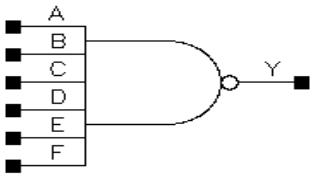
[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.45	0.43 + 0.008*SL	0.44 + 0.007*SL	0.44 + 0.006*SL
	t_{PHL}	0.56	0.55 + 0.006*SL	0.55 + 0.006*SL	0.58 + 0.004*SL
	t_R	0.14	0.11 + 0.015*SL	0.12 + 0.014*SL	0.09 + 0.015*SL
	t_F	0.19	0.19 + -0.002*SL	0.17 + 0.006*SL	0.18 + 0.005*SL
B to Y	t_{PLH}	0.49	0.48 + 0.008*SL	0.48 + 0.007*SL	0.49 + 0.006*SL
	t_{PHL}	0.58	0.57 + 0.005*SL	0.57 + 0.006*SL	0.60 + 0.004*SL
	t_R	0.13	0.10 + 0.017*SL	0.11 + 0.014*SL	0.09 + 0.015*SL
	t_F	0.20	0.18 + 0.006*SL	0.19 + 0.005*SL	0.18 + 0.005*SL
C to Y	t_{PLH}	0.53	0.52 + 0.007*SL	0.52 + 0.007*SL	0.53 + 0.006*SL
	t_{PHL}	0.58	0.57 + 0.005*SL	0.57 + 0.005*SL	0.60 + 0.004*SL
	t_R	0.14	0.10 + 0.019*SL	0.11 + 0.014*SL	0.10 + 0.014*SL
	t_F	0.19	0.18 + 0.006*SL	0.18 + 0.005*SL	0.18 + 0.005*SL
D to Y	t_{PLH}	0.57	0.55 + 0.009*SL	0.56 + 0.007*SL	0.56 + 0.006*SL
	t_{PHL}	0.57	0.56 + 0.006*SL	0.56 + 0.005*SL	0.59 + 0.004*SL
	t_R	0.13	0.10 + 0.014*SL	0.10 + 0.015*SL	0.12 + 0.014*SL
	t_F	0.19	0.19 + -0.002*SL	0.17 + 0.006*SL	0.18 + 0.005*SL
E to Y	t_{PLH}	0.58	0.57 + 0.007*SL	0.57 + 0.007*SL	0.58 + 0.006*SL
	t_{PHL}	0.55	0.53 + 0.006*SL	0.54 + 0.006*SL	0.57 + 0.004*SL
	t_R	0.14	0.10 + 0.018*SL	0.11 + 0.014*SL	0.12 + 0.014*SL
	t_F	0.20	0.19 + 0.004*SL	0.19 + 0.005*SL	0.18 + 0.005*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: A, B, C, D, E, F
Output: Y
Input Loading (SL): All : 1
Maximum Fanout (Rec. SL):
- ND6: 28
- ND6D2: 56
- ND6D4: 112
- ND6D8: 224

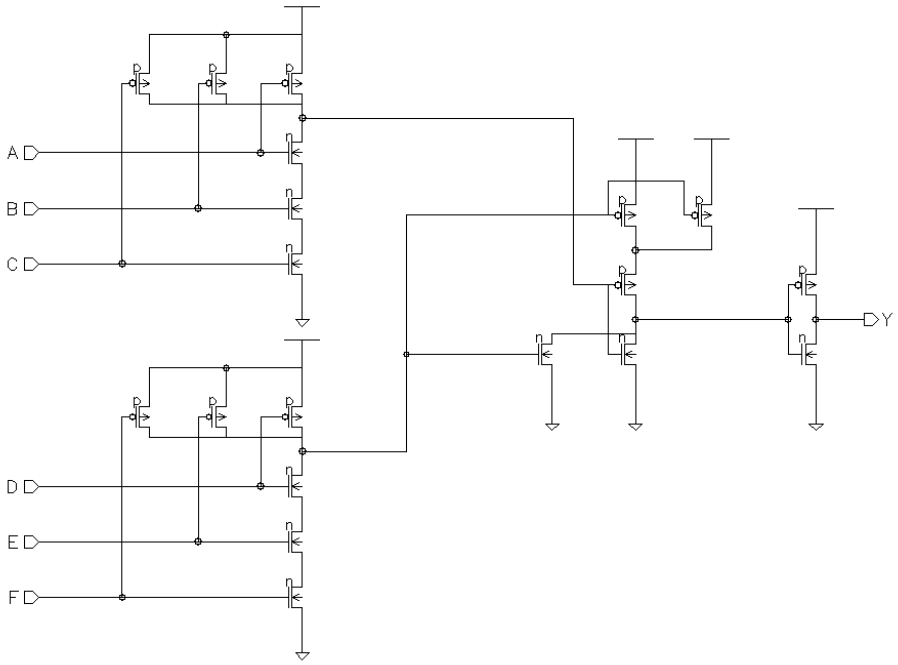
Gate Count:
- ND6: 5
- ND6D2: 5
- ND6D4: 6
- ND6D8: 9



Symbol

A	B	C	D	E	F	Y
0	x	x	x	x	x	1
x	0	x	x	x	x	1
x	x	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
1	1	1	1	1	1	0

Truth Table



Schematic

ND6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.38	0.31 + 0.036*SL	0.31 + 0.037*SL	0.32 + 0.036*SL
	tPHL	0.34	0.30 + 0.023*SL	0.31 + 0.017*SL	0.34 + 0.016*SL
	tR	0.24	0.07 + 0.080*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.15	0.08 + 0.036*SL	0.09 + 0.031*SL	0.07 + 0.032*SL
B to Y	tPLH	0.44	0.36 + 0.038*SL	0.37 + 0.036*SL	0.37 + 0.036*SL
	tPHL	0.34	0.29 + 0.024*SL	0.31 + 0.017*SL	0.34 + 0.016*SL
	tR	0.23	0.08 + 0.076*SL	0.06 + 0.084*SL	0.05 + 0.084*SL
	tF	0.15	0.07 + 0.037*SL	0.09 + 0.031*SL	0.06 + 0.032*SL
C to Y	tPLH	0.48	0.41 + 0.036*SL	0.41 + 0.037*SL	0.42 + 0.036*SL
	tPHL	0.30	0.25 + 0.025*SL	0.28 + 0.017*SL	0.29 + 0.016*SL
	tR	0.24	0.09 + 0.075*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.15	0.08 + 0.034*SL	0.09 + 0.031*SL	0.06 + 0.032*SL
D to Y	tPLH	0.44	0.37 + 0.038*SL	0.37 + 0.036*SL	0.37 + 0.036*SL
	tPHL	0.37	0.32 + 0.025*SL	0.34 + 0.017*SL	0.37 + 0.016*SL
	tR	0.24	0.07 + 0.081*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.08 + 0.034*SL	0.08 + 0.031*SL	0.06 + 0.032*SL
E to Y	tPLH	0.49	0.42 + 0.039*SL	0.42 + 0.036*SL	0.42 + 0.036*SL
	tPHL	0.35	0.30 + 0.024*SL	0.32 + 0.018*SL	0.35 + 0.016*SL
	tR	0.24	0.08 + 0.078*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.15	0.07 + 0.038*SL	0.09 + 0.031*SL	0.06 + 0.033*SL
F to Y	tPLH	0.53	0.46 + 0.039*SL	0.46 + 0.036*SL	0.46 + 0.036*SL
	tPHL	0.32	0.27 + 0.024*SL	0.29 + 0.017*SL	0.31 + 0.016*SL
	tR	0.24	0.07 + 0.082*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.15	0.08 + 0.037*SL	0.09 + 0.031*SL	0.07 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

ND6D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.38	0.34 + 0.019*SL	0.34 + 0.018*SL	0.35 + 0.018*SL
	tPHL	0.41	0.38 + 0.017*SL	0.40 + 0.011*SL	0.45 + 0.009*SL
	tR	0.16	0.08 + 0.042*SL	0.08 + 0.041*SL	0.05 + 0.042*SL
	tF	0.16	0.12 + 0.020*SL	0.14 + 0.015*SL	0.14 + 0.015*SL
B to Y	tPLH	0.43	0.39 + 0.020*SL	0.40 + 0.018*SL	0.40 + 0.018*SL
	tPHL	0.40	0.37 + 0.019*SL	0.39 + 0.011*SL	0.44 + 0.009*SL
	tR	0.16	0.09 + 0.036*SL	0.07 + 0.041*SL	0.05 + 0.043*SL
	tF	0.17	0.12 + 0.027*SL	0.15 + 0.015*SL	0.13 + 0.016*SL
C to Y	tPLH	0.47	0.43 + 0.021*SL	0.44 + 0.018*SL	0.44 + 0.018*SL
	tPHL	0.37	0.33 + 0.019*SL	0.35 + 0.011*SL	0.40 + 0.009*SL
	tR	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.05 + 0.042*SL
	tF	0.16	0.12 + 0.023*SL	0.14 + 0.015*SL	0.13 + 0.015*SL
D to Y	tPLH	0.39	0.35 + 0.019*SL	0.35 + 0.019*SL	0.36 + 0.018*SL
	tPHL	0.42	0.38 + 0.018*SL	0.40 + 0.011*SL	0.45 + 0.009*SL
	tR	0.15	0.07 + 0.041*SL	0.07 + 0.042*SL	0.05 + 0.042*SL
	tF	0.17	0.14 + 0.013*SL	0.13 + 0.016*SL	0.14 + 0.015*SL
E to Y	tPLH	0.44	0.40 + 0.020*SL	0.41 + 0.018*SL	0.41 + 0.018*SL
	tPHL	0.41	0.37 + 0.022*SL	0.40 + 0.011*SL	0.44 + 0.009*SL
	tR	0.17	0.09 + 0.037*SL	0.08 + 0.041*SL	0.05 + 0.042*SL
	tF	0.16	0.13 + 0.020*SL	0.14 + 0.015*SL	0.14 + 0.015*SL
F to Y	tPLH	0.49	0.45 + 0.020*SL	0.45 + 0.018*SL	0.45 + 0.018*SL
	tPHL	0.37	0.33 + 0.020*SL	0.35 + 0.011*SL	0.40 + 0.009*SL
	tR	0.16	0.08 + 0.042*SL	0.08 + 0.041*SL	0.05 + 0.042*SL
	tF	0.16	0.12 + 0.018*SL	0.13 + 0.016*SL	0.14 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 < SL < 20.00, *Range3 : 20.00 < SL

ND6D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.41	0.39 + 0.011*SL	0.39 + 0.010*SL	0.40 + 0.009*SL
	tPHL	0.51	0.49 + 0.011*SL	0.50 + 0.008*SL	0.54 + 0.006*SL
	tR	0.14	0.09 + 0.026*SL	0.10 + 0.021*SL	0.07 + 0.022*SL
	tF	0.22	0.20 + 0.008*SL	0.20 + 0.009*SL	0.21 + 0.008*SL
B to Y	tPLH	0.46	0.44 + 0.012*SL	0.44 + 0.010*SL	0.45 + 0.009*SL
	tPHL	0.51	0.49 + 0.010*SL	0.50 + 0.008*SL	0.54 + 0.006*SL
	tR	0.13	0.08 + 0.023*SL	0.09 + 0.022*SL	0.08 + 0.022*SL
	tF	0.22	0.20 + 0.008*SL	0.20 + 0.009*SL	0.21 + 0.008*SL
C to Y	tPLH	0.50	0.48 + 0.010*SL	0.48 + 0.010*SL	0.50 + 0.009*SL
	tPHL	0.47	0.44 + 0.013*SL	0.46 + 0.008*SL	0.50 + 0.006*SL
	tR	0.14	0.08 + 0.029*SL	0.11 + 0.021*SL	0.08 + 0.022*SL
	tF	0.22	0.21 + 0.005*SL	0.20 + 0.008*SL	0.20 + 0.008*SL
D to Y	tPLH	0.42	0.39 + 0.012*SL	0.40 + 0.010*SL	0.41 + 0.009*SL
	tPHL	0.52	0.50 + 0.010*SL	0.50 + 0.008*SL	0.54 + 0.006*SL
	tR	0.13	0.10 + 0.018*SL	0.09 + 0.022*SL	0.08 + 0.022*SL
	tF	0.22	0.20 + 0.008*SL	0.20 + 0.009*SL	0.21 + 0.008*SL
E to Y	tPLH	0.47	0.45 + 0.011*SL	0.45 + 0.010*SL	0.47 + 0.009*SL
	tPHL	0.51	0.48 + 0.012*SL	0.50 + 0.008*SL	0.54 + 0.006*SL
	tR	0.13	0.09 + 0.022*SL	0.09 + 0.022*SL	0.08 + 0.022*SL
	tF	0.22	0.21 + 0.005*SL	0.20 + 0.009*SL	0.21 + 0.008*SL
F to Y	tPLH	0.52	0.49 + 0.012*SL	0.50 + 0.010*SL	0.51 + 0.009*SL
	tPHL	0.46	0.43 + 0.015*SL	0.46 + 0.008*SL	0.50 + 0.006*SL
	tR	0.14	0.10 + 0.021*SL	0.10 + 0.022*SL	0.09 + 0.022*SL
	tF	0.22	0.22 + 0.004*SL	0.20 + 0.008*SL	0.20 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

ND6D8 Switching Characteristics

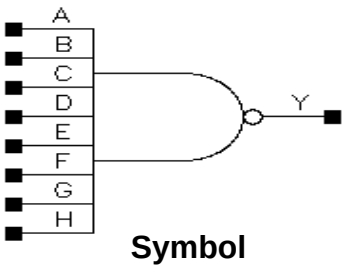
[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.45	0.44 + 0.005*SL	0.44 + 0.005*SL	0.46 + 0.005*SL
	t_{PHL}	0.57	0.55 + 0.010*SL	0.57 + 0.005*SL	0.59 + 0.004*SL
	t_R	0.12	0.09 + 0.015*SL	0.10 + 0.010*SL	0.09 + 0.011*SL
	t_F	0.23	0.23 + 0.004*SL	0.23 + 0.004*SL	0.21 + 0.004*SL
B to Y	t_{PLH}	0.50	0.49 + 0.006*SL	0.49 + 0.005*SL	0.50 + 0.005*SL
	t_{PHL}	0.57	0.56 + 0.006*SL	0.56 + 0.005*SL	0.59 + 0.004*SL
	t_R	0.12	0.09 + 0.015*SL	0.10 + 0.011*SL	0.10 + 0.011*SL
	t_F	0.23	0.22 + 0.004*SL	0.22 + 0.004*SL	0.20 + 0.005*SL
C to Y	t_{PLH}	0.54	0.53 + 0.006*SL	0.53 + 0.005*SL	0.53 + 0.005*SL
	t_{PHL}	0.52	0.51 + 0.006*SL	0.51 + 0.005*SL	0.54 + 0.004*SL
	t_R	0.12	0.09 + 0.011*SL	0.10 + 0.010*SL	0.08 + 0.011*SL
	t_F	0.23	0.22 + 0.004*SL	0.22 + 0.004*SL	0.23 + 0.004*SL
D to Y	t_{PLH}	0.46	0.45 + 0.005*SL	0.45 + 0.005*SL	0.46 + 0.005*SL
	t_{PHL}	0.58	0.56 + 0.009*SL	0.57 + 0.005*SL	0.60 + 0.004*SL
	t_R	0.12	0.09 + 0.013*SL	0.10 + 0.010*SL	0.09 + 0.011*SL
	t_F	0.23	0.23 + 0.001*SL	0.22 + 0.004*SL	0.22 + 0.004*SL
E to Y	t_{PLH}	0.51	0.50 + 0.006*SL	0.50 + 0.005*SL	0.51 + 0.005*SL
	t_{PHL}	0.56	0.55 + 0.008*SL	0.56 + 0.005*SL	0.58 + 0.004*SL
	t_R	0.12	0.10 + 0.012*SL	0.10 + 0.010*SL	0.09 + 0.011*SL
	t_F	0.23	0.23 + 0.002*SL	0.22 + 0.004*SL	0.21 + 0.005*SL
F to Y	t_{PLH}	0.55	0.54 + 0.006*SL	0.54 + 0.005*SL	0.55 + 0.005*SL
	t_{PHL}	0.52	0.51 + 0.005*SL	0.51 + 0.005*SL	0.54 + 0.004*SL
	t_R	0.12	0.10 + 0.012*SL	0.10 + 0.011*SL	0.10 + 0.011*SL
	t_F	0.23	0.22 + 0.004*SL	0.22 + 0.004*SL	0.22 + 0.004*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: A, B, C, D, E, F, G, H
Output: Y
Input Loading (SL): All : 1
Maximum Fanout (Rec. SL):
- ND8: 28
- ND8D2: 56
- ND8D4: 112
- ND8D8: 224

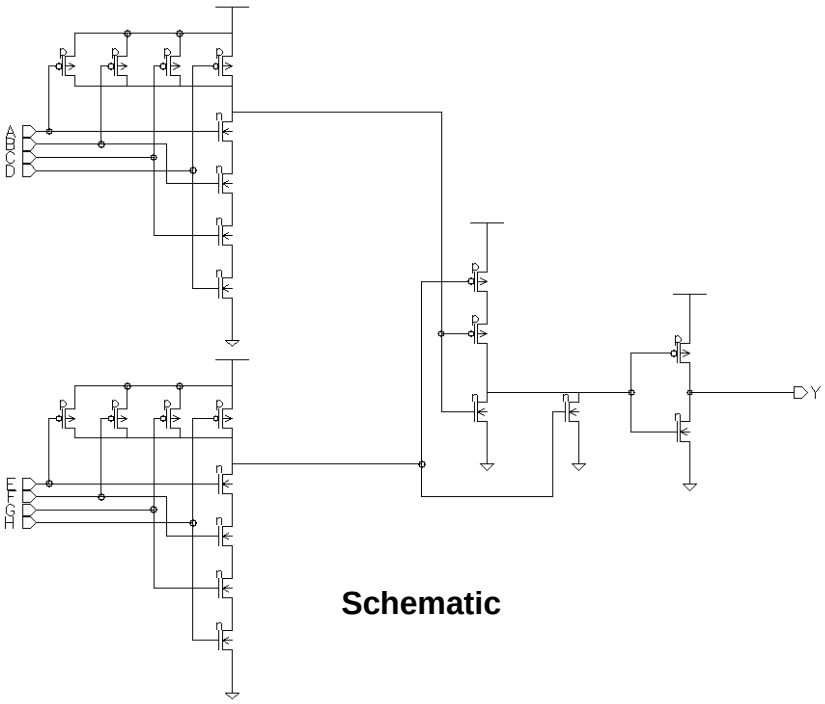
Gate Count:
- ND8: 6
- ND8D2: 6
- ND8D4: 7
- ND8D8: 10



Symbol

A	B	C	D	E	F	G	H	Y
0	x	x	x	x	x	x	x	1
x	0	x	x	x	x	x	x	1
x	x	0	x	x	x	x	x	1
x	x	x	0	x	x	x	x	1
x	x	x	x	0	x	x	x	1
x	x	x	x	x	0	x	x	1
x	x	x	x	x	x	0	x	1
x	x	x	x	x	x	x	0	1
1	1	1	1	1	1	1	1	0

Truth Table



Schematic

ND8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.40	0.33 + 0.036*SL	0.33 + 0.037*SL	0.33 + 0.036*SL
	tPHL	0.45	0.39 + 0.026*SL	0.42 + 0.018*SL	0.45 + 0.016*SL
	tR	0.27	0.11 + 0.076*SL	0.09 + 0.084*SL	0.08 + 0.085*SL
	tF	0.18	0.11 + 0.035*SL	0.13 + 0.030*SL	0.10 + 0.032*SL
B to Y	tPLH	0.45	0.37 + 0.038*SL	0.38 + 0.037*SL	0.38 + 0.036*SL
	tPHL	0.46	0.41 + 0.025*SL	0.43 + 0.018*SL	0.46 + 0.016*SL
	tR	0.27	0.11 + 0.078*SL	0.09 + 0.084*SL	0.08 + 0.085*SL
	tF	0.18	0.11 + 0.033*SL	0.12 + 0.031*SL	0.09 + 0.032*SL
C to Y	tPLH	0.49	0.41 + 0.038*SL	0.41 + 0.037*SL	0.42 + 0.036*SL
	tPHL	0.44	0.38 + 0.026*SL	0.41 + 0.018*SL	0.45 + 0.016*SL
	tR	0.27	0.09 + 0.086*SL	0.10 + 0.084*SL	0.08 + 0.085*SL
	tF	0.18	0.10 + 0.038*SL	0.13 + 0.031*SL	0.10 + 0.032*SL
D to Y	tPLH	0.51	0.44 + 0.037*SL	0.44 + 0.036*SL	0.44 + 0.036*SL
	tPHL	0.42	0.37 + 0.025*SL	0.39 + 0.018*SL	0.42 + 0.016*SL
	tR	0.27	0.12 + 0.076*SL	0.10 + 0.084*SL	0.08 + 0.085*SL
	tF	0.18	0.10 + 0.039*SL	0.13 + 0.030*SL	0.09 + 0.032*SL
E to Y	tPLH	0.42	0.34 + 0.037*SL	0.35 + 0.036*SL	0.35 + 0.036*SL
	tPHL	0.46	0.41 + 0.024*SL	0.43 + 0.018*SL	0.46 + 0.016*SL
	tR	0.27	0.10 + 0.082*SL	0.10 + 0.084*SL	0.08 + 0.085*SL
	tF	0.18	0.11 + 0.033*SL	0.12 + 0.031*SL	0.09 + 0.032*SL
F to Y	tPLH	0.47	0.40 + 0.037*SL	0.40 + 0.036*SL	0.40 + 0.036*SL
	tPHL	0.46	0.41 + 0.024*SL	0.43 + 0.018*SL	0.47 + 0.016*SL
	tR	0.27	0.11 + 0.079*SL	0.10 + 0.084*SL	0.08 + 0.085*SL
	tF	0.19	0.12 + 0.031*SL	0.12 + 0.031*SL	0.09 + 0.032*SL
G to Y	tPLH	0.50	0.43 + 0.037*SL	0.43 + 0.036*SL	0.43 + 0.036*SL
	tPHL	0.44	0.39 + 0.024*SL	0.41 + 0.018*SL	0.45 + 0.016*SL
	tR	0.27	0.11 + 0.080*SL	0.10 + 0.084*SL	0.08 + 0.085*SL
	tF	0.18	0.12 + 0.034*SL	0.13 + 0.031*SL	0.09 + 0.032*SL
H to Y	tPLH	0.53	0.46 + 0.037*SL	0.46 + 0.036*SL	0.46 + 0.036*SL
	tPHL	0.42	0.37 + 0.024*SL	0.39 + 0.018*SL	0.42 + 0.016*SL
	tR	0.27	0.10 + 0.082*SL	0.10 + 0.084*SL	0.08 + 0.085*SL
	tF	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.09 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

ND8D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.38	0.34 + 0.020*SL	0.34 + 0.018*SL	0.34 + 0.018*SL
	tPHL	0.47	0.44 + 0.017*SL	0.45 + 0.011*SL	0.50 + 0.009*SL
	tR	0.16	0.08 + 0.038*SL	0.07 + 0.042*SL	0.05 + 0.043*SL
	tF	0.16	0.13 + 0.018*SL	0.13 + 0.016*SL	0.13 + 0.016*SL
B to Y	tPLH	0.43	0.38 + 0.021*SL	0.39 + 0.018*SL	0.38 + 0.019*SL
	tPHL	0.48	0.44 + 0.018*SL	0.46 + 0.011*SL	0.51 + 0.009*SL
	tR	0.16	0.09 + 0.037*SL	0.07 + 0.042*SL	0.05 + 0.043*SL
	tF	0.16	0.12 + 0.021*SL	0.14 + 0.015*SL	0.13 + 0.016*SL
C to Y	tPLH	0.46	0.42 + 0.020*SL	0.43 + 0.018*SL	0.43 + 0.018*SL
	tPHL	0.46	0.43 + 0.018*SL	0.45 + 0.011*SL	0.50 + 0.009*SL
	tR	0.17	0.09 + 0.040*SL	0.08 + 0.041*SL	0.05 + 0.043*SL
	tF	0.16	0.12 + 0.020*SL	0.13 + 0.016*SL	0.14 + 0.016*SL
D to Y	tPLH	0.49	0.45 + 0.019*SL	0.46 + 0.018*SL	0.46 + 0.018*SL
	tPHL	0.44	0.41 + 0.017*SL	0.43 + 0.011*SL	0.46 + 0.009*SL
	tR	0.17	0.09 + 0.040*SL	0.08 + 0.041*SL	0.05 + 0.043*SL
	tF	0.16	0.12 + 0.019*SL	0.13 + 0.016*SL	0.14 + 0.015*SL
E to Y	tPLH	0.39	0.35 + 0.019*SL	0.36 + 0.018*SL	0.36 + 0.018*SL
	tPHL	0.47	0.44 + 0.018*SL	0.46 + 0.011*SL	0.51 + 0.009*SL
	tR	0.16	0.08 + 0.039*SL	0.07 + 0.042*SL	0.05 + 0.043*SL
	tF	0.16	0.12 + 0.023*SL	0.14 + 0.015*SL	0.14 + 0.015*SL
F to Y	tPLH	0.44	0.40 + 0.020*SL	0.41 + 0.019*SL	0.41 + 0.018*SL
	tPHL	0.48	0.45 + 0.017*SL	0.46 + 0.011*SL	0.51 + 0.009*SL
	tR	0.16	0.07 + 0.045*SL	0.08 + 0.041*SL	0.05 + 0.043*SL
	tF	0.16	0.13 + 0.019*SL	0.14 + 0.015*SL	0.14 + 0.016*SL
G to Y	tPLH	0.48	0.45 + 0.019*SL	0.45 + 0.018*SL	0.45 + 0.018*SL
	tPHL	0.46	0.43 + 0.016*SL	0.44 + 0.011*SL	0.49 + 0.009*SL
	tR	0.17	0.09 + 0.039*SL	0.08 + 0.042*SL	0.06 + 0.043*SL
	tF	0.16	0.13 + 0.016*SL	0.13 + 0.016*SL	0.14 + 0.015*SL
H to Y	tPLH	0.51	0.47 + 0.019*SL	0.48 + 0.018*SL	0.48 + 0.018*SL
	tPHL	0.43	0.40 + 0.017*SL	0.42 + 0.011*SL	0.47 + 0.009*SL
	tR	0.16	0.09 + 0.033*SL	0.07 + 0.042*SL	0.06 + 0.043*SL
	tF	0.16	0.12 + 0.019*SL	0.13 + 0.016*SL	0.14 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

ND8D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.41	0.39 + 0.011*SL	0.39 + 0.010*SL	0.40 + 0.009*SL
	t_{PHL}	0.57	0.54 + 0.015*SL	0.56 + 0.008*SL	0.61 + 0.006*SL
	t_R	0.13	0.08 + 0.027*SL	0.10 + 0.021*SL	0.07 + 0.022*SL
	t_F	0.23	0.22 + 0.003*SL	0.21 + 0.008*SL	0.21 + 0.008*SL
B to Y	t_{PLH}	0.47	0.44 + 0.011*SL	0.45 + 0.010*SL	0.45 + 0.009*SL
	t_{PHL}	0.58	0.55 + 0.016*SL	0.57 + 0.008*SL	0.62 + 0.006*SL
	t_R	0.14	0.09 + 0.022*SL	0.09 + 0.021*SL	0.07 + 0.023*SL
	t_F	0.23	0.22 + 0.004*SL	0.21 + 0.008*SL	0.21 + 0.008*SL
C to Y	t_{PLH}	0.50	0.48 + 0.011*SL	0.48 + 0.010*SL	0.49 + 0.010*SL
	t_{PHL}	0.56	0.53 + 0.014*SL	0.55 + 0.008*SL	0.60 + 0.006*SL
	t_R	0.14	0.11 + 0.018*SL	0.09 + 0.021*SL	0.07 + 0.022*SL
	t_F	0.23	0.22 + 0.006*SL	0.21 + 0.008*SL	0.22 + 0.008*SL
D to Y	t_{PLH}	0.53	0.51 + 0.011*SL	0.51 + 0.010*SL	0.53 + 0.009*SL
	t_{PHL}	0.54	0.52 + 0.011*SL	0.52 + 0.008*SL	0.58 + 0.006*SL
	t_R	0.14	0.09 + 0.024*SL	0.10 + 0.022*SL	0.09 + 0.022*SL
	t_F	0.23	0.22 + 0.007*SL	0.22 + 0.008*SL	0.21 + 0.008*SL
E to Y	t_{PLH}	0.42	0.40 + 0.011*SL	0.40 + 0.010*SL	0.41 + 0.009*SL
	t_{PHL}	0.57	0.54 + 0.014*SL	0.56 + 0.008*SL	0.61 + 0.006*SL
	t_R	0.14	0.10 + 0.019*SL	0.10 + 0.021*SL	0.08 + 0.022*SL
	t_F	0.23	0.22 + 0.006*SL	0.21 + 0.008*SL	0.22 + 0.008*SL
F to Y	t_{PLH}	0.47	0.45 + 0.011*SL	0.46 + 0.010*SL	0.47 + 0.009*SL
	t_{PHL}	0.57	0.55 + 0.013*SL	0.56 + 0.008*SL	0.61 + 0.006*SL
	t_R	0.14	0.10 + 0.019*SL	0.09 + 0.022*SL	0.08 + 0.022*SL
	t_F	0.23	0.21 + 0.006*SL	0.21 + 0.008*SL	0.21 + 0.008*SL
G to Y	t_{PLH}	0.51	0.49 + 0.010*SL	0.50 + 0.010*SL	0.50 + 0.009*SL
	t_{PHL}	0.55	0.53 + 0.013*SL	0.54 + 0.008*SL	0.59 + 0.006*SL
	t_R	0.14	0.10 + 0.021*SL	0.10 + 0.022*SL	0.08 + 0.022*SL
	t_F	0.23	0.22 + 0.006*SL	0.21 + 0.008*SL	0.22 + 0.008*SL
H to Y	t_{PLH}	0.55	0.52 + 0.012*SL	0.53 + 0.010*SL	0.54 + 0.009*SL
	t_{PHL}	0.53	0.51 + 0.013*SL	0.52 + 0.008*SL	0.57 + 0.006*SL
	t_R	0.14	0.09 + 0.024*SL	0.10 + 0.022*SL	0.09 + 0.022*SL
	t_F	0.23	0.21 + 0.008*SL	0.21 + 0.008*SL	0.21 + 0.008*SL

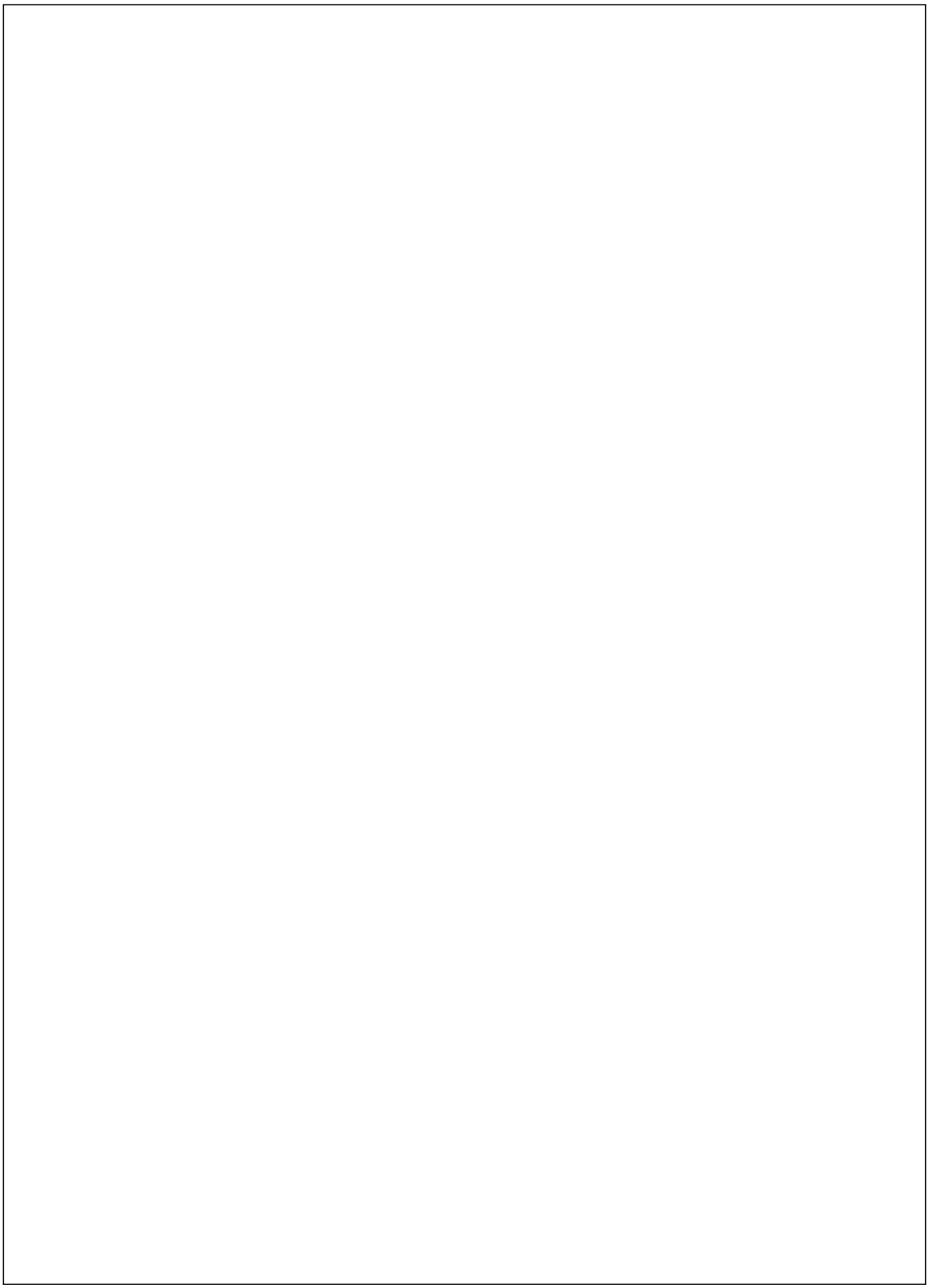
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

ND8D8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

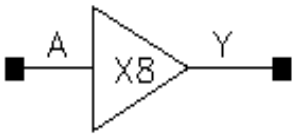
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.46	0.45 + 0.006*SL	0.45 + 0.005*SL	0.46 + 0.005*SL
	t_{PHL}	0.66	0.65 + 0.006*SL	0.66 + 0.005*SL	0.68 + 0.003*SL
	t_R	0.11	0.09 + 0.014*SL	0.10 + 0.011*SL	0.09 + 0.011*SL
	t_F	0.22	0.20 + 0.009*SL	0.22 + 0.004*SL	0.22 + 0.004*SL
B to Y	t_{PLH}	0.50	0.49 + 0.007*SL	0.49 + 0.005*SL	0.50 + 0.005*SL
	t_{PHL}	0.66	0.65 + 0.004*SL	0.65 + 0.005*SL	0.68 + 0.003*SL
	t_R	0.12	0.08 + 0.019*SL	0.11 + 0.010*SL	0.09 + 0.011*SL
	t_F	0.22	0.20 + 0.010*SL	0.22 + 0.005*SL	0.23 + 0.004*SL
C to Y	t_{PLH}	0.54	0.52 + 0.006*SL	0.53 + 0.005*SL	0.54 + 0.005*SL
	t_{PHL}	0.63	0.62 + 0.006*SL	0.63 + 0.005*SL	0.65 + 0.004*SL
	t_R	0.12	0.10 + 0.009*SL	0.10 + 0.011*SL	0.10 + 0.011*SL
	t_F	0.23	0.23 + -0.000*SL	0.22 + 0.005*SL	0.23 + 0.004*SL
D to Y	t_{PLH}	0.57	0.55 + 0.006*SL	0.56 + 0.005*SL	0.57 + 0.005*SL
	t_{PHL}	0.61	0.60 + 0.005*SL	0.60 + 0.005*SL	0.63 + 0.004*SL
	t_R	0.12	0.10 + 0.009*SL	0.10 + 0.011*SL	0.11 + 0.011*SL
	t_F	0.23	0.23 + 0.004*SL	0.23 + 0.004*SL	0.23 + 0.004*SL
E to Y	t_{PLH}	0.47	0.46 + 0.006*SL	0.46 + 0.005*SL	0.46 + 0.005*SL
	t_{PHL}	0.65	0.63 + 0.007*SL	0.64 + 0.005*SL	0.67 + 0.004*SL
	t_R	0.12	0.09 + 0.013*SL	0.10 + 0.011*SL	0.09 + 0.011*SL
	t_F	0.23	0.22 + 0.001*SL	0.21 + 0.005*SL	0.24 + 0.004*SL
F to Y	t_{PLH}	0.51	0.50 + 0.006*SL	0.50 + 0.005*SL	0.51 + 0.005*SL
	t_{PHL}	0.65	0.64 + 0.007*SL	0.64 + 0.005*SL	0.67 + 0.004*SL
	t_R	0.12	0.09 + 0.014*SL	0.11 + 0.010*SL	0.09 + 0.011*SL
	t_F	0.22	0.21 + 0.004*SL	0.21 + 0.005*SL	0.24 + 0.004*SL
G to Y	t_{PLH}	0.55	0.53 + 0.006*SL	0.54 + 0.005*SL	0.55 + 0.005*SL
	t_{PHL}	0.62	0.61 + 0.004*SL	0.61 + 0.005*SL	0.64 + 0.004*SL
	t_R	0.12	0.10 + 0.010*SL	0.10 + 0.011*SL	0.10 + 0.011*SL
	t_F	0.23	0.21 + 0.010*SL	0.23 + 0.004*SL	0.22 + 0.004*SL
H to Y	t_{PLH}	0.58	0.56 + 0.006*SL	0.57 + 0.005*SL	0.58 + 0.005*SL
	t_{PHL}	0.60	0.59 + 0.006*SL	0.59 + 0.005*SL	0.61 + 0.004*SL
	t_R	0.12	0.09 + 0.015*SL	0.10 + 0.011*SL	0.11 + 0.011*SL
	t_F	0.23	0.21 + 0.008*SL	0.23 + 0.003*SL	0.21 + 0.005*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL



Input: A
Output: Y
Input Loading (SL): All : 2
Maximum Fanout (Rec. SL):
- NID8: 224
- NID12: 336
- NID16: 456

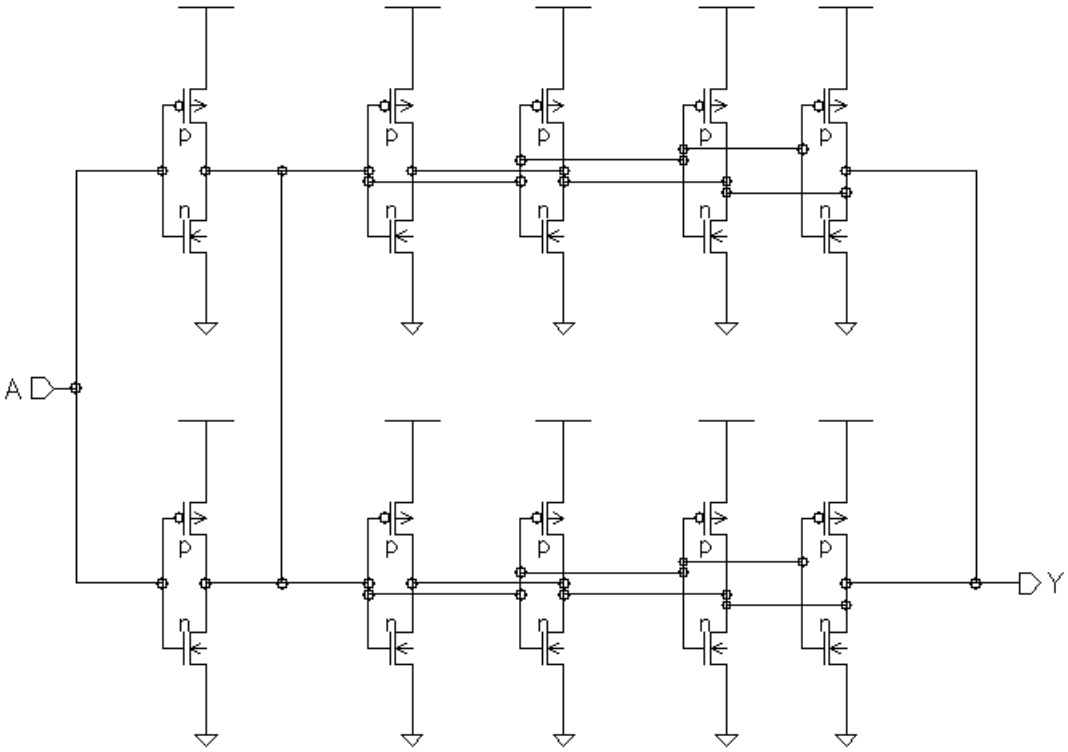
Gate Count:
- NID8: 5
- NID12: 7
- NID16: 9



Symbol

A	Y
0	0
1	1

Truth Table



Schematic

NID8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.18	0.17 + 0.006*SL	0.17 + 0.005*SL	0.18 + 0.005*SL
	tPHL	0.37	0.37 + 0.003*SL	0.36 + 0.004*SL	0.38 + 0.003*SL
	t_R	0.13	0.11 + 0.011*SL	0.12 + 0.009*SL	0.11 + 0.010*SL
	t_F	0.15	0.14 + 0.002*SL	0.14 + 0.004*SL	0.14 + 0.004*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NID12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.24	0.23 + 0.004*SL	0.23 + 0.004*SL	0.24 + 0.003*SL
	tPHL	0.44	0.44 + 0.003*SL	0.43 + 0.003*SL	0.45 + 0.002*SL
	t_R	0.13	0.13 + 0.003*SL	0.11 + 0.008*SL	0.13 + 0.007*SL
	t_F	0.18	0.17 + 0.004*SL	0.18 + 0.003*SL	0.18 + 0.003*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NID16 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

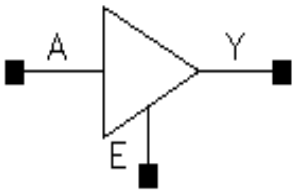
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.29	0.28 + 0.003*SL	0.28 + 0.003*SL	0.30 + 0.002*SL
	tPHL	0.50	0.49 + 0.003*SL	0.49 + 0.003*SL	0.51 + 0.002*SL
	t_R	0.16	0.15 + 0.002*SL	0.15 + 0.005*SL	0.14 + 0.005*SL
	t_F	0.22	0.22 + 0.001*SL	0.22 + 0.002*SL	0.22 + 0.002*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: A, E
Output: Y
Input Loading (SL):
- NIT: A : 1, E : 1.5
- NITD2: A : 1, E : 2
- NITD5: A: 2, E : 2
- NITD9:A: 2, E: 2

Maximum Fanout (Rec. SL):
- NIT: 28
- NITD2: 56
- NITD5: 112
- NITD9: 252

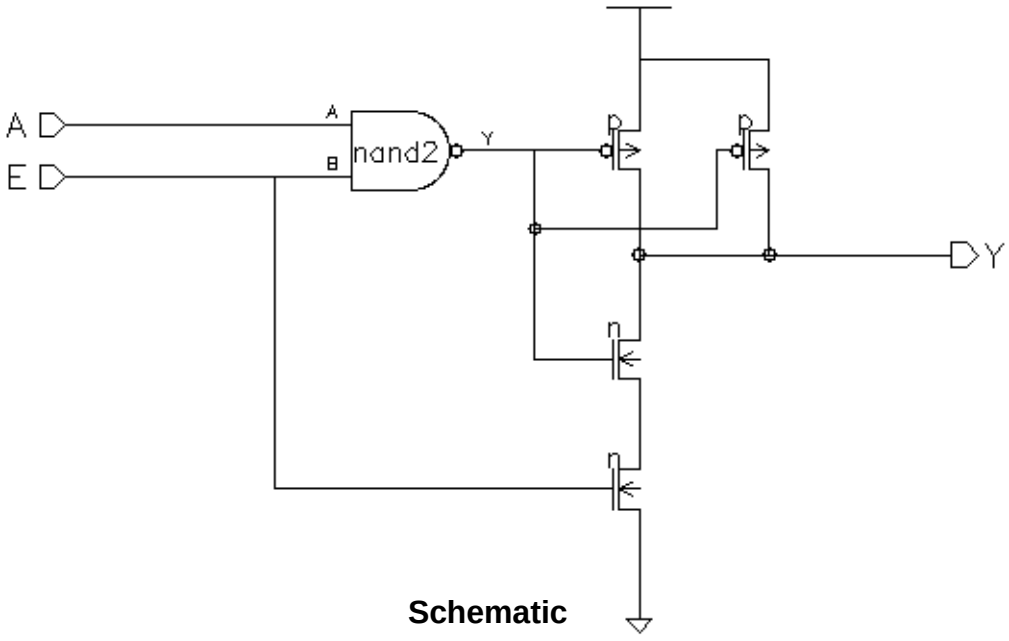
Gate Count:
- NIT: 2
- NITD2: 3
- NITD5: 5
- NITD9: 7



Symbol

A	E	Y
x	0	hi-z
1	1	1
0	1	0

Truth Table



Schematic

NIT Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.18	0.13 + 0.022*SL	0.14 + 0.019*SL	0.15 + 0.018*SL
	tPHL	0.37	0.31 + 0.033*SL	0.33 + 0.026*SL	0.33 + 0.026*SL
	tR	0.19	0.12 + 0.036*SL	0.11 + 0.040*SL	0.07 + 0.042*SL
	tF	0.22	0.11 + 0.058*SL	0.12 + 0.055*SL	0.07 + 0.057*SL
E to Y	tPLH	0.14	0.09 + 0.026*SL	0.11 + 0.019*SL	0.13 + 0.018*SL
	tPHL	0.02	-0.08 + 0.049*SL	-0.02 + 0.029*SL	0.05 + 0.026*SL
	tR	0.20	0.12 + 0.038*SL	0.11 + 0.040*SL	0.07 + 0.042*SL
	tF	0.32	0.22 + 0.054*SL	0.22 + 0.052*SL	0.16 + 0.055*SL
	tPLZ	0.40	0.40 + -0.000*SL	0.40 + -0.000*SL	0.40 + -0.000*SL
	tPHZ	0.43	0.44 + -0.000*SL	0.43 + -0.000*SL	0.43 + -0.000*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NITD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.22	0.19 + 0.013*SL	0.20 + 0.010*SL	0.22 + 0.009*SL
	tPHL	0.41	0.38 + 0.018*SL	0.39 + 0.014*SL	0.41 + 0.013*SL
	tR	0.16	0.12 + 0.022*SL	0.13 + 0.019*SL	0.10 + 0.020*SL
	tF	0.20	0.13 + 0.032*SL	0.15 + 0.028*SL	0.11 + 0.030*SL
E to Y	tPLH	0.17	0.14 + 0.014*SL	0.15 + 0.011*SL	0.18 + 0.009*SL
	tPHL	-0.04	-0.10 + 0.032*SL	-0.06 + 0.018*SL	0.03 + 0.014*SL
	tR	0.17	0.13 + 0.018*SL	0.13 + 0.019*SL	0.10 + 0.020*SL
	tF	0.26	0.18 + 0.041*SL	0.22 + 0.027*SL	0.20 + 0.028*SL
	tPLZ	0.40	0.40 + -0.000*SL	0.40 + -0.000*SL	0.40 + -0.000*SL
	tPHZ	0.52	0.52 + -0.000*SL	0.52 + -0.000*SL	0.52 + -0.000*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NITD5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.17	0.15 + 0.012*SL	0.16 + 0.009*SL	0.19 + 0.008*SL
	t_{PHL}	0.40	0.38 + 0.010*SL	0.39 + 0.007*SL	0.43 + 0.005*SL
	t_R	0.15	0.12 + 0.017*SL	0.11 + 0.018*SL	0.12 + 0.017*SL
	t_F	0.13	0.11 + 0.010*SL	0.12 + 0.008*SL	0.15 + 0.007*SL
E to Y	t_{PLH}	0.13	0.10 + 0.014*SL	0.11 + 0.010*SL	0.14 + 0.008*SL
	t_{PHL}	0.21	0.18 + 0.012*SL	0.20 + 0.007*SL	0.24 + 0.005*SL
	t_R	0.16	0.12 + 0.020*SL	0.13 + 0.017*SL	0.11 + 0.017*SL
	t_F	0.12	0.09 + 0.016*SL	0.11 + 0.008*SL	0.12 + 0.007*SL
	t_{PLZ}	0.41	0.41 + 0.000*SL	0.41 + -0.000*SL	0.41 + -0.000*SL
	t_{PHZ}	0.55	0.55 + 0.000*SL	0.55 + -0.000*SL	0.55 + -0.000*SL

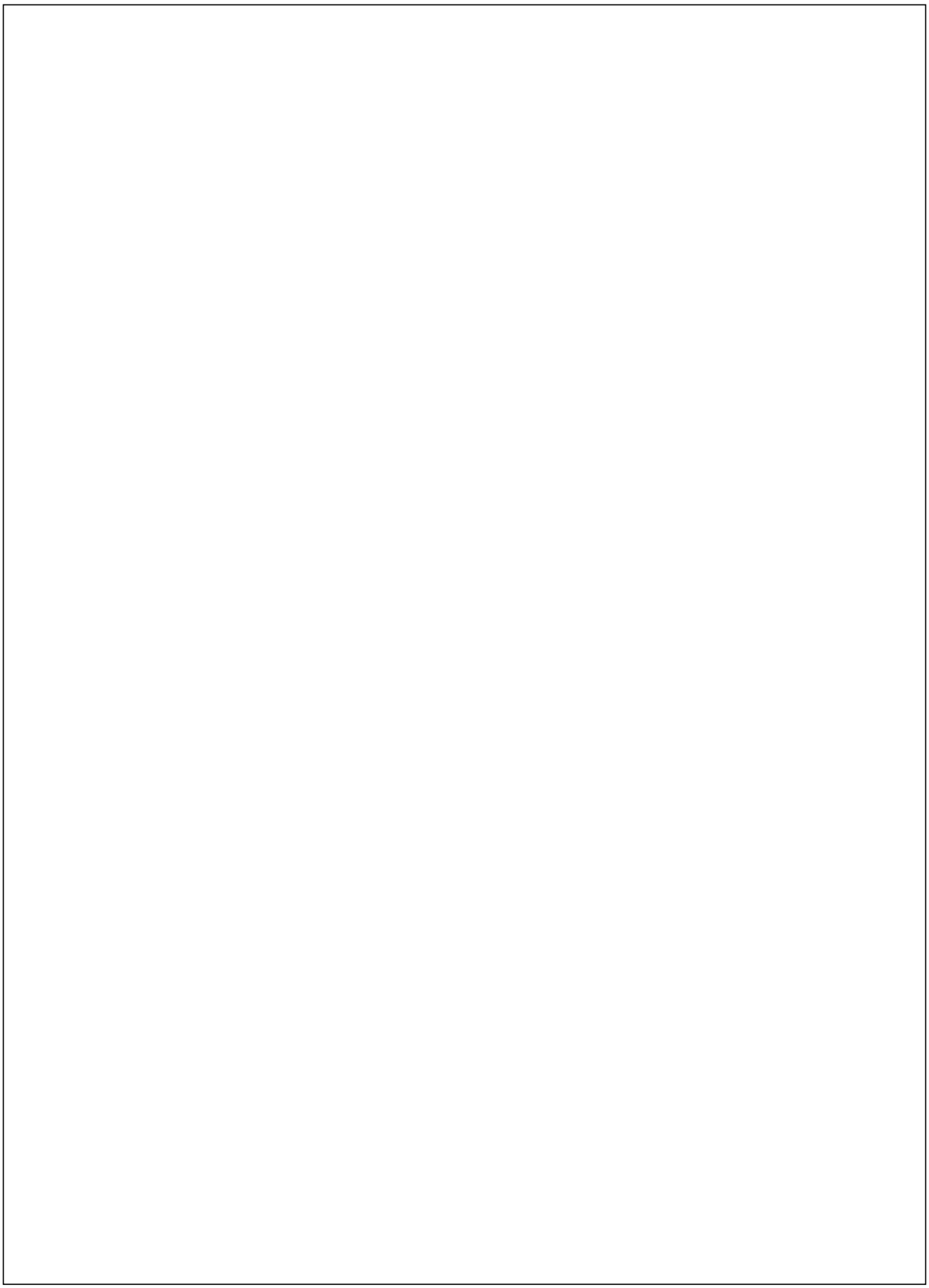
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NITD9 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.24	0.22 + 0.010*SL	0.24 + 0.005*SL	0.25 + 0.005*SL
	t_{PHL}	0.47	0.45 + 0.007*SL	0.46 + 0.005*SL	0.49 + 0.003*SL
	t_R	0.14	0.12 + 0.011*SL	0.12 + 0.011*SL	0.14 + 0.010*SL
	t_F	0.17	0.16 + 0.005*SL	0.16 + 0.005*SL	0.19 + 0.004*SL
E to Y	t_{PLH}	0.16	0.14 + 0.010*SL	0.15 + 0.007*SL	0.18 + 0.005*SL
	t_{PHL}	0.25	0.24 + 0.009*SL	0.25 + 0.005*SL	0.28 + 0.004*SL
	t_R	0.16	0.14 + 0.012*SL	0.14 + 0.009*SL	0.14 + 0.010*SL
	t_F	0.14	0.11 + 0.013*SL	0.13 + 0.006*SL	0.17 + 0.004*SL
	t_{PLZ}	0.47	0.47 + 0.000*SL	0.47 + 0.000*SL	0.48 + -0.000*SL
	t_{PHZ}	0.69	0.69 + -0.000*SL	0.69 + 0.000*SL	0.69 + -0.000*SL

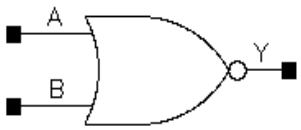
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B
Output: Y
Input Loading (SL):
- NR2: All : 1
- NR2D2: All : 2
- NR2D3: All: 1
- NR2D7: All: 1

Maximum Fanout (Rec. SL):
- NR2: 14
- NR2D2: 28
- NR2D3: 84
- NR2D7: 196

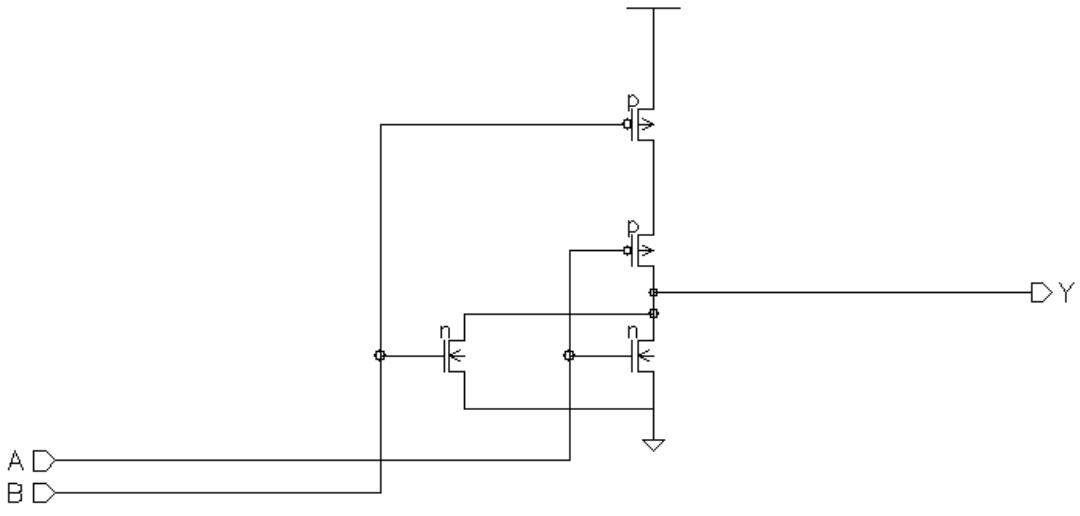
Gate Count:
- NR2: 1
- NR2D2: 2
- NR2D3: 3
- NR2D7: 5



Symbol

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table



Schematic

NR2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.43	0.28 + 0.073*SL	0.30 + 0.068*SL	0.27 + 0.070*SL
	t_{PHL}	0.03	-0.06 + 0.044*SL	0.01 + 0.023*SL	0.13 + 0.017*SL
	t_R	0.56	0.26 + 0.153*SL	0.23 + 0.161*SL	0.16 + 0.165*SL
	t_F	0.30	0.21 + 0.045*SL	0.25 + 0.030*SL	0.21 + 0.032*SL
B to Y	t_{PLH}	0.40	0.26 + 0.068*SL	0.26 + 0.068*SL	0.23 + 0.070*SL
	t_{PHL}	0.06	-0.02 + 0.041*SL	0.03 + 0.022*SL	0.14 + 0.017*SL
	t_R	0.57	0.27 + 0.152*SL	0.24 + 0.161*SL	0.16 + 0.165*SL
	t_F	0.34	0.27 + 0.033*SL	0.29 + 0.029*SL	0.24 + 0.031*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

NR2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.37	0.28 + 0.041*SL	0.30 + 0.036*SL	0.29 + 0.036*SL
	t_{PHL}	-0.01	-0.07 + 0.025*SL	-0.04 + 0.015*SL	0.08 + 0.010*SL
	t_R	0.43	0.26 + 0.085*SL	0.27 + 0.083*SL	0.20 + 0.086*SL
	t_F	0.25	0.21 + 0.024*SL	0.23 + 0.016*SL	0.26 + 0.014*SL
B to Y	t_{PLH}	0.34	0.26 + 0.036*SL	0.27 + 0.035*SL	0.25 + 0.036*SL
	t_{PHL}	0.01	-0.05 + 0.028*SL	-0.00 + 0.014*SL	0.09 + 0.010*SL
	t_R	0.44	0.28 + 0.078*SL	0.27 + 0.083*SL	0.20 + 0.086*SL
	t_F	0.30	0.27 + 0.017*SL	0.28 + 0.015*SL	0.29 + 0.014*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

NR2D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.51	0.48 + 0.015*SL	0.48 + 0.013*SL	0.49 + 0.013*SL
	tPHL	0.18	0.16 + 0.011*SL	0.17 + 0.007*SL	0.19 + 0.006*SL
	tR	0.15	0.09 + 0.026*SL	0.09 + 0.029*SL	0.06 + 0.030*SL
	tF	0.11	0.09 + 0.013*SL	0.09 + 0.011*SL	0.10 + 0.011*SL
B to Y	tPLH	0.48	0.46 + 0.014*SL	0.46 + 0.013*SL	0.46 + 0.013*SL
	tPHL	0.22	0.20 + 0.008*SL	0.20 + 0.007*SL	0.23 + 0.006*SL
	tR	0.15	0.10 + 0.025*SL	0.09 + 0.029*SL	0.06 + 0.030*SL
	tF	0.12	0.10 + 0.012*SL	0.10 + 0.011*SL	0.10 + 0.011*SL

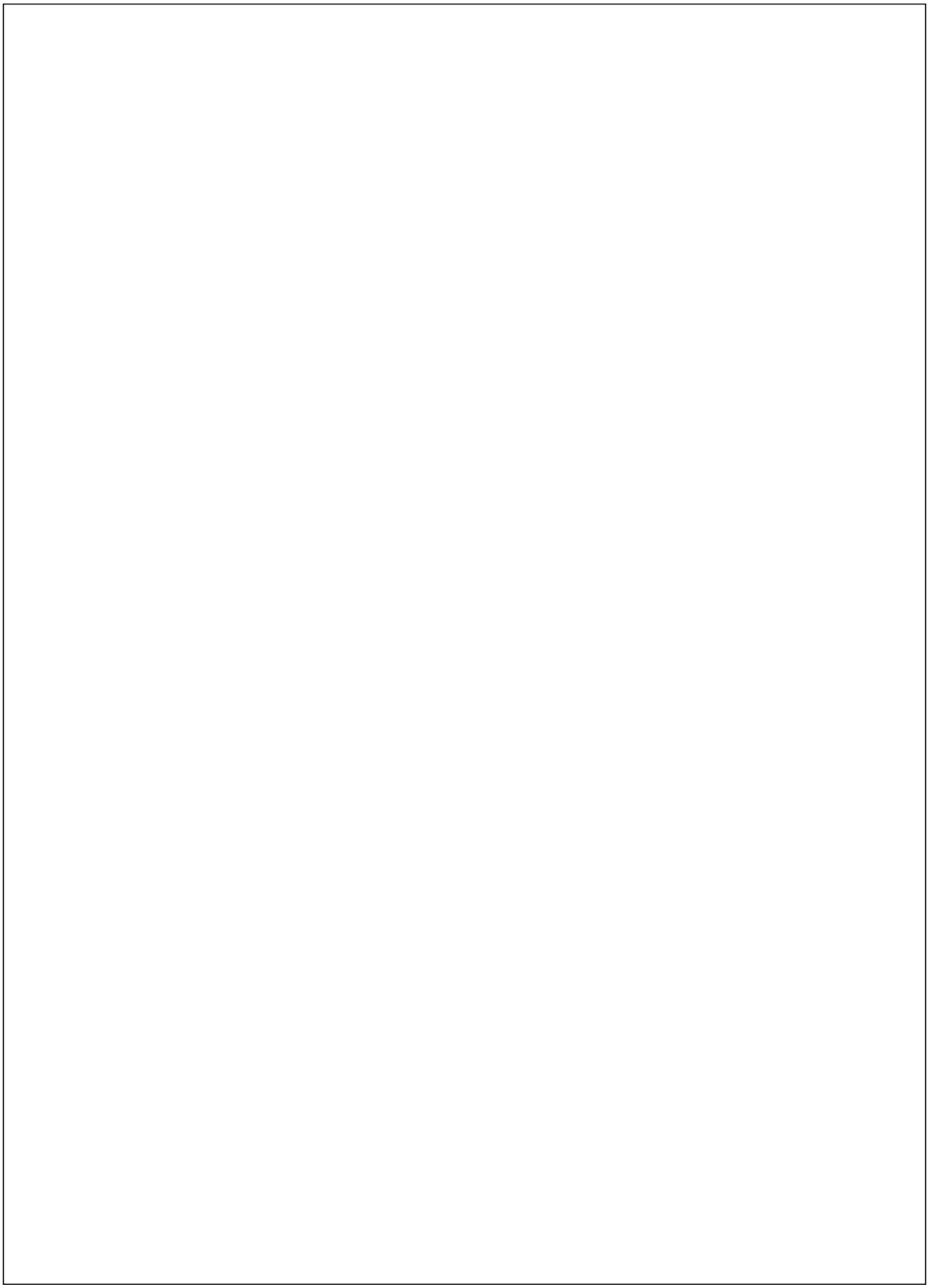
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR2D7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.59	0.57 + 0.007*SL	0.58 + 0.006*SL	0.59 + 0.005*SL
	tPHL	0.28	0.27 + 0.007*SL	0.27 + 0.005*SL	0.30 + 0.003*SL
	tR	0.13	0.10 + 0.016*SL	0.12 + 0.012*SL	0.10 + 0.013*SL
	tF	0.18	0.17 + 0.003*SL	0.17 + 0.005*SL	0.17 + 0.005*SL
B to Y	tPLH	0.56	0.55 + 0.006*SL	0.55 + 0.006*SL	0.56 + 0.006*SL
	tPHL	0.32	0.31 + 0.006*SL	0.31 + 0.005*SL	0.34 + 0.004*SL
	tR	0.14	0.11 + 0.013*SL	0.12 + 0.012*SL	0.10 + 0.012*SL
	tF	0.18	0.17 + 0.004*SL	0.16 + 0.006*SL	0.19 + 0.004*SL

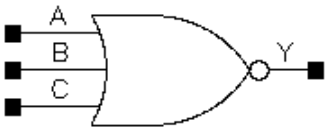
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C
Output: Y
Input Loading (SL):
- NR3: All : 1
- NR3D2: All : 2
- NR3D3: All: 1
- NR3D7: All: 1

Maximum Fanout (Rec. SL):
- NR3: 9
- NR3D2: 19
- NR3D3: 84
- NR3D7: 196

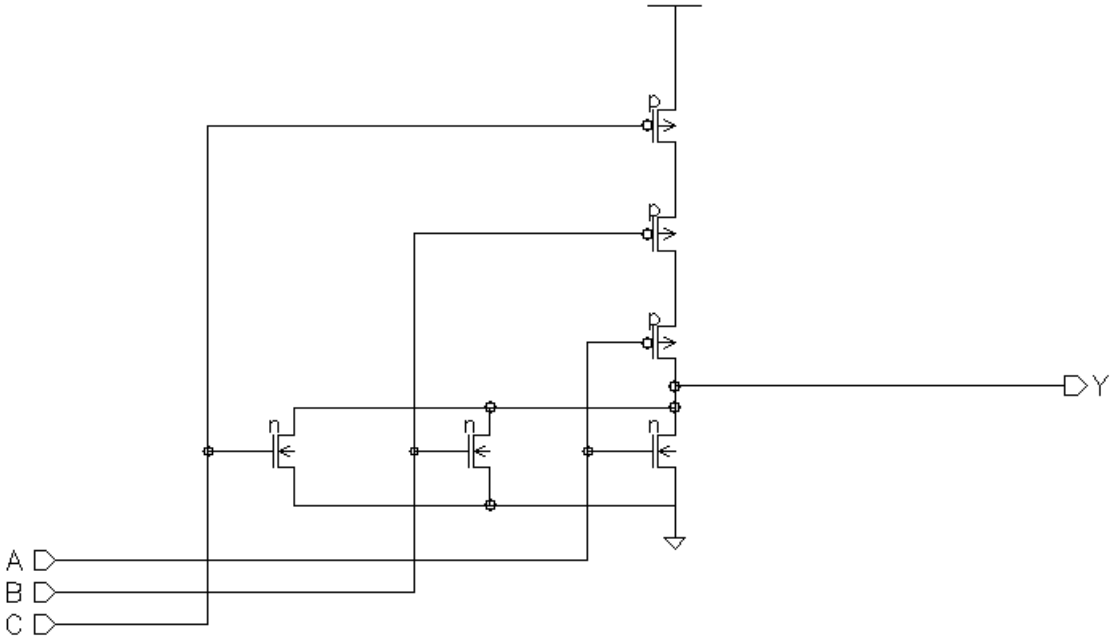
Gate Count:
- NR3: 3
- NR3D2: 4
- NR3D3: 4
- NR3D7: 6



Symbol

A	B	C	Y
0	0	0	1
1	x	x	0
x	1	x	0
x	x	1	0

Truth Table



Schematic

NR3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.56	0.35 + 0.103*SL	0.35 + 0.105*SL	0.30 + 0.107*SL
	t_{PHL}	0.04	-0.05 + 0.042*SL	0.01 + 0.023*SL	0.13 + 0.017*SL
	t_R	0.88	0.40 + 0.241*SL	0.37 + 0.250*SL	0.32 + 0.252*SL
	t_F	0.30	0.21 + 0.043*SL	0.25 + 0.030*SL	0.22 + 0.032*SL
B to Y	t_{PLH}	0.56	0.35 + 0.103*SL	0.35 + 0.106*SL	0.31 + 0.107*SL
	t_{PHL}	0.06	-0.02 + 0.040*SL	0.03 + 0.022*SL	0.15 + 0.017*SL
	t_R	0.89	0.42 + 0.236*SL	0.38 + 0.249*SL	0.33 + 0.252*SL
	t_F	0.33	0.25 + 0.041*SL	0.28 + 0.030*SL	0.25 + 0.031*SL
C to Y	t_{PLH}	0.54	0.34 + 0.103*SL	0.33 + 0.106*SL	0.30 + 0.107*SL
	t_{PHL}	0.06	-0.02 + 0.040*SL	0.04 + 0.022*SL	0.15 + 0.017*SL
	t_R	0.88	0.40 + 0.241*SL	0.37 + 0.249*SL	0.33 + 0.252*SL
	t_F	0.36	0.29 + 0.035*SL	0.31 + 0.029*SL	0.27 + 0.031*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR3D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.46	0.35 + 0.056*SL	0.36 + 0.053*SL	0.33 + 0.054*SL
	t_{PHL}	-0.01	-0.06 + 0.025*SL	-0.03 + 0.015*SL	0.08 + 0.010*SL
	t_R	0.66	0.42 + 0.120*SL	0.39 + 0.129*SL	0.34 + 0.131*SL
	t_F	0.25	0.21 + 0.024*SL	0.23 + 0.016*SL	0.27 + 0.014*SL
B to Y	t_{PLH}	0.46	0.35 + 0.055*SL	0.35 + 0.053*SL	0.33 + 0.055*SL
	t_{PHL}	0.01	-0.04 + 0.025*SL	-0.00 + 0.015*SL	0.10 + 0.010*SL
	t_R	0.67	0.42 + 0.124*SL	0.40 + 0.128*SL	0.35 + 0.131*SL
	t_F	0.29	0.26 + 0.019*SL	0.27 + 0.016*SL	0.29 + 0.014*SL
C to Y	t_{PLH}	0.45	0.34 + 0.053*SL	0.34 + 0.053*SL	0.31 + 0.055*SL
	t_{PHL}	0.02	-0.03 + 0.026*SL	-0.00 + 0.015*SL	0.10 + 0.010*SL
	t_R	0.66	0.43 + 0.118*SL	0.39 + 0.129*SL	0.35 + 0.131*SL
	t_F	0.32	0.28 + 0.021*SL	0.30 + 0.015*SL	0.31 + 0.014*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR3D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.46	0.42 + 0.017*SL	0.43 + 0.013*SL	0.44 + 0.013*SL
	t_{PHL}	0.19	0.17 + 0.010*SL	0.18 + 0.008*SL	0.21 + 0.006*SL
	t_R	0.16	0.10 + 0.033*SL	0.11 + 0.028*SL	0.08 + 0.030*SL
	t_F	0.12	0.10 + 0.011*SL	0.10 + 0.012*SL	0.11 + 0.011*SL
B to Y	t_{PLH}	0.56	0.53 + 0.015*SL	0.54 + 0.013*SL	0.55 + 0.013*SL
	t_{PHL}	0.21	0.18 + 0.012*SL	0.20 + 0.008*SL	0.24 + 0.006*SL
	t_R	0.17	0.10 + 0.031*SL	0.11 + 0.028*SL	0.09 + 0.030*SL
	t_F	0.13	0.10 + 0.013*SL	0.11 + 0.011*SL	0.12 + 0.011*SL
C to Y	t_{PLH}	0.54	0.50 + 0.019*SL	0.52 + 0.013*SL	0.54 + 0.012*SL
	t_{PHL}	0.24	0.22 + 0.011*SL	0.23 + 0.008*SL	0.27 + 0.006*SL
	t_R	0.16	0.10 + 0.031*SL	0.11 + 0.029*SL	0.09 + 0.029*SL
	t_F	0.13	0.10 + 0.014*SL	0.11 + 0.011*SL	0.12 + 0.011*SL

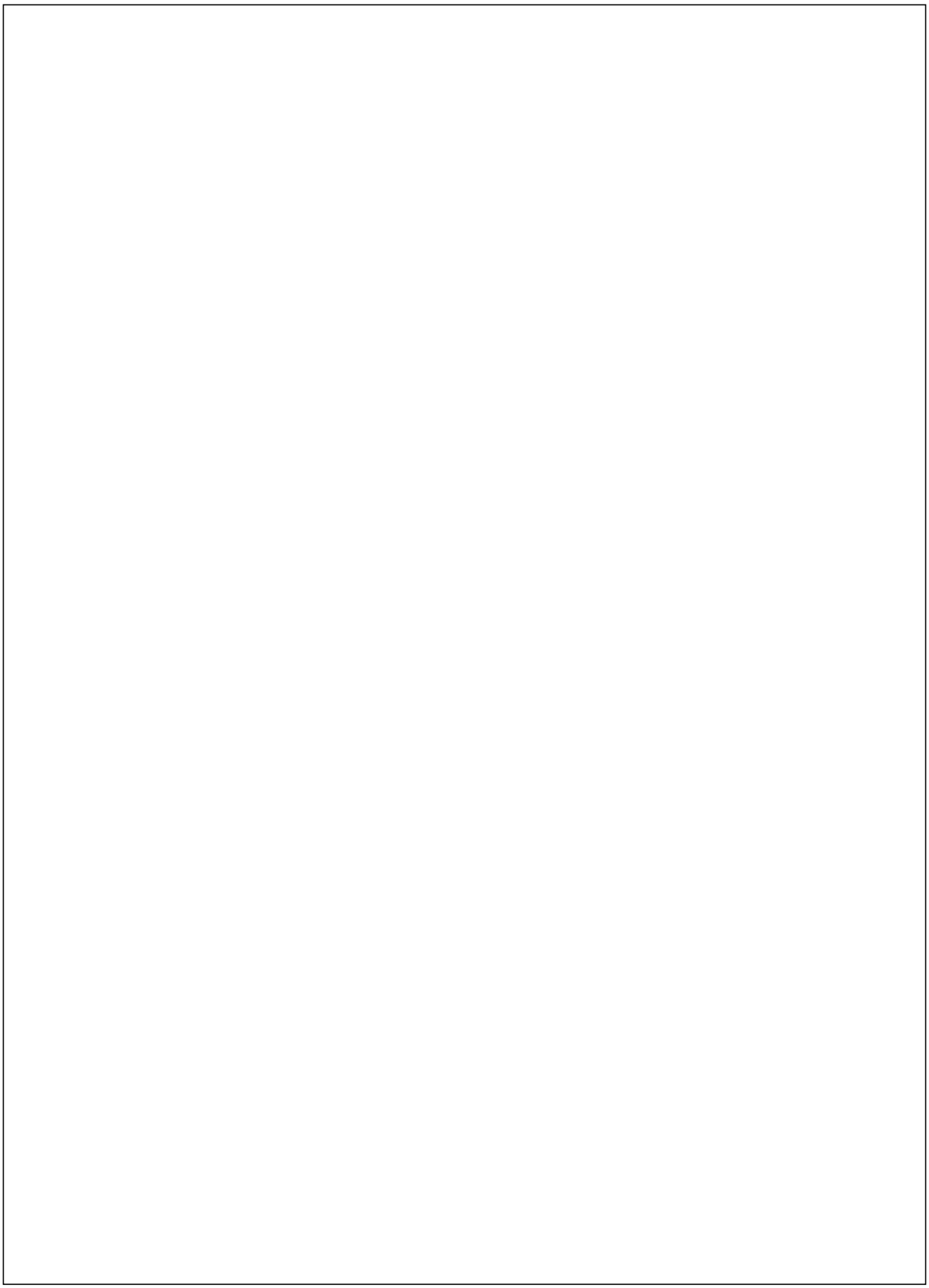
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR3D7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.56	0.54 + 0.009*SL	0.55 + 0.007*SL	0.57 + 0.006*SL
	t_{PHL}	0.30	0.28 + 0.011*SL	0.30 + 0.005*SL	0.32 + 0.004*SL
	t_R	0.18	0.15 + 0.011*SL	0.15 + 0.013*SL	0.17 + 0.012*SL
	t_F	0.18	0.17 + 0.005*SL	0.17 + 0.006*SL	0.19 + 0.005*SL
B to Y	t_{PLH}	0.68	0.66 + 0.010*SL	0.67 + 0.006*SL	0.68 + 0.006*SL
	t_{PHL}	0.31	0.29 + 0.007*SL	0.30 + 0.005*SL	0.33 + 0.004*SL
	t_R	0.19	0.16 + 0.016*SL	0.17 + 0.012*SL	0.16 + 0.012*SL
	t_F	0.19	0.18 + 0.006*SL	0.18 + 0.005*SL	0.19 + 0.005*SL
C to Y	t_{PLH}	0.65	0.64 + 0.007*SL	0.64 + 0.007*SL	0.66 + 0.006*SL
	t_{PHL}	0.35	0.33 + 0.008*SL	0.34 + 0.005*SL	0.36 + 0.004*SL
	t_R	0.19	0.17 + 0.009*SL	0.17 + 0.012*SL	0.16 + 0.012*SL
	t_F	0.20	0.19 + 0.008*SL	0.20 + 0.005*SL	0.20 + 0.005*SL

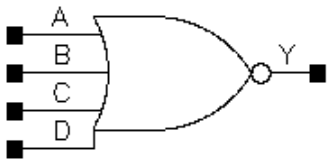
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D
Output: Y
Input Loading (SL):
- NR4: All : 1
- NR4D2: All: 1
- NR4D4:All: 1
- NR4D6: All: 1

Maximum Fanout (Rec. SL):
- NR4: 7
- NR4D2: 56
- NR4D4: 112
- NR4D6: 168

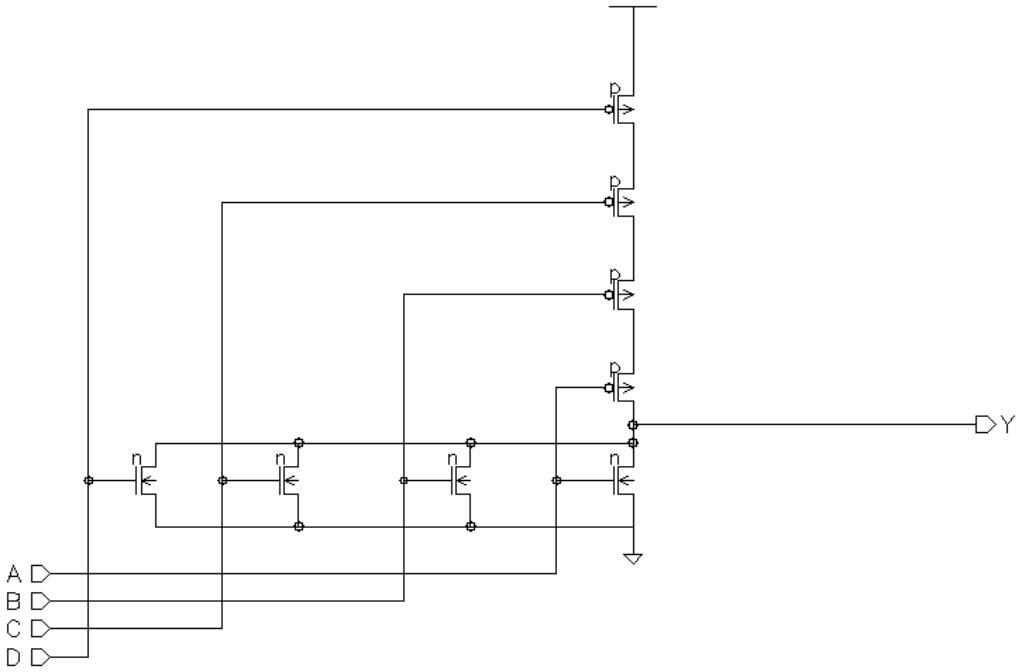
Gate Count:
- NR4: 2
- NR4D2: 4
- NR4D4: 5
- NR4D6: 6



Symbol

A	B	C	D	Y
0	0	0	0	1
1	x	x	x	0
x	1	x	x	0
x	x	1	x	0
x	x	x	1	0

Truth Table



Schematic

NR4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.67	0.41 + 0.133*SL	0.39 + 0.138*SL	0.34 + 0.140*SL
	tPHL	0.04	-0.04 + 0.041*SL	0.02 + 0.023*SL	0.14 + 0.017*SL
	tR	1.22	0.58 + 0.320*SL	0.56 + 0.328*SL	0.55 + 0.329*SL
	tF	0.31	0.22 + 0.046*SL	0.26 + 0.030*SL	0.23 + 0.032*SL
B to Y	tPLH	0.70	0.43 + 0.135*SL	0.42 + 0.139*SL	0.39 + 0.140*SL
	tPHL	0.07	-0.01 + 0.039*SL	0.04 + 0.022*SL	0.15 + 0.017*SL
	tR	1.25	0.62 + 0.316*SL	0.59 + 0.327*SL	0.55 + 0.329*SL
	tF	0.34	0.25 + 0.043*SL	0.29 + 0.030*SL	0.25 + 0.032*SL
C to Y	tPLH	0.71	0.45 + 0.134*SL	0.43 + 0.140*SL	0.41 + 0.141*SL
	tPHL	0.07	-0.00 + 0.039*SL	0.04 + 0.022*SL	0.16 + 0.017*SL
	tR	1.25	0.62 + 0.316*SL	0.58 + 0.327*SL	0.55 + 0.329*SL
	tF	0.36	0.29 + 0.038*SL	0.31 + 0.029*SL	0.27 + 0.031*SL
D to Y	tPLH	0.71	0.44 + 0.138*SL	0.43 + 0.140*SL	0.41 + 0.141*SL
	tPHL	0.07	-0.01 + 0.040*SL	0.04 + 0.023*SL	0.16 + 0.017*SL
	tR	1.24	0.60 + 0.318*SL	0.58 + 0.327*SL	0.55 + 0.329*SL
	tF	0.38	0.30 + 0.037*SL	0.33 + 0.030*SL	0.29 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.54	0.50 + 0.021*SL	0.51 + 0.019*SL	0.51 + 0.018*SL
	tPHL	0.16	0.13 + 0.014*SL	0.15 + 0.009*SL	0.17 + 0.008*SL
	tR	0.17	0.10 + 0.038*SL	0.09 + 0.042*SL	0.06 + 0.043*SL
	tF	0.11	0.07 + 0.019*SL	0.08 + 0.016*SL	0.07 + 0.017*SL
B to Y	tPLH	0.52	0.48 + 0.022*SL	0.49 + 0.019*SL	0.50 + 0.018*SL
	tPHL	0.19	0.17 + 0.013*SL	0.18 + 0.010*SL	0.20 + 0.009*SL
	tR	0.18	0.10 + 0.039*SL	0.09 + 0.041*SL	0.06 + 0.043*SL
	tF	0.11	0.08 + 0.015*SL	0.08 + 0.016*SL	0.07 + 0.017*SL
C to Y	tPLH	0.54	0.50 + 0.021*SL	0.50 + 0.019*SL	0.51 + 0.018*SL
	tPHL	0.18	0.15 + 0.015*SL	0.17 + 0.010*SL	0.20 + 0.008*SL
	tR	0.18	0.10 + 0.039*SL	0.10 + 0.041*SL	0.07 + 0.043*SL
	tF	0.12	0.08 + 0.021*SL	0.09 + 0.016*SL	0.10 + 0.016*SL
D to Y	tPLH	0.51	0.47 + 0.021*SL	0.48 + 0.019*SL	0.49 + 0.018*SL
	tPHL	0.22	0.18 + 0.017*SL	0.20 + 0.010*SL	0.24 + 0.008*SL
	tR	0.18	0.10 + 0.039*SL	0.09 + 0.042*SL	0.07 + 0.043*SL
	tF	0.12	0.08 + 0.022*SL	0.10 + 0.016*SL	0.09 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR4D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.60	0.57 + 0.014*SL	0.59 + 0.010*SL	0.59 + 0.010*SL
	tPHL	0.21	0.19 + 0.010*SL	0.20 + 0.006*SL	0.23 + 0.005*SL
	tR	0.16	0.11 + 0.024*SL	0.12 + 0.022*SL	0.12 + 0.022*SL
	tF	0.13	0.11 + 0.010*SL	0.12 + 0.008*SL	0.12 + 0.008*SL
B to Y	tPLH	0.58	0.55 + 0.015*SL	0.56 + 0.010*SL	0.58 + 0.009*SL
	tPHL	0.25	0.23 + 0.010*SL	0.24 + 0.006*SL	0.27 + 0.005*SL
	tR	0.16	0.12 + 0.023*SL	0.12 + 0.022*SL	0.11 + 0.022*SL
	tF	0.14	0.11 + 0.012*SL	0.12 + 0.009*SL	0.14 + 0.008*SL
C to Y	tPLH	0.59	0.57 + 0.010*SL	0.57 + 0.010*SL	0.58 + 0.010*SL
	tPHL	0.23	0.21 + 0.010*SL	0.22 + 0.007*SL	0.26 + 0.005*SL
	tR	0.17	0.11 + 0.030*SL	0.14 + 0.020*SL	0.10 + 0.022*SL
	tF	0.14	0.13 + 0.008*SL	0.12 + 0.009*SL	0.15 + 0.008*SL
D to Y	tPLH	0.57	0.54 + 0.015*SL	0.56 + 0.010*SL	0.57 + 0.010*SL
	tPHL	0.27	0.26 + 0.008*SL	0.26 + 0.007*SL	0.30 + 0.005*SL
	tR	0.16	0.12 + 0.023*SL	0.12 + 0.022*SL	0.12 + 0.022*SL
	tF	0.15	0.14 + 0.005*SL	0.13 + 0.009*SL	0.14 + 0.008*SL

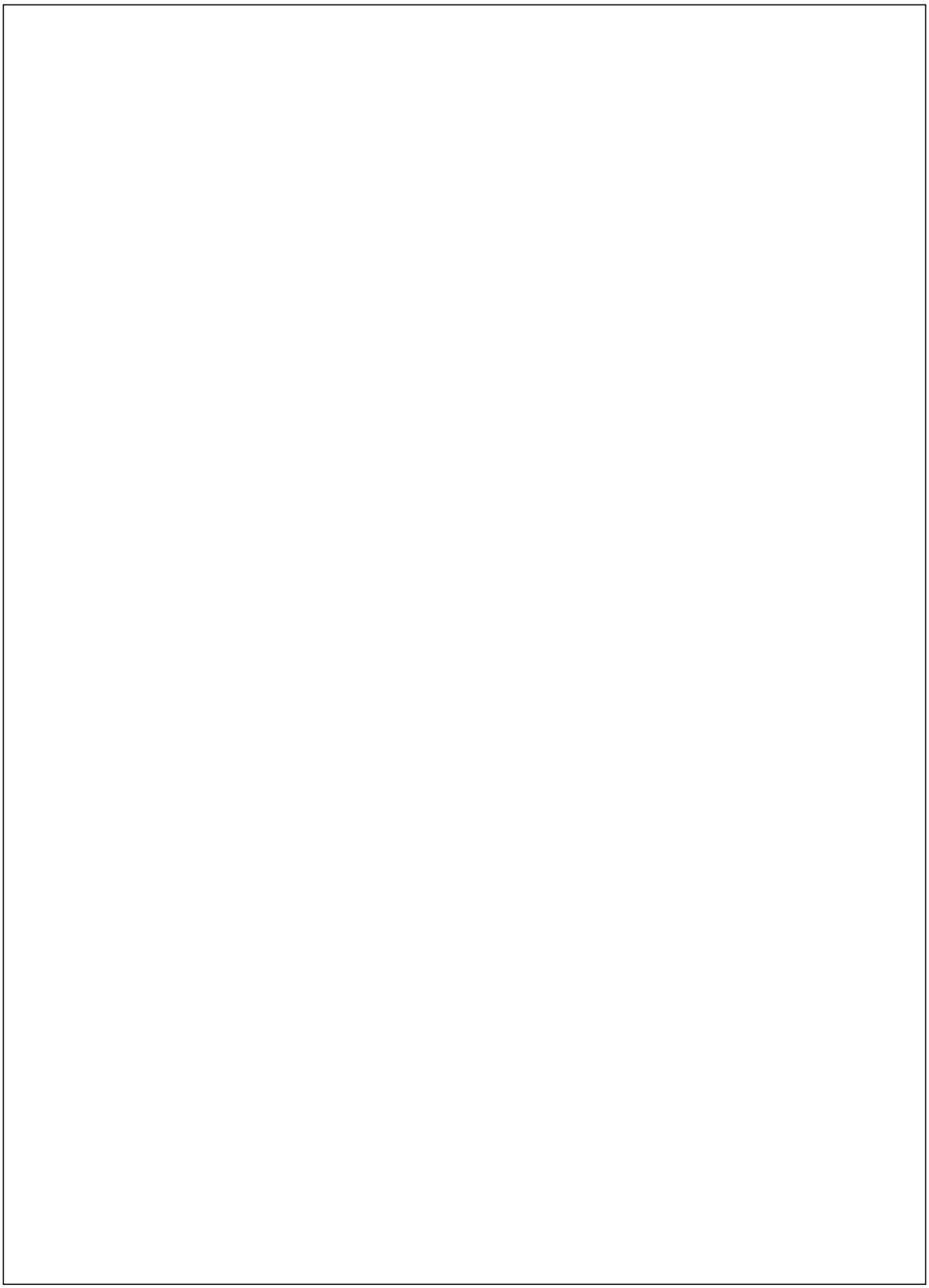
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR4D6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

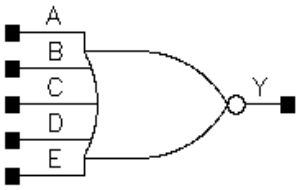
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.66	0.64 + 0.009*SL	0.65 + 0.007*SL	0.66 + 0.007*SL
	tPHL	0.27	0.25 + 0.007*SL	0.26 + 0.005*SL	0.29 + 0.004*SL
	tR	0.17	0.15 + 0.010*SL	0.13 + 0.015*SL	0.15 + 0.014*SL
	tF	0.16	0.15 + 0.005*SL	0.15 + 0.006*SL	0.17 + 0.005*SL
B to Y	tPLH	0.64	0.62 + 0.009*SL	0.62 + 0.007*SL	0.64 + 0.007*SL
	tPHL	0.30	0.29 + 0.005*SL	0.29 + 0.006*SL	0.32 + 0.004*SL
	tR	0.17	0.14 + 0.014*SL	0.14 + 0.015*SL	0.16 + 0.014*SL
	tF	0.16	0.15 + 0.005*SL	0.15 + 0.006*SL	0.17 + 0.005*SL
C to Y	tPLH	0.65	0.63 + 0.008*SL	0.63 + 0.007*SL	0.65 + 0.007*SL
	tPHL	0.28	0.27 + 0.004*SL	0.27 + 0.006*SL	0.30 + 0.004*SL
	tR	0.17	0.15 + 0.012*SL	0.14 + 0.014*SL	0.14 + 0.014*SL
	tF	0.17	0.17 + 0.002*SL	0.15 + 0.007*SL	0.19 + 0.005*SL
D to Y	tPLH	0.62	0.60 + 0.010*SL	0.61 + 0.008*SL	0.64 + 0.006*SL
	tPHL	0.32	0.31 + 0.008*SL	0.31 + 0.006*SL	0.34 + 0.004*SL
	tR	0.18	0.16 + 0.009*SL	0.15 + 0.014*SL	0.14 + 0.014*SL
	tF	0.17	0.16 + 0.006*SL	0.16 + 0.007*SL	0.21 + 0.004*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D, E
Output: Y
Input Loading (SL): All: 1
Maximum Fanout (Rec. SL):
- NR5: 2
- NR5D2: 56
- NR5D4: 112
- NR5D6: 168

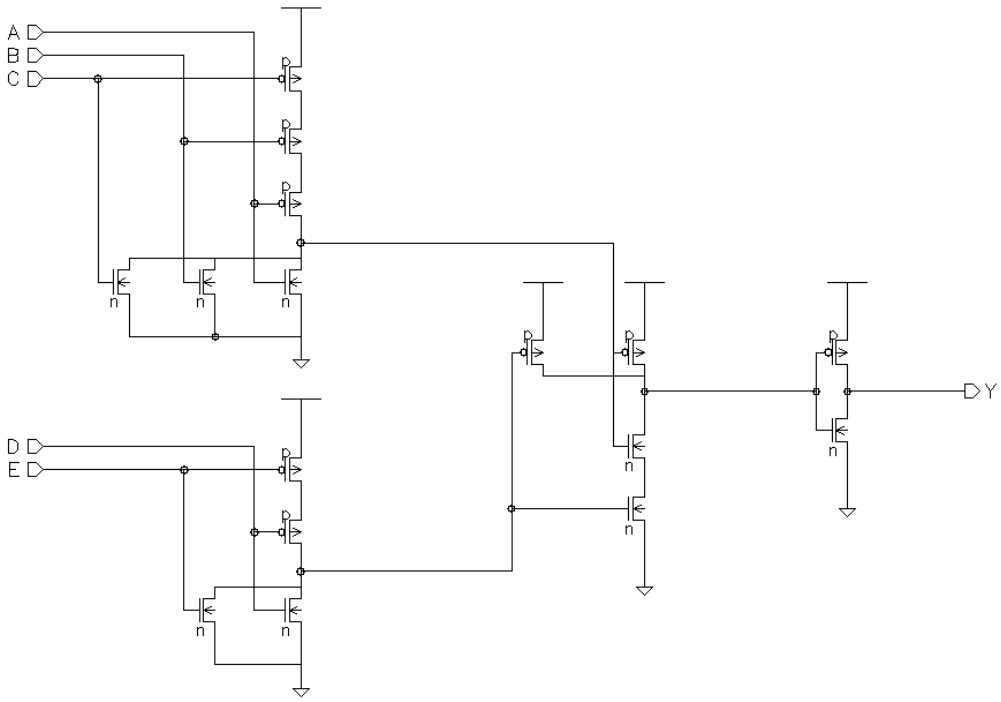
Gate Count
- NR5: 4
- NR5D2: 5
- NR5D4: 6
- NR5D6: 7



Symbol

A	B	C	D	E	Y
0	0	0	0	0	1
1	x	x	x	x	0
x	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0

Truth Table



Schematic

NR5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.65	0.57 + 0.038*SL	0.58 + 0.037*SL	0.58 + 0.036*SL
	tPHL	0.15	0.11 + 0.021*SL	0.12 + 0.017*SL	0.13 + 0.016*SL
	tR	0.25	0.09 + 0.080*SL	0.08 + 0.083*SL	0.06 + 0.085*SL
	tF	0.13	0.06 + 0.032*SL	0.06 + 0.032*SL	0.04 + 0.033*SL
B to Y	tPLH	0.66	0.58 + 0.038*SL	0.58 + 0.037*SL	0.59 + 0.036*SL
	tPHL	0.18	0.14 + 0.022*SL	0.15 + 0.017*SL	0.16 + 0.016*SL
	tR	0.26	0.10 + 0.079*SL	0.09 + 0.083*SL	0.06 + 0.085*SL
	tF	0.13	0.05 + 0.038*SL	0.07 + 0.032*SL	0.04 + 0.033*SL
C to Y	tPLH	0.63	0.55 + 0.038*SL	0.56 + 0.037*SL	0.56 + 0.036*SL
	tPHL	0.20	0.16 + 0.020*SL	0.16 + 0.017*SL	0.18 + 0.016*SL
	tR	0.26	0.10 + 0.079*SL	0.09 + 0.083*SL	0.06 + 0.085*SL
	tF	0.13	0.07 + 0.030*SL	0.06 + 0.032*SL	0.04 + 0.033*SL
D to Y	tPLH	0.54	0.46 + 0.039*SL	0.47 + 0.037*SL	0.47 + 0.036*SL
	tPHL	0.17	0.13 + 0.023*SL	0.15 + 0.017*SL	0.16 + 0.016*SL
	tR	0.24	0.08 + 0.080*SL	0.07 + 0.084*SL	0.05 + 0.085*SL
	tF	0.14	0.07 + 0.032*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
E to Y	tPLH	0.51	0.43 + 0.040*SL	0.45 + 0.037*SL	0.45 + 0.036*SL
	tPHL	0.21	0.16 + 0.024*SL	0.18 + 0.017*SL	0.20 + 0.016*SL
	tR	0.25	0.10 + 0.075*SL	0.08 + 0.083*SL	0.06 + 0.085*SL
	tF	0.14	0.08 + 0.030*SL	0.07 + 0.032*SL	0.05 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR5D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.60	0.56 + 0.024*SL	0.57 + 0.019*SL	0.58 + 0.018*SL
	tPHL	0.17	0.14 + 0.015*SL	0.15 + 0.009*SL	0.18 + 0.008*SL
	tR	0.20	0.12 + 0.040*SL	0.11 + 0.041*SL	0.08 + 0.042*SL
	tF	0.11	0.08 + 0.017*SL	0.08 + 0.015*SL	0.06 + 0.016*SL
B to Y	tPLH	0.58	0.53 + 0.026*SL	0.55 + 0.019*SL	0.56 + 0.018*SL
	tPHL	0.20	0.19 + 0.010*SL	0.18 + 0.010*SL	0.22 + 0.008*SL
	tR	0.20	0.11 + 0.045*SL	0.12 + 0.041*SL	0.09 + 0.042*SL
	tF	0.11	0.08 + 0.016*SL	0.08 + 0.016*SL	0.08 + 0.016*SL
C to Y	tPLH	0.61	0.57 + 0.021*SL	0.57 + 0.019*SL	0.59 + 0.018*SL
	tPHL	0.19	0.16 + 0.014*SL	0.17 + 0.010*SL	0.21 + 0.008*SL
	tR	0.20	0.11 + 0.048*SL	0.13 + 0.040*SL	0.09 + 0.042*SL
	tF	0.13	0.09 + 0.017*SL	0.10 + 0.016*SL	0.10 + 0.015*SL
D to Y	tPLH	0.59	0.54 + 0.023*SL	0.55 + 0.019*SL	0.57 + 0.018*SL
	tPHL	0.22	0.19 + 0.016*SL	0.21 + 0.010*SL	0.25 + 0.008*SL
	tR	0.20	0.11 + 0.046*SL	0.13 + 0.040*SL	0.09 + 0.042*SL
	tF	0.12	0.09 + 0.017*SL	0.09 + 0.016*SL	0.10 + 0.015*SL
E to Y	tPLH	0.51	0.45 + 0.026*SL	0.48 + 0.019*SL	0.49 + 0.018*SL
	tPHL	0.21	0.17 + 0.017*SL	0.20 + 0.010*SL	0.24 + 0.008*SL
	tR	0.20	0.11 + 0.042*SL	0.12 + 0.041*SL	0.09 + 0.042*SL
	tF	0.14	0.10 + 0.021*SL	0.12 + 0.015*SL	0.12 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR5D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.60	0.57 + 0.014*SL	0.59 + 0.010*SL	0.59 + 0.010*SL
	t_{PHL}	0.21	0.19 + 0.010*SL	0.20 + 0.006*SL	0.23 + 0.005*SL
	t_R	0.16	0.11 + 0.024*SL	0.12 + 0.022*SL	0.12 + 0.022*SL
	t_F	0.13	0.11 + 0.009*SL	0.12 + 0.008*SL	0.12 + 0.008*SL
B to Y	t_{PLH}	0.58	0.55 + 0.015*SL	0.56 + 0.010*SL	0.58 + 0.009*SL
	t_{PHL}	0.25	0.23 + 0.010*SL	0.24 + 0.006*SL	0.27 + 0.005*SL
	t_R	0.16	0.12 + 0.023*SL	0.12 + 0.022*SL	0.11 + 0.022*SL
	t_F	0.14	0.11 + 0.012*SL	0.12 + 0.009*SL	0.14 + 0.008*SL
C to Y	t_{PLH}	0.73	0.71 + 0.013*SL	0.72 + 0.010*SL	0.73 + 0.009*SL
	t_{PHL}	0.27	0.25 + 0.010*SL	0.26 + 0.007*SL	0.29 + 0.005*SL
	t_R	0.17	0.13 + 0.020*SL	0.13 + 0.021*SL	0.12 + 0.022*SL
	t_F	0.15	0.14 + 0.005*SL	0.13 + 0.009*SL	0.15 + 0.008*SL
D to Y	t_{PLH}	0.74	0.71 + 0.012*SL	0.72 + 0.010*SL	0.74 + 0.009*SL
	t_{PHL}	0.30	0.27 + 0.011*SL	0.29 + 0.007*SL	0.32 + 0.005*SL
	t_R	0.17	0.13 + 0.019*SL	0.13 + 0.021*SL	0.12 + 0.022*SL
	t_F	0.15	0.13 + 0.011*SL	0.14 + 0.008*SL	0.14 + 0.008*SL
E to Y	t_{PLH}	0.72	0.70 + 0.012*SL	0.70 + 0.010*SL	0.72 + 0.010*SL
	t_{PHL}	0.31	0.29 + 0.009*SL	0.30 + 0.007*SL	0.34 + 0.005*SL
	t_R	0.17	0.13 + 0.020*SL	0.13 + 0.021*SL	0.12 + 0.022*SL
	t_F	0.15	0.13 + 0.010*SL	0.13 + 0.009*SL	0.14 + 0.008*SL

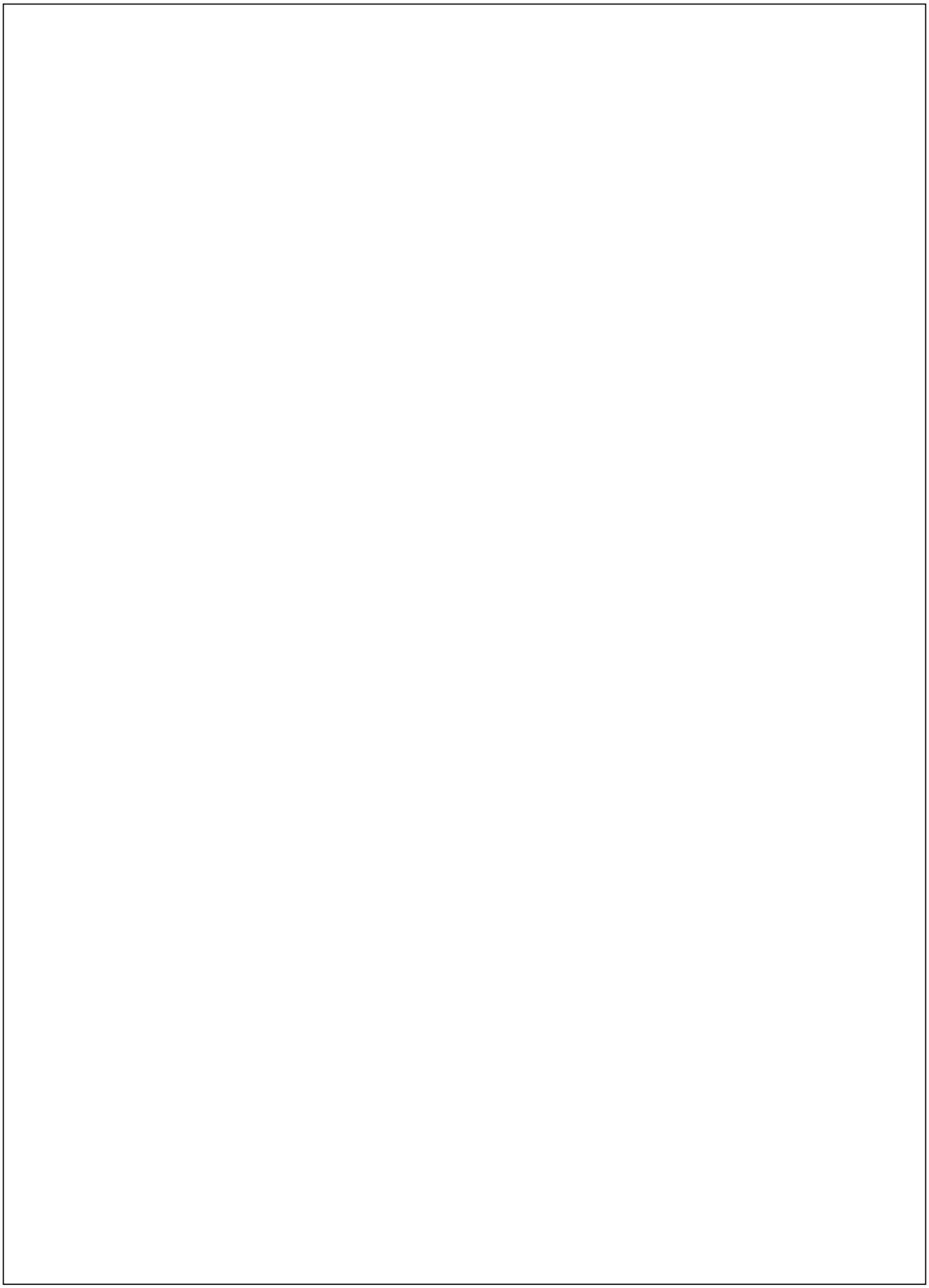
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR5D6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

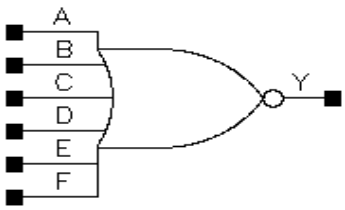
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.66	0.64 + 0.009*SL	0.65 + 0.007*SL	0.66 + 0.007*SL
	t_{PHL}	0.27	0.25 + 0.007*SL	0.26 + 0.005*SL	0.29 + 0.004*SL
	t_R	0.17	0.15 + 0.010*SL	0.13 + 0.015*SL	0.15 + 0.014*SL
	t_F	0.16	0.15 + 0.007*SL	0.15 + 0.006*SL	0.17 + 0.005*SL
B to Y	t_{PLH}	0.64	0.62 + 0.009*SL	0.62 + 0.007*SL	0.64 + 0.007*SL
	t_{PHL}	0.30	0.29 + 0.005*SL	0.29 + 0.006*SL	0.32 + 0.004*SL
	t_R	0.17	0.14 + 0.014*SL	0.14 + 0.015*SL	0.16 + 0.014*SL
	t_F	0.16	0.15 + 0.005*SL	0.15 + 0.007*SL	0.18 + 0.005*SL
C to Y	t_{PLH}	0.79	0.78 + 0.009*SL	0.78 + 0.008*SL	0.80 + 0.007*SL
	t_{PHL}	0.32	0.30 + 0.009*SL	0.31 + 0.005*SL	0.33 + 0.004*SL
	t_R	0.18	0.16 + 0.009*SL	0.15 + 0.014*SL	0.14 + 0.015*SL
	t_F	0.17	0.15 + 0.008*SL	0.16 + 0.007*SL	0.18 + 0.005*SL
D to Y	t_{PLH}	0.80	0.78 + 0.011*SL	0.79 + 0.007*SL	0.80 + 0.007*SL
	t_{PHL}	0.35	0.33 + 0.008*SL	0.34 + 0.006*SL	0.37 + 0.004*SL
	t_R	0.18	0.15 + 0.018*SL	0.16 + 0.014*SL	0.15 + 0.014*SL
	t_F	0.18	0.15 + 0.011*SL	0.17 + 0.006*SL	0.19 + 0.005*SL
E to Y	t_{PLH}	0.78	0.76 + 0.010*SL	0.77 + 0.007*SL	0.79 + 0.007*SL
	t_{PHL}	0.36	0.34 + 0.008*SL	0.35 + 0.006*SL	0.38 + 0.004*SL
	t_R	0.18	0.16 + 0.013*SL	0.15 + 0.014*SL	0.14 + 0.014*SL
	t_F	0.19	0.18 + 0.003*SL	0.17 + 0.006*SL	0.20 + 0.005*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D, E, F
Output: Y
Input Loading (SL): All : 1
Maximum Fanout (Rec. SL):
- NR6: 28
- NR6D2: 56

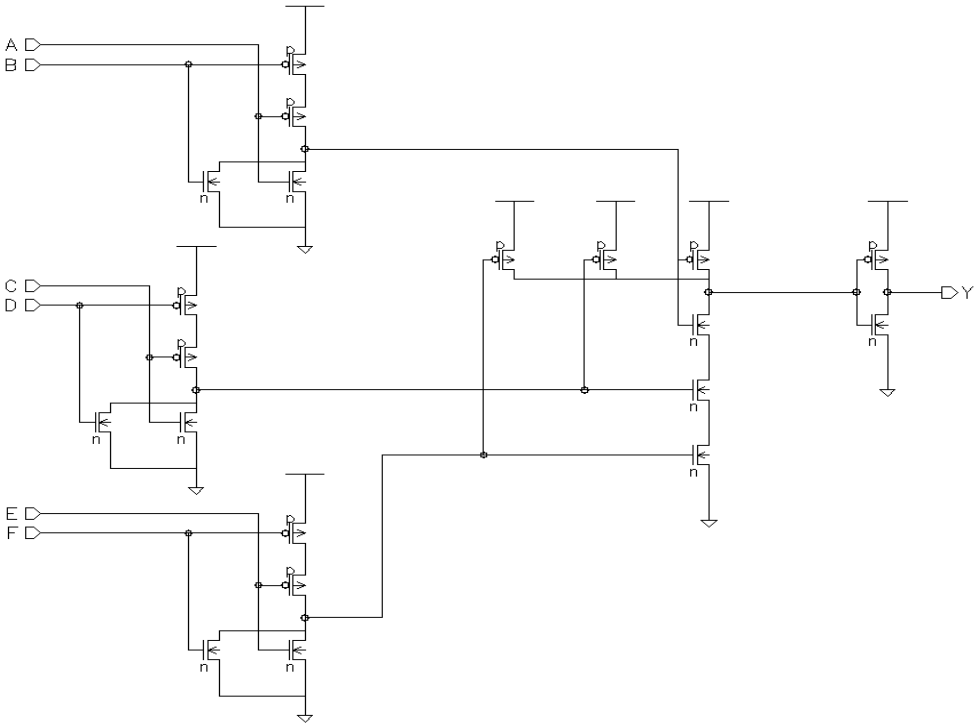
Gate Count:
- NR6: 5
- NR6D2: 6



Symbol

A	B	C	D	E	F	Y
0	0	0	0	0	0	1
1	x	x	x	x	x	0
x	1	x	x	x	x	0
x	x	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0

Truth Table



Schematic

NR6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.60	0.52 + 0.040*SL	0.53 + 0.036*SL	0.53 + 0.036*SL
	tPHL	0.16	0.11 + 0.022*SL	0.13 + 0.017*SL	0.14 + 0.016*SL
	tR	0.27	0.11 + 0.077*SL	0.10 + 0.083*SL	0.06 + 0.084*SL
	tF	0.13	0.06 + 0.035*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
B to Y	tPLH	0.57	0.49 + 0.040*SL	0.51 + 0.036*SL	0.51 + 0.036*SL
	tPHL	0.19	0.15 + 0.023*SL	0.16 + 0.017*SL	0.18 + 0.016*SL
	tR	0.27	0.11 + 0.078*SL	0.10 + 0.083*SL	0.06 + 0.084*SL
	tF	0.13	0.06 + 0.034*SL	0.07 + 0.031*SL	0.05 + 0.033*SL
C to Y	tPLH	0.61	0.53 + 0.041*SL	0.54 + 0.036*SL	0.55 + 0.036*SL
	tPHL	0.18	0.13 + 0.024*SL	0.16 + 0.017*SL	0.17 + 0.016*SL
	tR	0.27	0.11 + 0.080*SL	0.10 + 0.082*SL	0.06 + 0.084*SL
	tF	0.14	0.08 + 0.031*SL	0.07 + 0.031*SL	0.05 + 0.033*SL
D to Y	tPLH	0.58	0.50 + 0.044*SL	0.52 + 0.036*SL	0.52 + 0.036*SL
	tPHL	0.22	0.17 + 0.024*SL	0.19 + 0.017*SL	0.21 + 0.016*SL
	tR	0.27	0.11 + 0.080*SL	0.10 + 0.083*SL	0.06 + 0.084*SL
	tF	0.14	0.08 + 0.032*SL	0.08 + 0.031*SL	0.05 + 0.033*SL
E to Y	tPLH	0.61	0.52 + 0.043*SL	0.54 + 0.036*SL	0.54 + 0.036*SL
	tPHL	0.20	0.15 + 0.025*SL	0.18 + 0.017*SL	0.20 + 0.016*SL
	tR	0.26	0.09 + 0.086*SL	0.10 + 0.083*SL	0.06 + 0.084*SL
	tF	0.16	0.09 + 0.035*SL	0.10 + 0.031*SL	0.07 + 0.032*SL
F to Y	tPLH	0.58	0.50 + 0.043*SL	0.52 + 0.037*SL	0.52 + 0.036*SL
	tPHL	0.24	0.19 + 0.025*SL	0.21 + 0.017*SL	0.23 + 0.016*SL
	tR	0.27	0.10 + 0.082*SL	0.10 + 0.083*SL	0.06 + 0.084*SL
	tF	0.15	0.09 + 0.030*SL	0.09 + 0.031*SL	0.06 + 0.032*SL

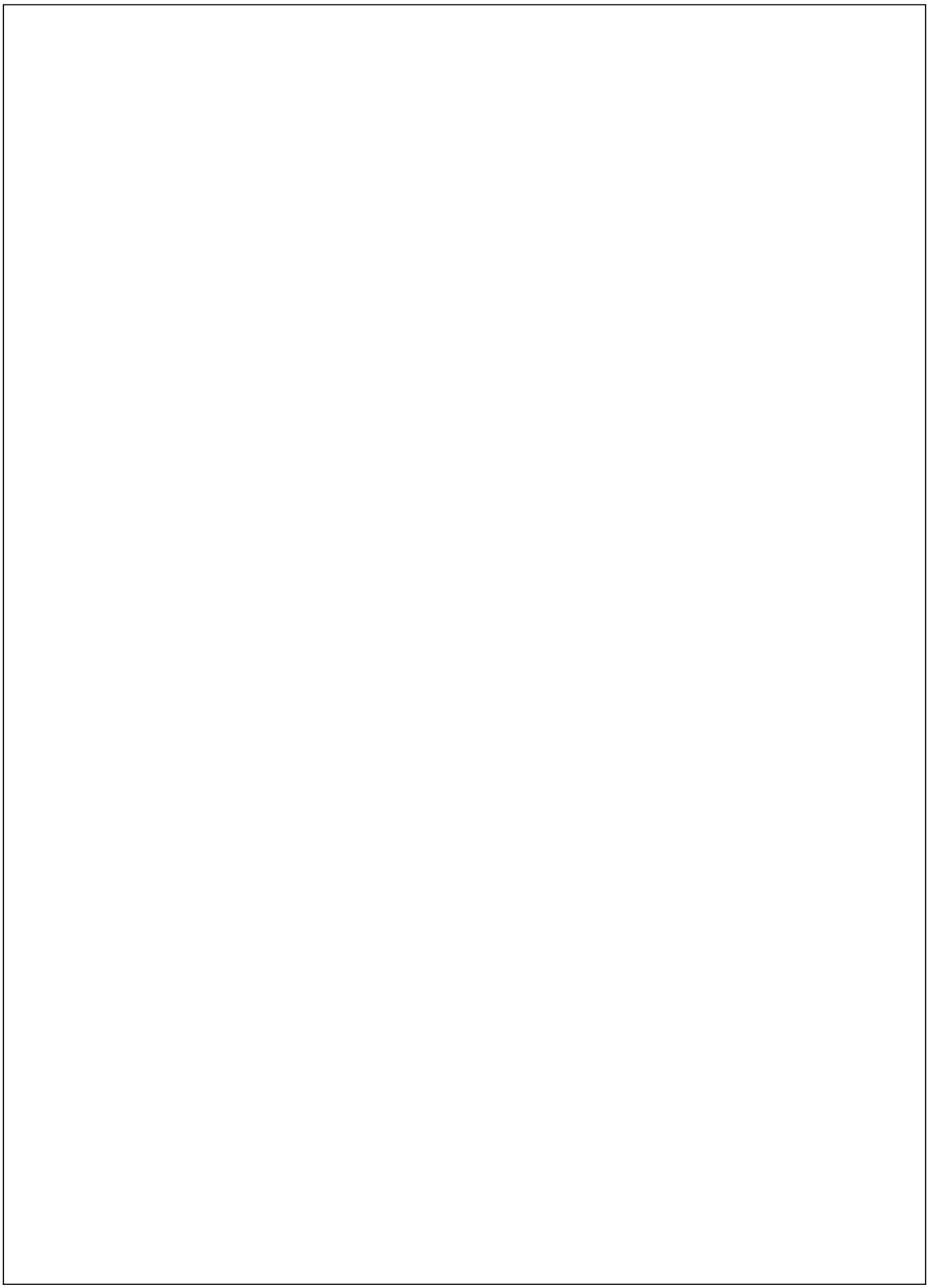
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR6D2 Switching Characteristics

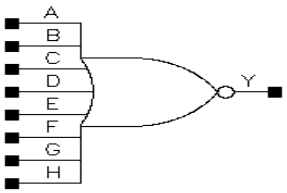
[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.60	0.56 + 0.017*SL	0.57 + 0.013*SL	0.59 + 0.012*SL
	t_{PHL}	0.19	0.16 + 0.014*SL	0.18 + 0.010*SL	0.21 + 0.008*SL
	t_R	0.18	0.12 + 0.028*SL	0.13 + 0.026*SL	0.11 + 0.027*SL
	t_F	0.12	0.09 + 0.019*SL	0.09 + 0.016*SL	0.09 + 0.016*SL
B to Y	t_{PLH}	0.57	0.53 + 0.020*SL	0.55 + 0.013*SL	0.57 + 0.012*SL
	t_{PHL}	0.23	0.20 + 0.013*SL	0.21 + 0.010*SL	0.25 + 0.008*SL
	t_R	0.17	0.12 + 0.028*SL	0.12 + 0.027*SL	0.11 + 0.027*SL
	t_F	0.12	0.09 + 0.019*SL	0.10 + 0.016*SL	0.10 + 0.016*SL
C to Y	t_{PLH}	0.61	0.58 + 0.013*SL	0.58 + 0.014*SL	0.61 + 0.012*SL
	t_{PHL}	0.22	0.19 + 0.016*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
	t_R	0.19	0.15 + 0.021*SL	0.13 + 0.026*SL	0.11 + 0.027*SL
	t_F	0.14	0.10 + 0.020*SL	0.11 + 0.015*SL	0.09 + 0.016*SL
D to Y	t_{PLH}	0.58	0.54 + 0.021*SL	0.56 + 0.013*SL	0.58 + 0.012*SL
	t_{PHL}	0.26	0.23 + 0.015*SL	0.24 + 0.010*SL	0.27 + 0.008*SL
	t_R	0.19	0.12 + 0.033*SL	0.14 + 0.026*SL	0.11 + 0.027*SL
	t_F	0.14	0.10 + 0.017*SL	0.11 + 0.015*SL	0.09 + 0.016*SL
E to Y	t_{PLH}	0.60	0.58 + 0.014*SL	0.58 + 0.014*SL	0.61 + 0.012*SL
	t_{PHL}	0.24	0.21 + 0.015*SL	0.23 + 0.010*SL	0.26 + 0.008*SL
	t_R	0.19	0.14 + 0.021*SL	0.13 + 0.026*SL	0.11 + 0.027*SL
	t_F	0.15	0.12 + 0.013*SL	0.12 + 0.015*SL	0.11 + 0.016*SL
F to Y	t_{PLH}	0.58	0.54 + 0.018*SL	0.55 + 0.014*SL	0.58 + 0.012*SL
	t_{PHL}	0.27	0.24 + 0.015*SL	0.26 + 0.010*SL	0.30 + 0.008*SL
	t_R	0.18	0.12 + 0.032*SL	0.13 + 0.026*SL	0.12 + 0.027*SL
	t_F	0.15	0.12 + 0.014*SL	0.12 + 0.016*SL	0.12 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL



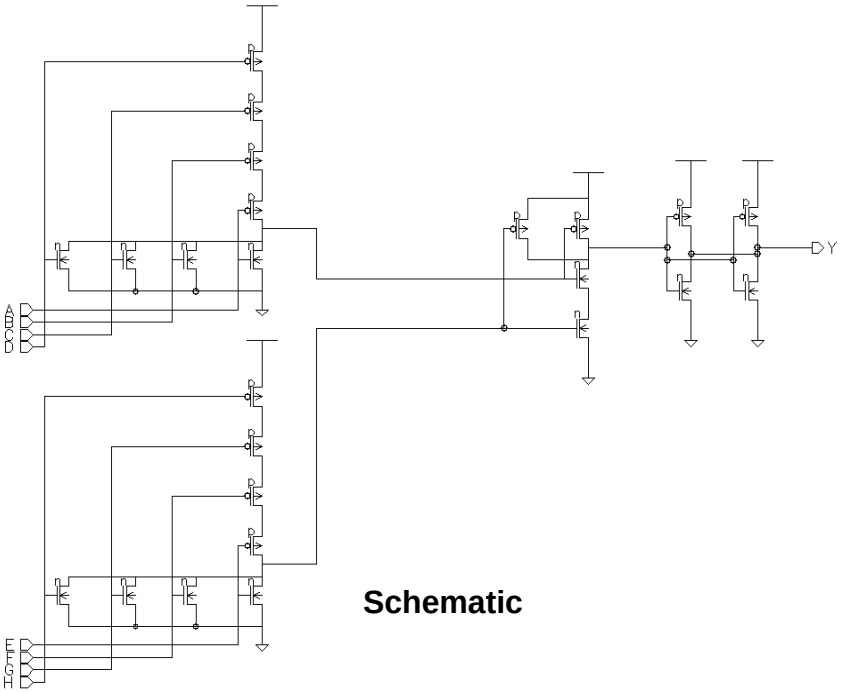
Inputs: A, B, C, D, E, F, G, H
Output: Y
Input Loading (SL): All : 1
Maximum Fanout (Rec. SL): 56
Gate Count:
- NR8: 6
- NR8D2: 7



Symbol

A	B	C	D	E	F	G	H	Y
0	0	0	0	0	0	0	0	1
1	x	x	x	x	x	x	x	0
x	1	x	x	x	x	x	x	0
x	x	1	x	x	x	x	x	0
x	x	x	1	x	x	x	x	0
x	x	x	x	1	x	x	x	0
x	x	x	x	x	1	x	x	0
x	x	x	x	x	x	1	x	0
x	x	x	x	x	x	x	1	0

Truth Table



Schematic

NR8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.74	0.70 + 0.020*SL	0.70 + 0.019*SL	0.71 + 0.018*SL
	t_{PHL}	0.18	0.15 + 0.013*SL	0.16 + 0.009*SL	0.18 + 0.008*SL
	t_R	0.18	0.11 + 0.036*SL	0.10 + 0.041*SL	0.07 + 0.043*SL
	t_F	0.11	0.07 + 0.018*SL	0.08 + 0.016*SL	0.06 + 0.016*SL
B to Y	t_{PLH}	0.76	0.72 + 0.021*SL	0.73 + 0.019*SL	0.73 + 0.018*SL
	t_{PHL}	0.20	0.18 + 0.013*SL	0.19 + 0.009*SL	0.21 + 0.008*SL
	t_R	0.19	0.11 + 0.036*SL	0.10 + 0.041*SL	0.07 + 0.043*SL
	t_F	0.11	0.07 + 0.018*SL	0.08 + 0.015*SL	0.07 + 0.016*SL
C to Y	t_{PLH}	0.78	0.73 + 0.023*SL	0.74 + 0.018*SL	0.75 + 0.018*SL
	t_{PHL}	0.22	0.19 + 0.015*SL	0.21 + 0.009*SL	0.23 + 0.008*SL
	t_R	0.19	0.11 + 0.040*SL	0.10 + 0.041*SL	0.08 + 0.043*SL
	t_F	0.11	0.07 + 0.019*SL	0.08 + 0.016*SL	0.08 + 0.016*SL
D to Y	t_{PLH}	0.77	0.73 + 0.020*SL	0.73 + 0.019*SL	0.74 + 0.018*SL
	t_{PHL}	0.22	0.20 + 0.011*SL	0.20 + 0.010*SL	0.23 + 0.008*SL
	t_R	0.19	0.11 + 0.038*SL	0.10 + 0.041*SL	0.08 + 0.043*SL
	t_F	0.12	0.08 + 0.017*SL	0.09 + 0.015*SL	0.08 + 0.016*SL
E to Y	t_{PLH}	0.71	0.67 + 0.018*SL	0.67 + 0.019*SL	0.68 + 0.018*SL
	t_{PHL}	0.20	0.17 + 0.015*SL	0.18 + 0.010*SL	0.21 + 0.008*SL
	t_R	0.19	0.11 + 0.041*SL	0.11 + 0.041*SL	0.08 + 0.043*SL
	t_F	0.12	0.07 + 0.023*SL	0.10 + 0.015*SL	0.08 + 0.016*SL
F to Y	t_{PLH}	0.74	0.70 + 0.022*SL	0.70 + 0.019*SL	0.71 + 0.018*SL
	t_{PHL}	0.23	0.20 + 0.014*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
	t_R	0.19	0.11 + 0.040*SL	0.11 + 0.041*SL	0.07 + 0.043*SL
	t_F	0.12	0.09 + 0.018*SL	0.10 + 0.015*SL	0.09 + 0.016*SL
G to Y	t_{PLH}	0.75	0.71 + 0.022*SL	0.72 + 0.019*SL	0.73 + 0.018*SL
	t_{PHL}	0.24	0.21 + 0.014*SL	0.23 + 0.010*SL	0.26 + 0.008*SL
	t_R	0.19	0.12 + 0.038*SL	0.11 + 0.041*SL	0.07 + 0.043*SL
	t_F	0.12	0.09 + 0.017*SL	0.10 + 0.015*SL	0.08 + 0.016*SL
H to Y	t_{PLH}	0.74	0.70 + 0.021*SL	0.71 + 0.019*SL	0.71 + 0.018*SL
	t_{PHL}	0.24	0.21 + 0.015*SL	0.23 + 0.010*SL	0.26 + 0.008*SL
	t_R	0.19	0.12 + 0.035*SL	0.11 + 0.041*SL	0.07 + 0.043*SL
	t_F	0.12	0.09 + 0.015*SL	0.09 + 0.016*SL	0.09 + 0.016*SL

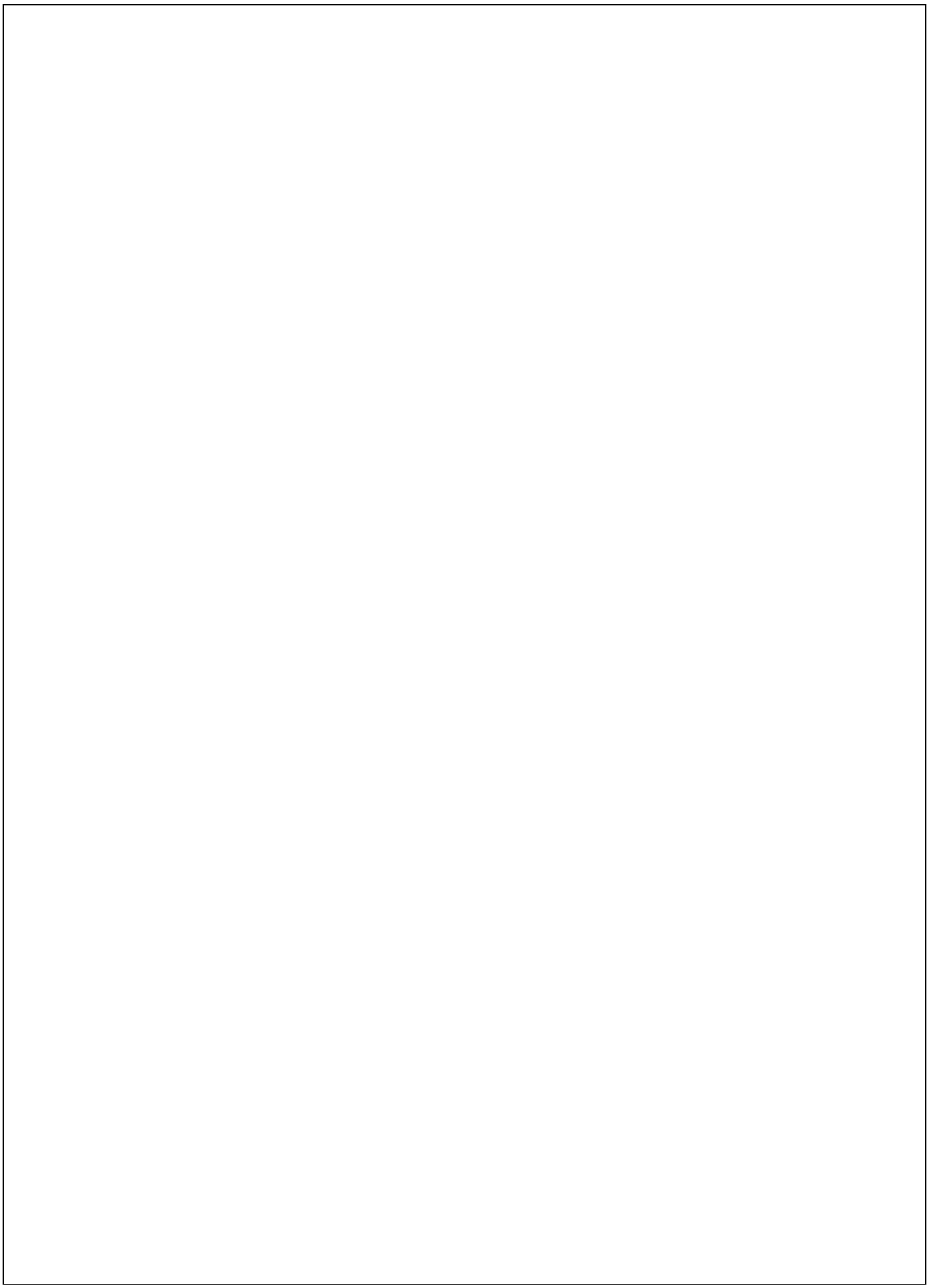
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

NR8D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.66	0.61 + 0.024*SL	0.62 + 0.020*SL	0.65 + 0.019*SL
	t_{PHL}	0.18	0.15 + 0.015*SL	0.16 + 0.010*SL	0.19 + 0.008*SL
	t_R	0.23	0.15 + 0.042*SL	0.14 + 0.043*SL	0.12 + 0.045*SL
	t_F	0.12	0.09 + 0.015*SL	0.09 + 0.016*SL	0.08 + 0.016*SL
B to Y	t_{PLH}	0.64	0.60 + 0.023*SL	0.61 + 0.020*SL	0.63 + 0.019*SL
	t_{PHL}	0.22	0.18 + 0.017*SL	0.20 + 0.010*SL	0.23 + 0.008*SL
	t_R	0.23	0.15 + 0.038*SL	0.14 + 0.044*SL	0.11 + 0.045*SL
	t_F	0.12	0.07 + 0.023*SL	0.10 + 0.015*SL	0.09 + 0.016*SL
C to Y	t_{PLH}	0.68	0.63 + 0.024*SL	0.64 + 0.020*SL	0.67 + 0.019*SL
	t_{PHL}	0.21	0.17 + 0.016*SL	0.19 + 0.010*SL	0.23 + 0.008*SL
	t_R	0.24	0.16 + 0.039*SL	0.15 + 0.043*SL	0.12 + 0.045*SL
	t_F	0.13	0.09 + 0.019*SL	0.10 + 0.016*SL	0.10 + 0.016*SL
D to Y	t_{PLH}	0.66	0.61 + 0.026*SL	0.62 + 0.020*SL	0.65 + 0.019*SL
	t_{PHL}	0.24	0.21 + 0.016*SL	0.23 + 0.010*SL	0.27 + 0.008*SL
	t_R	0.23	0.15 + 0.041*SL	0.14 + 0.043*SL	0.12 + 0.045*SL
	t_F	0.13	0.10 + 0.015*SL	0.10 + 0.015*SL	0.10 + 0.016*SL
E to Y	t_{PLH}	0.69	0.63 + 0.028*SL	0.66 + 0.020*SL	0.68 + 0.019*SL
	t_{PHL}	0.22	0.19 + 0.017*SL	0.21 + 0.011*SL	0.26 + 0.008*SL
	t_R	0.23	0.15 + 0.040*SL	0.13 + 0.044*SL	0.12 + 0.045*SL
	t_F	0.14	0.11 + 0.019*SL	0.11 + 0.015*SL	0.11 + 0.016*SL
F to Y	t_{PLH}	0.67	0.61 + 0.027*SL	0.63 + 0.020*SL	0.65 + 0.019*SL
	t_{PHL}	0.26	0.23 + 0.017*SL	0.25 + 0.011*SL	0.29 + 0.008*SL
	t_R	0.23	0.15 + 0.042*SL	0.15 + 0.043*SL	0.11 + 0.045*SL
	t_F	0.15	0.10 + 0.023*SL	0.12 + 0.015*SL	0.11 + 0.016*SL
G to Y	t_{PLH}	0.70	0.65 + 0.024*SL	0.66 + 0.021*SL	0.69 + 0.019*SL
	t_{PHL}	0.23	0.20 + 0.016*SL	0.22 + 0.011*SL	0.27 + 0.009*SL
	t_R	0.23	0.13 + 0.052*SL	0.16 + 0.043*SL	0.11 + 0.045*SL
	t_F	0.16	0.13 + 0.015*SL	0.12 + 0.016*SL	0.13 + 0.015*SL
H to Y	t_{PLH}	0.67	0.62 + 0.027*SL	0.64 + 0.020*SL	0.67 + 0.019*SL
	t_{PHL}	0.27	0.23 + 0.019*SL	0.26 + 0.011*SL	0.31 + 0.009*SL
	t_R	0.24	0.16 + 0.040*SL	0.15 + 0.043*SL	0.11 + 0.045*SL
	t_F	0.16	0.12 + 0.018*SL	0.13 + 0.016*SL	0.14 + 0.015*SL

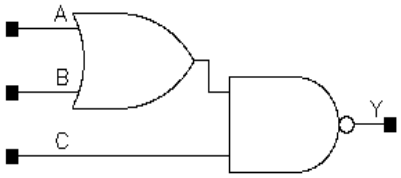
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C
Output: Y
Input Loading (SL):
- OA21: All : 1
- OA21D2: All : 2
- OA21D4: All: 1
- OA21D6: All: 1

Maximum Fanout (Rec. SL):
- OA21: 14
- OA21D2: 28
- OA21D4: 112
- OA21D6: 168

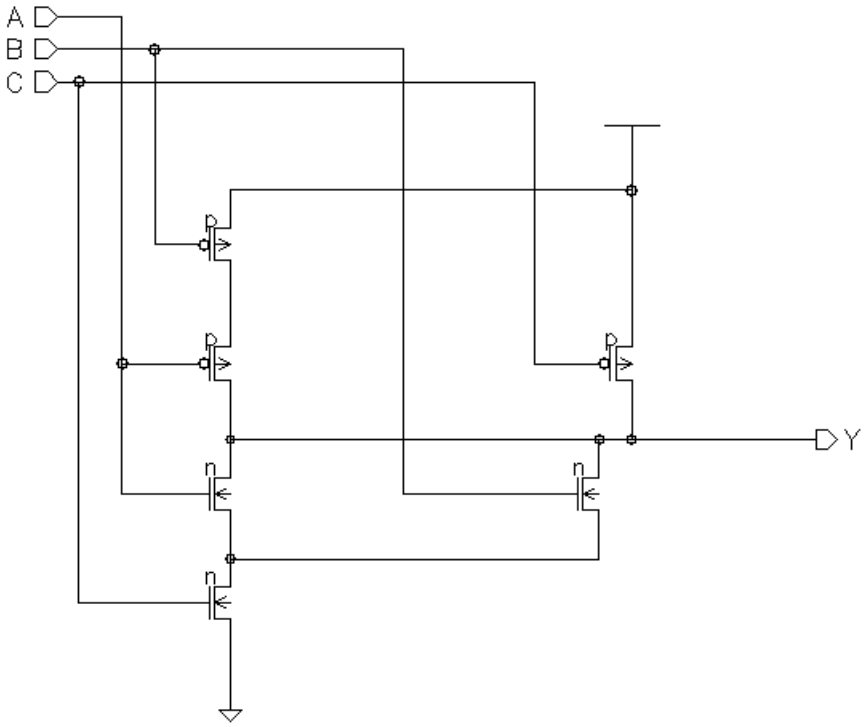
Gate Count:
- OA21: 2
- OA21D2: 3
- OA21D4: 4
- OA21D6: 5



Symbol

A	B	C	Y
1	x	1	0
x	1	1	0
0	0	x	1
x	x	0	1

Truth Table



Schematic

OA21 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.43	0.28 + 0.074*SL	0.29 + 0.069*SL	0.27 + 0.070*SL
	t_{PHL}	0.12	0.02 + 0.053*SL	0.08 + 0.031*SL	0.16 + 0.027*SL
	t_R	0.62	0.33 + 0.144*SL	0.28 + 0.161*SL	0.19 + 0.165*SL
	t_F	0.38	0.28 + 0.053*SL	0.27 + 0.057*SL	0.20 + 0.060*SL
B to Y	t_{PLH}	0.39	0.25 + 0.071*SL	0.26 + 0.069*SL	0.24 + 0.070*SL
	t_{PHL}	0.15	0.06 + 0.048*SL	0.11 + 0.030*SL	0.18 + 0.027*SL
	t_R	0.62	0.33 + 0.143*SL	0.28 + 0.161*SL	0.19 + 0.165*SL
	t_F	0.43	0.32 + 0.056*SL	0.32 + 0.055*SL	0.24 + 0.060*SL
C to Y	t_{PLH}	0.38	0.30 + 0.041*SL	0.31 + 0.037*SL	0.30 + 0.037*SL
	t_{PHL}	0.09	0.02 + 0.038*SL	0.06 + 0.024*SL	0.13 + 0.020*SL
	t_R	0.49	0.35 + 0.068*SL	0.31 + 0.082*SL	0.22 + 0.087*SL
	t_F	0.37	0.29 + 0.039*SL	0.28 + 0.041*SL	0.20 + 0.045*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OA21D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.36	0.28 + 0.041*SL	0.29 + 0.035*SL	0.29 + 0.036*SL
	t_{PHL}	0.06	-0.00 + 0.032*SL	0.04 + 0.019*SL	0.14 + 0.014*SL
	t_R	0.49	0.33 + 0.077*SL	0.32 + 0.080*SL	0.24 + 0.084*SL
	t_F	0.32	0.25 + 0.036*SL	0.28 + 0.028*SL	0.26 + 0.029*SL
B to Y	t_{PLH}	0.33	0.25 + 0.038*SL	0.26 + 0.035*SL	0.25 + 0.036*SL
	t_{PHL}	0.10	0.04 + 0.028*SL	0.07 + 0.018*SL	0.16 + 0.014*SL
	t_R	0.49	0.34 + 0.072*SL	0.32 + 0.080*SL	0.23 + 0.084*SL
	t_F	0.38	0.33 + 0.030*SL	0.34 + 0.026*SL	0.30 + 0.028*SL
C to Y	t_{PLH}	0.33	0.29 + 0.023*SL	0.30 + 0.018*SL	0.31 + 0.018*SL
	t_{PHL}	0.05	0.01 + 0.022*SL	0.03 + 0.014*SL	0.10 + 0.011*SL
	t_R	0.40	0.32 + 0.039*SL	0.33 + 0.038*SL	0.27 + 0.040*SL
	t_F	0.33	0.30 + 0.014*SL	0.28 + 0.020*SL	0.26 + 0.021*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OA21D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.52	0.50 + 0.011*SL	0.50 + 0.010*SL	0.51 + 0.009*SL
	tPHL	0.29	0.28 + 0.007*SL	0.28 + 0.006*SL	0.31 + 0.005*SL
	tR	0.14	0.09 + 0.024*SL	0.10 + 0.021*SL	0.08 + 0.022*SL
	tF	0.14	0.13 + 0.005*SL	0.12 + 0.008*SL	0.12 + 0.008*SL
B to Y	tPLH	0.50	0.47 + 0.010*SL	0.48 + 0.010*SL	0.49 + 0.009*SL
	tPHL	0.34	0.32 + 0.006*SL	0.32 + 0.007*SL	0.36 + 0.005*SL
	tR	0.14	0.09 + 0.024*SL	0.10 + 0.021*SL	0.08 + 0.022*SL
	tF	0.13	0.11 + 0.010*SL	0.11 + 0.009*SL	0.12 + 0.008*SL
C to Y	tPLH	0.50	0.48 + 0.012*SL	0.49 + 0.010*SL	0.49 + 0.009*SL
	tPHL	0.29	0.27 + 0.007*SL	0.28 + 0.006*SL	0.31 + 0.005*SL
	tR	0.14	0.09 + 0.022*SL	0.10 + 0.021*SL	0.08 + 0.022*SL
	tF	0.13	0.12 + 0.009*SL	0.12 + 0.008*SL	0.11 + 0.009*SL

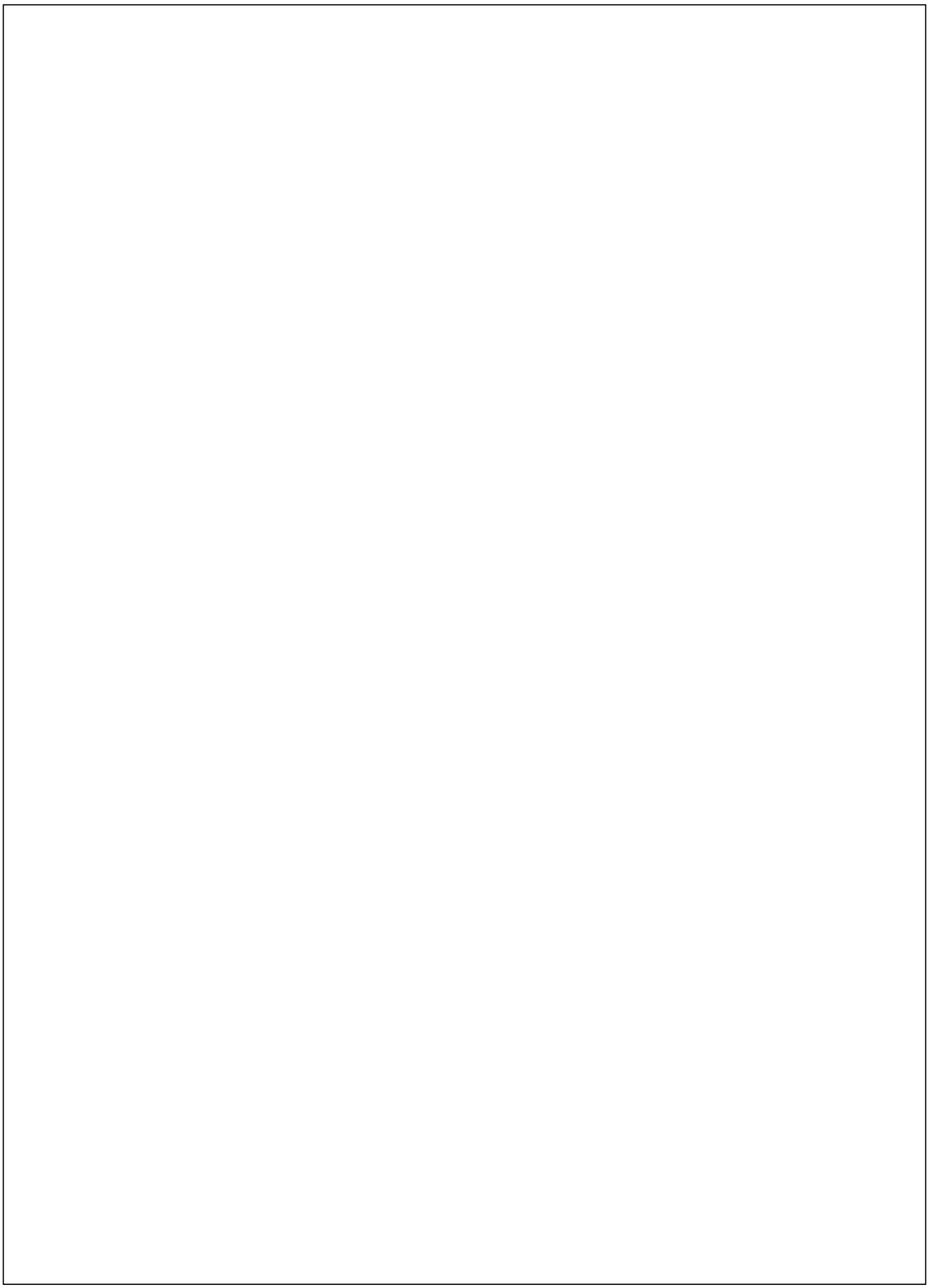
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OA21D6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.56	0.55 + 0.008*SL	0.55 + 0.007*SL	0.56 + 0.006*SL
	tPHL	0.34	0.33 + 0.008*SL	0.33 + 0.005*SL	0.36 + 0.004*SL
	tR	0.13	0.10 + 0.016*SL	0.11 + 0.014*SL	0.10 + 0.014*SL
	tF	0.16	0.14 + 0.010*SL	0.15 + 0.006*SL	0.17 + 0.005*SL
B to Y	tPLH	0.53	0.52 + 0.008*SL	0.52 + 0.007*SL	0.53 + 0.006*SL
	tPHL	0.39	0.38 + 0.007*SL	0.38 + 0.005*SL	0.41 + 0.004*SL
	tR	0.14	0.10 + 0.016*SL	0.11 + 0.014*SL	0.11 + 0.014*SL
	tF	0.17	0.16 + 0.004*SL	0.16 + 0.006*SL	0.17 + 0.005*SL
C to Y	tPLH	0.54	0.52 + 0.008*SL	0.53 + 0.007*SL	0.54 + 0.006*SL
	tPHL	0.34	0.33 + 0.006*SL	0.33 + 0.005*SL	0.36 + 0.004*SL
	tR	0.13	0.10 + 0.014*SL	0.10 + 0.015*SL	0.11 + 0.014*SL
	tF	0.16	0.15 + 0.008*SL	0.15 + 0.006*SL	0.17 + 0.005*SL

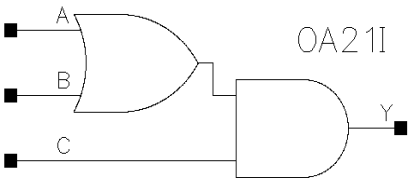
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C
Output: Y
Input Loading (SL):
- OA21I: All: 1
- OA21ID3: All: 1
- OA21ID5: All: 1
- OA21ID8: All: 2

Maximum Fanout (Rec. SL):
- OA21I: 28
- OA21ID3: 84
- OA21ID5: 140
- OA21ID8: 224

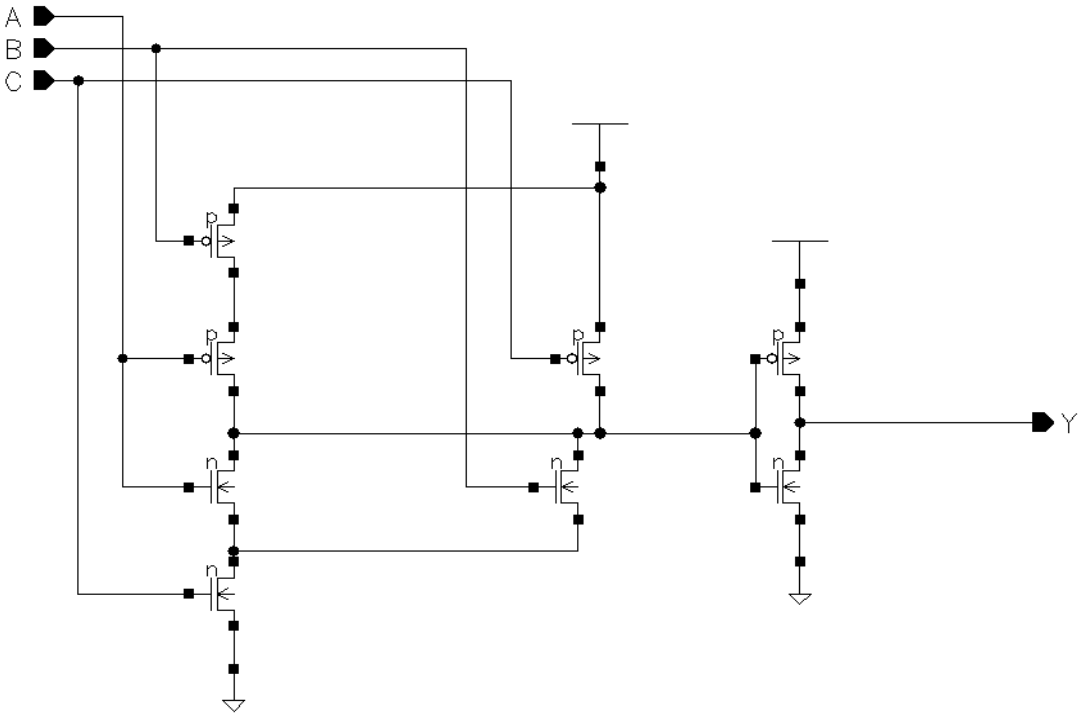
Gate Count:
- OA21I: 2
- OA21ID3: 3
- OA21ID5: 5
- OA21ID8: 8



Symbol

A	B	C	Y
1	x	1	0
x	1	1	0
0	0	1	0
x	x	0	1

Truth Table



Schematic

OA21I Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.21	0.13 + 0.043*SL	0.14 + 0.038*SL	0.15 + 0.038*SL
	t_{PHL}	0.40	0.35 + 0.027*SL	0.38 + 0.018*SL	0.42 + 0.016*SL
	t_R	0.27	0.11 + 0.081*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
	t_F	0.19	0.11 + 0.039*SL	0.14 + 0.030*SL	0.09 + 0.032*SL
B to Y	t_{PLH}	0.26	0.17 + 0.042*SL	0.19 + 0.037*SL	0.19 + 0.037*SL
	t_{PHL}	0.38	0.32 + 0.027*SL	0.35 + 0.018*SL	0.39 + 0.016*SL
	t_R	0.27	0.10 + 0.086*SL	0.10 + 0.086*SL	0.06 + 0.088*SL
	t_F	0.19	0.12 + 0.034*SL	0.13 + 0.030*SL	0.10 + 0.032*SL
C to Y	t_{PLH}	0.21	0.14 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.037*SL
	t_{PHL}	0.39	0.34 + 0.025*SL	0.36 + 0.017*SL	0.39 + 0.016*SL
	t_R	0.28	0.11 + 0.082*SL	0.10 + 0.086*SL	0.06 + 0.088*SL
	t_F	0.19	0.13 + 0.029*SL	0.13 + 0.029*SL	0.07 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

OA21ID3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.26	0.23 + 0.016*SL	0.24 + 0.013*SL	0.25 + 0.013*SL
	t_{PHL}	0.49	0.46 + 0.013*SL	0.47 + 0.009*SL	0.52 + 0.007*SL
	t_R	0.18	0.12 + 0.031*SL	0.13 + 0.028*SL	0.11 + 0.029*SL
	t_F	0.21	0.19 + 0.008*SL	0.19 + 0.010*SL	0.18 + 0.010*SL
B to Y	t_{PLH}	0.30	0.27 + 0.015*SL	0.28 + 0.013*SL	0.29 + 0.012*SL
	t_{PHL}	0.45	0.42 + 0.014*SL	0.44 + 0.009*SL	0.48 + 0.007*SL
	t_R	0.19	0.12 + 0.034*SL	0.14 + 0.028*SL	0.11 + 0.029*SL
	t_F	0.21	0.19 + 0.012*SL	0.19 + 0.010*SL	0.19 + 0.010*SL
C to Y	t_{PLH}	0.23	0.19 + 0.016*SL	0.20 + 0.013*SL	0.22 + 0.012*SL
	t_{PHL}	0.42	0.39 + 0.014*SL	0.41 + 0.008*SL	0.46 + 0.006*SL
	t_R	0.17	0.12 + 0.029*SL	0.12 + 0.028*SL	0.10 + 0.029*SL
	t_F	0.17	0.14 + 0.015*SL	0.15 + 0.010*SL	0.15 + 0.010*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

OA21ID5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.35	0.32 + 0.011*SL	0.33 + 0.009*SL	0.35 + 0.008*SL
	tPHL	0.58	0.57 + 0.009*SL	0.57 + 0.007*SL	0.61 + 0.005*SL
	tR	0.18	0.14 + 0.021*SL	0.15 + 0.017*SL	0.16 + 0.017*SL
	tF	0.25	0.24 + 0.006*SL	0.24 + 0.007*SL	0.26 + 0.006*SL
B to Y	tPLH	0.38	0.35 + 0.011*SL	0.36 + 0.008*SL	0.37 + 0.008*SL
	tPHL	0.55	0.53 + 0.009*SL	0.54 + 0.007*SL	0.57 + 0.005*SL
	tR	0.19	0.16 + 0.015*SL	0.15 + 0.017*SL	0.15 + 0.017*SL
	tF	0.26	0.24 + 0.010*SL	0.25 + 0.007*SL	0.26 + 0.006*SL
C to Y	tPLH	0.28	0.26 + 0.014*SL	0.27 + 0.008*SL	0.28 + 0.008*SL
	tPHL	0.47	0.46 + 0.007*SL	0.46 + 0.006*SL	0.50 + 0.005*SL
	tR	0.17	0.14 + 0.017*SL	0.14 + 0.017*SL	0.14 + 0.017*SL
	tF	0.20	0.18 + 0.010*SL	0.19 + 0.006*SL	0.19 + 0.006*SL

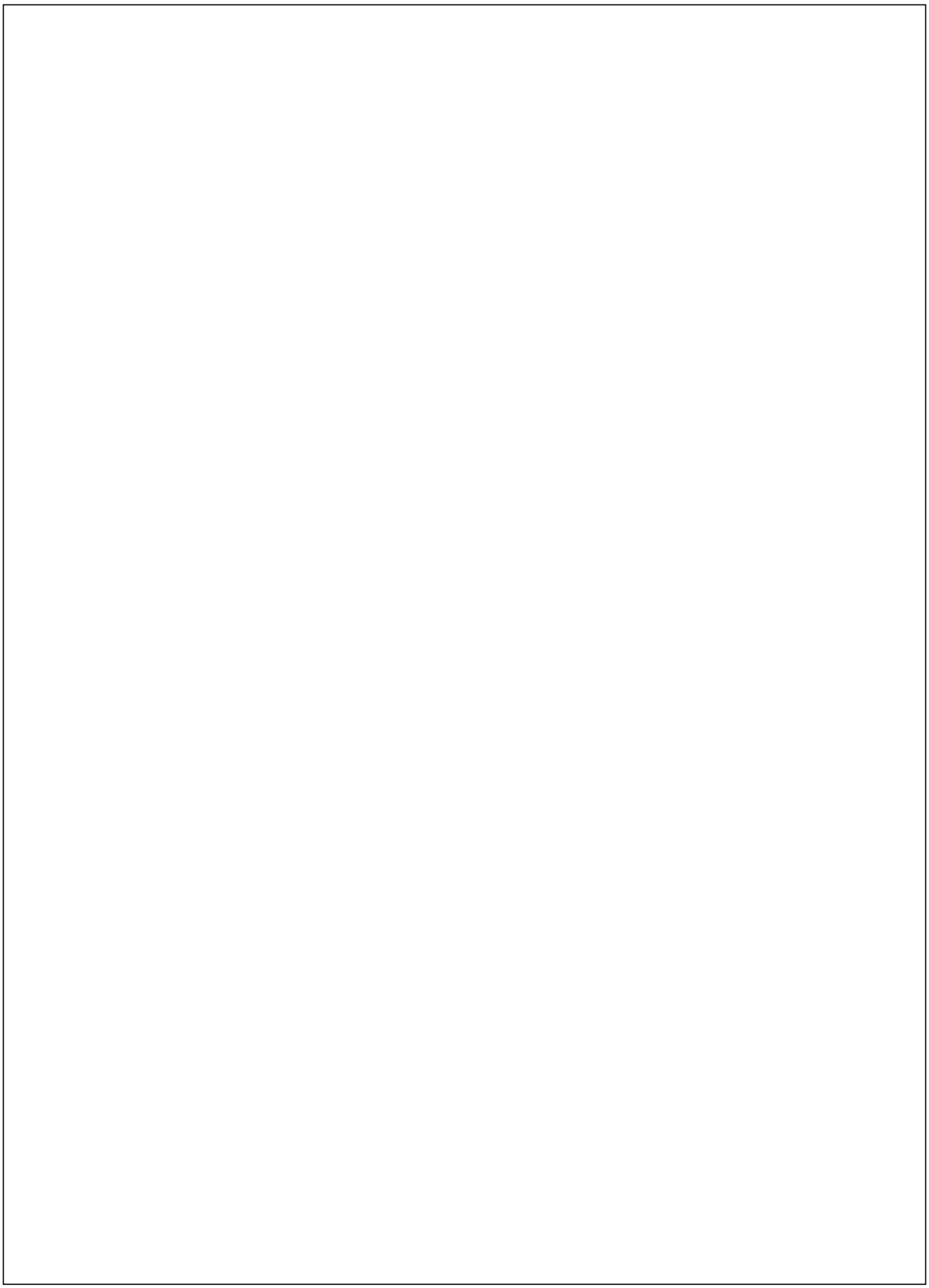
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OA21ID8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.30	0.29 + 0.007*SL	0.29 + 0.006*SL	0.30 + 0.005*SL
	tPHL	0.55	0.54 + 0.006*SL	0.54 + 0.005*SL	0.57 + 0.003*SL
	tR	0.16	0.15 + 0.006*SL	0.13 + 0.011*SL	0.13 + 0.011*SL
	tF	0.22	0.21 + 0.005*SL	0.21 + 0.005*SL	0.24 + 0.004*SL
B to Y	tPLH	0.34	0.32 + 0.007*SL	0.33 + 0.006*SL	0.34 + 0.005*SL
	tPHL	0.51	0.50 + 0.007*SL	0.50 + 0.005*SL	0.53 + 0.004*SL
	tR	0.16	0.14 + 0.011*SL	0.15 + 0.010*SL	0.13 + 0.011*SL
	tF	0.24	0.23 + 0.004*SL	0.23 + 0.004*SL	0.23 + 0.004*SL
C to Y	tPLH	0.25	0.24 + 0.007*SL	0.24 + 0.006*SL	0.25 + 0.005*SL
	tPHL	0.44	0.43 + 0.007*SL	0.43 + 0.005*SL	0.46 + 0.003*SL
	tR	0.15	0.14 + 0.009*SL	0.13 + 0.011*SL	0.14 + 0.010*SL
	tF	0.18	0.18 + 0.003*SL	0.17 + 0.005*SL	0.21 + 0.003*SL

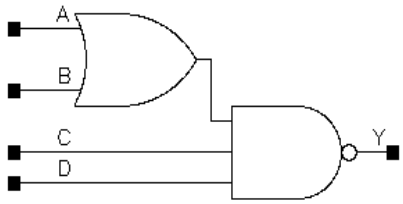
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D
Output: Y
Input Loading (SL):
- OA211: All : 1
- OA211D2: All : 2
- OA211D3: All: 1
- OA211D7: All: 1

Maximum Fanout (Rec. SL):
- OA211: 14
- OA211D2: 28
- OA211D3: 84
- OA211D7: 196

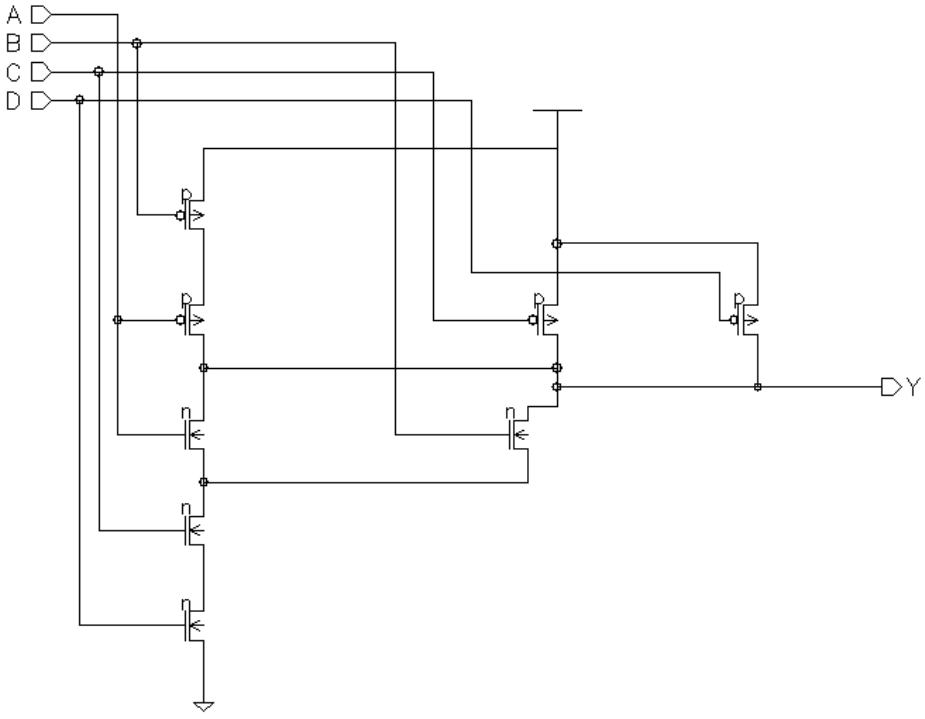
Gate Count:
- OA211: 2
- OA211D2: 4
- OA211D3: 4
- OA211D7: 6



Symbol

A	B	C	D	Y
1	x	1	1	0
x	1	1	1	0
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1

Truth Table



Schematic

OA211 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.43	0.28 + 0.075*SL	0.30 + 0.070*SL	0.28 + 0.070*SL
	t_{PHL}	0.18	0.07 + 0.059*SL	0.13 + 0.039*SL	0.17 + 0.037*SL
	t_R	0.66	0.36 + 0.148*SL	0.32 + 0.160*SL	0.23 + 0.165*SL
	t_F	0.48	0.32 + 0.081*SL	0.32 + 0.081*SL	0.22 + 0.086*SL
B to Y	t_{PLH}	0.40	0.25 + 0.072*SL	0.26 + 0.070*SL	0.25 + 0.070*SL
	t_{PHL}	0.22	0.12 + 0.053*SL	0.16 + 0.039*SL	0.19 + 0.037*SL
	t_R	0.65	0.36 + 0.146*SL	0.31 + 0.161*SL	0.23 + 0.165*SL
	t_F	0.54	0.39 + 0.074*SL	0.38 + 0.080*SL	0.26 + 0.085*SL
C to Y	t_{PLH}	0.37	0.29 + 0.043*SL	0.30 + 0.037*SL	0.30 + 0.037*SL
	t_{PHL}	0.18	0.09 + 0.045*SL	0.12 + 0.032*SL	0.16 + 0.030*SL
	t_R	0.51	0.36 + 0.075*SL	0.34 + 0.082*SL	0.23 + 0.087*SL
	t_F	0.47	0.36 + 0.057*SL	0.33 + 0.066*SL	0.24 + 0.071*SL
D to Y	t_{PLH}	0.41	0.33 + 0.040*SL	0.33 + 0.037*SL	0.33 + 0.037*SL
	t_{PHL}	0.13	0.05 + 0.040*SL	0.08 + 0.032*SL	0.10 + 0.030*SL
	t_R	0.56	0.42 + 0.070*SL	0.38 + 0.082*SL	0.28 + 0.087*SL
	t_F	0.44	0.33 + 0.059*SL	0.30 + 0.067*SL	0.21 + 0.071*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OA211D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.37	0.28 + 0.043*SL	0.30 + 0.037*SL	0.30 + 0.037*SL
	t_{PHL}	0.13	0.06 + 0.033*SL	0.09 + 0.023*SL	0.17 + 0.019*SL
	t_R	0.54	0.39 + 0.077*SL	0.37 + 0.083*SL	0.28 + 0.087*SL
	t_F	0.41	0.33 + 0.041*SL	0.32 + 0.042*SL	0.29 + 0.044*SL
B to Y	t_{PLH}	0.33	0.25 + 0.040*SL	0.26 + 0.037*SL	0.26 + 0.037*SL
	t_{PHL}	0.18	0.11 + 0.031*SL	0.14 + 0.022*SL	0.20 + 0.019*SL
	t_R	0.53	0.38 + 0.076*SL	0.35 + 0.084*SL	0.28 + 0.087*SL
	t_F	0.49	0.41 + 0.037*SL	0.40 + 0.041*SL	0.34 + 0.044*SL
C to Y	t_{PLH}	0.32	0.27 + 0.023*SL	0.29 + 0.019*SL	0.31 + 0.018*SL
	t_{PHL}	0.14	0.09 + 0.025*SL	0.10 + 0.019*SL	0.16 + 0.016*SL
	t_R	0.43	0.36 + 0.036*SL	0.36 + 0.037*SL	0.30 + 0.040*SL
	t_F	0.42	0.36 + 0.032*SL	0.35 + 0.033*SL	0.30 + 0.036*SL
D to Y	t_{PLH}	0.36	0.32 + 0.021*SL	0.32 + 0.018*SL	0.33 + 0.018*SL
	t_{PHL}	0.10	0.05 + 0.021*SL	0.06 + 0.017*SL	0.09 + 0.016*SL
	t_R	0.49	0.43 + 0.032*SL	0.41 + 0.036*SL	0.34 + 0.040*SL
	t_F	0.40	0.35 + 0.026*SL	0.32 + 0.034*SL	0.26 + 0.037*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OA211D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.51	0.48 + 0.014*SL	0.49 + 0.013*SL	0.49 + 0.013*SL
	tPHL	0.34	0.32 + 0.009*SL	0.33 + 0.008*SL	0.36 + 0.006*SL
	tR	0.14	0.08 + 0.028*SL	0.08 + 0.029*SL	0.06 + 0.030*SL
	tF	0.12	0.10 + 0.010*SL	0.10 + 0.012*SL	0.12 + 0.011*SL
B to Y	tPLH	0.48	0.45 + 0.014*SL	0.46 + 0.013*SL	0.46 + 0.013*SL
	tPHL	0.39	0.37 + 0.010*SL	0.38 + 0.007*SL	0.41 + 0.006*SL
	tR	0.15	0.09 + 0.029*SL	0.09 + 0.028*SL	0.06 + 0.030*SL
	tF	0.13	0.11 + 0.009*SL	0.11 + 0.011*SL	0.10 + 0.011*SL
C to Y	tPLH	0.48	0.45 + 0.015*SL	0.46 + 0.013*SL	0.46 + 0.013*SL
	tPHL	0.36	0.34 + 0.010*SL	0.35 + 0.008*SL	0.38 + 0.006*SL
	tR	0.15	0.09 + 0.030*SL	0.09 + 0.028*SL	0.06 + 0.030*SL
	tF	0.13	0.10 + 0.014*SL	0.11 + 0.011*SL	0.11 + 0.011*SL
D to Y	tPLH	0.52	0.49 + 0.014*SL	0.49 + 0.013*SL	0.50 + 0.013*SL
	tPHL	0.32	0.30 + 0.012*SL	0.31 + 0.008*SL	0.34 + 0.006*SL
	tR	0.14	0.10 + 0.024*SL	0.08 + 0.029*SL	0.07 + 0.030*SL
	tF	0.13	0.10 + 0.013*SL	0.11 + 0.011*SL	0.10 + 0.011*SL

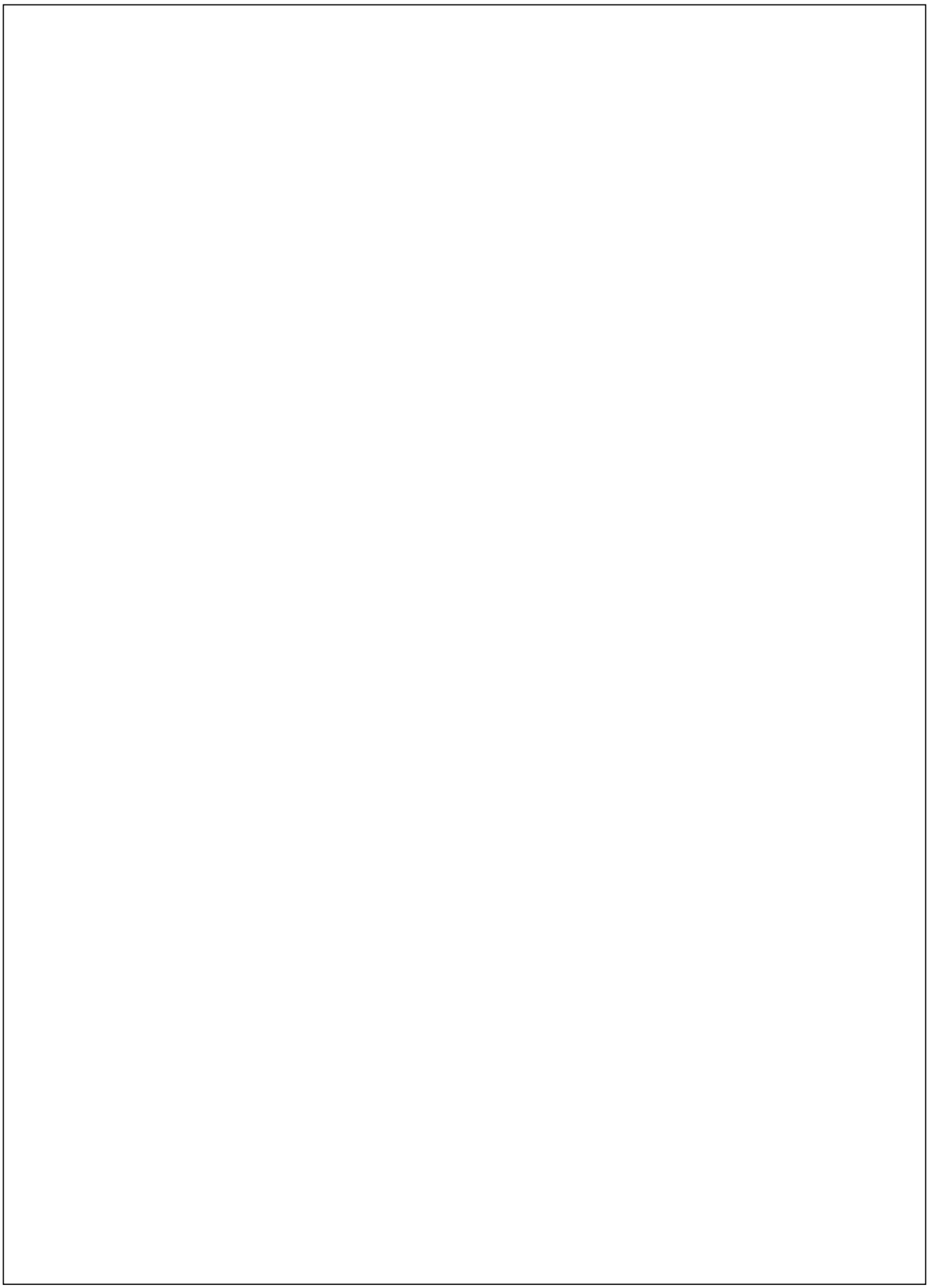
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OA211D7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.59	0.57 + 0.009*SL	0.58 + 0.006*SL	0.59 + 0.005*SL
	tPHL	0.45	0.44 + 0.006*SL	0.44 + 0.005*SL	0.47 + 0.004*SL
	tR	0.14	0.11 + 0.014*SL	0.11 + 0.012*SL	0.12 + 0.012*SL
	tF	0.20	0.19 + 0.007*SL	0.20 + 0.004*SL	0.19 + 0.005*SL
B to Y	tPLH	0.56	0.55 + 0.006*SL	0.55 + 0.006*SL	0.56 + 0.005*SL
	tPHL	0.51	0.49 + 0.008*SL	0.50 + 0.005*SL	0.52 + 0.003*SL
	tR	0.14	0.12 + 0.008*SL	0.11 + 0.013*SL	0.13 + 0.012*SL
	tF	0.19	0.18 + 0.005*SL	0.18 + 0.005*SL	0.21 + 0.004*SL
C to Y	tPLH	0.55	0.54 + 0.008*SL	0.54 + 0.006*SL	0.55 + 0.006*SL
	tPHL	0.47	0.45 + 0.008*SL	0.46 + 0.005*SL	0.49 + 0.004*SL
	tR	0.13	0.11 + 0.009*SL	0.11 + 0.012*SL	0.10 + 0.012*SL
	tF	0.20	0.20 + 0.002*SL	0.19 + 0.004*SL	0.19 + 0.005*SL
D to Y	tPLH	0.60	0.59 + 0.003*SL	0.58 + 0.006*SL	0.59 + 0.006*SL
	tPHL	0.43	0.42 + 0.007*SL	0.43 + 0.005*SL	0.45 + 0.004*SL
	tR	0.13	0.11 + 0.009*SL	0.10 + 0.013*SL	0.11 + 0.012*SL
	tF	0.20	0.20 + 0.000*SL	0.18 + 0.005*SL	0.20 + 0.004*SL

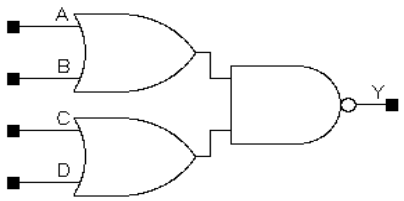
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D
Outputs: Y
Input Loading (SL):
- OA22: All : 1
- OA22D2: All : 2
- OA22D3: All: 1
- OA22D7: All: 1

Maximum Fanout (Rec. SL):
- OA22: 14
- OA22D2: 28
- OA22D3: 84
- OA22D7: 196

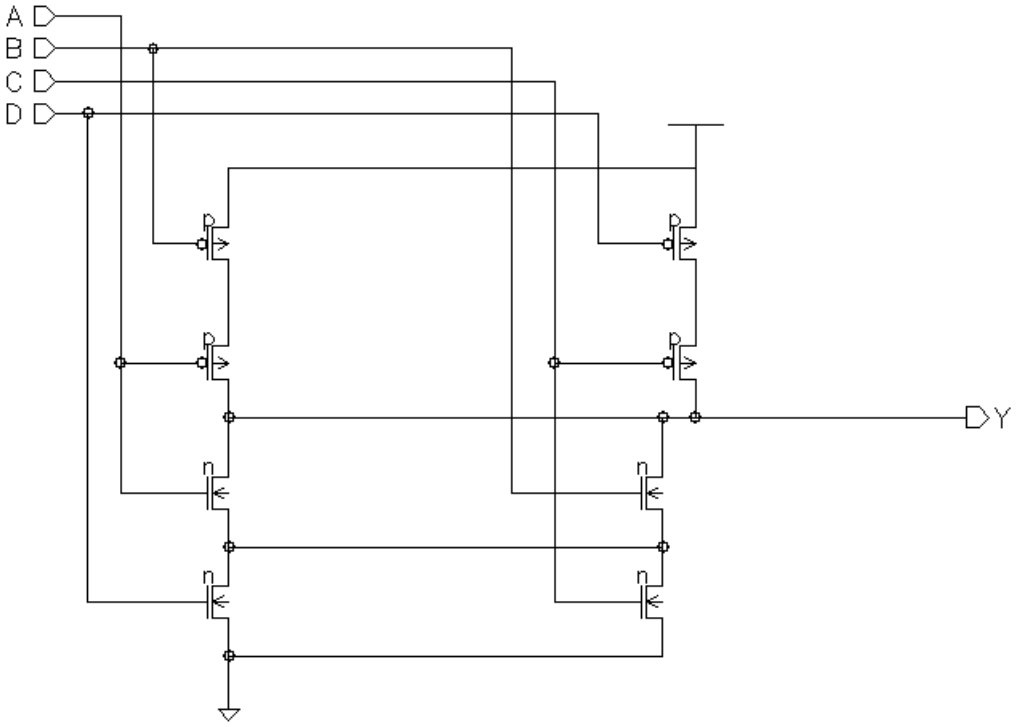
Gate Count:
- OA22: 2
- OA22D2: 4
- OA22D3: 4
- OA22D7: 6



Symbol

A	B	C	D	Y
0	0	x	x	1
x	x	0	0	1
1	x	x	1	0
x	1	x	1	0
1	x	1	x	0
x	1	1	x	0

Truth Table



Schematic

OA22 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.44	0.29 + 0.072*SL	0.30 + 0.069*SL	0.28 + 0.070*SL
	tPHL	0.08	-0.01 + 0.047*SL	0.05 + 0.026*SL	0.15 + 0.021*SL
	tR	0.61	0.32 + 0.144*SL	0.27 + 0.161*SL	0.19 + 0.165*SL
	tF	0.34	0.25 + 0.047*SL	0.26 + 0.041*SL	0.21 + 0.044*SL
B to Y	tPLH	0.40	0.27 + 0.069*SL	0.27 + 0.069*SL	0.24 + 0.070*SL
	tPHL	0.11	0.02 + 0.043*SL	0.07 + 0.026*SL	0.17 + 0.021*SL
	tR	0.61	0.32 + 0.145*SL	0.28 + 0.161*SL	0.19 + 0.165*SL
	tF	0.38	0.29 + 0.044*SL	0.31 + 0.040*SL	0.23 + 0.043*SL
C to Y	tPLH	0.55	0.42 + 0.068*SL	0.41 + 0.069*SL	0.39 + 0.070*SL
	tPHL	0.08	0.00 + 0.041*SL	0.05 + 0.024*SL	0.13 + 0.020*SL
	tR	0.75	0.45 + 0.155*SL	0.42 + 0.162*SL	0.35 + 0.165*SL
	tF	0.36	0.27 + 0.042*SL	0.28 + 0.040*SL	0.21 + 0.043*SL
D to Y	tPLH	0.52	0.38 + 0.067*SL	0.38 + 0.069*SL	0.35 + 0.070*SL
	tPHL	0.10	0.03 + 0.037*SL	0.07 + 0.023*SL	0.14 + 0.020*SL
	tR	0.76	0.45 + 0.150*SL	0.42 + 0.162*SL	0.35 + 0.165*SL
	tF	0.39	0.31 + 0.036*SL	0.31 + 0.039*SL	0.24 + 0.042*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

OA22D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.37	0.29 + 0.040*SL	0.30 + 0.035*SL	0.29 + 0.036*SL
	tPHL	0.03	-0.03 + 0.029*SL	0.01 + 0.017*SL	0.12 + 0.012*SL
	tR	0.47	0.30 + 0.083*SL	0.31 + 0.080*SL	0.23 + 0.084*SL
	tF	0.29	0.23 + 0.030*SL	0.26 + 0.021*SL	0.25 + 0.022*SL
B to Y	tPLH	0.34	0.26 + 0.037*SL	0.27 + 0.035*SL	0.25 + 0.036*SL
	tPHL	0.07	0.02 + 0.025*SL	0.04 + 0.016*SL	0.13 + 0.011*SL
	tR	0.48	0.33 + 0.074*SL	0.31 + 0.080*SL	0.23 + 0.084*SL
	tF	0.34	0.30 + 0.024*SL	0.31 + 0.020*SL	0.29 + 0.021*SL
C to Y	tPLH	0.49	0.42 + 0.035*SL	0.42 + 0.035*SL	0.41 + 0.036*SL
	tPHL	0.04	-0.00 + 0.023*SL	0.02 + 0.015*SL	0.10 + 0.011*SL
	tR	0.62	0.47 + 0.073*SL	0.45 + 0.081*SL	0.39 + 0.084*SL
	tF	0.31	0.27 + 0.024*SL	0.28 + 0.020*SL	0.25 + 0.021*SL
D to Y	tPLH	0.46	0.39 + 0.035*SL	0.39 + 0.035*SL	0.37 + 0.036*SL
	tPHL	0.07	0.02 + 0.022*SL	0.05 + 0.014*SL	0.12 + 0.011*SL
	tR	0.62	0.48 + 0.075*SL	0.46 + 0.081*SL	0.40 + 0.084*SL
	tF	0.36	0.32 + 0.021*SL	0.32 + 0.019*SL	0.29 + 0.021*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

OA22D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.51	0.49 + 0.014*SL	0.49 + 0.013*SL	0.49 + 0.013*SL
	tPHL	0.23	0.21 + 0.010*SL	0.22 + 0.007*SL	0.25 + 0.006*SL
	tR	0.14	0.09 + 0.027*SL	0.08 + 0.029*SL	0.06 + 0.030*SL
	tF	0.12	0.09 + 0.012*SL	0.10 + 0.011*SL	0.09 + 0.011*SL
B to Y	tPLH	0.48	0.46 + 0.014*SL	0.46 + 0.013*SL	0.46 + 0.013*SL
	tPHL	0.27	0.25 + 0.011*SL	0.26 + 0.007*SL	0.29 + 0.006*SL
	tR	0.14	0.09 + 0.028*SL	0.08 + 0.029*SL	0.06 + 0.030*SL
	tF	0.12	0.10 + 0.012*SL	0.10 + 0.011*SL	0.09 + 0.011*SL
C to Y	tPLH	0.64	0.62 + 0.014*SL	0.62 + 0.013*SL	0.62 + 0.013*SL
	tPHL	0.26	0.24 + 0.008*SL	0.24 + 0.007*SL	0.27 + 0.006*SL
	tR	0.15	0.09 + 0.027*SL	0.09 + 0.029*SL	0.06 + 0.030*SL
	tF	0.13	0.11 + 0.009*SL	0.10 + 0.010*SL	0.09 + 0.011*SL
D to Y	tPLH	0.61	0.57 + 0.015*SL	0.58 + 0.013*SL	0.59 + 0.012*SL
	tPHL	0.29	0.26 + 0.012*SL	0.28 + 0.007*SL	0.31 + 0.006*SL
	tR	0.15	0.09 + 0.031*SL	0.10 + 0.028*SL	0.07 + 0.030*SL
	tF	0.12	0.10 + 0.011*SL	0.10 + 0.011*SL	0.11 + 0.011*SL

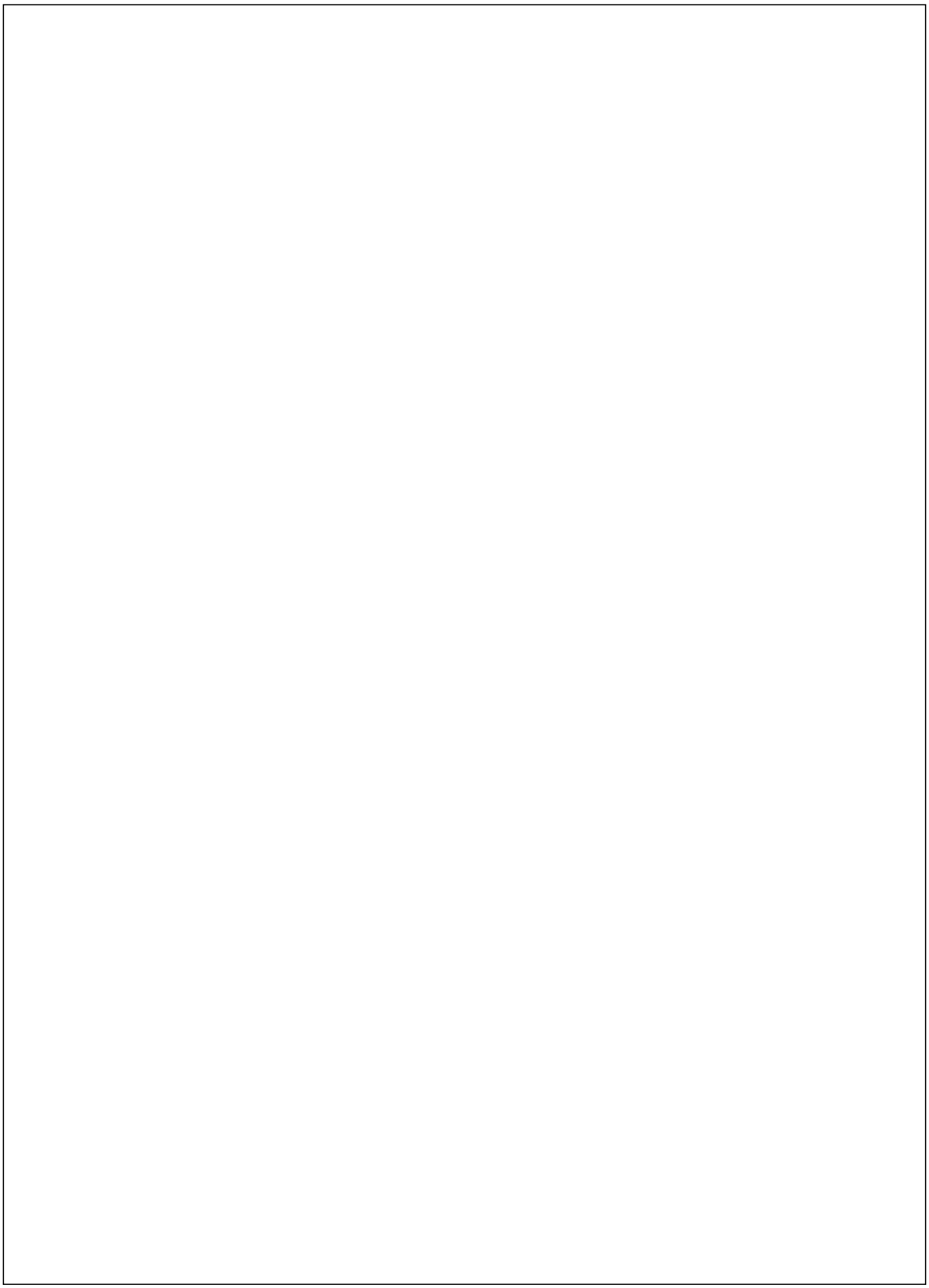
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OA22D7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.59	0.57 + 0.009*SL	0.58 + 0.006*SL	0.59 + 0.005*SL
	tPHL	0.34	0.33 + 0.006*SL	0.33 + 0.005*SL	0.35 + 0.004*SL
	tR	0.14	0.10 + 0.016*SL	0.12 + 0.012*SL	0.11 + 0.012*SL
	tF	0.18	0.16 + 0.011*SL	0.18 + 0.005*SL	0.18 + 0.005*SL
B to Y	tPLH	0.57	0.55 + 0.008*SL	0.56 + 0.006*SL	0.56 + 0.006*SL
	tPHL	0.38	0.37 + 0.006*SL	0.37 + 0.005*SL	0.40 + 0.003*SL
	tR	0.13	0.10 + 0.015*SL	0.11 + 0.013*SL	0.13 + 0.012*SL
	tF	0.19	0.18 + 0.003*SL	0.18 + 0.005*SL	0.17 + 0.005*SL
C to Y	tPLH	0.73	0.72 + 0.005*SL	0.72 + 0.006*SL	0.73 + 0.006*SL
	tPHL	0.37	0.35 + 0.008*SL	0.36 + 0.005*SL	0.39 + 0.004*SL
	tR	0.15	0.13 + 0.011*SL	0.12 + 0.012*SL	0.11 + 0.012*SL
	tF	0.19	0.19 + 0.003*SL	0.18 + 0.005*SL	0.18 + 0.005*SL
D to Y	tPLH	0.70	0.69 + 0.007*SL	0.69 + 0.006*SL	0.70 + 0.006*SL
	tPHL	0.40	0.39 + 0.006*SL	0.39 + 0.005*SL	0.42 + 0.003*SL
	tR	0.15	0.11 + 0.016*SL	0.13 + 0.012*SL	0.12 + 0.012*SL
	tF	0.19	0.18 + 0.006*SL	0.18 + 0.005*SL	0.20 + 0.004*SL

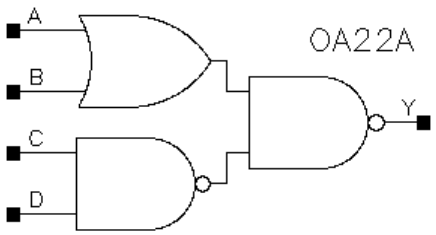
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D
Output: Y
Input Loading (SL):
- OA22A: All : 1
- OA22D2A: A,B : 2
  C,D : 1

Maximum Fanout (Rec. SL):
- OA22A: 14
- OA22D2A: 28

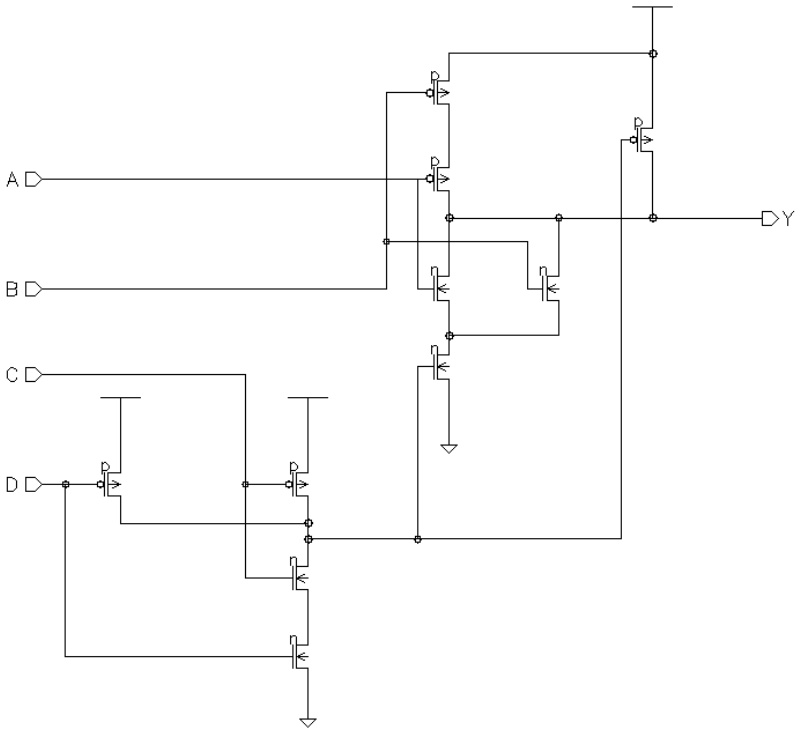
Gate Count:
- OA22A: 3
- OA22D2A: 4



Symbol

A	B	C	D	Y
0	0	x	x	1
x	x	1	1	1
1	x	0	x	0
1	x	x	0	0
x	1	0	x	0
x	1	x	0	0

Truth Table



Schematic

OA22A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.43	0.28 + 0.074*SL	0.29 + 0.069*SL	0.27 + 0.070*SL
	tPHL	0.12	0.01 + 0.052*SL	0.08 + 0.031*SL	0.16 + 0.027*SL
	tR	0.62	0.33 + 0.144*SL	0.28 + 0.161*SL	0.19 + 0.165*SL
	tF	0.38	0.28 + 0.053*SL	0.27 + 0.056*SL	0.20 + 0.059*SL
B to Y	tPLH	0.40	0.25 + 0.071*SL	0.26 + 0.069*SL	0.24 + 0.070*SL
	tPHL	0.15	0.05 + 0.048*SL	0.11 + 0.030*SL	0.18 + 0.027*SL
	tR	0.62	0.33 + 0.143*SL	0.28 + 0.161*SL	0.19 + 0.165*SL
	tF	0.43	0.32 + 0.054*SL	0.32 + 0.055*SL	0.24 + 0.059*SL
C to Y	tPLH	0.28	0.20 + 0.040*SL	0.21 + 0.038*SL	0.21 + 0.038*SL
	tPHL	0.33	0.28 + 0.026*SL	0.29 + 0.020*SL	0.30 + 0.020*SL
	tR	0.37	0.20 + 0.085*SL	0.20 + 0.087*SL	0.17 + 0.088*SL
	tF	0.21	0.13 + 0.040*SL	0.12 + 0.044*SL	0.09 + 0.046*SL
D to Y	tPLH	0.26	0.18 + 0.039*SL	0.18 + 0.038*SL	0.18 + 0.038*SL
	tPHL	0.39	0.34 + 0.023*SL	0.35 + 0.020*SL	0.36 + 0.020*SL
	tR	0.38	0.20 + 0.086*SL	0.20 + 0.086*SL	0.17 + 0.088*SL
	tF	0.23	0.15 + 0.038*SL	0.13 + 0.044*SL	0.09 + 0.046*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OA22D2A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

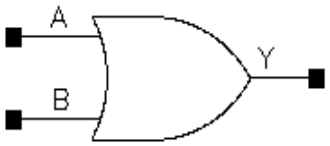
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.36	0.28 + 0.040*SL	0.29 + 0.035*SL	0.29 + 0.036*SL
	tPHL	0.06	-0.00 + 0.032*SL	0.04 + 0.019*SL	0.13 + 0.014*SL
	tR	0.48	0.33 + 0.076*SL	0.32 + 0.079*SL	0.23 + 0.084*SL
	tF	0.32	0.25 + 0.036*SL	0.28 + 0.027*SL	0.26 + 0.027*SL
B to Y	tPLH	0.33	0.25 + 0.038*SL	0.26 + 0.035*SL	0.25 + 0.036*SL
	tPHL	0.10	0.04 + 0.027*SL	0.07 + 0.018*SL	0.15 + 0.014*SL
	tR	0.48	0.33 + 0.074*SL	0.32 + 0.080*SL	0.24 + 0.084*SL
	tF	0.38	0.32 + 0.029*SL	0.33 + 0.025*SL	0.30 + 0.027*SL
C to Y	tPLH	0.29	0.25 + 0.020*SL	0.25 + 0.018*SL	0.26 + 0.018*SL
	tPHL	0.36	0.33 + 0.017*SL	0.34 + 0.010*SL	0.35 + 0.010*SL
	tR	0.28	0.20 + 0.040*SL	0.20 + 0.041*SL	0.19 + 0.042*SL
	tF	0.20	0.15 + 0.025*SL	0.16 + 0.020*SL	0.13 + 0.021*SL
D to Y	tPLH	0.25	0.21 + 0.019*SL	0.22 + 0.018*SL	0.22 + 0.018*SL
	tPHL	0.41	0.38 + 0.013*SL	0.38 + 0.011*SL	0.41 + 0.010*SL
	tR	0.29	0.22 + 0.040*SL	0.21 + 0.040*SL	0.18 + 0.042*SL
	tF	0.20	0.19 + 0.010*SL	0.15 + 0.020*SL	0.14 + 0.021*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: A, B
Output: Y
Input Loading (SL):
- OR2D2:All : 1
- OR2D4 All: 1
- OR2D8: All: 2

Maximum Fanout (Rec. SL):
- OR2D2: 56
- OR2D4: 112
- OR2D8: 224

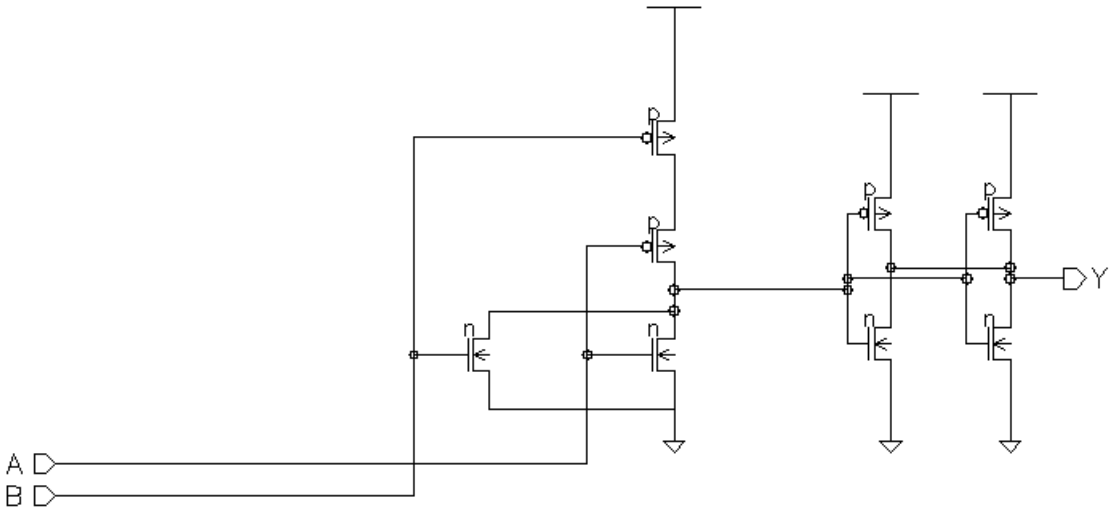
Gate Count:
- OR2D2: 2
- OR2D4: 3
- OR2D8: 6



Symbol

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Truth Table



Schematic

OR2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.13	0.09 + 0.022*SL	0.10 + 0.019*SL	0.10 + 0.019*SL
	t_{PHL}	0.45	0.42 + 0.013*SL	0.43 + 0.011*SL	0.47 + 0.009*SL
	t_R	0.18	0.09 + 0.048*SL	0.10 + 0.044*SL	0.07 + 0.045*SL
	t_F	0.18	0.14 + 0.021*SL	0.15 + 0.016*SL	0.14 + 0.017*SL
B to Y	t_{PLH}	0.16	0.12 + 0.022*SL	0.13 + 0.019*SL	0.13 + 0.019*SL
	t_{PHL}	0.41	0.38 + 0.018*SL	0.40 + 0.012*SL	0.46 + 0.009*SL
	t_R	0.18	0.10 + 0.042*SL	0.09 + 0.044*SL	0.07 + 0.045*SL
	t_F	0.17	0.12 + 0.025*SL	0.15 + 0.016*SL	0.14 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OR2D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.19	0.16 + 0.012*SL	0.17 + 0.010*SL	0.18 + 0.009*SL
	t_{PHL}	0.54	0.51 + 0.014*SL	0.53 + 0.008*SL	0.57 + 0.006*SL
	t_R	0.16	0.12 + 0.019*SL	0.12 + 0.021*SL	0.10 + 0.022*SL
	t_F	0.23	0.22 + 0.004*SL	0.21 + 0.008*SL	0.21 + 0.008*SL
B to Y	t_{PLH}	0.22	0.19 + 0.011*SL	0.20 + 0.010*SL	0.20 + 0.009*SL
	t_{PHL}	0.50	0.48 + 0.013*SL	0.49 + 0.008*SL	0.54 + 0.006*SL
	t_R	0.16	0.12 + 0.017*SL	0.11 + 0.022*SL	0.11 + 0.022*SL
	t_F	0.23	0.21 + 0.008*SL	0.21 + 0.008*SL	0.21 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

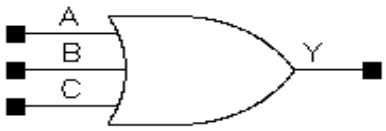
OR2D8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.18	0.16 + 0.006*SL	0.17 + 0.005*SL	0.17 + 0.005*SL
	t_{PHL}	0.56	0.54 + 0.007*SL	0.55 + 0.005*SL	0.57 + 0.003*SL
	t_R	0.13	0.10 + 0.015*SL	0.12 + 0.010*SL	0.11 + 0.011*SL
	t_F	0.22	0.21 + 0.006*SL	0.21 + 0.005*SL	0.23 + 0.004*SL
B to Y	t_{PLH}	0.20	0.19 + 0.006*SL	0.19 + 0.005*SL	0.21 + 0.005*SL
	t_{PHL}	0.51	0.50 + 0.006*SL	0.50 + 0.005*SL	0.53 + 0.004*SL
	t_R	0.14	0.12 + 0.010*SL	0.11 + 0.011*SL	0.11 + 0.011*SL
	t_F	0.23	0.23 + 0.002*SL	0.23 + 0.004*SL	0.21 + 0.004*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

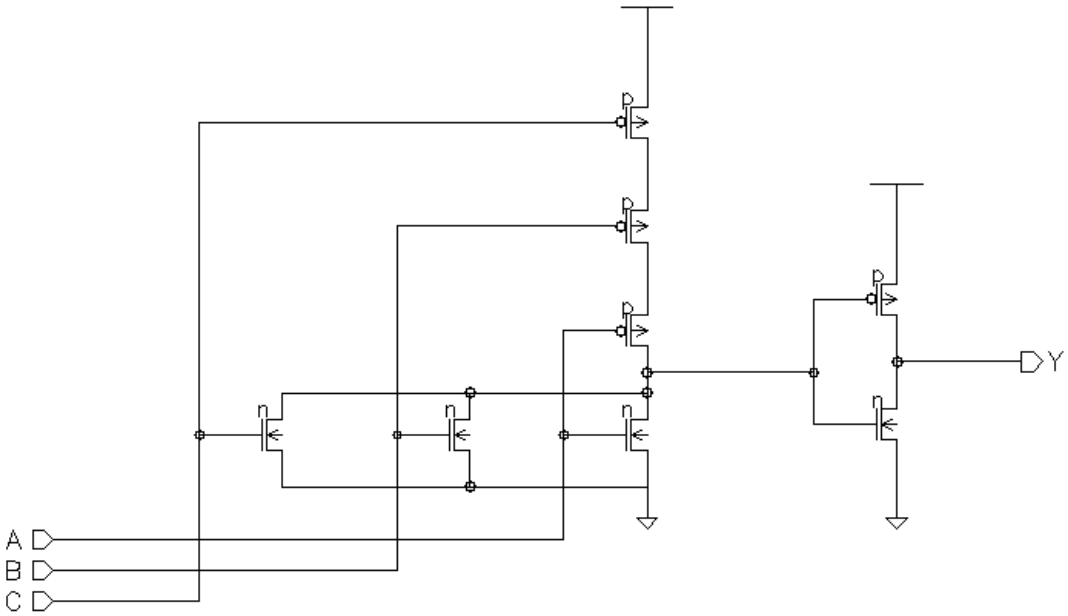
Inputs: A, B, C
Output: Y
Input Loading (SL):
‘ - OR3: All : 1
- OR3D2: All : 1
- OR3D6: All: 2
- OR3D8: All: 2
Maximum Fanout (Rec. SL):
- OR3: 28
- OR3D2: 84
- OR3D6: 168
- OR3D8: 224
Gate Count:
- OR3: 2
- OR3D2: 3
- OR3D6: 6
- OR3D8: 8



Symbol

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Truth Table



Schematic

OR3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.13	0.05 + 0.038*SL	0.05 + 0.038*SL	0.06 + 0.038*SL
	tPHL	0.50	0.44 + 0.032*SL	0.48 + 0.020*SL	0.54 + 0.017*SL
	tR	0.26	0.10 + 0.078*SL	0.08 + 0.087*SL	0.06 + 0.088*SL
	tF	0.22	0.13 + 0.043*SL	0.17 + 0.031*SL	0.15 + 0.032*SL
B to Y	tPLH	0.16	0.08 + 0.038*SL	0.09 + 0.038*SL	0.09 + 0.038*SL
	tPHL	0.51	0.44 + 0.033*SL	0.48 + 0.020*SL	0.55 + 0.017*SL
	tR	0.26	0.09 + 0.084*SL	0.08 + 0.087*SL	0.06 + 0.088*SL
	tF	0.23	0.15 + 0.038*SL	0.17 + 0.031*SL	0.15 + 0.032*SL
C to Y	tPLH	0.17	0.09 + 0.040*SL	0.10 + 0.038*SL	0.10 + 0.038*SL
	tPHL	0.48	0.42 + 0.032*SL	0.45 + 0.021*SL	0.53 + 0.017*SL
	tR	0.27	0.10 + 0.085*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
	tF	0.22	0.15 + 0.037*SL	0.17 + 0.031*SL	0.15 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OR3D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.16	0.13 + 0.015*SL	0.14 + 0.013*SL	0.15 + 0.013*SL
	tPHL	0.62	0.59 + 0.017*SL	0.61 + 0.011*SL	0.67 + 0.008*SL
	tR	0.16	0.11 + 0.026*SL	0.10 + 0.029*SL	0.08 + 0.029*SL
	tF	0.26	0.24 + 0.012*SL	0.24 + 0.011*SL	0.25 + 0.011*SL
B to Y	tPLH	0.19	0.16 + 0.013*SL	0.16 + 0.013*SL	0.17 + 0.013*SL
	tPHL	0.62	0.58 + 0.020*SL	0.61 + 0.011*SL	0.67 + 0.008*SL
	tR	0.17	0.11 + 0.030*SL	0.11 + 0.028*SL	0.09 + 0.029*SL
	tF	0.27	0.24 + 0.017*SL	0.25 + 0.011*SL	0.25 + 0.011*SL
C to Y	tPLH	0.20	0.17 + 0.013*SL	0.17 + 0.013*SL	0.18 + 0.012*SL
	tPHL	0.60	0.56 + 0.019*SL	0.59 + 0.011*SL	0.65 + 0.008*SL
	tR	0.17	0.12 + 0.028*SL	0.12 + 0.028*SL	0.09 + 0.029*SL
	tF	0.26	0.24 + 0.014*SL	0.24 + 0.011*SL	0.25 + 0.011*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OR3D6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.14	0.13 + 0.008*SL	0.13 + 0.007*SL	0.14 + 0.006*SL
	tPHL	0.62	0.60 + 0.010*SL	0.61 + 0.007*SL	0.65 + 0.005*SL
	tR	0.14	0.11 + 0.014*SL	0.11 + 0.014*SL	0.11 + 0.014*SL
	tF	0.25	0.24 + 0.006*SL	0.24 + 0.007*SL	0.26 + 0.006*SL
B to Y	tPLH	0.17	0.16 + 0.008*SL	0.16 + 0.007*SL	0.17 + 0.006*SL
	tPHL	0.61	0.59 + 0.012*SL	0.61 + 0.007*SL	0.65 + 0.005*SL
	tR	0.14	0.10 + 0.017*SL	0.12 + 0.014*SL	0.10 + 0.015*SL
	tF	0.26	0.25 + 0.007*SL	0.25 + 0.006*SL	0.27 + 0.005*SL
C to Y	tPLH	0.19	0.17 + 0.009*SL	0.18 + 0.007*SL	0.18 + 0.006*SL
	tPHL	0.60	0.58 + 0.010*SL	0.59 + 0.007*SL	0.63 + 0.005*SL
	tR	0.14	0.10 + 0.022*SL	0.12 + 0.014*SL	0.11 + 0.014*SL
	tF	0.26	0.25 + 0.006*SL	0.24 + 0.006*SL	0.26 + 0.006*SL

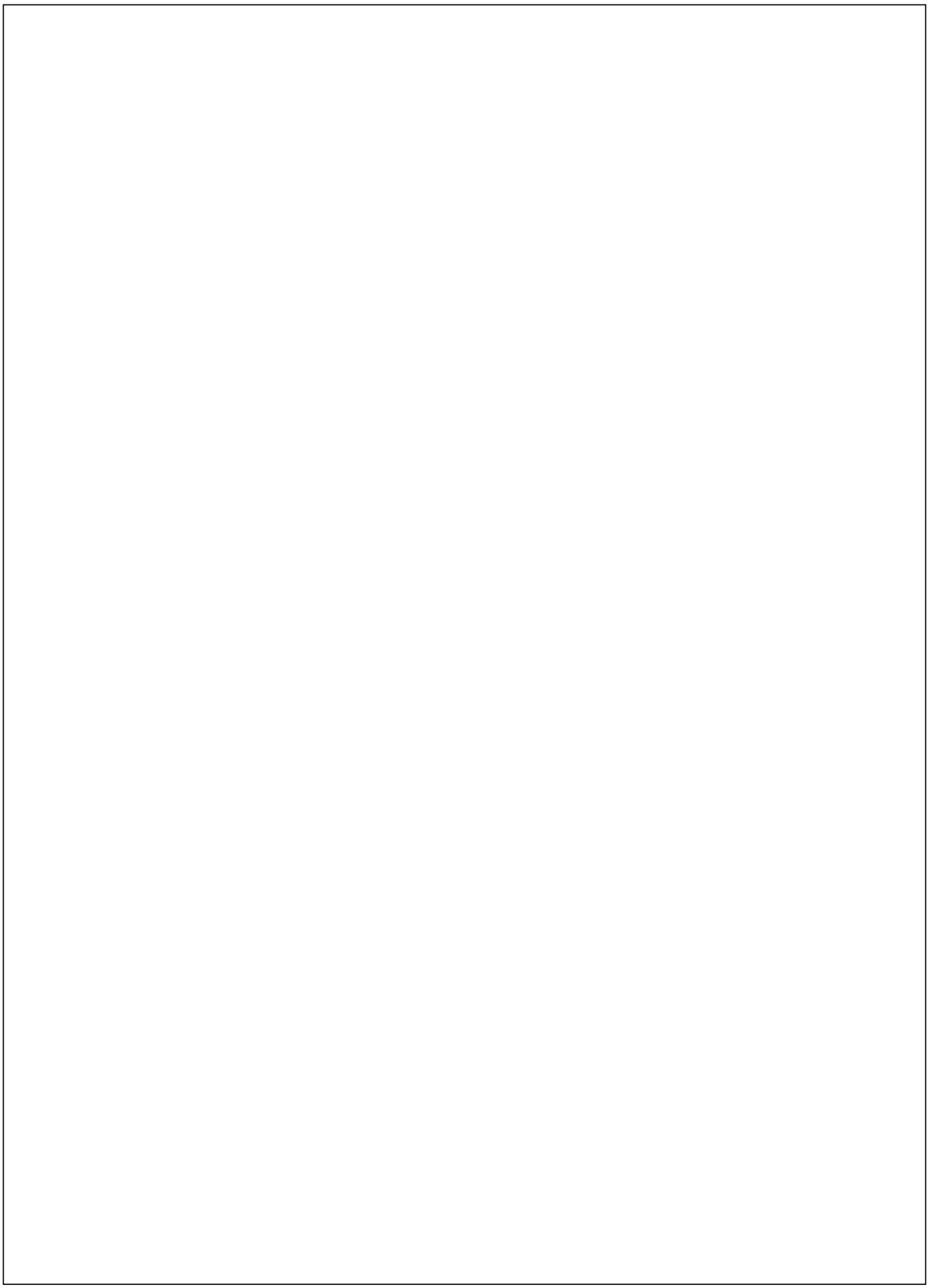
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OR3D8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

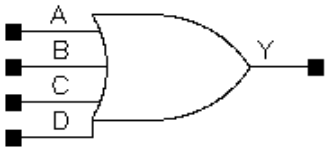
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.18	0.17 + 0.005*SL	0.17 + 0.005*SL	0.18 + 0.005*SL
	tPHL	0.70	0.68 + 0.007*SL	0.69 + 0.006*SL	0.71 + 0.004*SL
	tR	0.13	0.11 + 0.013*SL	0.12 + 0.010*SL	0.11 + 0.011*SL
	tF	0.31	0.29 + 0.006*SL	0.30 + 0.005*SL	0.30 + 0.004*SL
B to Y	tPLH	0.20	0.19 + 0.005*SL	0.19 + 0.005*SL	0.20 + 0.005*SL
	tPHL	0.69	0.68 + 0.008*SL	0.68 + 0.006*SL	0.71 + 0.004*SL
	tR	0.13	0.11 + 0.012*SL	0.11 + 0.011*SL	0.13 + 0.010*SL
	tF	0.30	0.30 + 0.001*SL	0.29 + 0.005*SL	0.30 + 0.005*SL
C to Y	tPLH	0.21	0.20 + 0.006*SL	0.21 + 0.005*SL	0.21 + 0.005*SL
	tPHL	0.68	0.66 + 0.007*SL	0.67 + 0.006*SL	0.69 + 0.004*SL
	tR	0.14	0.11 + 0.016*SL	0.13 + 0.010*SL	0.11 + 0.011*SL
	tF	0.31	0.29 + 0.005*SL	0.30 + 0.005*SL	0.30 + 0.005*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D
Output: YAll: 1
Input Loading (SL): All: 1
Maximum Fanout (Rec. SL):
- OR4: 28
- OR4D2: 56
- OR4D5: 140
- OR4D7:196

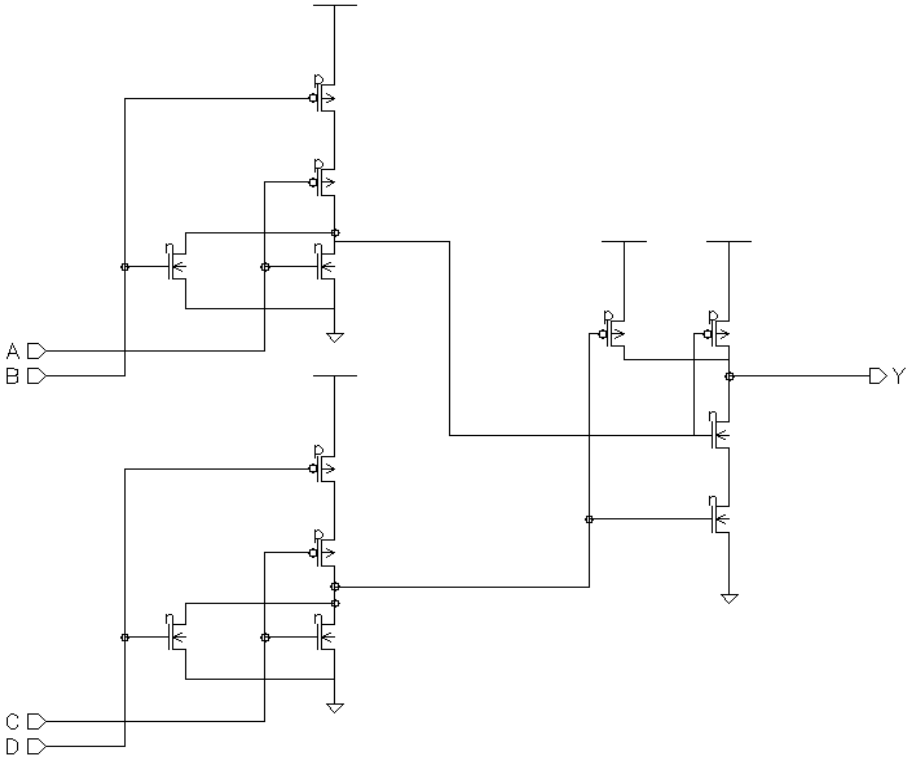
Gate Count:
- OR4: 3
- OR4D2: 4
- OR4D5: 6
- OR4D7: 7



Symbol

A	B	C	D	Y
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

Truth Table



Schematic

OR4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.13	0.05 + 0.041*SL	0.06 + 0.036*SL	0.06 + 0.036*SL
	t_{PHL}	0.45	0.39 + 0.034*SL	0.41 + 0.027*SL	0.43 + 0.026*SL
	t_R	0.27	0.10 + 0.083*SL	0.10 + 0.083*SL	0.07 + 0.084*SL
	t_F	0.24	0.12 + 0.059*SL	0.14 + 0.054*SL	0.10 + 0.057*SL
B to Y	t_{PLH}	0.17	0.09 + 0.039*SL	0.10 + 0.036*SL	0.09 + 0.036*SL
	t_{PHL}	0.43	0.36 + 0.035*SL	0.38 + 0.027*SL	0.41 + 0.026*SL
	t_R	0.27	0.13 + 0.072*SL	0.10 + 0.083*SL	0.07 + 0.084*SL
	t_F	0.25	0.13 + 0.058*SL	0.15 + 0.054*SL	0.09 + 0.057*SL
C to Y	t_{PLH}	0.16	0.08 + 0.038*SL	0.08 + 0.038*SL	0.09 + 0.037*SL
	t_{PHL}	0.44	0.39 + 0.029*SL	0.39 + 0.026*SL	0.41 + 0.026*SL
	t_R	0.32	0.15 + 0.081*SL	0.14 + 0.085*SL	0.12 + 0.086*SL
	t_F	0.22	0.12 + 0.050*SL	0.10 + 0.056*SL	0.09 + 0.057*SL
D to Y	t_{PLH}	0.19	0.11 + 0.042*SL	0.12 + 0.037*SL	0.12 + 0.037*SL
	t_{PHL}	0.42	0.36 + 0.031*SL	0.37 + 0.026*SL	0.38 + 0.026*SL
	t_R	0.32	0.15 + 0.083*SL	0.14 + 0.085*SL	0.12 + 0.086*SL
	t_F	0.23	0.14 + 0.048*SL	0.12 + 0.055*SL	0.08 + 0.057*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OR4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.13	0.09 + 0.020*SL	0.10 + 0.018*SL	0.10 + 0.018*SL
	t_{PHL}	0.49	0.44 + 0.021*SL	0.46 + 0.015*SL	0.50 + 0.013*SL
	t_R	0.19	0.12 + 0.036*SL	0.11 + 0.041*SL	0.08 + 0.042*SL
	t_F	0.21	0.16 + 0.029*SL	0.16 + 0.028*SL	0.14 + 0.029*SL
B to Y	t_{PLH}	0.16	0.12 + 0.020*SL	0.12 + 0.019*SL	0.15 + 0.018*SL
	t_{PHL}	0.46	0.41 + 0.022*SL	0.43 + 0.015*SL	0.47 + 0.013*SL
	t_R	0.19	0.12 + 0.036*SL	0.10 + 0.041*SL	0.08 + 0.042*SL
	t_F	0.22	0.16 + 0.031*SL	0.17 + 0.027*SL	0.14 + 0.029*SL
C to Y	t_{PLH}	0.15	0.11 + 0.020*SL	0.12 + 0.018*SL	0.12 + 0.018*SL
	t_{PHL}	0.48	0.44 + 0.019*SL	0.45 + 0.015*SL	0.48 + 0.013*SL
	t_R	0.24	0.17 + 0.037*SL	0.16 + 0.040*SL	0.13 + 0.042*SL
	t_F	0.20	0.15 + 0.026*SL	0.14 + 0.028*SL	0.13 + 0.029*SL
D to Y	t_{PLH}	0.19	0.15 + 0.019*SL	0.15 + 0.018*SL	0.15 + 0.018*SL
	t_{PHL}	0.44	0.41 + 0.019*SL	0.42 + 0.015*SL	0.45 + 0.013*SL
	t_R	0.24	0.18 + 0.035*SL	0.16 + 0.040*SL	0.13 + 0.042*SL
	t_F	0.21	0.16 + 0.026*SL	0.15 + 0.028*SL	0.12 + 0.029*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OR4D5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.30	0.28 + 0.009*SL	0.29 + 0.008*SL	0.30 + 0.007*SL
	tPHL	0.65	0.64 + 0.006*SL	0.64 + 0.006*SL	0.67 + 0.004*SL
	tR	0.13	0.09 + 0.019*SL	0.10 + 0.017*SL	0.08 + 0.018*SL
	tF	0.14	0.13 + 0.006*SL	0.13 + 0.007*SL	0.15 + 0.006*SL
B to Y	tPLH	0.34	0.32 + 0.009*SL	0.32 + 0.008*SL	0.33 + 0.008*SL
	tPHL	0.62	0.61 + 0.008*SL	0.61 + 0.006*SL	0.64 + 0.004*SL
	tR	0.13	0.09 + 0.020*SL	0.09 + 0.017*SL	0.09 + 0.017*SL
	tF	0.15	0.13 + 0.006*SL	0.13 + 0.007*SL	0.15 + 0.006*SL
C to Y	tPLH	0.27	0.25 + 0.010*SL	0.26 + 0.008*SL	0.27 + 0.008*SL
	tPHL	0.65	0.64 + 0.006*SL	0.64 + 0.006*SL	0.68 + 0.004*SL
	tR	0.13	0.10 + 0.015*SL	0.09 + 0.017*SL	0.09 + 0.017*SL
	tF	0.14	0.13 + 0.006*SL	0.12 + 0.007*SL	0.15 + 0.006*SL
D to Y	tPLH	0.31	0.30 + 0.007*SL	0.29 + 0.008*SL	0.31 + 0.007*SL
	tPHL	0.62	0.61 + 0.008*SL	0.62 + 0.006*SL	0.64 + 0.004*SL
	tR	0.13	0.08 + 0.026*SL	0.10 + 0.016*SL	0.08 + 0.017*SL
	tF	0.14	0.12 + 0.008*SL	0.13 + 0.007*SL	0.14 + 0.006*SL

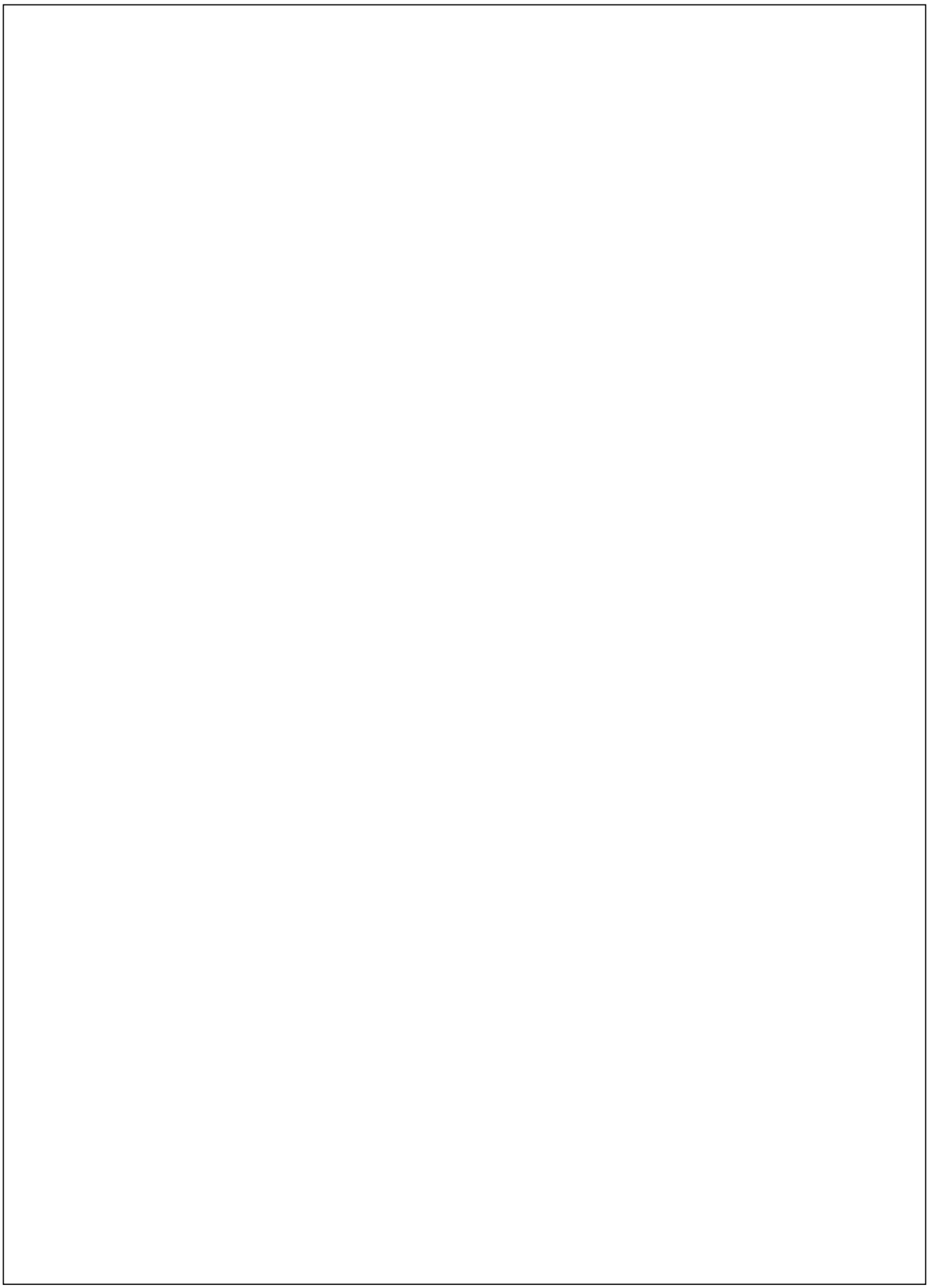
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OR4D7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

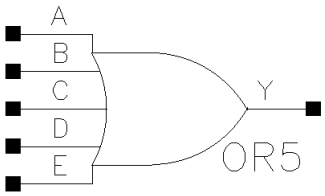
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.34	0.33 + 0.007*SL	0.33 + 0.006*SL	0.34 + 0.005*SL
	tPHL	0.70	0.69 + 0.005*SL	0.69 + 0.005*SL	0.71 + 0.004*SL
	tR	0.14	0.11 + 0.011*SL	0.11 + 0.012*SL	0.11 + 0.012*SL
	tF	0.18	0.18 + 0.002*SL	0.17 + 0.005*SL	0.18 + 0.005*SL
B to Y	tPLH	0.37	0.36 + 0.008*SL	0.36 + 0.006*SL	0.37 + 0.005*SL
	tPHL	0.67	0.66 + 0.007*SL	0.67 + 0.005*SL	0.69 + 0.003*SL
	tR	0.13	0.11 + 0.012*SL	0.11 + 0.012*SL	0.10 + 0.012*SL
	tF	0.18	0.17 + 0.005*SL	0.17 + 0.005*SL	0.18 + 0.005*SL
C to Y	tPLH	0.31	0.29 + 0.006*SL	0.30 + 0.006*SL	0.31 + 0.005*SL
	tPHL	0.70	0.68 + 0.007*SL	0.69 + 0.005*SL	0.72 + 0.004*SL
	tR	0.13	0.10 + 0.011*SL	0.10 + 0.013*SL	0.12 + 0.012*SL
	tF	0.19	0.18 + 0.006*SL	0.18 + 0.004*SL	0.18 + 0.005*SL
D to Y	tPLH	0.35	0.33 + 0.007*SL	0.33 + 0.006*SL	0.34 + 0.006*SL
	tPHL	0.67	0.66 + 0.006*SL	0.67 + 0.005*SL	0.69 + 0.004*SL
	tR	0.14	0.12 + 0.013*SL	0.12 + 0.012*SL	0.11 + 0.012*SL
	tF	0.18	0.18 + -0.001*SL	0.16 + 0.006*SL	0.18 + 0.005*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C, D, E
Output: Y
Input Loading (SL): All: 1
Maximum Fanout (Rec. SL):
- OR5: 28
- OR5D2: 56

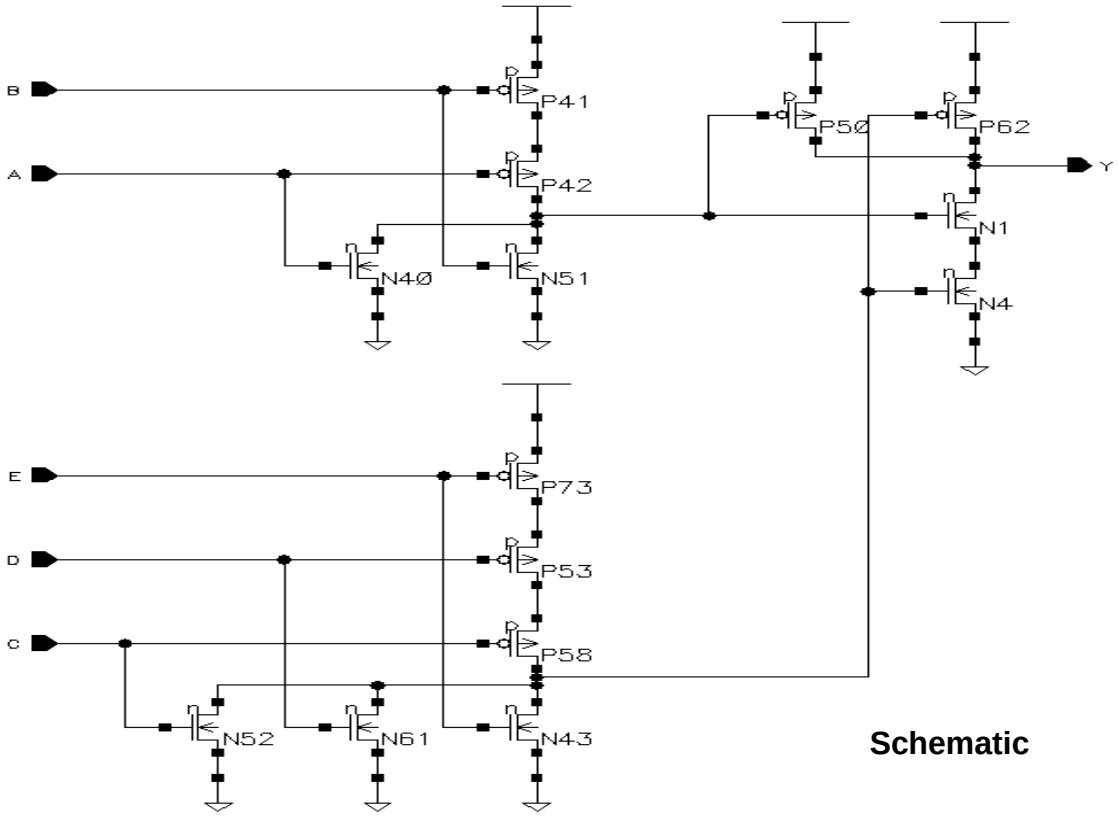
Gate Count:
- OR5: 4
- OR5D2: 5



Symbol

A	B	C	D	E	Y
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

Truth Table



Schematic

OR5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.13	0.05 + 0.041*SL	0.06 + 0.038*SL	0.06 + 0.038*SL
	tPHL	0.45	0.38 + 0.034*SL	0.40 + 0.027*SL	0.42 + 0.026*SL
	tR	0.27	0.10 + 0.084*SL	0.09 + 0.087*SL	0.07 + 0.088*SL
	tF	0.24	0.13 + 0.058*SL	0.13 + 0.056*SL	0.09 + 0.058*SL
B to Y	tPLH	0.17	0.09 + 0.039*SL	0.09 + 0.038*SL	0.09 + 0.038*SL
	tPHL	0.42	0.36 + 0.034*SL	0.38 + 0.027*SL	0.41 + 0.026*SL
	tR	0.28	0.13 + 0.075*SL	0.10 + 0.087*SL	0.07 + 0.088*SL
	tF	0.26	0.15 + 0.056*SL	0.15 + 0.056*SL	0.09 + 0.058*SL
C to Y	tPLH	0.19	0.11 + 0.039*SL	0.11 + 0.038*SL	0.12 + 0.038*SL
	tPHL	0.57	0.50 + 0.036*SL	0.53 + 0.028*SL	0.56 + 0.026*SL
	tR	0.32	0.16 + 0.080*SL	0.14 + 0.087*SL	0.11 + 0.088*SL
	tF	0.28	0.18 + 0.051*SL	0.17 + 0.056*SL	0.12 + 0.058*SL
D to Y	tPLH	0.22	0.14 + 0.040*SL	0.14 + 0.037*SL	0.14 + 0.038*SL
	tPHL	0.58	0.50 + 0.036*SL	0.53 + 0.028*SL	0.56 + 0.026*SL
	tR	0.32	0.15 + 0.086*SL	0.15 + 0.086*SL	0.12 + 0.088*SL
	tF	0.29	0.18 + 0.054*SL	0.17 + 0.056*SL	0.13 + 0.058*SL
E to Y	tPLH	0.23	0.15 + 0.039*SL	0.15 + 0.038*SL	0.16 + 0.038*SL
	tPHL	0.56	0.49 + 0.036*SL	0.51 + 0.028*SL	0.54 + 0.026*SL
	tR	0.33	0.18 + 0.076*SL	0.15 + 0.087*SL	0.12 + 0.088*SL
	tF	0.29	0.19 + 0.050*SL	0.17 + 0.056*SL	0.13 + 0.058*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

OR5D2 Switching Characteristics

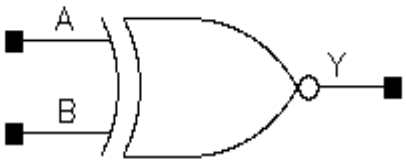
[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.14	0.10 + 0.022*SL	0.10 + 0.019*SL	0.11 + 0.019*SL
	tPHL	0.49	0.45 + 0.022*SL	0.46 + 0.016*SL	0.50 + 0.014*SL
	tR	0.20	0.12 + 0.038*SL	0.11 + 0.044*SL	0.08 + 0.045*SL
	tF	0.23	0.17 + 0.029*SL	0.16 + 0.031*SL	0.14 + 0.032*SL
B to Y	tPLH	0.17	0.13 + 0.020*SL	0.13 + 0.019*SL	0.14 + 0.019*SL
	tPHL	0.46	0.42 + 0.022*SL	0.43 + 0.016*SL	0.47 + 0.014*SL
	tR	0.21	0.14 + 0.032*SL	0.11 + 0.044*SL	0.08 + 0.045*SL
	tF	0.23	0.17 + 0.030*SL	0.17 + 0.031*SL	0.15 + 0.032*SL
C to Y	tPLH	0.19	0.15 + 0.020*SL	0.15 + 0.019*SL	0.16 + 0.019*SL
	tPHL	0.63	0.59 + 0.023*SL	0.60 + 0.017*SL	0.65 + 0.014*SL
	tR	0.26	0.19 + 0.038*SL	0.17 + 0.043*SL	0.14 + 0.045*SL
	tF	0.30	0.24 + 0.029*SL	0.24 + 0.029*SL	0.19 + 0.032*SL
D to Y	tPLH	0.22	0.18 + 0.020*SL	0.18 + 0.019*SL	0.18 + 0.019*SL
	tPHL	0.63	0.58 + 0.024*SL	0.60 + 0.017*SL	0.64 + 0.015*SL
	tR	0.26	0.18 + 0.041*SL	0.17 + 0.044*SL	0.14 + 0.045*SL
	tF	0.30	0.23 + 0.033*SL	0.24 + 0.029*SL	0.20 + 0.031*SL
E to Y	tPLH	0.23	0.19 + 0.021*SL	0.19 + 0.019*SL	0.20 + 0.019*SL
	tPHL	0.61	0.56 + 0.024*SL	0.58 + 0.017*SL	0.62 + 0.015*SL
	tR	0.27	0.19 + 0.040*SL	0.18 + 0.043*SL	0.15 + 0.045*SL
	tF	0.30	0.24 + 0.027*SL	0.23 + 0.030*SL	0.20 + 0.031*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: A, B
Output: Y
Input Loading (SL): All: A : 1,B : 2
Maximum Fanout (Rec. SL):
- XN2: 28
- XN2D2: 56
- XN2D3: 84
- XN2D5: 140

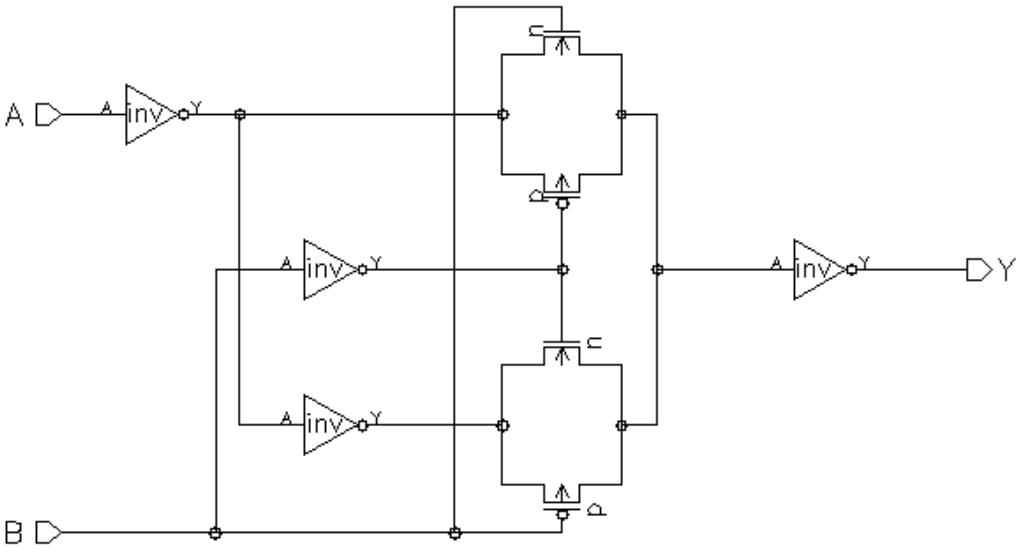
Gate Count:
- XN2: 3
- XN2D2: 4
- XN2D3: 4
- XN2D5: 5



Symbol

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Truth Table



Schematic

XN2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.28	0.20 + 0.040*SL	0.21 + 0.037*SL	0.21 + 0.037*SL
	t_{PHL}	0.46	0.39 + 0.032*SL	0.43 + 0.020*SL	0.50 + 0.016*SL
	t_R	0.27	0.11 + 0.078*SL	0.09 + 0.085*SL	0.06 + 0.086*SL
	t_F	0.21	0.13 + 0.039*SL	0.16 + 0.030*SL	0.13 + 0.031*SL
B to Y	t_{PLH}	0.19	0.11 + 0.040*SL	0.12 + 0.037*SL	0.12 + 0.037*SL
	t_{PHL}	0.37	0.31 + 0.028*SL	0.34 + 0.019*SL	0.39 + 0.016*SL
	t_R	0.27	0.11 + 0.081*SL	0.09 + 0.085*SL	0.06 + 0.086*SL
	t_F	0.17	0.10 + 0.036*SL	0.11 + 0.031*SL	0.10 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

XN2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.28	0.24 + 0.022*SL	0.24 + 0.019*SL	0.25 + 0.018*SL
	t_{PHL}	0.47	0.43 + 0.019*SL	0.45 + 0.013*SL	0.51 + 0.009*SL
	t_R	0.19	0.12 + 0.034*SL	0.11 + 0.041*SL	0.09 + 0.042*SL
	t_F	0.19	0.15 + 0.018*SL	0.16 + 0.016*SL	0.17 + 0.015*SL
B to Y	t_{PLH}	0.20	0.15 + 0.023*SL	0.17 + 0.018*SL	0.17 + 0.018*SL
	t_{PHL}	0.37	0.34 + 0.018*SL	0.35 + 0.012*SL	0.41 + 0.009*SL
	t_R	0.19	0.13 + 0.032*SL	0.10 + 0.041*SL	0.09 + 0.042*SL
	t_F	0.15	0.10 + 0.022*SL	0.12 + 0.017*SL	0.14 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

XN2D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.30	0.27 + 0.017*SL	0.28 + 0.013*SL	0.29 + 0.013*SL
	tPHL	0.49	0.46 + 0.015*SL	0.48 + 0.010*SL	0.53 + 0.007*SL
	tR	0.18	0.13 + 0.027*SL	0.12 + 0.028*SL	0.11 + 0.029*SL
	tF	0.19	0.16 + 0.017*SL	0.18 + 0.012*SL	0.20 + 0.011*SL
B to Y	tPLH	0.23	0.20 + 0.016*SL	0.21 + 0.013*SL	0.22 + 0.013*SL
	tPHL	0.39	0.36 + 0.014*SL	0.37 + 0.009*SL	0.42 + 0.007*SL
	tR	0.18	0.13 + 0.025*SL	0.12 + 0.029*SL	0.11 + 0.029*SL
	tF	0.15	0.12 + 0.017*SL	0.13 + 0.013*SL	0.16 + 0.011*SL

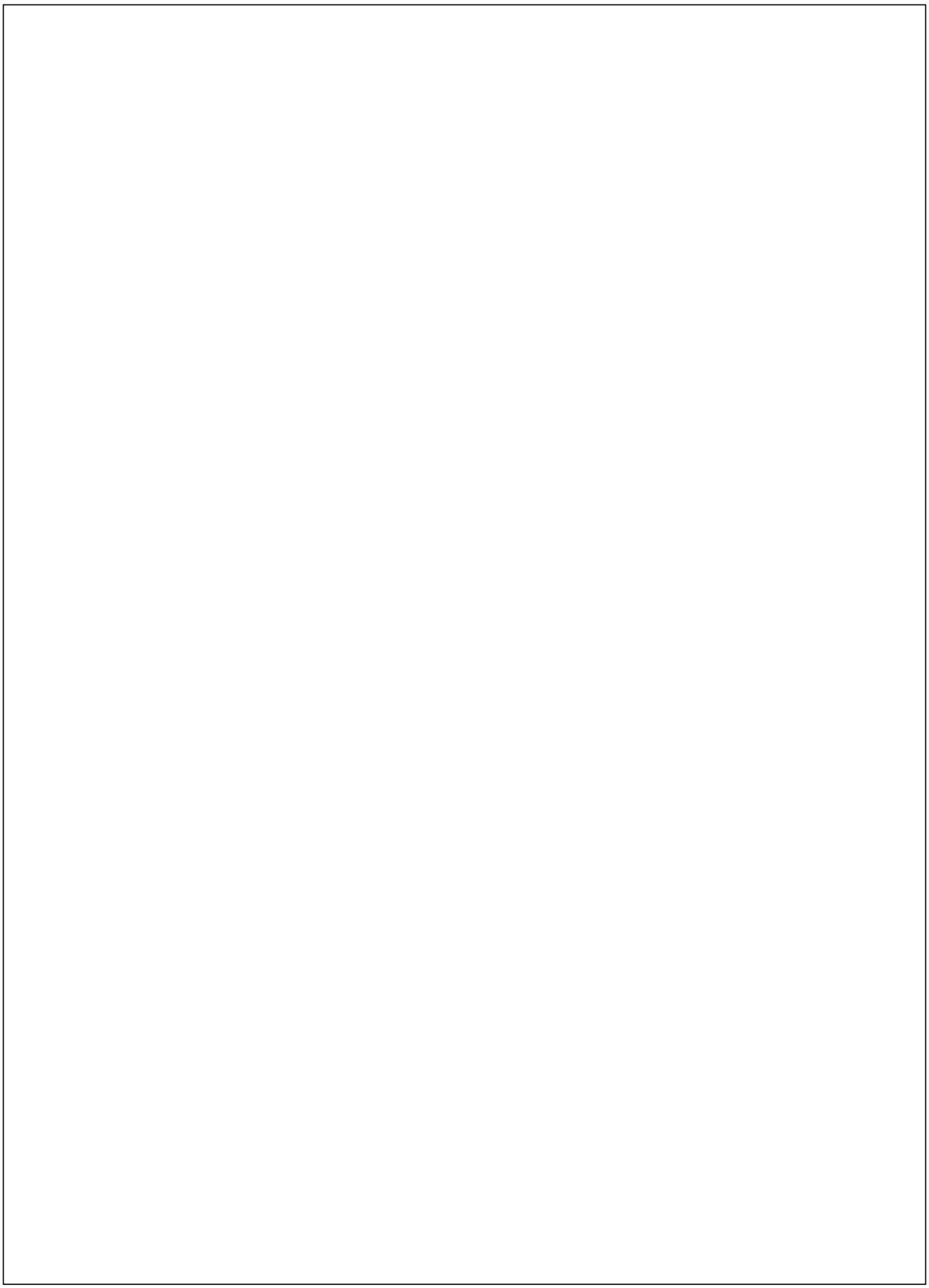
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

XN2D5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.36	0.34 + 0.010*SL	0.34 + 0.009*SL	0.36 + 0.008*SL
	tPHL	0.54	0.52 + 0.011*SL	0.53 + 0.007*SL	0.57 + 0.005*SL
	tR	0.18	0.14 + 0.018*SL	0.14 + 0.017*SL	0.15 + 0.017*SL
	tF	0.21	0.19 + 0.012*SL	0.20 + 0.008*SL	0.22 + 0.007*SL
B to Y	tPLH	0.30	0.28 + 0.008*SL	0.28 + 0.009*SL	0.30 + 0.008*SL
	tPHL	0.43	0.41 + 0.011*SL	0.42 + 0.007*SL	0.45 + 0.005*SL
	tR	0.19	0.16 + 0.013*SL	0.15 + 0.017*SL	0.15 + 0.017*SL
	tF	0.18	0.15 + 0.016*SL	0.17 + 0.008*SL	0.20 + 0.007*SL

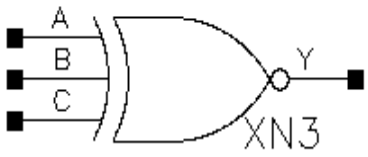
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B, C
Output: Y
Input Loading (SL):
- XN3: A, C: 2
  B: 1
- XN3D2: A, C : 2
  B: 1

Maximum Fanout (Rec. SL):
- XN3: 28
- XN3D2: 84

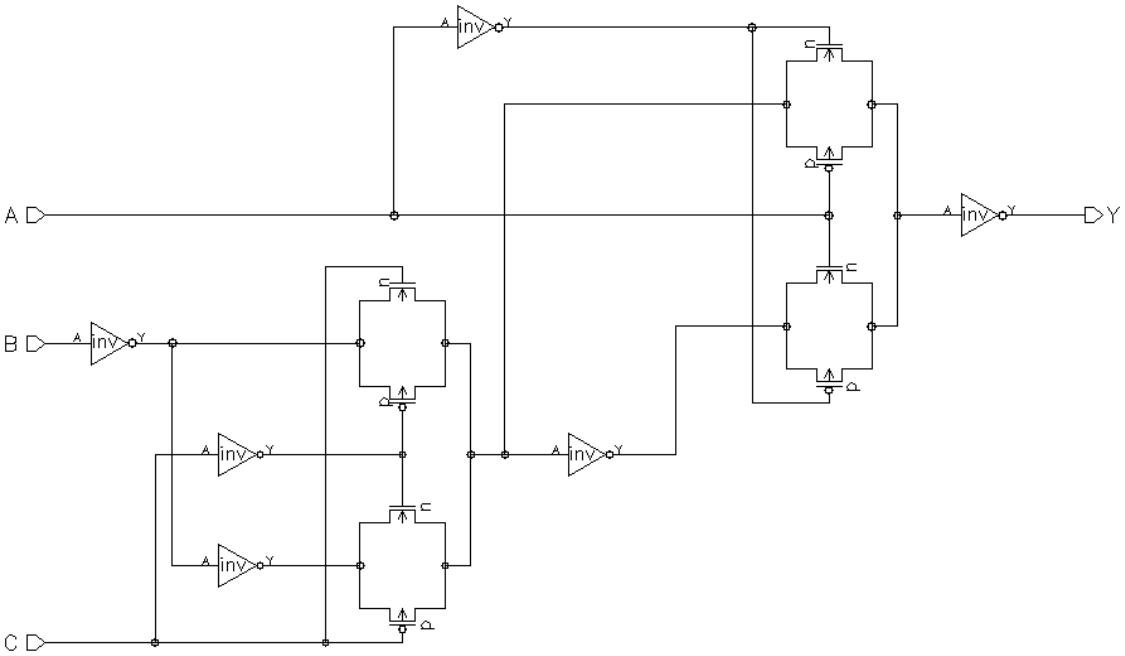
Gate Count:
- XN3: 5
- XN3D2: 6



Symbol

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table



Schematic

XN3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.46	0.37 + 0.044*SL	0.39 + 0.038*SL	0.40 + 0.037*SL
	tPHL	0.20	0.14 + 0.028*SL	0.17 + 0.018*SL	0.22 + 0.016*SL
	tR	0.27	0.10 + 0.086*SL	0.10 + 0.085*SL	0.07 + 0.086*SL
	tF	0.17	0.10 + 0.036*SL	0.12 + 0.031*SL	0.10 + 0.032*SL
B to Y	tPLH	0.68	0.60 + 0.041*SL	0.61 + 0.037*SL	0.61 + 0.037*SL
	tPHL	0.42	0.36 + 0.031*SL	0.40 + 0.019*SL	0.44 + 0.016*SL
	tR	0.27	0.12 + 0.078*SL	0.10 + 0.085*SL	0.06 + 0.087*SL
	tF	0.18	0.10 + 0.040*SL	0.13 + 0.031*SL	0.11 + 0.032*SL
C to Y	tPLH	0.58	0.49 + 0.041*SL	0.51 + 0.037*SL	0.51 + 0.037*SL
	tPHL	0.34	0.27 + 0.032*SL	0.31 + 0.019*SL	0.36 + 0.016*SL
	tR	0.26	0.11 + 0.080*SL	0.09 + 0.085*SL	0.06 + 0.087*SL
	tF	0.18	0.09 + 0.043*SL	0.13 + 0.030*SL	0.11 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

XN3D3 Switching Characteristics

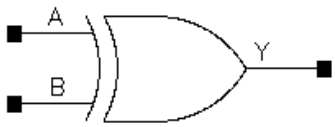
[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.49	0.45 + 0.016*SL	0.46 + 0.014*SL	0.49 + 0.012*SL
	tPHL	0.25	0.21 + 0.016*SL	0.23 + 0.009*SL	0.28 + 0.007*SL
	tR	0.20	0.15 + 0.025*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	tF	0.19	0.17 + 0.009*SL	0.17 + 0.011*SL	0.20 + 0.010*SL
B to Y	tPLH	0.69	0.66 + 0.016*SL	0.66 + 0.013*SL	0.68 + 0.012*SL
	tPHL	0.45	0.42 + 0.014*SL	0.44 + 0.009*SL	0.49 + 0.007*SL
	tR	0.17	0.12 + 0.026*SL	0.12 + 0.027*SL	0.10 + 0.028*SL
	tF	0.17	0.13 + 0.018*SL	0.15 + 0.012*SL	0.19 + 0.010*SL
C to Y	tPLH	0.58	0.56 + 0.012*SL	0.56 + 0.013*SL	0.58 + 0.012*SL
	tPHL	0.36	0.33 + 0.014*SL	0.35 + 0.009*SL	0.40 + 0.007*SL
	tR	0.17	0.11 + 0.029*SL	0.12 + 0.027*SL	0.10 + 0.028*SL
	tF	0.17	0.14 + 0.016*SL	0.15 + 0.012*SL	0.18 + 0.010*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

Inputs: A, B
Output: Y
Input Loading (SL): All: A : 1, B : 2
Maximum Fanout (Rec. SL):
- XO2: 28
- XO2D2: 56
- XO2D3: 84
- XO2D5: 140

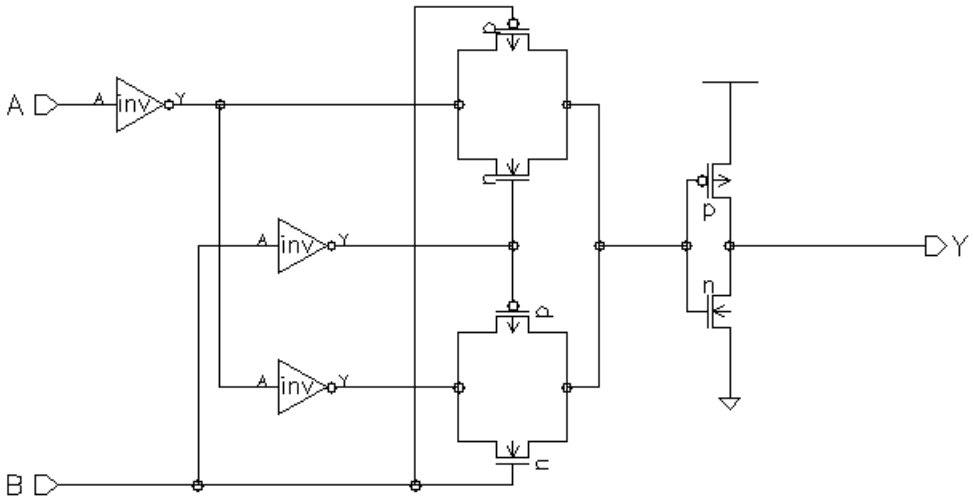
Gate Count:
- XO2: 3
- XO2D2: 4
- XO2D3: 4
- XO2D5: 5



Symbol

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table



Schematic

XO2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.51	0.43 + 0.040*SL	0.44 + 0.037*SL	0.44 + 0.037*SL
	t_{PHL}	0.27	0.21 + 0.030*SL	0.24 + 0.019*SL	0.29 + 0.016*SL
	t_R	0.25	0.10 + 0.075*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	t_F	0.17	0.10 + 0.036*SL	0.11 + 0.031*SL	0.11 + 0.032*SL
B to Y	t_{PLH}	0.43	0.35 + 0.040*SL	0.36 + 0.037*SL	0.36 + 0.037*SL
	t_{PHL}	0.20	0.15 + 0.027*SL	0.17 + 0.018*SL	0.22 + 0.016*SL
	t_R	0.25	0.09 + 0.079*SL	0.07 + 0.086*SL	0.06 + 0.087*SL
	t_F	0.17	0.10 + 0.035*SL	0.12 + 0.031*SL	0.10 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

XO2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.50	0.46 + 0.020*SL	0.47 + 0.019*SL	0.48 + 0.018*SL
	t_{PHL}	0.27	0.24 + 0.018*SL	0.25 + 0.012*SL	0.31 + 0.009*SL
	t_R	0.18	0.11 + 0.034*SL	0.09 + 0.041*SL	0.07 + 0.042*SL
	t_F	0.15	0.11 + 0.021*SL	0.12 + 0.017*SL	0.15 + 0.016*SL
B to Y	t_{PLH}	0.42	0.38 + 0.020*SL	0.38 + 0.019*SL	0.39 + 0.018*SL
	t_{PHL}	0.22	0.19 + 0.014*SL	0.20 + 0.012*SL	0.25 + 0.009*SL
	t_R	0.18	0.10 + 0.037*SL	0.09 + 0.041*SL	0.07 + 0.042*SL
	t_F	0.17	0.13 + 0.019*SL	0.14 + 0.016*SL	0.15 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

XO2D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.52	0.49 + 0.016*SL	0.50 + 0.013*SL	0.51 + 0.012*SL
	t_{PHL}	0.30	0.27 + 0.013*SL	0.28 + 0.010*SL	0.33 + 0.007*SL
	t_R	0.17	0.10 + 0.031*SL	0.11 + 0.028*SL	0.09 + 0.029*SL
	t_F	0.17	0.14 + 0.014*SL	0.15 + 0.012*SL	0.17 + 0.011*SL
B to Y	t_{PLH}	0.43	0.40 + 0.016*SL	0.41 + 0.013*SL	0.42 + 0.012*SL
	t_{PHL}	0.25	0.21 + 0.016*SL	0.24 + 0.009*SL	0.29 + 0.007*SL
	t_R	0.17	0.11 + 0.028*SL	0.11 + 0.028*SL	0.09 + 0.029*SL
	t_F	0.19	0.15 + 0.017*SL	0.17 + 0.012*SL	0.19 + 0.011*SL

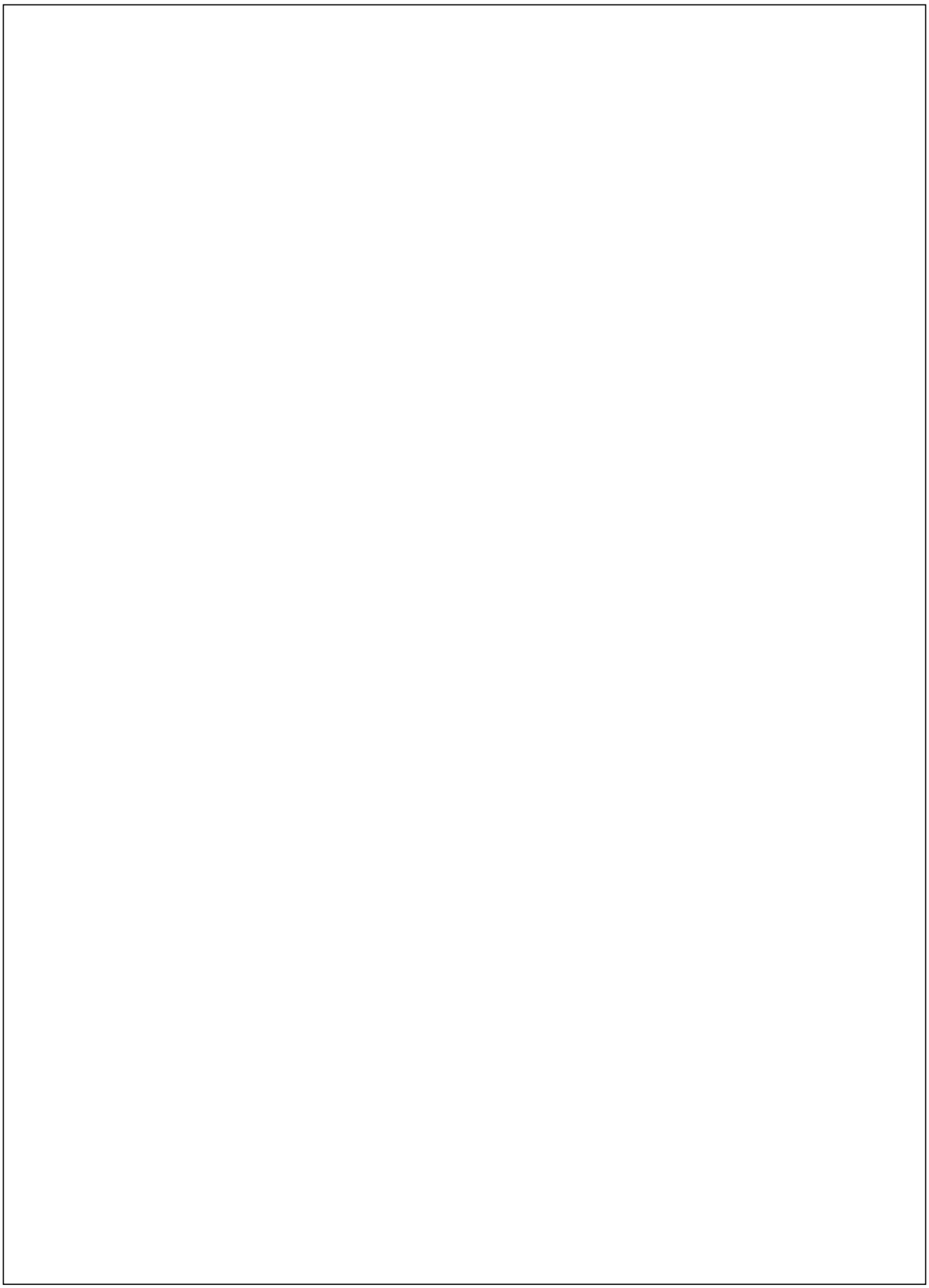
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

XO2D5 Switching Characteristics

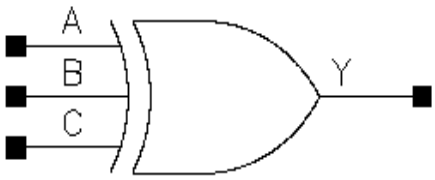
[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.56	0.54 + 0.008*SL	0.54 + 0.008*SL	0.55 + 0.008*SL
	t_{PHL}	0.34	0.32 + 0.011*SL	0.33 + 0.007*SL	0.37 + 0.005*SL
	t_R	0.17	0.15 + 0.013*SL	0.13 + 0.017*SL	0.12 + 0.017*SL
	t_F	0.20	0.17 + 0.012*SL	0.18 + 0.008*SL	0.21 + 0.007*SL
B to Y	t_{PLH}	0.47	0.45 + 0.011*SL	0.46 + 0.008*SL	0.47 + 0.008*SL
	t_{PHL}	0.30	0.28 + 0.012*SL	0.29 + 0.007*SL	0.33 + 0.005*SL
	t_R	0.17	0.14 + 0.014*SL	0.14 + 0.017*SL	0.13 + 0.017*SL
	t_F	0.22	0.20 + 0.009*SL	0.20 + 0.008*SL	0.22 + 0.007*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



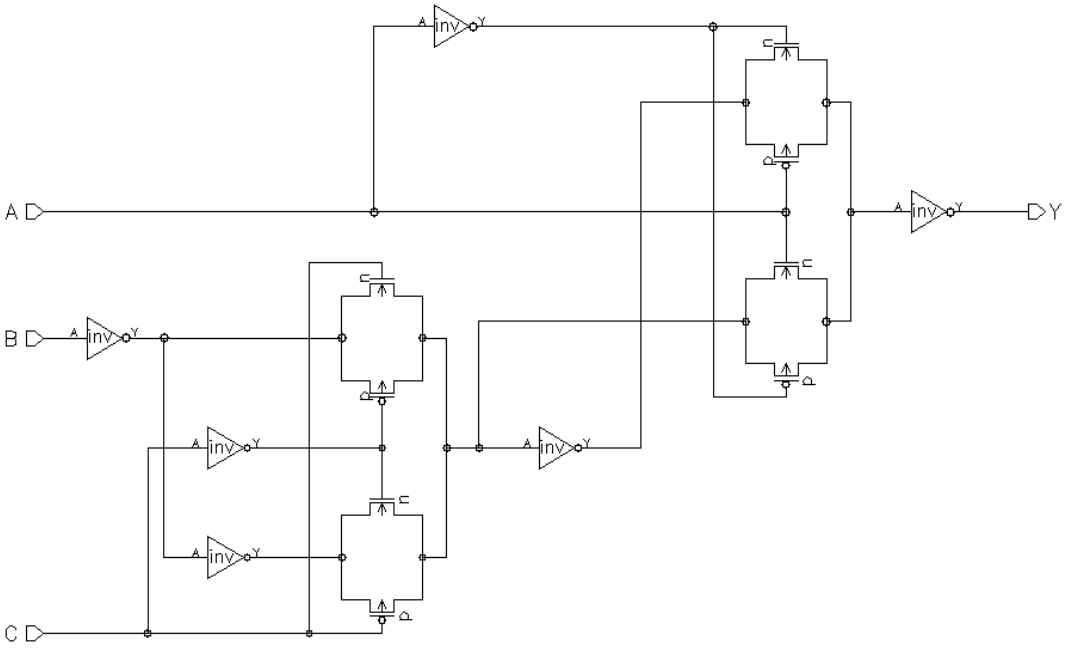
Inputs: A, B, C
Output: Y
Input Loading (SL):
‘ - XO3: A, C: 2
B : 1
- XO3D2: A, C: 2
B : 1
Maximum Fanout (Rec. SL):
- XO3: 28
- XO3D2: 84
Gate Count:
- XO3: 5
- XO3D2: 6



Symbol

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Truth Table



Schematic

XO3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.23	0.14 + 0.044*SL	0.16 + 0.038*SL	0.18 + 0.037*SL
	t_{PHL}	0.36	0.31 + 0.028*SL	0.33 + 0.019*SL	0.39 + 0.016*SL
	t_R	0.29	0.13 + 0.078*SL	0.11 + 0.085*SL	0.08 + 0.086*SL
	t_F	0.17	0.10 + 0.035*SL	0.12 + 0.031*SL	0.10 + 0.032*SL
B to Y	t_{PLH}	0.43	0.35 + 0.044*SL	0.36 + 0.038*SL	0.38 + 0.037*SL
	t_{PHL}	0.61	0.53 + 0.040*SL	0.58 + 0.024*SL	0.70 + 0.018*SL
	t_R	0.30	0.14 + 0.079*SL	0.13 + 0.084*SL	0.08 + 0.086*SL
	t_F	0.27	0.18 + 0.046*SL	0.22 + 0.033*SL	0.25 + 0.031*SL
C to Y	t_{PLH}	0.37	0.29 + 0.043*SL	0.30 + 0.038*SL	0.31 + 0.037*SL
	t_{PHL}	0.50	0.42 + 0.039*SL	0.47 + 0.024*SL	0.58 + 0.018*SL
	t_R	0.30	0.14 + 0.081*SL	0.13 + 0.084*SL	0.08 + 0.086*SL
	t_F	0.24	0.14 + 0.046*SL	0.18 + 0.033*SL	0.22 + 0.031*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

XO3D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

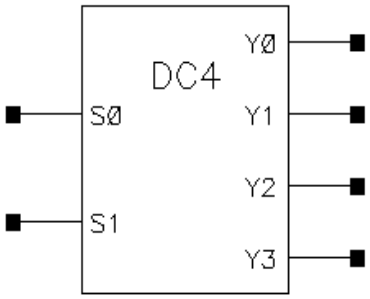
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t_{PLH}	0.28	0.25 + 0.017*SL	0.26 + 0.014*SL	0.29 + 0.012*SL
	t_{PHL}	0.38	0.36 + 0.014*SL	0.37 + 0.009*SL	0.42 + 0.007*SL
	t_R	0.20	0.14 + 0.032*SL	0.15 + 0.027*SL	0.15 + 0.027*SL
	t_F	0.16	0.11 + 0.020*SL	0.14 + 0.012*SL	0.17 + 0.011*SL
B to Y	t_{PLH}	0.46	0.42 + 0.019*SL	0.43 + 0.014*SL	0.46 + 0.012*SL
	t_{PHL}	0.64	0.60 + 0.019*SL	0.62 + 0.012*SL	0.68 + 0.009*SL
	t_R	0.22	0.16 + 0.027*SL	0.16 + 0.027*SL	0.15 + 0.027*SL
	t_F	0.26	0.21 + 0.022*SL	0.24 + 0.013*SL	0.27 + 0.011*SL
C to Y	t_{PLH}	0.40	0.36 + 0.018*SL	0.37 + 0.014*SL	0.40 + 0.012*SL
	t_{PHL}	0.51	0.47 + 0.019*SL	0.50 + 0.012*SL	0.56 + 0.009*SL
	t_R	0.21	0.15 + 0.031*SL	0.17 + 0.027*SL	0.15 + 0.027*SL
	t_F	0.22	0.19 + 0.016*SL	0.19 + 0.014*SL	0.25 + 0.012*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

Inputs: S0, S1
Outputs: Y0, Y1, Y2, Y3
Input Loading (SL):
- DC4: All : 3
- DC4D2: All: 3
- DC4D4: All: 3

Maximum Fanout (Rec. SL):
- DC4: 28
- DC4D2: 56
- DC4D4: 112

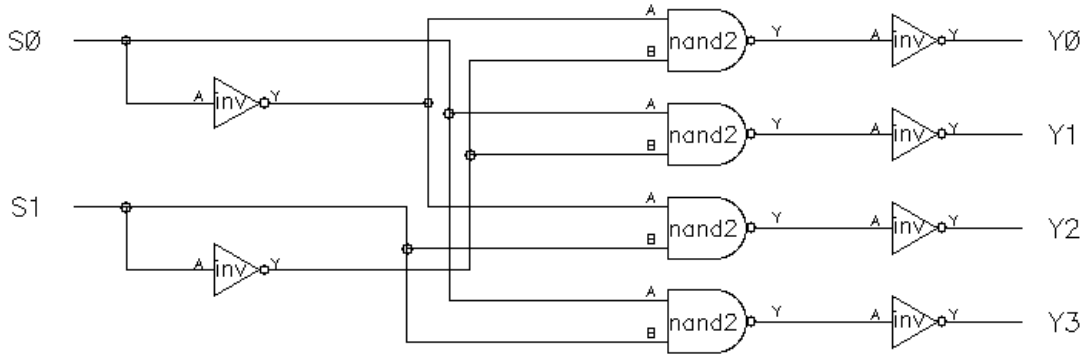
Gate Count:
- DC4: 7
- DC4D2: 9
- DC4D4: 13



Symbol

S1	S0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Truth Table



Schematic

DC4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to Y0	t_{PLH}	0.48	0.41 + 0.038*SL	0.42 + 0.036*SL	0.41 + 0.036*SL
	t_{PHL}	0.20	0.15 + 0.023*SL	0.17 + 0.017*SL	0.18 + 0.016*SL
	t_R	0.24	0.07 + 0.084*SL	0.08 + 0.083*SL	0.05 + 0.085*SL
	t_F	0.13	0.05 + 0.042*SL	0.08 + 0.032*SL	0.04 + 0.034*SL
S1 to Y0	t_{PLH}	0.49	0.41 + 0.039*SL	0.42 + 0.037*SL	0.42 + 0.036*SL
	t_{PHL}	0.23	0.19 + 0.023*SL	0.21 + 0.017*SL	0.22 + 0.016*SL
	t_R	0.24	0.08 + 0.080*SL	0.07 + 0.083*SL	0.05 + 0.085*SL
	t_F	0.14	0.07 + 0.032*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
S0 to Y1	t_{PLH}	0.21	0.13 + 0.039*SL	0.14 + 0.037*SL	0.14 + 0.036*SL
	t_{PHL}	0.29	0.25 + 0.025*SL	0.27 + 0.017*SL	0.28 + 0.016*SL
	t_R	0.25	0.08 + 0.085*SL	0.09 + 0.083*SL	0.06 + 0.084*SL
	t_F	0.15	0.08 + 0.031*SL	0.08 + 0.033*SL	0.05 + 0.034*SL
S1 to Y1	t_{PLH}	0.49	0.41 + 0.039*SL	0.42 + 0.037*SL	0.42 + 0.036*SL
	t_{PHL}	0.24	0.19 + 0.024*SL	0.21 + 0.017*SL	0.23 + 0.016*SL
	t_R	0.24	0.08 + 0.081*SL	0.07 + 0.083*SL	0.05 + 0.085*SL
	t_F	0.14	0.08 + 0.029*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
S0 to Y2	t_{PLH}	0.49	0.41 + 0.038*SL	0.42 + 0.036*SL	0.41 + 0.036*SL
	t_{PHL}	0.20	0.15 + 0.023*SL	0.17 + 0.017*SL	0.18 + 0.016*SL
	t_R	0.24	0.07 + 0.084*SL	0.08 + 0.083*SL	0.05 + 0.085*SL
	t_F	0.13	0.05 + 0.042*SL	0.08 + 0.032*SL	0.04 + 0.034*SL
S1 to Y2	t_{PLH}	0.18	0.10 + 0.040*SL	0.11 + 0.036*SL	0.12 + 0.036*SL
	t_{PHL}	0.35	0.30 + 0.025*SL	0.32 + 0.017*SL	0.33 + 0.016*SL
	t_R	0.26	0.10 + 0.081*SL	0.09 + 0.083*SL	0.06 + 0.084*SL
	t_F	0.16	0.10 + 0.031*SL	0.09 + 0.032*SL	0.05 + 0.034*SL
S0 to Y3	t_{PLH}	0.21	0.13 + 0.039*SL	0.14 + 0.037*SL	0.14 + 0.036*SL
	t_{PHL}	0.29	0.24 + 0.025*SL	0.27 + 0.017*SL	0.28 + 0.016*SL
	t_R	0.25	0.08 + 0.085*SL	0.09 + 0.083*SL	0.06 + 0.084*SL
	t_F	0.15	0.08 + 0.032*SL	0.08 + 0.032*SL	0.05 + 0.034*SL
S1 to Y3	t_{PLH}	0.18	0.10 + 0.040*SL	0.11 + 0.036*SL	0.11 + 0.036*SL
	t_{PHL}	0.35	0.30 + 0.025*SL	0.32 + 0.017*SL	0.34 + 0.016*SL
	t_R	0.26	0.09 + 0.082*SL	0.09 + 0.083*SL	0.06 + 0.084*SL
	t_F	0.16	0.10 + 0.031*SL	0.09 + 0.032*SL	0.06 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

DC4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to Y0	tPLH	0.48	0.44 + 0.022*SL	0.45 + 0.019*SL	0.45 + 0.019*SL
	tPHL	0.21	0.18 + 0.015*SL	0.20 + 0.010*SL	0.22 + 0.009*SL
	tR	0.17	0.08 + 0.045*SL	0.09 + 0.044*SL	0.07 + 0.045*SL
	tF	0.11	0.07 + 0.021*SL	0.09 + 0.017*SL	0.08 + 0.017*SL
S1 to Y0	tPLH	0.49	0.44 + 0.022*SL	0.45 + 0.019*SL	0.46 + 0.019*SL
	tPHL	0.25	0.22 + 0.015*SL	0.23 + 0.010*SL	0.26 + 0.008*SL
	tR	0.18	0.10 + 0.042*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	tF	0.12	0.08 + 0.021*SL	0.10 + 0.016*SL	0.08 + 0.017*SL
S0 to Y1	tPLH	0.22	0.18 + 0.023*SL	0.19 + 0.019*SL	0.20 + 0.019*SL
	tPHL	0.32	0.29 + 0.014*SL	0.30 + 0.010*SL	0.33 + 0.008*SL
	tR	0.18	0.10 + 0.044*SL	0.10 + 0.044*SL	0.07 + 0.045*SL
	tF	0.14	0.11 + 0.014*SL	0.10 + 0.016*SL	0.09 + 0.017*SL
S1 to Y1	tPLH	0.49	0.44 + 0.022*SL	0.45 + 0.019*SL	0.46 + 0.019*SL
	tPHL	0.25	0.22 + 0.015*SL	0.23 + 0.010*SL	0.26 + 0.008*SL
	tR	0.18	0.10 + 0.041*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	tF	0.12	0.08 + 0.020*SL	0.10 + 0.016*SL	0.07 + 0.017*SL
S0 to Y2	tPLH	0.48	0.44 + 0.022*SL	0.45 + 0.019*SL	0.45 + 0.019*SL
	tPHL	0.21	0.18 + 0.015*SL	0.20 + 0.010*SL	0.21 + 0.009*SL
	tR	0.17	0.08 + 0.045*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	tF	0.11	0.07 + 0.022*SL	0.09 + 0.017*SL	0.08 + 0.017*SL
S1 to Y2	tPLH	0.19	0.14 + 0.023*SL	0.15 + 0.019*SL	0.16 + 0.019*SL
	tPHL	0.37	0.33 + 0.016*SL	0.35 + 0.010*SL	0.38 + 0.008*SL
	tR	0.20	0.12 + 0.040*SL	0.11 + 0.043*SL	0.07 + 0.045*SL
	tF	0.15	0.12 + 0.014*SL	0.11 + 0.016*SL	0.10 + 0.017*SL
S0 to Y3	tPLH	0.22	0.18 + 0.023*SL	0.19 + 0.019*SL	0.20 + 0.019*SL
	tPHL	0.32	0.29 + 0.015*SL	0.30 + 0.010*SL	0.33 + 0.008*SL
	tR	0.18	0.10 + 0.044*SL	0.10 + 0.044*SL	0.07 + 0.045*SL
	tF	0.14	0.11 + 0.017*SL	0.11 + 0.016*SL	0.09 + 0.017*SL
S1 to Y3	tPLH	0.19	0.14 + 0.022*SL	0.15 + 0.019*SL	0.16 + 0.019*SL
	tPHL	0.36	0.33 + 0.016*SL	0.35 + 0.010*SL	0.39 + 0.008*SL
	tR	0.20	0.12 + 0.040*SL	0.11 + 0.043*SL	0.07 + 0.045*SL
	tF	0.15	0.12 + 0.014*SL	0.11 + 0.016*SL	0.10 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

DC4D4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

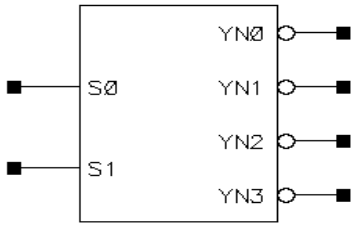
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to Y0	tPLH	0.53	0.50 + 0.013*SL	0.51 + 0.010*SL	0.53 + 0.010*SL
	tPHL	0.26	0.24 + 0.008*SL	0.25 + 0.006*SL	0.28 + 0.005*SL
	tR	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.11 + 0.022*SL
	tF	0.13	0.11 + 0.009*SL	0.11 + 0.009*SL	0.13 + 0.008*SL
S1 to Y0	tPLH	0.53	0.50 + 0.012*SL	0.51 + 0.010*SL	0.52 + 0.010*SL
	tPHL	0.29	0.27 + 0.009*SL	0.28 + 0.007*SL	0.32 + 0.005*SL
	tR	0.16	0.12 + 0.021*SL	0.11 + 0.022*SL	0.11 + 0.022*SL
	tF	0.14	0.14 + 0.004*SL	0.12 + 0.009*SL	0.16 + 0.008*SL
S0 to Y1	tPLH	0.29	0.27 + 0.012*SL	0.27 + 0.010*SL	0.29 + 0.009*SL
	tPHL	0.38	0.36 + 0.010*SL	0.37 + 0.006*SL	0.40 + 0.005*SL
	tR	0.16	0.13 + 0.018*SL	0.12 + 0.022*SL	0.12 + 0.021*SL
	tF	0.16	0.14 + 0.008*SL	0.14 + 0.008*SL	0.13 + 0.008*SL
S1 to Y1	tPLH	0.52	0.50 + 0.012*SL	0.50 + 0.010*SL	0.52 + 0.009*SL
	tPHL	0.29	0.27 + 0.010*SL	0.28 + 0.007*SL	0.32 + 0.005*SL
	tR	0.15	0.11 + 0.021*SL	0.11 + 0.021*SL	0.12 + 0.021*SL
	tF	0.14	0.12 + 0.008*SL	0.12 + 0.009*SL	0.15 + 0.008*SL
S0 to Y2	tPLH	0.53	0.50 + 0.013*SL	0.51 + 0.010*SL	0.53 + 0.010*SL
	tPHL	0.26	0.24 + 0.008*SL	0.25 + 0.006*SL	0.28 + 0.005*SL
	tR	0.16	0.11 + 0.025*SL	0.12 + 0.021*SL	0.11 + 0.022*SL
	tF	0.13	0.11 + 0.009*SL	0.11 + 0.009*SL	0.13 + 0.008*SL
S1 to Y2	tPLH	0.24	0.22 + 0.011*SL	0.22 + 0.010*SL	0.24 + 0.009*SL
	tPHL	0.42	0.40 + 0.010*SL	0.41 + 0.007*SL	0.44 + 0.005*SL
	tR	0.16	0.13 + 0.018*SL	0.12 + 0.022*SL	0.12 + 0.022*SL
	tF	0.16	0.14 + 0.010*SL	0.15 + 0.008*SL	0.16 + 0.008*SL
S0 to Y3	tPLH	0.29	0.27 + 0.012*SL	0.27 + 0.010*SL	0.29 + 0.009*SL
	tPHL	0.38	0.36 + 0.010*SL	0.37 + 0.006*SL	0.40 + 0.005*SL
	tR	0.17	0.13 + 0.018*SL	0.12 + 0.022*SL	0.12 + 0.021*SL
	tF	0.16	0.14 + 0.008*SL	0.14 + 0.008*SL	0.13 + 0.008*SL
S1 to Y3	tPLH	0.25	0.22 + 0.012*SL	0.23 + 0.010*SL	0.24 + 0.009*SL
	tPHL	0.41	0.39 + 0.012*SL	0.41 + 0.007*SL	0.44 + 0.005*SL
	tR	0.17	0.13 + 0.018*SL	0.12 + 0.021*SL	0.12 + 0.021*SL
	tF	0.16	0.14 + 0.010*SL	0.14 + 0.009*SL	0.16 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: S0, S1
Outputs: YN0, YN1, YN2, YN3
Input Loading (SL):
- DC4I: All : 3
- DC4ID2: All: 3
- DC4ID4: All: 3

Maximum Fanout (Rec. SL):
- DC4I: 28
- DC4ID2: 56
- DC4ID4: 112

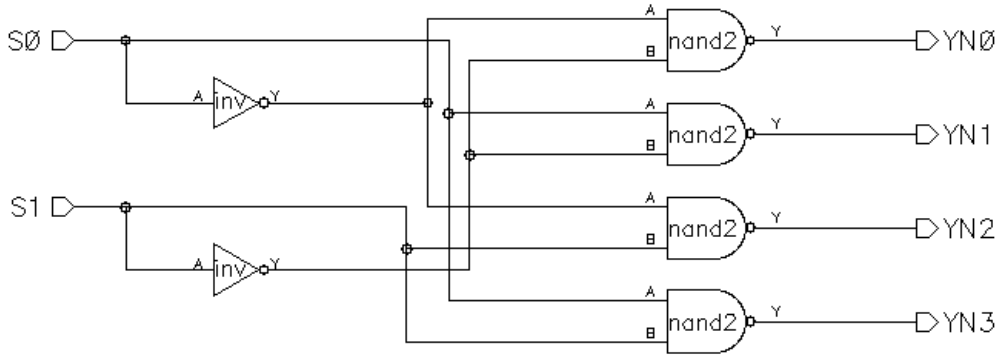
Gate Count:
- DC4I: 5
- DC4ID2: 9
- DC4ID4: 13



Symbol

S1	S0	YN0	YN1	YN2	YN3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Truth Table



Schematic

DC4I Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN0	tPLH	0.18	0.10 + 0.039*SL	0.11 + 0.036*SL	0.09 + 0.037*SL
	tPHL	0.38	0.32 + 0.034*SL	0.34 + 0.026*SL	0.35 + 0.026*SL
	tR	0.27	0.09 + 0.088*SL	0.11 + 0.082*SL	0.07 + 0.084*SL
	tF	0.22	0.11 + 0.057*SL	0.11 + 0.056*SL	0.07 + 0.058*SL
S1 to YN0	tPLH	0.21	0.13 + 0.038*SL	0.14 + 0.036*SL	0.13 + 0.036*SL
	tPHL	0.39	0.32 + 0.034*SL	0.34 + 0.026*SL	0.35 + 0.026*SL
	tR	0.30	0.15 + 0.079*SL	0.13 + 0.083*SL	0.11 + 0.084*SL
	tF	0.22	0.11 + 0.056*SL	0.11 + 0.056*SL	0.06 + 0.058*SL
S0 to YN1	tPLH	0.29	0.19 + 0.049*SL	0.22 + 0.038*SL	0.24 + 0.037*SL
	tPHL	0.12	0.02 + 0.047*SL	0.08 + 0.030*SL	0.15 + 0.026*SL
	tR	0.40	0.24 + 0.080*SL	0.24 + 0.081*SL	0.12 + 0.087*SL
	tF	0.37	0.25 + 0.058*SL	0.27 + 0.052*SL	0.19 + 0.056*SL
S1 to YN1	tPLH	0.22	0.14 + 0.039*SL	0.14 + 0.037*SL	0.14 + 0.038*SL
	tPHL	0.39	0.33 + 0.031*SL	0.34 + 0.026*SL	0.35 + 0.026*SL
	tR	0.32	0.15 + 0.083*SL	0.14 + 0.087*SL	0.11 + 0.088*SL
	tF	0.22	0.12 + 0.054*SL	0.11 + 0.056*SL	0.06 + 0.059*SL
S0 to YN2	tPLH	0.18	0.10 + 0.039*SL	0.11 + 0.036*SL	0.09 + 0.037*SL
	tPHL	0.39	0.32 + 0.033*SL	0.34 + 0.026*SL	0.35 + 0.026*SL
	tR	0.27	0.09 + 0.089*SL	0.11 + 0.082*SL	0.07 + 0.084*SL
	tF	0.22	0.11 + 0.057*SL	0.11 + 0.056*SL	0.07 + 0.058*SL
S1 to YN2	tPLH	0.33	0.24 + 0.042*SL	0.26 + 0.036*SL	0.26 + 0.036*SL
	tPHL	0.08	-0.01 + 0.041*SL	0.03 + 0.028*SL	0.08 + 0.026*SL
	tR	0.44	0.30 + 0.072*SL	0.28 + 0.077*SL	0.16 + 0.083*SL
	tF	0.34	0.24 + 0.048*SL	0.23 + 0.052*SL	0.14 + 0.057*SL
S0 to YN3	tPLH	0.29	0.19 + 0.049*SL	0.22 + 0.038*SL	0.24 + 0.037*SL
	tPHL	0.12	0.02 + 0.047*SL	0.08 + 0.030*SL	0.15 + 0.026*SL
	tR	0.40	0.24 + 0.080*SL	0.24 + 0.081*SL	0.12 + 0.087*SL
	tF	0.37	0.25 + 0.058*SL	0.27 + 0.052*SL	0.19 + 0.056*SL
S1 to YN3	tPLH	0.33	0.25 + 0.043*SL	0.27 + 0.037*SL	0.27 + 0.037*SL
	tPHL	0.07	-0.01 + 0.042*SL	0.03 + 0.028*SL	0.08 + 0.026*SL
	tR	0.45	0.30 + 0.075*SL	0.28 + 0.081*SL	0.17 + 0.087*SL
	tF	0.34	0.24 + 0.049*SL	0.23 + 0.053*SL	0.14 + 0.057*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

DC4ID2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN0	tPLH	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.10 + 0.019*SL
	tPHL	0.45	0.41 + 0.018*SL	0.43 + 0.011*SL	0.47 + 0.009*SL
	tR	0.18	0.09 + 0.045*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	tF	0.17	0.13 + 0.020*SL	0.14 + 0.016*SL	0.13 + 0.017*SL
S1 to YN0	tPLH	0.16	0.12 + 0.022*SL	0.13 + 0.019*SL	0.13 + 0.019*SL
	tPHL	0.41	0.38 + 0.018*SL	0.40 + 0.011*SL	0.45 + 0.009*SL
	tR	0.18	0.09 + 0.048*SL	0.10 + 0.044*SL	0.07 + 0.045*SL
	tF	0.16	0.13 + 0.019*SL	0.13 + 0.017*SL	0.14 + 0.017*SL
S0 to YN1	tPLH	0.43	0.39 + 0.022*SL	0.40 + 0.019*SL	0.40 + 0.019*SL
	tPHL	0.29	0.25 + 0.019*SL	0.28 + 0.011*SL	0.33 + 0.009*SL
	tR	0.17	0.08 + 0.043*SL	0.07 + 0.044*SL	0.05 + 0.045*SL
	tF	0.15	0.11 + 0.021*SL	0.13 + 0.017*SL	0.13 + 0.017*SL
S1 to YN1	tPLH	0.16	0.12 + 0.022*SL	0.13 + 0.019*SL	0.13 + 0.019*SL
	tPHL	0.41	0.38 + 0.018*SL	0.40 + 0.011*SL	0.45 + 0.009*SL
	tR	0.18	0.09 + 0.044*SL	0.09 + 0.044*SL	0.07 + 0.045*SL
	tF	0.16	0.13 + 0.018*SL	0.13 + 0.017*SL	0.14 + 0.017*SL
S0 to YN2	tPLH	0.13	0.09 + 0.021*SL	0.09 + 0.019*SL	0.10 + 0.019*SL
	tPHL	0.45	0.41 + 0.018*SL	0.43 + 0.011*SL	0.47 + 0.009*SL
	tR	0.18	0.09 + 0.047*SL	0.10 + 0.043*SL	0.06 + 0.045*SL
	tF	0.17	0.13 + 0.019*SL	0.14 + 0.016*SL	0.13 + 0.017*SL
S1 to YN2	tPLH	0.46	0.42 + 0.021*SL	0.42 + 0.019*SL	0.43 + 0.019*SL
	tPHL	0.31	0.28 + 0.018*SL	0.30 + 0.011*SL	0.35 + 0.009*SL
	tR	0.17	0.08 + 0.045*SL	0.08 + 0.044*SL	0.05 + 0.046*SL
	tF	0.16	0.11 + 0.025*SL	0.13 + 0.016*SL	0.13 + 0.017*SL
S0 to YN3	tPLH	0.44	0.39 + 0.022*SL	0.40 + 0.019*SL	0.40 + 0.019*SL
	tPHL	0.29	0.25 + 0.019*SL	0.28 + 0.011*SL	0.33 + 0.009*SL
	tR	0.17	0.08 + 0.043*SL	0.08 + 0.044*SL	0.05 + 0.045*SL
	tF	0.16	0.11 + 0.021*SL	0.13 + 0.017*SL	0.13 + 0.017*SL
S1 to YN3	tPLH	0.46	0.42 + 0.021*SL	0.42 + 0.019*SL	0.43 + 0.019*SL
	tPHL	0.32	0.28 + 0.020*SL	0.30 + 0.011*SL	0.35 + 0.009*SL
	tR	0.17	0.08 + 0.044*SL	0.08 + 0.044*SL	0.05 + 0.046*SL
	tF	0.16	0.11 + 0.024*SL	0.13 + 0.017*SL	0.14 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

DC4ID4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

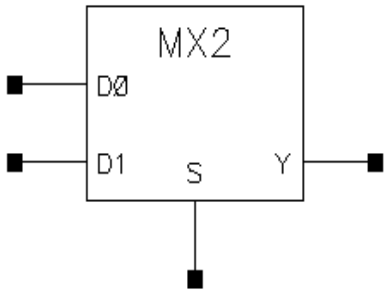
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN0	tPLH	0.19	0.16 + 0.011*SL	0.17 + 0.010*SL	0.17 + 0.009*SL
	tPHL	0.54	0.51 + 0.012*SL	0.53 + 0.007*SL	0.56 + 0.006*SL
	tR	0.15	0.10 + 0.027*SL	0.11 + 0.021*SL	0.09 + 0.022*SL
	tF	0.21	0.18 + 0.015*SL	0.20 + 0.009*SL	0.22 + 0.008*SL
S1 to YN0	tPLH	0.21	0.19 + 0.009*SL	0.19 + 0.010*SL	0.20 + 0.009*SL
	tPHL	0.50	0.48 + 0.010*SL	0.49 + 0.008*SL	0.53 + 0.006*SL
	tR	0.15	0.12 + 0.017*SL	0.11 + 0.021*SL	0.09 + 0.022*SL
	tF	0.21	0.19 + 0.010*SL	0.20 + 0.009*SL	0.21 + 0.008*SL
S0 to YN1	tPLH	0.46	0.44 + 0.010*SL	0.44 + 0.010*SL	0.45 + 0.010*SL
	tPHL	0.39	0.37 + 0.011*SL	0.38 + 0.008*SL	0.42 + 0.006*SL
	tR	0.14	0.10 + 0.021*SL	0.10 + 0.021*SL	0.08 + 0.022*SL
	tF	0.21	0.19 + 0.011*SL	0.19 + 0.009*SL	0.21 + 0.008*SL
S1 to YN1	tPLH	0.21	0.19 + 0.010*SL	0.19 + 0.010*SL	0.20 + 0.009*SL
	tPHL	0.50	0.48 + 0.011*SL	0.49 + 0.008*SL	0.53 + 0.006*SL
	tR	0.15	0.12 + 0.015*SL	0.10 + 0.022*SL	0.09 + 0.022*SL
	tF	0.21	0.19 + 0.009*SL	0.19 + 0.009*SL	0.21 + 0.008*SL
S0 to YN2	tPLH	0.19	0.16 + 0.011*SL	0.17 + 0.010*SL	0.17 + 0.010*SL
	tPHL	0.54	0.51 + 0.012*SL	0.53 + 0.007*SL	0.56 + 0.006*SL
	tR	0.15	0.09 + 0.028*SL	0.12 + 0.021*SL	0.08 + 0.022*SL
	tF	0.21	0.18 + 0.015*SL	0.20 + 0.009*SL	0.21 + 0.008*SL
S1 to YN2	tPLH	0.49	0.46 + 0.012*SL	0.47 + 0.010*SL	0.48 + 0.010*SL
	tPHL	0.41	0.38 + 0.012*SL	0.39 + 0.008*SL	0.44 + 0.006*SL
	tR	0.13	0.10 + 0.018*SL	0.09 + 0.022*SL	0.08 + 0.022*SL
	tF	0.20	0.19 + 0.009*SL	0.19 + 0.009*SL	0.20 + 0.008*SL
S0 to YN3	tPLH	0.46	0.44 + 0.010*SL	0.44 + 0.010*SL	0.45 + 0.010*SL
	tPHL	0.39	0.37 + 0.011*SL	0.38 + 0.008*SL	0.42 + 0.006*SL
	tR	0.14	0.10 + 0.021*SL	0.10 + 0.021*SL	0.08 + 0.022*SL
	tF	0.21	0.19 + 0.010*SL	0.19 + 0.009*SL	0.21 + 0.008*SL
S1 to YN3	tPLH	0.49	0.46 + 0.013*SL	0.47 + 0.010*SL	0.48 + 0.009*SL
	tPHL	0.41	0.39 + 0.009*SL	0.39 + 0.008*SL	0.44 + 0.006*SL
	tR	0.14	0.10 + 0.017*SL	0.09 + 0.022*SL	0.08 + 0.022*SL
	tF	0.21	0.19 + 0.013*SL	0.20 + 0.008*SL	0.20 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: D0, D1, S
Output: Y
Input Loading (SL):
- MX2: D0, D1:1
  S: 2
- MX2D3: D0, D1:1
  S: 2

Maximum Fanout (Rec. SL):
- MX2: 28
- MX2D3: 84

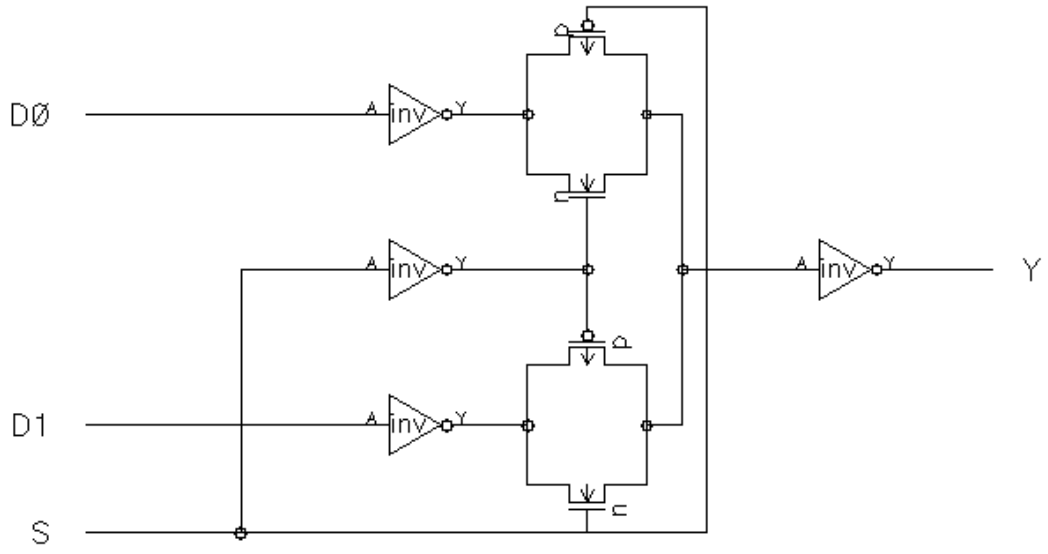
Gate Count:
- MX2: 3
- MX2D3: 4



Symbol

D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

Truth Table



Schematic

MX2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S to Y	t_{PLH}	0.43	0.35 + 0.041*SL	0.36 + 0.037*SL	0.36 + 0.037*SL
	t_{PHL}	0.20	0.15 + 0.028*SL	0.17 + 0.019*SL	0.22 + 0.016*SL
	t_R	0.26	0.09 + 0.082*SL	0.08 + 0.085*SL	0.06 + 0.087*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.031*SL	0.10 + 0.032*SL
D0 to Y	t_{PLH}	0.25	0.17 + 0.042*SL	0.18 + 0.037*SL	0.18 + 0.037*SL
	t_{PHL}	0.42	0.35 + 0.032*SL	0.39 + 0.019*SL	0.44 + 0.016*SL
	t_R	0.27	0.11 + 0.083*SL	0.10 + 0.084*SL	0.06 + 0.087*SL
	t_F	0.20	0.11 + 0.041*SL	0.15 + 0.030*SL	0.12 + 0.032*SL
D1 to Y	t_{PLH}	0.25	0.17 + 0.042*SL	0.18 + 0.037*SL	0.18 + 0.037*SL
	t_{PHL}	0.41	0.35 + 0.032*SL	0.39 + 0.019*SL	0.45 + 0.016*SL
	t_R	0.27	0.11 + 0.083*SL	0.10 + 0.084*SL	0.06 + 0.087*SL
	t_F	0.20	0.12 + 0.041*SL	0.15 + 0.030*SL	0.11 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

MX2D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

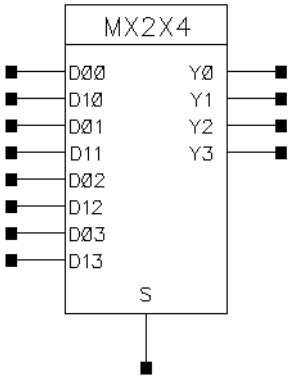
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S to Y	t_{PLH}	0.43	0.40 + 0.018*SL	0.41 + 0.013*SL	0.43 + 0.012*SL
	t_{PHL}	0.25	0.21 + 0.017*SL	0.24 + 0.009*SL	0.28 + 0.007*SL
	t_R	0.17	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.028*SL
	t_F	0.20	0.18 + 0.007*SL	0.17 + 0.011*SL	0.19 + 0.010*SL
D0 to Y	t_{PLH}	0.27	0.24 + 0.015*SL	0.25 + 0.013*SL	0.27 + 0.012*SL
	t_{PHL}	0.46	0.43 + 0.014*SL	0.44 + 0.009*SL	0.49 + 0.007*SL
	t_R	0.18	0.12 + 0.029*SL	0.13 + 0.027*SL	0.11 + 0.028*SL
	t_F	0.19	0.18 + 0.008*SL	0.17 + 0.011*SL	0.17 + 0.011*SL
D1 to Y	t_{PLH}	0.27	0.23 + 0.017*SL	0.25 + 0.013*SL	0.26 + 0.012*SL
	t_{PHL}	0.45	0.42 + 0.015*SL	0.44 + 0.009*SL	0.49 + 0.007*SL
	t_R	0.18	0.12 + 0.029*SL	0.13 + 0.027*SL	0.11 + 0.028*SL
	t_F	0.19	0.16 + 0.012*SL	0.17 + 0.011*SL	0.18 + 0.011*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: D00, D10, D01, D11, D02, D12,
D03, D13, S
Outputs: Y0, Y1, Y2, Y3
Input Loading (SL):
- MX2X4:All : 1
- MX2D2X4: D: 1, S: 4

Maximum Fanout (Rec. SL):
- MX2X4: All : 28
- MX2D2X4: 56

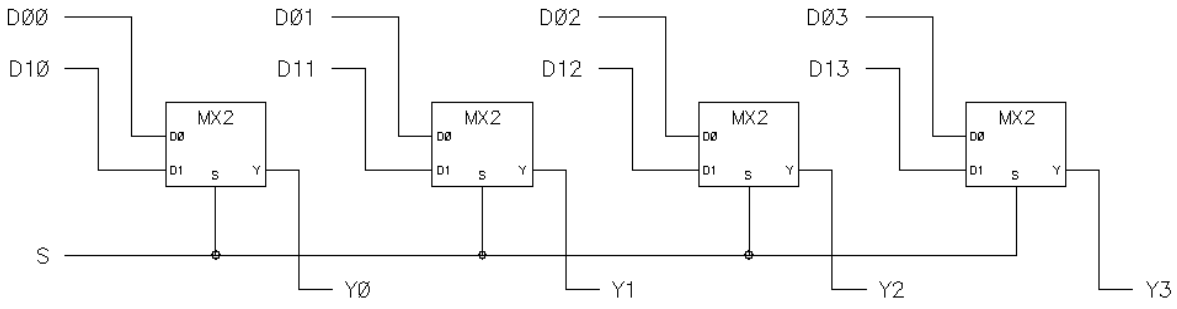
Gate Count:
- MX2X4: 11
- MX2D2X4: 13



Symbol

S	Y0	Y1	Y2	Y3
0	D00	D01	D02	D03
1	D10	D11	D12	D13

Truth Table



Schematic

MX2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S to Y0	tPLH	0.57	0.49 + 0.040*SL	0.50 + 0.036*SL	0.51 + 0.036*SL
	tPHL	0.36	0.31 + 0.026*SL	0.33 + 0.018*SL	0.38 + 0.016*SL
	tR	0.25	0.09 + 0.078*SL	0.08 + 0.084*SL	0.05 + 0.085*SL
	tF	0.17	0.08 + 0.042*SL	0.11 + 0.032*SL	0.09 + 0.033*SL
D00 to Y0	tPLH	0.25	0.16 + 0.041*SL	0.18 + 0.036*SL	0.18 + 0.036*SL
	tPHL	0.41	0.35 + 0.032*SL	0.39 + 0.019*SL	0.44 + 0.017*SL
	tR	0.26	0.10 + 0.080*SL	0.10 + 0.083*SL	0.06 + 0.085*SL
	tF	0.20	0.12 + 0.041*SL	0.15 + 0.031*SL	0.11 + 0.032*SL
D10 to Y0	tPLH	0.24	0.16 + 0.041*SL	0.18 + 0.036*SL	0.18 + 0.036*SL
	tPHL	0.41	0.35 + 0.032*SL	0.38 + 0.019*SL	0.44 + 0.017*SL
	tR	0.26	0.10 + 0.080*SL	0.09 + 0.083*SL	0.05 + 0.085*SL
	tF	0.20	0.11 + 0.042*SL	0.15 + 0.031*SL	0.11 + 0.032*SL
S to Y1	tPLH	0.57	0.50 + 0.039*SL	0.50 + 0.036*SL	0.51 + 0.036*SL
	tPHL	0.36	0.31 + 0.027*SL	0.33 + 0.018*SL	0.38 + 0.016*SL
	tR	0.25	0.09 + 0.078*SL	0.08 + 0.084*SL	0.05 + 0.085*SL
	tF	0.17	0.08 + 0.042*SL	0.11 + 0.032*SL	0.09 + 0.033*SL
D01 to Y1	tPLH	0.25	0.17 + 0.041*SL	0.18 + 0.036*SL	0.19 + 0.036*SL
	tPHL	0.41	0.35 + 0.032*SL	0.39 + 0.019*SL	0.44 + 0.017*SL
	tR	0.27	0.11 + 0.081*SL	0.10 + 0.083*SL	0.06 + 0.085*SL
	tF	0.20	0.11 + 0.042*SL	0.15 + 0.031*SL	0.11 + 0.032*SL
D11 to Y1	tPLH	0.25	0.17 + 0.041*SL	0.18 + 0.036*SL	0.18 + 0.036*SL
	tPHL	0.41	0.35 + 0.032*SL	0.38 + 0.019*SL	0.44 + 0.017*SL
	tR	0.27	0.11 + 0.080*SL	0.10 + 0.083*SL	0.06 + 0.085*SL
	tF	0.20	0.11 + 0.042*SL	0.15 + 0.031*SL	0.11 + 0.032*SL
S to Y2	tPLH	0.58	0.50 + 0.040*SL	0.51 + 0.036*SL	0.51 + 0.036*SL
	tPHL	0.36	0.31 + 0.027*SL	0.33 + 0.018*SL	0.38 + 0.016*SL
	tR	0.25	0.09 + 0.078*SL	0.08 + 0.084*SL	0.05 + 0.085*SL
	tF	0.17	0.08 + 0.042*SL	0.11 + 0.032*SL	0.09 + 0.033*SL
D02 to Y2	tPLH	0.25	0.17 + 0.041*SL	0.18 + 0.036*SL	0.19 + 0.036*SL
	tPHL	0.41	0.35 + 0.032*SL	0.39 + 0.019*SL	0.44 + 0.017*SL
	tR	0.27	0.11 + 0.081*SL	0.10 + 0.083*SL	0.06 + 0.085*SL
	tF	0.20	0.11 + 0.042*SL	0.15 + 0.031*SL	0.11 + 0.032*SL
D12 to Y2	tPLH	0.25	0.17 + 0.041*SL	0.18 + 0.036*SL	0.18 + 0.036*SL
	tPHL	0.41	0.35 + 0.031*SL	0.38 + 0.019*SL	0.44 + 0.017*SL
	tR	0.27	0.11 + 0.080*SL	0.10 + 0.083*SL	0.06 + 0.085*SL
	tF	0.20	0.12 + 0.040*SL	0.14 + 0.031*SL	0.11 + 0.032*SL
S to Y3	tPLH	0.57	0.49 + 0.039*SL	0.50 + 0.036*SL	0.51 + 0.036*SL
	tPHL	0.36	0.31 + 0.026*SL	0.33 + 0.018*SL	0.38 + 0.016*SL
	tR	0.25	0.09 + 0.078*SL	0.07 + 0.084*SL	0.05 + 0.085*SL
	tF	0.17	0.08 + 0.042*SL	0.11 + 0.032*SL	0.09 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

MX2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D03 to Y3	t_{PLH}	0.25	0.16 + 0.041*SL	0.18 + 0.036*SL	0.18 + 0.036*SL
	t_{PHL}	0.41	0.35 + 0.031*SL	0.39 + 0.019*SL	0.44 + 0.017*SL
	t_R	0.26	0.10 + 0.080*SL	0.10 + 0.083*SL	0.05 + 0.085*SL
	t_F	0.20	0.12 + 0.040*SL	0.15 + 0.031*SL	0.11 + 0.032*SL
D13 to Y3	t_{PLH}	0.24	0.16 + 0.041*SL	0.18 + 0.036*SL	0.18 + 0.036*SL
	t_{PHL}	0.41	0.35 + 0.032*SL	0.38 + 0.019*SL	0.44 + 0.017*SL
	t_R	0.27	0.10 + 0.083*SL	0.10 + 0.083*SL	0.06 + 0.085*SL
	t_F	0.20	0.11 + 0.042*SL	0.15 + 0.031*SL	0.11 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

MX2D2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S to Y0	tPLH	0.58	0.53 + 0.023*SL	0.54 + 0.020*SL	0.55 + 0.019*SL
	tPHL	0.40	0.36 + 0.021*SL	0.38 + 0.011*SL	0.43 + 0.009*SL
	tR	0.19	0.10 + 0.045*SL	0.10 + 0.044*SL	0.07 + 0.045*SL
	tF	0.17	0.12 + 0.026*SL	0.15 + 0.016*SL	0.14 + 0.017*SL
D00 to Y0	tPLH	0.25	0.20 + 0.022*SL	0.21 + 0.020*SL	0.23 + 0.019*SL
	tPHL	0.42	0.38 + 0.020*SL	0.41 + 0.012*SL	0.47 + 0.009*SL
	tR	0.20	0.11 + 0.043*SL	0.11 + 0.044*SL	0.08 + 0.045*SL
	tF	0.18	0.14 + 0.020*SL	0.15 + 0.016*SL	0.15 + 0.017*SL
D10 to Y0	tPLH	0.24	0.20 + 0.022*SL	0.21 + 0.020*SL	0.22 + 0.019*SL
	tPHL	0.42	0.38 + 0.020*SL	0.41 + 0.012*SL	0.47 + 0.009*SL
	tR	0.20	0.11 + 0.043*SL	0.11 + 0.043*SL	0.08 + 0.045*SL
	tF	0.18	0.14 + 0.022*SL	0.15 + 0.016*SL	0.15 + 0.017*SL
S to Y1	tPLH	0.58	0.54 + 0.023*SL	0.55 + 0.020*SL	0.56 + 0.019*SL
	tPHL	0.40	0.36 + 0.019*SL	0.38 + 0.011*SL	0.43 + 0.009*SL
	tR	0.19	0.09 + 0.047*SL	0.10 + 0.044*SL	0.07 + 0.045*SL
	tF	0.17	0.11 + 0.026*SL	0.15 + 0.016*SL	0.14 + 0.016*SL
D01 to Y1	tPLH	0.25	0.21 + 0.020*SL	0.22 + 0.020*SL	0.23 + 0.019*SL
	tPHL	0.42	0.38 + 0.020*SL	0.41 + 0.012*SL	0.47 + 0.009*SL
	tR	0.20	0.13 + 0.034*SL	0.10 + 0.044*SL	0.08 + 0.045*SL
	tF	0.18	0.14 + 0.020*SL	0.15 + 0.016*SL	0.15 + 0.016*SL
D11 to Y1	tPLH	0.25	0.21 + 0.020*SL	0.21 + 0.020*SL	0.23 + 0.019*SL
	tPHL	0.42	0.38 + 0.020*SL	0.40 + 0.012*SL	0.47 + 0.009*SL
	tR	0.20	0.14 + 0.032*SL	0.10 + 0.044*SL	0.08 + 0.045*SL
	tF	0.18	0.14 + 0.022*SL	0.15 + 0.016*SL	0.15 + 0.016*SL
S to Y2	tPLH	0.58	0.54 + 0.022*SL	0.54 + 0.020*SL	0.56 + 0.019*SL
	tPHL	0.40	0.36 + 0.019*SL	0.38 + 0.011*SL	0.43 + 0.009*SL
	tR	0.19	0.09 + 0.046*SL	0.10 + 0.044*SL	0.07 + 0.045*SL
	tF	0.17	0.11 + 0.026*SL	0.15 + 0.016*SL	0.14 + 0.016*SL
D02 to Y2	tPLH	0.25	0.21 + 0.021*SL	0.21 + 0.020*SL	0.23 + 0.019*SL
	tPHL	0.42	0.38 + 0.020*SL	0.41 + 0.012*SL	0.47 + 0.009*SL
	tR	0.20	0.13 + 0.037*SL	0.11 + 0.044*SL	0.08 + 0.045*SL
	tF	0.18	0.14 + 0.020*SL	0.15 + 0.016*SL	0.15 + 0.016*SL
D12 to Y2	tPLH	0.25	0.20 + 0.023*SL	0.21 + 0.020*SL	0.23 + 0.019*SL
	tPHL	0.42	0.37 + 0.022*SL	0.40 + 0.012*SL	0.47 + 0.009*SL
	tR	0.19	0.11 + 0.040*SL	0.10 + 0.044*SL	0.08 + 0.045*SL
	tF	0.18	0.13 + 0.022*SL	0.15 + 0.016*SL	0.15 + 0.016*SL
S to Y3	tPLH	0.58	0.53 + 0.022*SL	0.54 + 0.020*SL	0.55 + 0.019*SL
	tPHL	0.40	0.36 + 0.021*SL	0.38 + 0.011*SL	0.43 + 0.009*SL
	tR	0.19	0.09 + 0.046*SL	0.10 + 0.044*SL	0.07 + 0.045*SL
	tF	0.17	0.12 + 0.026*SL	0.15 + 0.016*SL	0.14 + 0.017*SL

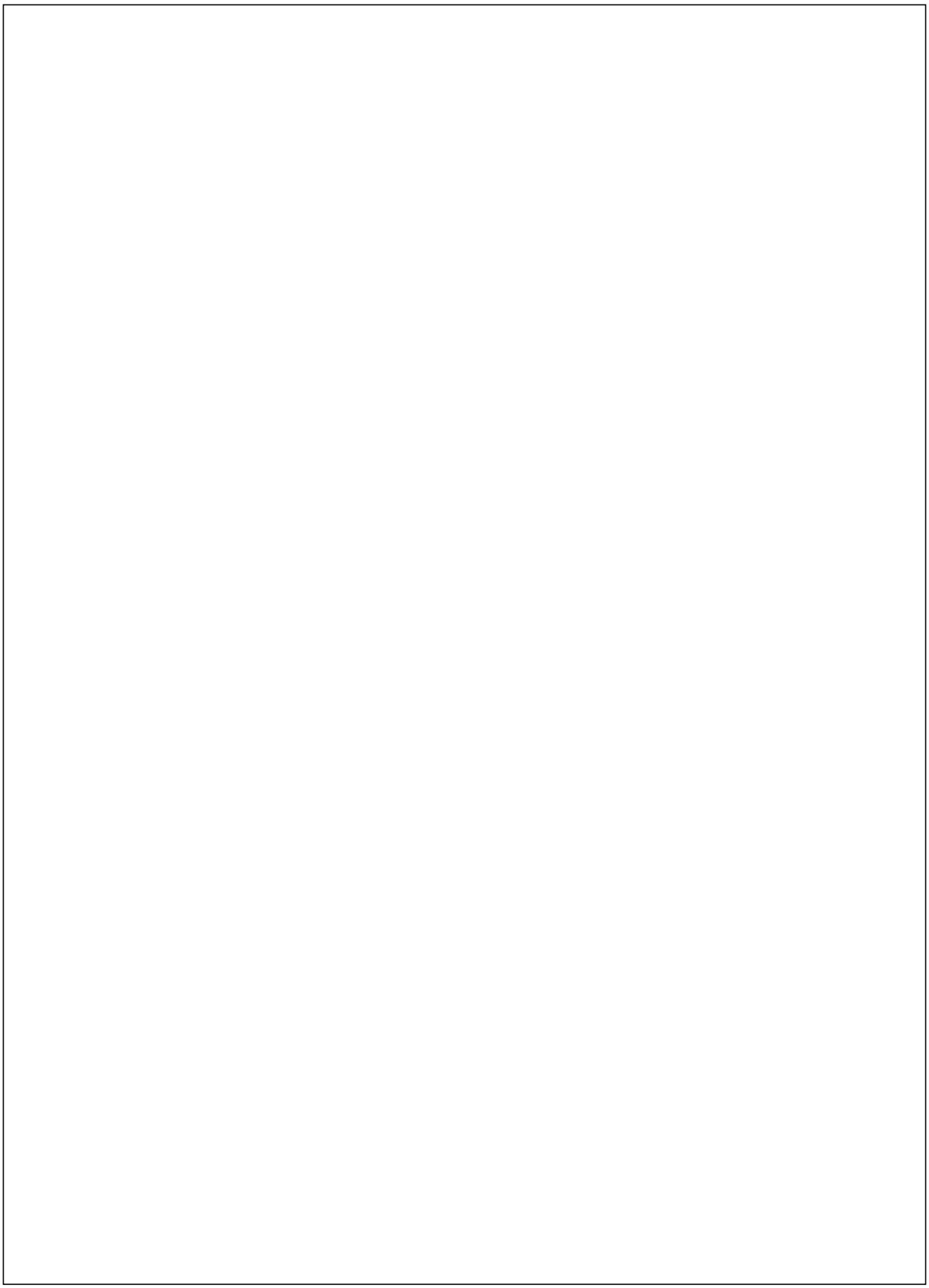
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

MX2D2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D03 to Y3	t_{PLH}	0.25	0.20 + 0.022*SL	0.21 + 0.020*SL	0.23 + 0.019*SL
	t_{PHL}	0.42	0.38 + 0.020*SL	0.41 + 0.012*SL	0.47 + 0.009*SL
	t_R	0.20	0.11 + 0.043*SL	0.11 + 0.044*SL	0.08 + 0.045*SL
	t_F	0.18	0.14 + 0.020*SL	0.15 + 0.016*SL	0.15 + 0.017*SL
D13 to Y3	t_{PLH}	0.24	0.20 + 0.022*SL	0.21 + 0.020*SL	0.22 + 0.019*SL
	t_{PHL}	0.42	0.38 + 0.020*SL	0.41 + 0.012*SL	0.47 + 0.009*SL
	t_R	0.20	0.11 + 0.043*SL	0.11 + 0.043*SL	0.08 + 0.045*SL
	t_F	0.18	0.14 + 0.020*SL	0.15 + 0.016*SL	0.15 + 0.017*SL

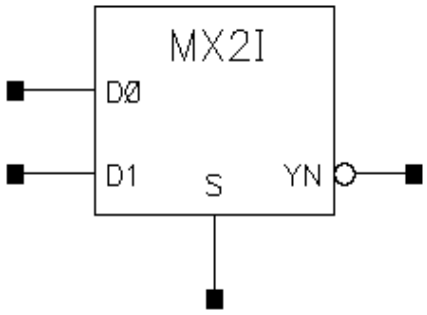
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL



Inputs: D0, D1, S
Output: YN
Input Loading (SL): S: All : 2
- MX2I: D0, D1: 3
- MX2ID2: D0, D1: 4
- MX2ID3: D0, D1: 5

Maximum Fanout (Rec. SL):
- MX2I: 28
- MX2ID2: 56
- MX2ID3: 84

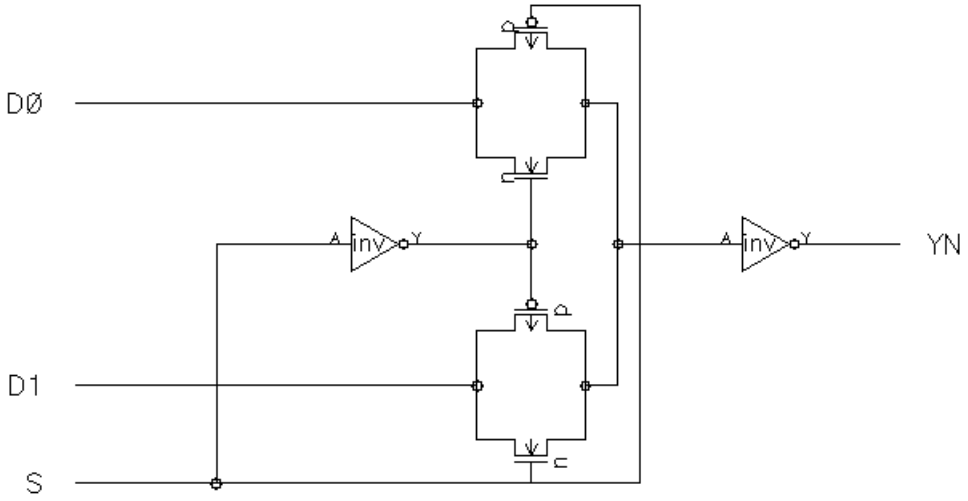
Gate Count:
- MX21: 2
- MX21D2: 3
- MX2ID3: 3



Symbol

S	D0	D1	YN
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Truth Table



Schematic

MX2I Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	tPLH	0.34	0.24 + 0.045*SL	0.27 + 0.037*SL	0.27 + 0.037*SL
	tPHL	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.016*SL
	tR	0.36	0.21 + 0.079*SL	0.20 + 0.081*SL	0.10 + 0.085*SL
	tF	0.30	0.22 + 0.039*SL	0.26 + 0.029*SL	0.24 + 0.030*SL
D1 to YN	tPLH	0.33	0.24 + 0.045*SL	0.27 + 0.037*SL	0.27 + 0.037*SL
	tPHL	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.016*SL
	tR	0.36	0.21 + 0.078*SL	0.20 + 0.081*SL	0.10 + 0.085*SL
	tF	0.30	0.22 + 0.040*SL	0.26 + 0.029*SL	0.24 + 0.030*SL
S to YN	tPLH	0.15	0.07 + 0.038*SL	0.07 + 0.037*SL	0.08 + 0.037*SL
	tPHL	0.32	0.27 + 0.024*SL	0.29 + 0.017*SL	0.30 + 0.016*SL
	tR	0.25	0.09 + 0.079*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	tF	0.15	0.09 + 0.027*SL	0.08 + 0.031*SL	0.05 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

MX2ID2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	tPLH	0.30	0.24 + 0.025*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	tPHL	0.04	-0.01 + 0.027*SL	0.03 + 0.015*SL	0.12 + 0.010*SL
	tR	0.29	0.20 + 0.043*SL	0.22 + 0.037*SL	0.16 + 0.040*SL
	tF	0.27	0.22 + 0.026*SL	0.25 + 0.015*SL	0.28 + 0.014*SL
D1 to YN	tPLH	0.29	0.24 + 0.025*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	tPHL	0.04	-0.01 + 0.027*SL	0.03 + 0.015*SL	0.13 + 0.010*SL
	tR	0.29	0.20 + 0.043*SL	0.22 + 0.037*SL	0.15 + 0.040*SL
	tF	0.28	0.22 + 0.027*SL	0.26 + 0.015*SL	0.28 + 0.014*SL
S to YN	tPLH	0.15	0.10 + 0.022*SL	0.11 + 0.018*SL	0.11 + 0.018*SL
	tPHL	0.32	0.30 + 0.013*SL	0.31 + 0.010*SL	0.34 + 0.008*SL
	tR	0.18	0.10 + 0.040*SL	0.10 + 0.040*SL	0.06 + 0.042*SL
	tF	0.12	0.10 + 0.015*SL	0.09 + 0.016*SL	0.10 + 0.015*SL

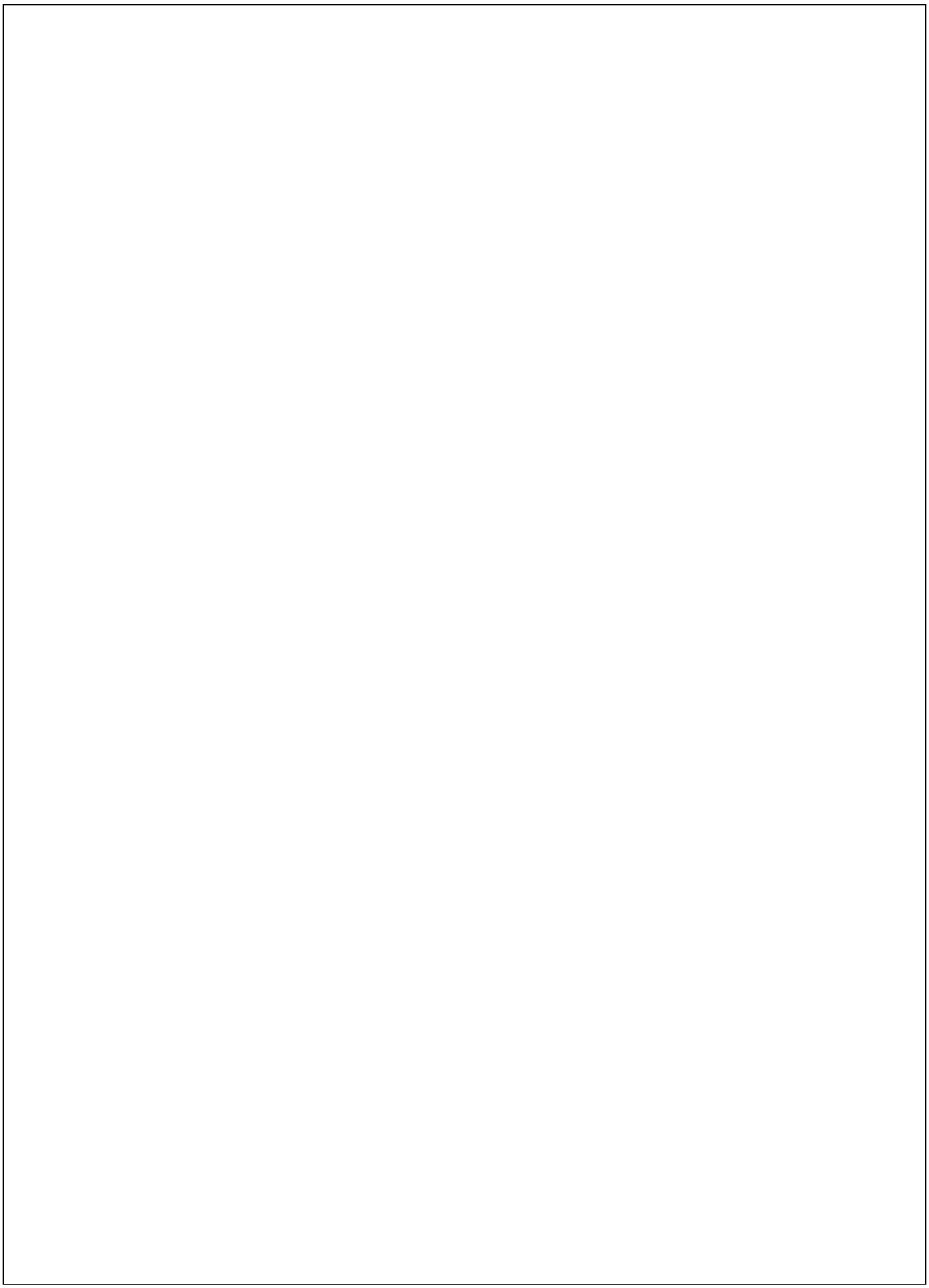
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

MX2ID3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	t_{PLH}	0.30	0.26 + 0.020*SL	0.27 + 0.014*SL	0.30 + 0.012*SL
	t_{PHL}	0.04	0.01 + 0.017*SL	0.03 + 0.012*SL	0.10 + 0.008*SL
	t_R	0.27	0.21 + 0.030*SL	0.22 + 0.026*SL	0.18 + 0.028*SL
	t_F	0.27	0.24 + 0.014*SL	0.25 + 0.012*SL	0.28 + 0.010*SL
D1 to YN	t_{PLH}	0.29	0.25 + 0.021*SL	0.27 + 0.014*SL	0.30 + 0.012*SL
	t_{PHL}	0.04	0.00 + 0.020*SL	0.03 + 0.012*SL	0.10 + 0.008*SL
	t_R	0.26	0.21 + 0.027*SL	0.21 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.27	0.25 + 0.010*SL	0.25 + 0.012*SL	0.28 + 0.010*SL
S to YN	t_{PLH}	0.16	0.14 + 0.014*SL	0.14 + 0.013*SL	0.15 + 0.013*SL
	t_{PHL}	0.34	0.32 + 0.009*SL	0.32 + 0.008*SL	0.36 + 0.006*SL
	t_R	0.17	0.12 + 0.024*SL	0.11 + 0.028*SL	0.08 + 0.029*SL
	t_F	0.12	0.11 + 0.009*SL	0.10 + 0.011*SL	0.11 + 0.011*SL

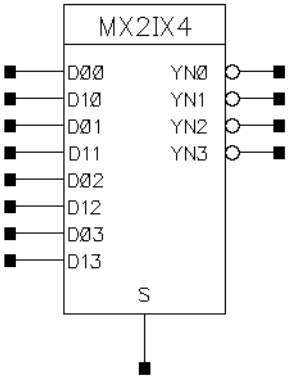
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL



Inputs: D00, D10, D01, D11, D02, D12, D03, D13, S
Outputs: YN0, YN1, YN2, YN3
Input Loading (SL):
- MX2IX4: D00, D10, D01, D11, , D12,D03, D13: 3, S: 1
- MX2ID2X4: D00, D10, D01, D11, D02, D12, D03, D13: 4, S: 1

Maximum Fanout (Rec. SL): All
- MX2IX4: 28
- MX2ID2X4: 56

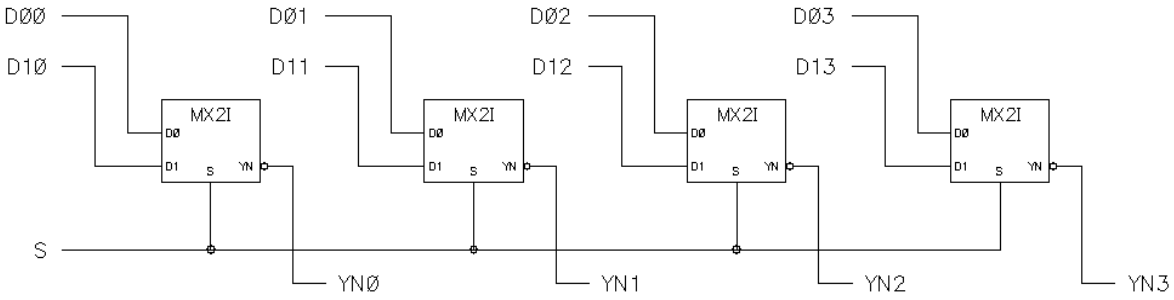
Gate Count:
- MX2IX4: 7
- MX2ID2X4: 9



Symbol

S	$\overline{YN0}$	$\overline{YN1}$	$\overline{YN2}$	$\overline{YN3}$
0	$\overline{D00}$	$\overline{D01}$	$\overline{D02}$	$\overline{D03}$
1	$\overline{D10}$	$\overline{D11}$	$\overline{D12}$	$\overline{D13}$

Truth Table



Schematic

MX2IX4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S to YN0	t_{PLH}	0.43	0.35 + 0.038*SL	0.35 + 0.037*SL	0.35 + 0.037*SL
	t_{PHL}	0.58	0.54 + 0.023*SL	0.55 + 0.017*SL	0.56 + 0.016*SL
	t_R	0.25	0.08 + 0.083*SL	0.08 + 0.085*SL	0.05 + 0.086*SL
	t_F	0.14	0.07 + 0.035*SL	0.08 + 0.032*SL	0.04 + 0.033*SL
D00 to YN0	t_{PLH}	0.33	0.24 + 0.045*SL	0.27 + 0.036*SL	0.27 + 0.036*SL
	t_{PHL}	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.017*SL
	t_R	0.36	0.21 + 0.077*SL	0.20 + 0.080*SL	0.11 + 0.085*SL
	t_F	0.31	0.23 + 0.040*SL	0.26 + 0.029*SL	0.23 + 0.031*SL
D10 to YN0	t_{PLH}	0.33	0.24 + 0.045*SL	0.27 + 0.036*SL	0.27 + 0.036*SL
	t_{PHL}	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.017*SL
	t_R	0.36	0.21 + 0.077*SL	0.20 + 0.080*SL	0.10 + 0.085*SL
	t_F	0.31	0.23 + 0.040*SL	0.26 + 0.029*SL	0.23 + 0.031*SL
S to YN1	t_{PLH}	0.43	0.35 + 0.038*SL	0.35 + 0.037*SL	0.35 + 0.037*SL
	t_{PHL}	0.58	0.53 + 0.023*SL	0.55 + 0.017*SL	0.56 + 0.016*SL
	t_R	0.25	0.08 + 0.083*SL	0.08 + 0.085*SL	0.05 + 0.086*SL
	t_F	0.14	0.07 + 0.035*SL	0.08 + 0.032*SL	0.05 + 0.033*SL
D01 to YN1	t_{PLH}	0.33	0.24 + 0.045*SL	0.27 + 0.036*SL	0.27 + 0.036*SL
	t_{PHL}	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.017*SL
	t_R	0.36	0.21 + 0.077*SL	0.20 + 0.080*SL	0.11 + 0.085*SL
	t_F	0.31	0.23 + 0.040*SL	0.26 + 0.029*SL	0.23 + 0.031*SL
D11 to YN1	t_{PLH}	0.33	0.24 + 0.045*SL	0.27 + 0.036*SL	0.27 + 0.036*SL
	t_{PHL}	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.017*SL
	t_R	0.36	0.21 + 0.077*SL	0.20 + 0.080*SL	0.11 + 0.085*SL
	t_F	0.31	0.23 + 0.040*SL	0.26 + 0.029*SL	0.23 + 0.031*SL
S to YN2	t_{PLH}	0.43	0.35 + 0.038*SL	0.35 + 0.037*SL	0.35 + 0.037*SL
	t_{PHL}	0.58	0.54 + 0.023*SL	0.55 + 0.017*SL	0.56 + 0.016*SL
	t_R	0.25	0.08 + 0.083*SL	0.08 + 0.085*SL	0.05 + 0.086*SL
	t_F	0.14	0.07 + 0.035*SL	0.08 + 0.032*SL	0.04 + 0.033*SL
D02 to YN2	t_{PLH}	0.33	0.24 + 0.045*SL	0.27 + 0.036*SL	0.27 + 0.036*SL
	t_{PHL}	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.017*SL
	t_R	0.36	0.21 + 0.077*SL	0.20 + 0.080*SL	0.11 + 0.085*SL
	t_F	0.31	0.23 + 0.040*SL	0.26 + 0.029*SL	0.23 + 0.031*SL
D12 to YN2	t_{PLH}	0.33	0.24 + 0.045*SL	0.27 + 0.036*SL	0.27 + 0.036*SL
	t_{PHL}	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.017*SL
	t_R	0.36	0.21 + 0.077*SL	0.20 + 0.080*SL	0.10 + 0.085*SL
	t_F	0.31	0.23 + 0.040*SL	0.26 + 0.029*SL	0.23 + 0.031*SL
S to YN3	t_{PLH}	0.43	0.35 + 0.038*SL	0.35 + 0.037*SL	0.35 + 0.037*SL
	t_{PHL}	0.58	0.53 + 0.023*SL	0.55 + 0.017*SL	0.56 + 0.016*SL
	t_R	0.25	0.08 + 0.083*SL	0.08 + 0.085*SL	0.05 + 0.086*SL
	t_F	0.14	0.07 + 0.035*SL	0.08 + 0.032*SL	0.05 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

MX2IX4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D03 to YN3	tPLH	0.33	0.24 + 0.045*SL	0.27 + 0.036*SL	0.27 + 0.036*SL
	tPHL	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.017*SL
	tR	0.36	0.21 + 0.077*SL	0.20 + 0.080*SL	0.11 + 0.085*SL
	tF	0.31	0.23 + 0.040*SL	0.26 + 0.029*SL	0.23 + 0.031*SL
D13 to YN3	tPLH	0.33	0.24 + 0.045*SL	0.27 + 0.036*SL	0.27 + 0.036*SL
	tPHL	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.017*SL
	tR	0.36	0.21 + 0.077*SL	0.20 + 0.080*SL	0.11 + 0.085*SL
	tF	0.31	0.23 + 0.040*SL	0.26 + 0.029*SL	0.23 + 0.031*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

MX2ID2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D00 to YN0	tPLH	0.29	0.24 + 0.027*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	tPHL	0.04	-0.01 + 0.026*SL	0.02 + 0.015*SL	0.12 + 0.010*SL
	tR	0.29	0.21 + 0.039*SL	0.21 + 0.040*SL	0.16 + 0.042*SL
	tF	0.28	0.23 + 0.026*SL	0.26 + 0.016*SL	0.28 + 0.015*SL
D10 to YN0	tPLH	0.29	0.24 + 0.026*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	tPHL	0.04	-0.01 + 0.026*SL	0.02 + 0.015*SL	0.12 + 0.010*SL
	tR	0.30	0.21 + 0.044*SL	0.22 + 0.039*SL	0.16 + 0.042*SL
	tF	0.28	0.23 + 0.026*SL	0.26 + 0.016*SL	0.28 + 0.015*SL
S to YN0	tPLH	0.41	0.37 + 0.021*SL	0.38 + 0.018*SL	0.37 + 0.018*SL
	tPHL	0.57	0.54 + 0.015*SL	0.56 + 0.010*SL	0.59 + 0.008*SL
	tR	0.17	0.08 + 0.045*SL	0.09 + 0.042*SL	0.05 + 0.044*SL
	tF	0.12	0.08 + 0.016*SL	0.08 + 0.016*SL	0.07 + 0.017*SL
D01 to YN1	tPLH	0.29	0.24 + 0.027*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	tPHL	0.04	-0.01 + 0.026*SL	0.02 + 0.015*SL	0.12 + 0.010*SL
	tR	0.29	0.21 + 0.038*SL	0.21 + 0.040*SL	0.16 + 0.042*SL
	tF	0.28	0.23 + 0.026*SL	0.26 + 0.016*SL	0.28 + 0.015*SL
D11 to YN1	tPLH	0.29	0.24 + 0.026*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	tPHL	0.04	-0.01 + 0.026*SL	0.02 + 0.015*SL	0.12 + 0.010*SL
	tR	0.30	0.21 + 0.044*SL	0.22 + 0.039*SL	0.16 + 0.042*SL
	tF	0.28	0.23 + 0.026*SL	0.26 + 0.016*SL	0.28 + 0.015*SL
S to YN1	tPLH	0.41	0.37 + 0.021*SL	0.38 + 0.018*SL	0.38 + 0.018*SL
	tPHL	0.57	0.55 + 0.014*SL	0.56 + 0.010*SL	0.59 + 0.008*SL
	tR	0.17	0.08 + 0.045*SL	0.09 + 0.042*SL	0.05 + 0.044*SL
	tF	0.12	0.09 + 0.015*SL	0.08 + 0.016*SL	0.07 + 0.017*SL
D02 to YN2	tPLH	0.29	0.24 + 0.027*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	tPHL	0.04	-0.01 + 0.026*SL	0.02 + 0.015*SL	0.12 + 0.010*SL
	tR	0.29	0.21 + 0.038*SL	0.21 + 0.040*SL	0.16 + 0.042*SL
	tF	0.28	0.23 + 0.026*SL	0.26 + 0.016*SL	0.28 + 0.015*SL
D12 to YN2	tPLH	0.29	0.24 + 0.026*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	tPHL	0.04	-0.01 + 0.026*SL	0.02 + 0.015*SL	0.12 + 0.010*SL
	tR	0.30	0.21 + 0.044*SL	0.22 + 0.039*SL	0.16 + 0.042*SL
	tF	0.28	0.23 + 0.026*SL	0.26 + 0.016*SL	0.28 + 0.015*SL
S to YN2	tPLH	0.41	0.37 + 0.021*SL	0.38 + 0.018*SL	0.38 + 0.018*SL
	tPHL	0.57	0.55 + 0.014*SL	0.56 + 0.010*SL	0.59 + 0.008*SL
	tR	0.17	0.08 + 0.045*SL	0.09 + 0.042*SL	0.05 + 0.044*SL
	tF	0.12	0.09 + 0.015*SL	0.08 + 0.016*SL	0.07 + 0.017*SL
D03 to YN3	tPLH	0.29	0.24 + 0.027*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	tPHL	0.04	-0.01 + 0.026*SL	0.02 + 0.015*SL	0.12 + 0.010*SL
	tR	0.29	0.21 + 0.039*SL	0.21 + 0.040*SL	0.16 + 0.042*SL
	tF	0.28	0.23 + 0.026*SL	0.26 + 0.016*SL	0.28 + 0.015*SL

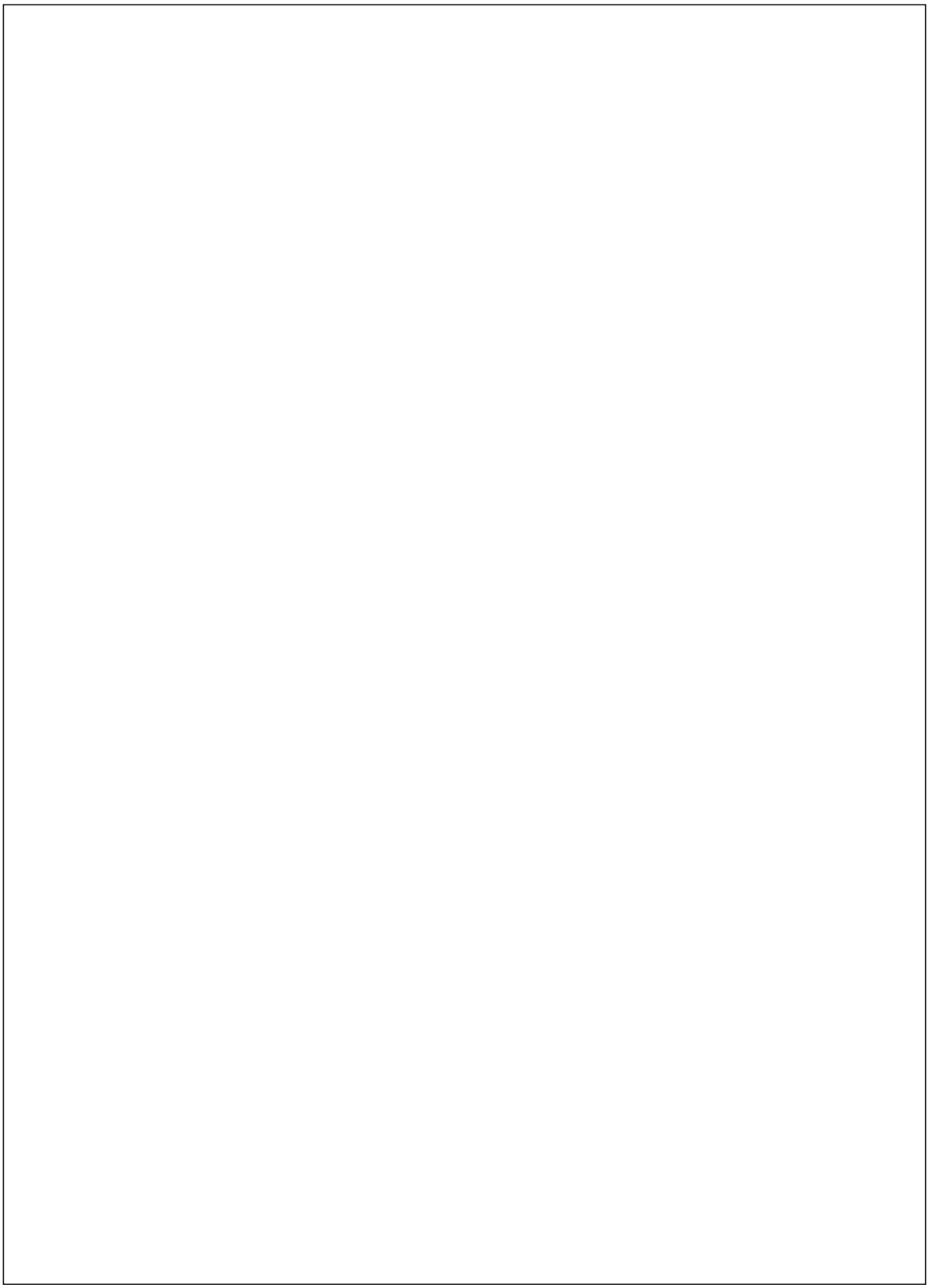
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

MX2ID2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D13 to YN3	t_{PLH}	0.29	0.24 + 0.026*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	t_{PHL}	0.04	-0.01 + 0.026*SL	0.02 + 0.015*SL	0.12 + 0.010*SL
	t_R	0.30	0.21 + 0.044*SL	0.22 + 0.039*SL	0.16 + 0.042*SL
	t_F	0.28	0.23 + 0.026*SL	0.26 + 0.016*SL	0.28 + 0.015*SL
S to YN3	t_{PLH}	0.41	0.37 + 0.021*SL	0.38 + 0.018*SL	0.38 + 0.018*SL
	t_{PHL}	0.57	0.54 + 0.015*SL	0.56 + 0.010*SL	0.59 + 0.008*SL
	t_R	0.17	0.08 + 0.045*SL	0.09 + 0.042*SL	0.05 + 0.044*SL
	t_F	0.12	0.08 + 0.016*SL	0.08 + 0.016*SL	0.07 + 0.017*SL

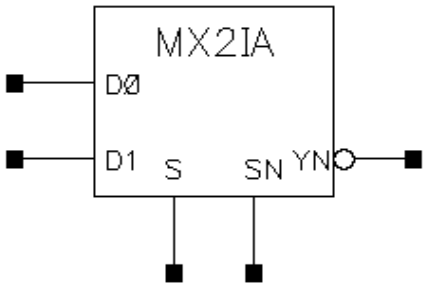
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL



Inputs: D0, D1, S, SN
Output: YN
Input Loading (SL): S, SN: All: 1
- MX2IA: D0, D1: 3
- MX2ID2A: D0, D1: 4
- MX2ID4A: DO: 3, D1: 6

Maximum Fanout (Rec. SL):
- MX2IA: 28
- MX2ID2A: 56
- MX2ID4A: 112

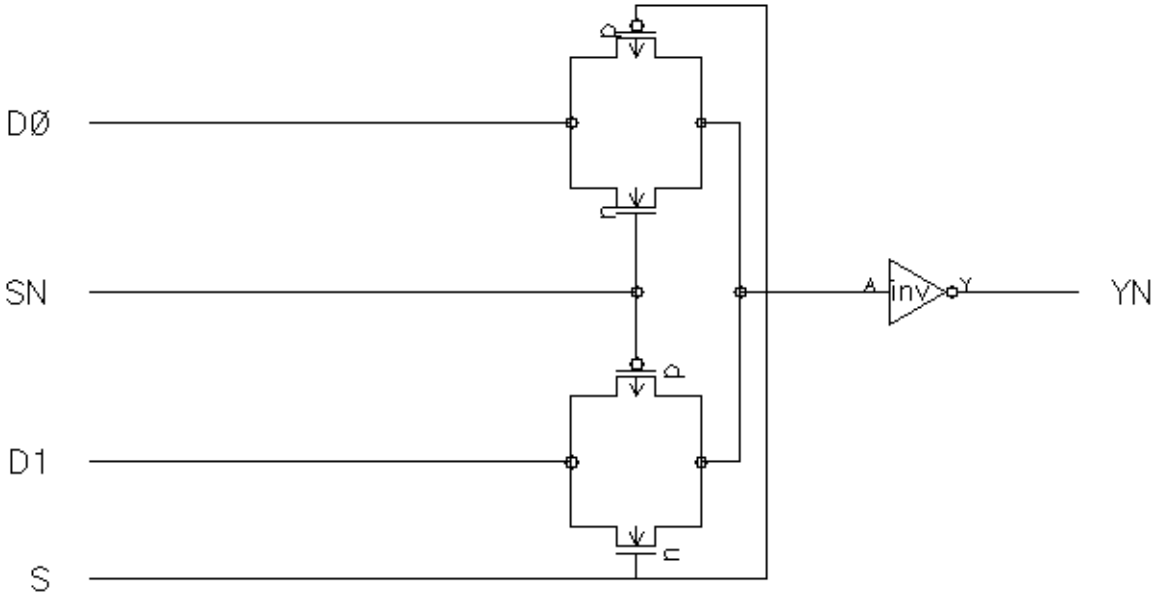
Gate Count:
- MX2IA: 2
- MX2ID2A: 2
- MX2ID4A: 3



Symbol

S	SN	D0	D1	YN
0	1	0	x	1
0	1	1	x	0
1	0	x	0	1
1	0	x	1	0

Truth Table



Schematic

MX2IA Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	t_{PLH}	0.33	0.24 + 0.045*SL	0.27 + 0.036*SL	0.27 + 0.036*SL
	t_{PHL}	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.016*SL
	t_R	0.36	0.21 + 0.073*SL	0.20 + 0.078*SL	0.11 + 0.082*SL
	t_F	0.30	0.22 + 0.040*SL	0.26 + 0.028*SL	0.24 + 0.029*SL
D1 to YN	t_{PLH}	0.33	0.24 + 0.045*SL	0.27 + 0.036*SL	0.27 + 0.036*SL
	t_{PHL}	0.07	-0.02 + 0.044*SL	0.04 + 0.023*SL	0.17 + 0.016*SL
	t_R	0.36	0.21 + 0.073*SL	0.20 + 0.078*SL	0.11 + 0.082*SL
	t_F	0.30	0.22 + 0.040*SL	0.26 + 0.028*SL	0.24 + 0.029*SL
S to YN	t_{PLH}	0.15	0.08 + 0.039*SL	0.08 + 0.036*SL	0.09 + 0.036*SL
	t_{PHL}	0.28	0.23 + 0.024*SL	0.26 + 0.017*SL	0.28 + 0.016*SL
	t_R	0.25	0.10 + 0.077*SL	0.08 + 0.082*SL	0.06 + 0.083*SL
	t_F	0.19	0.13 + 0.028*SL	0.13 + 0.029*SL	0.07 + 0.032*SL
SN to YN	t_{PLH}	0.15	0.08 + 0.039*SL	0.08 + 0.036*SL	0.09 + 0.036*SL
	t_{PHL}	0.28	0.23 + 0.024*SL	0.26 + 0.017*SL	0.28 + 0.016*SL
	t_R	0.25	0.10 + 0.077*SL	0.08 + 0.082*SL	0.06 + 0.083*SL
	t_F	0.19	0.13 + 0.028*SL	0.13 + 0.029*SL	0.07 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

MX2ID2A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	t_{PLH}	0.29	0.24 + 0.026*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	t_{PHL}	0.04	-0.01 + 0.027*SL	0.02 + 0.015*SL	0.13 + 0.010*SL
	t_R	0.29	0.20 + 0.043*SL	0.22 + 0.038*SL	0.15 + 0.041*SL
	t_F	0.28	0.22 + 0.027*SL	0.26 + 0.015*SL	0.28 + 0.014*SL
D1 to YN	t_{PLH}	0.29	0.24 + 0.026*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	t_{PHL}	0.04	-0.01 + 0.027*SL	0.02 + 0.015*SL	0.13 + 0.010*SL
	t_R	0.29	0.20 + 0.043*SL	0.22 + 0.038*SL	0.15 + 0.041*SL
	t_F	0.28	0.22 + 0.027*SL	0.26 + 0.015*SL	0.28 + 0.014*SL
S to YN	t_{PLH}	0.15	0.11 + 0.020*SL	0.12 + 0.018*SL	0.12 + 0.018*SL
	t_{PHL}	0.29	0.26 + 0.014*SL	0.27 + 0.010*SL	0.31 + 0.008*SL
	t_R	0.18	0.08 + 0.047*SL	0.10 + 0.041*SL	0.07 + 0.043*SL
	t_F	0.17	0.15 + 0.012*SL	0.14 + 0.015*SL	0.13 + 0.015*SL
SN to YN	t_{PLH}	0.15	0.11 + 0.020*SL	0.12 + 0.018*SL	0.12 + 0.018*SL
	t_{PHL}	0.29	0.26 + 0.014*SL	0.27 + 0.010*SL	0.31 + 0.008*SL
	t_R	0.18	0.08 + 0.047*SL	0.10 + 0.041*SL	0.07 + 0.043*SL
	t_F	0.17	0.15 + 0.012*SL	0.14 + 0.015*SL	0.13 + 0.015*SL

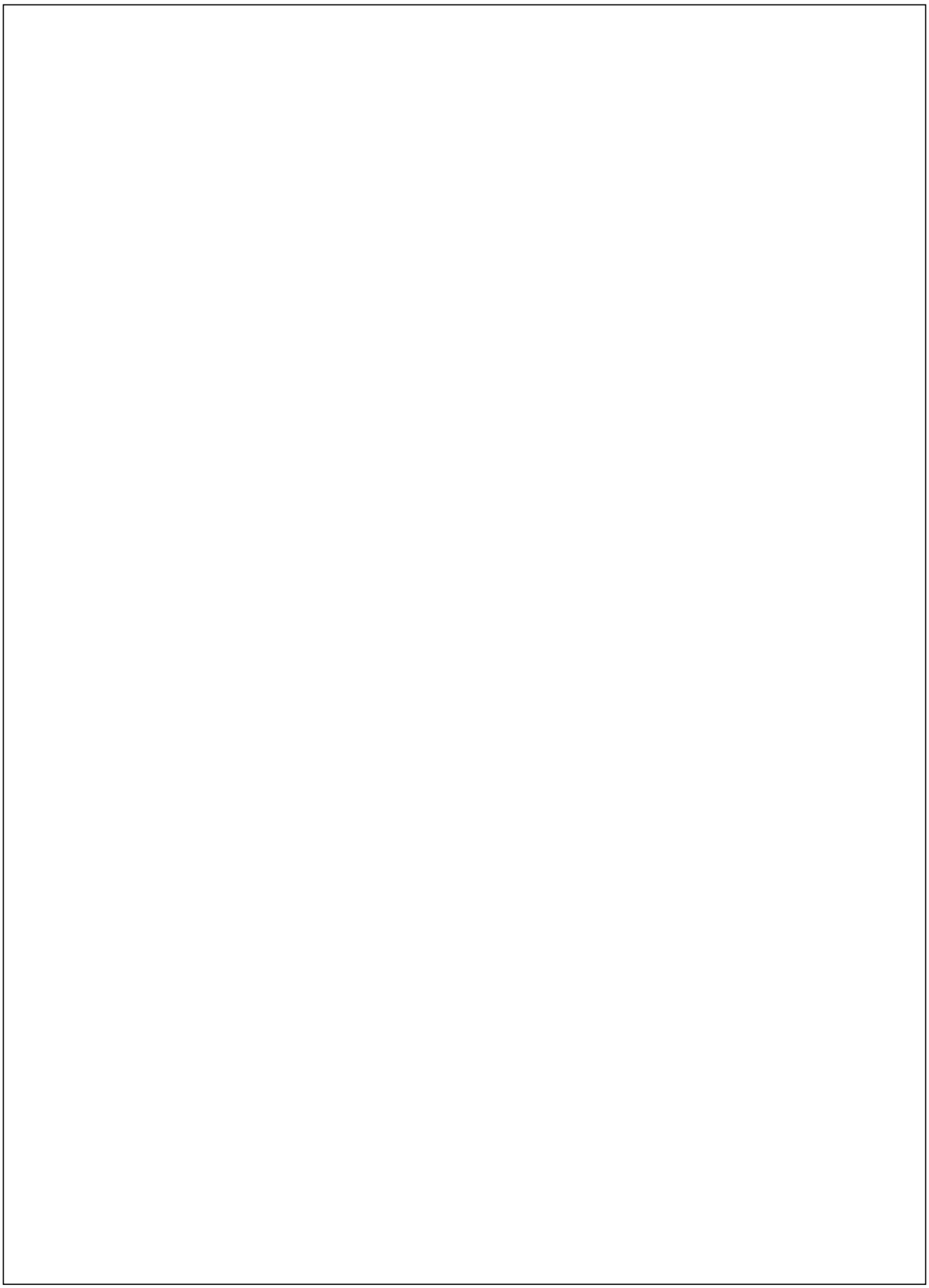
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

MX2ID4A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	t_{PLH}	0.29	0.26 + 0.015*SL	0.28 + 0.011*SL	0.31 + 0.009*SL
	t_{PHL}	0.05	0.02 + 0.014*SL	0.03 + 0.010*SL	0.09 + 0.007*SL
	t_R	0.25	0.20 + 0.024*SL	0.22 + 0.019*SL	0.19 + 0.021*SL
	t_F	0.27	0.26 + 0.007*SL	0.25 + 0.009*SL	0.28 + 0.008*SL
D1 to YN	t_{PLH}	0.29	0.26 + 0.015*SL	0.28 + 0.011*SL	0.31 + 0.009*SL
	t_{PHL}	0.05	0.02 + 0.014*SL	0.03 + 0.010*SL	0.09 + 0.007*SL
	t_R	0.25	0.20 + 0.024*SL	0.22 + 0.019*SL	0.19 + 0.021*SL
	t_F	0.27	0.26 + 0.007*SL	0.25 + 0.009*SL	0.28 + 0.008*SL
S to YN	t_{PLH}	0.20	0.18 + 0.011*SL	0.18 + 0.010*SL	0.19 + 0.009*SL
	t_{PHL}	0.31	0.29 + 0.010*SL	0.30 + 0.007*SL	0.34 + 0.005*SL
	t_R	0.15	0.11 + 0.019*SL	0.11 + 0.021*SL	0.09 + 0.022*SL
	t_F	0.18	0.17 + 0.006*SL	0.16 + 0.009*SL	0.18 + 0.007*SL
SN to YN	t_{PLH}	0.20	0.18 + 0.011*SL	0.18 + 0.010*SL	0.19 + 0.009*SL
	t_{PHL}	0.31	0.29 + 0.010*SL	0.30 + 0.007*SL	0.34 + 0.005*SL
	t_R	0.15	0.11 + 0.019*SL	0.11 + 0.021*SL	0.09 + 0.022*SL
	t_F	0.18	0.17 + 0.006*SL	0.16 + 0.009*SL	0.18 + 0.007*SL

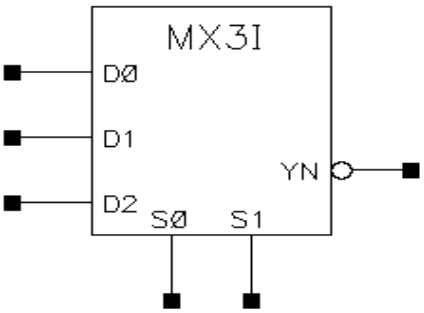
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL



Inputs: D0, D1, D2, S0, S1
Output: YN
Input Loading (SL):
- MX3I: D0, D1: 3, D2:1, S0, S1:2
- MX3ID2: D0, D1:6, D2:4,S0,S1:2
- MX3ID4: D0, D1: 3, D2: 6,
  S0, S1: 2

Maximum Fanout (Rec. SL):
- MX3: 14
- MX3ID2: 56
- MX3ID: 112

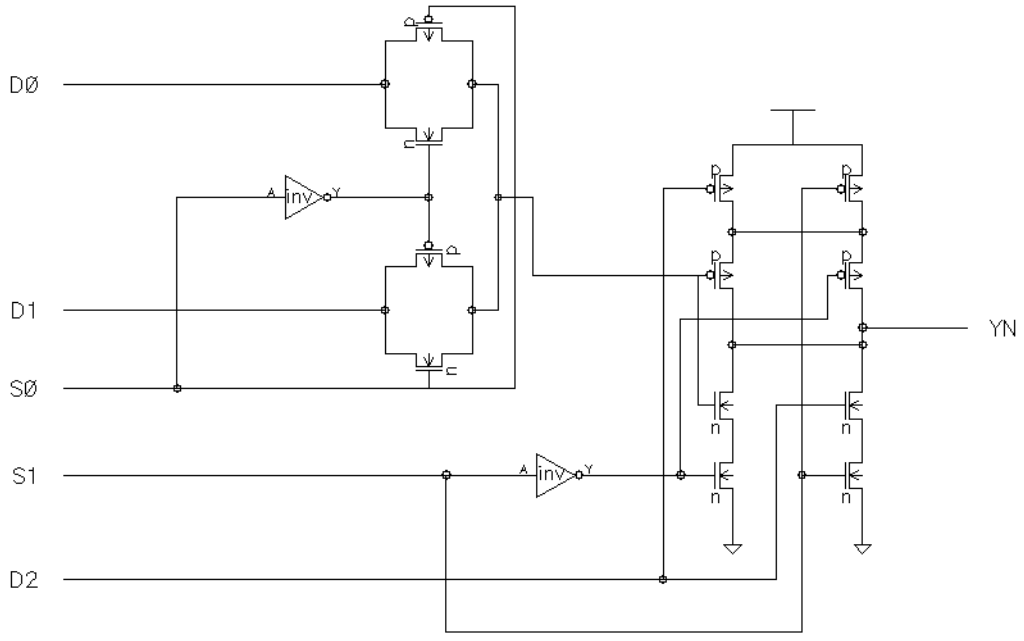
Gate Count:
- MX3I: 4
- MX3ID2: 5
- MX3ID4: 6



Symbol

S0	S1	YN
0	0	$\overline{D0}$
1	0	$\overline{D1}$
x	1	$\overline{D2}$

Truth Table



Schematic

MX3I Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN	t_{PLH}	0.32	0.18 + 0.073*SL	0.18 + 0.072*SL	0.19 + 0.072*SL
	t_{PHL}	0.37	0.31 + 0.032*SL	0.33 + 0.026*SL	0.34 + 0.026*SL
	t_R	0.63	0.31 + 0.163*SL	0.29 + 0.168*SL	0.29 + 0.168*SL
	t_F	0.27	0.17 + 0.053*SL	0.16 + 0.056*SL	0.12 + 0.058*SL
S1 to YN	t_{PLH}	0.27	0.13 + 0.070*SL	0.13 + 0.071*SL	0.14 + 0.071*SL
	t_{PHL}	0.35	0.29 + 0.030*SL	0.30 + 0.026*SL	0.31 + 0.026*SL
	t_R	0.61	0.29 + 0.162*SL	0.28 + 0.165*SL	0.28 + 0.165*SL
	t_F	0.22	0.11 + 0.055*SL	0.10 + 0.057*SL	0.07 + 0.058*SL
D0 to YN	t_{PLH}	0.52	0.38 + 0.071*SL	0.38 + 0.071*SL	0.36 + 0.072*SL
	t_{PHL}	0.16	0.06 + 0.049*SL	0.12 + 0.030*SL	0.21 + 0.026*SL
	t_R	0.70	0.39 + 0.157*SL	0.37 + 0.165*SL	0.29 + 0.168*SL
	t_F	0.43	0.32 + 0.057*SL	0.34 + 0.052*SL	0.26 + 0.056*SL
D1 to YN	t_{PLH}	0.52	0.38 + 0.071*SL	0.38 + 0.071*SL	0.36 + 0.072*SL
	t_{PHL}	0.16	0.07 + 0.049*SL	0.12 + 0.030*SL	0.21 + 0.026*SL
	t_R	0.70	0.39 + 0.156*SL	0.37 + 0.165*SL	0.29 + 0.168*SL
	t_F	0.44	0.33 + 0.054*SL	0.34 + 0.052*SL	0.26 + 0.056*SL
D2 to YN	t_{PLH}	0.47	0.33 + 0.070*SL	0.33 + 0.070*SL	0.31 + 0.070*SL
	t_{PHL}	0.17	0.08 + 0.043*SL	0.13 + 0.029*SL	0.19 + 0.026*SL
	t_R	0.70	0.40 + 0.150*SL	0.36 + 0.161*SL	0.29 + 0.165*SL
	t_F	0.49	0.39 + 0.048*SL	0.38 + 0.051*SL	0.29 + 0.056*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

MX3ID2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN	t_{PLH}	0.33	0.28 + 0.023*SL	0.30 + 0.019*SL	0.31 + 0.018*SL
	t_{PHL}	0.53	0.51 + 0.013*SL	0.51 + 0.012*SL	0.57 + 0.009*SL
	t_R	0.17	0.09 + 0.039*SL	0.09 + 0.041*SL	0.07 + 0.042*SL
	t_F	0.16	0.13 + 0.015*SL	0.13 + 0.016*SL	0.14 + 0.016*SL
S1 to YN	t_{PLH}	0.12	0.08 + 0.020*SL	0.09 + 0.018*SL	0.09 + 0.018*SL
	t_{PHL}	0.38	0.34 + 0.018*SL	0.36 + 0.012*SL	0.42 + 0.009*SL
	t_R	0.17	0.10 + 0.036*SL	0.08 + 0.041*SL	0.06 + 0.042*SL
	t_F	0.15	0.10 + 0.024*SL	0.12 + 0.017*SL	0.14 + 0.016*SL
D0 to YN	t_{PLH}	0.50	0.46 + 0.023*SL	0.47 + 0.018*SL	0.48 + 0.018*SL
	t_{PHL}	0.28	0.24 + 0.020*SL	0.27 + 0.012*SL	0.32 + 0.009*SL
	t_R	0.17	0.10 + 0.036*SL	0.08 + 0.041*SL	0.07 + 0.042*SL
	t_F	0.16	0.14 + 0.012*SL	0.12 + 0.017*SL	0.14 + 0.016*SL
D1 to YN	t_{PLH}	0.50	0.46 + 0.023*SL	0.47 + 0.018*SL	0.48 + 0.018*SL
	t_{PHL}	0.28	0.25 + 0.019*SL	0.27 + 0.012*SL	0.32 + 0.009*SL
	t_R	0.17	0.10 + 0.036*SL	0.08 + 0.041*SL	0.07 + 0.042*SL
	t_F	0.15	0.11 + 0.020*SL	0.12 + 0.017*SL	0.14 + 0.016*SL
D2 to YN	t_{PLH}	0.29	0.24 + 0.027*SL	0.26 + 0.019*SL	0.29 + 0.018*SL
	t_{PHL}	0.04	-0.01 + 0.027*SL	0.02 + 0.015*SL	0.13 + 0.010*SL
	t_R	0.28	0.21 + 0.037*SL	0.21 + 0.038*SL	0.15 + 0.040*SL
	t_F	0.28	0.22 + 0.028*SL	0.26 + 0.015*SL	0.28 + 0.014*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

MX3ID4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

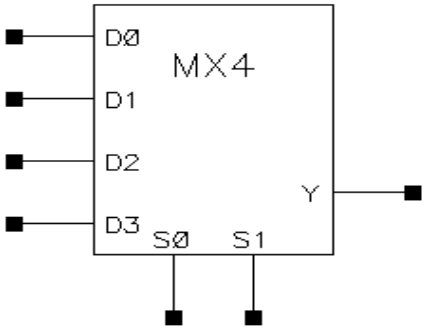
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN	tPLH	0.37	0.34 + 0.012*SL	0.35 + 0.010*SL	0.37 + 0.010*SL
	tPHL	0.57	0.55 + 0.013*SL	0.56 + 0.008*SL	0.61 + 0.006*SL
	tR	0.16	0.12 + 0.017*SL	0.11 + 0.022*SL	0.11 + 0.022*SL
	tF	0.18	0.16 + 0.010*SL	0.16 + 0.010*SL	0.18 + 0.009*SL
S1 to YN	tPLH	0.17	0.15 + 0.011*SL	0.15 + 0.010*SL	0.16 + 0.009*SL
	tPHL	0.42	0.40 + 0.011*SL	0.40 + 0.008*SL	0.45 + 0.006*SL
	tR	0.16	0.13 + 0.014*SL	0.11 + 0.021*SL	0.09 + 0.022*SL
	tF	0.17	0.14 + 0.013*SL	0.15 + 0.011*SL	0.19 + 0.008*SL
D0 to YN	tPLH	0.54	0.52 + 0.013*SL	0.52 + 0.011*SL	0.54 + 0.009*SL
	tPHL	0.32	0.30 + 0.012*SL	0.31 + 0.008*SL	0.36 + 0.006*SL
	tR	0.16	0.12 + 0.021*SL	0.12 + 0.021*SL	0.11 + 0.022*SL
	tF	0.18	0.16 + 0.013*SL	0.17 + 0.010*SL	0.19 + 0.009*SL
D1 to YN	tPLH	0.54	0.52 + 0.013*SL	0.52 + 0.011*SL	0.54 + 0.010*SL
	tPHL	0.32	0.30 + 0.012*SL	0.31 + 0.008*SL	0.36 + 0.006*SL
	tR	0.16	0.12 + 0.021*SL	0.12 + 0.021*SL	0.11 + 0.022*SL
	tF	0.18	0.16 + 0.013*SL	0.17 + 0.010*SL	0.19 + 0.009*SL
D2 to YN	tPLH	0.29	0.26 + 0.015*SL	0.27 + 0.011*SL	0.31 + 0.009*SL
	tPHL	0.05	0.02 + 0.014*SL	0.03 + 0.010*SL	0.09 + 0.007*SL
	tR	0.25	0.21 + 0.024*SL	0.22 + 0.020*SL	0.19 + 0.021*SL
	tF	0.27	0.26 + 0.007*SL	0.25 + 0.009*SL	0.28 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: D0, D1, D2, D3, S0, S1
Outputs: Y
Input Loading (SL):
- D0, D1, D2, D3, S0: 3
- S1: 2

Maximum Fanout (Rec. SL):
MX4: 28
MX4D2: 56

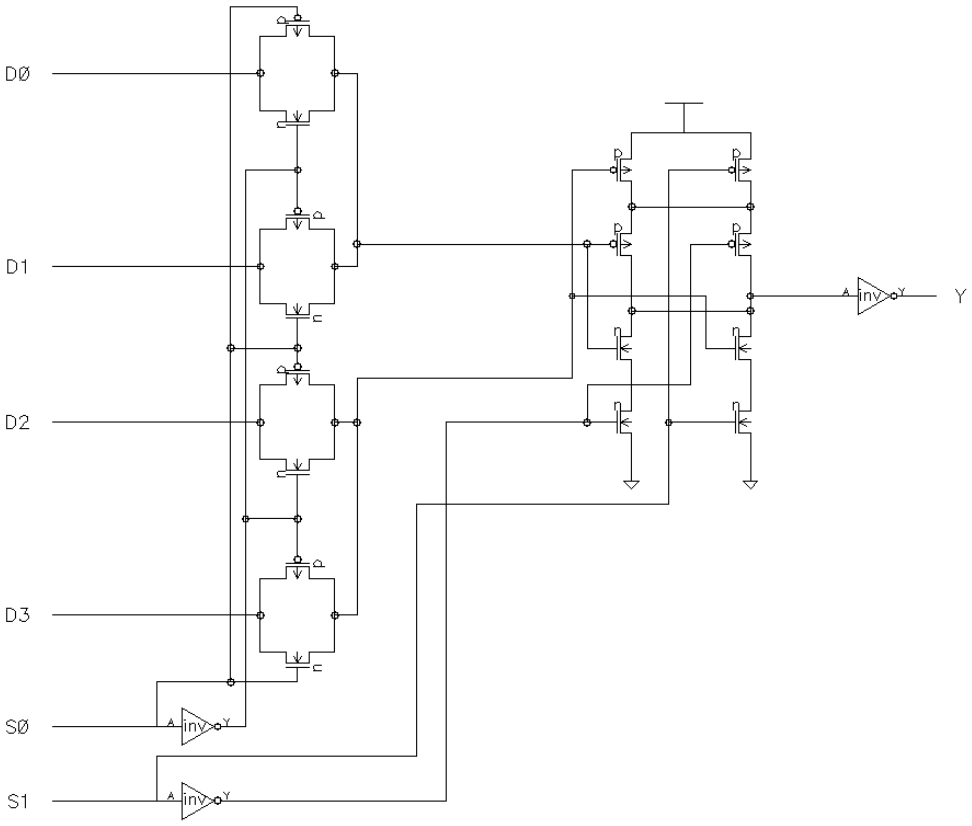
Gate Count: 6



Symbol

S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Truth Table



Schematic

MX4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Y	tPLH	0.28	0.19 + 0.042*SL	0.21 + 0.038*SL	0.21 + 0.038*SL
	tPHL	0.51	0.44 + 0.031*SL	0.48 + 0.020*SL	0.53 + 0.017*SL
	tR	0.28	0.12 + 0.082*SL	0.10 + 0.086*SL	0.07 + 0.088*SL
	tF	0.21	0.14 + 0.034*SL	0.15 + 0.032*SL	0.12 + 0.033*SL
D1 to Y	tPLH	0.28	0.19 + 0.042*SL	0.21 + 0.038*SL	0.21 + 0.038*SL
	tPHL	0.50	0.44 + 0.031*SL	0.48 + 0.020*SL	0.53 + 0.017*SL
	tR	0.28	0.12 + 0.082*SL	0.10 + 0.086*SL	0.07 + 0.088*SL
	tF	0.21	0.14 + 0.034*SL	0.15 + 0.032*SL	0.12 + 0.033*SL
D2 to Y	tPLH	0.34	0.25 + 0.042*SL	0.27 + 0.038*SL	0.27 + 0.037*SL
	tPHL	0.49	0.42 + 0.034*SL	0.46 + 0.020*SL	0.52 + 0.017*SL
	tR	0.29	0.12 + 0.086*SL	0.12 + 0.086*SL	0.07 + 0.088*SL
	tF	0.21	0.13 + 0.041*SL	0.16 + 0.031*SL	0.12 + 0.033*SL
D3 to Y	tPLH	0.34	0.25 + 0.043*SL	0.27 + 0.038*SL	0.27 + 0.037*SL
	tPHL	0.49	0.42 + 0.034*SL	0.46 + 0.020*SL	0.52 + 0.017*SL
	tR	0.29	0.11 + 0.087*SL	0.12 + 0.086*SL	0.07 + 0.088*SL
	tF	0.21	0.13 + 0.040*SL	0.16 + 0.032*SL	0.12 + 0.033*SL
S0 to Y	tPLH	0.53	0.44 + 0.043*SL	0.46 + 0.038*SL	0.46 + 0.038*SL
	tPHL	0.35	0.29 + 0.032*SL	0.32 + 0.019*SL	0.38 + 0.017*SL
	tR	0.27	0.10 + 0.082*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
	tF	0.20	0.11 + 0.044*SL	0.15 + 0.032*SL	0.11 + 0.033*SL
S1 to Y	tPLH	0.46	0.38 + 0.041*SL	0.39 + 0.038*SL	0.39 + 0.038*SL
	tPHL	0.27	0.21 + 0.028*SL	0.24 + 0.019*SL	0.29 + 0.017*SL
	tR	0.26	0.09 + 0.084*SL	0.08 + 0.087*SL	0.05 + 0.088*SL
	tF	0.20	0.13 + 0.035*SL	0.13 + 0.032*SL	0.11 + 0.033*SL

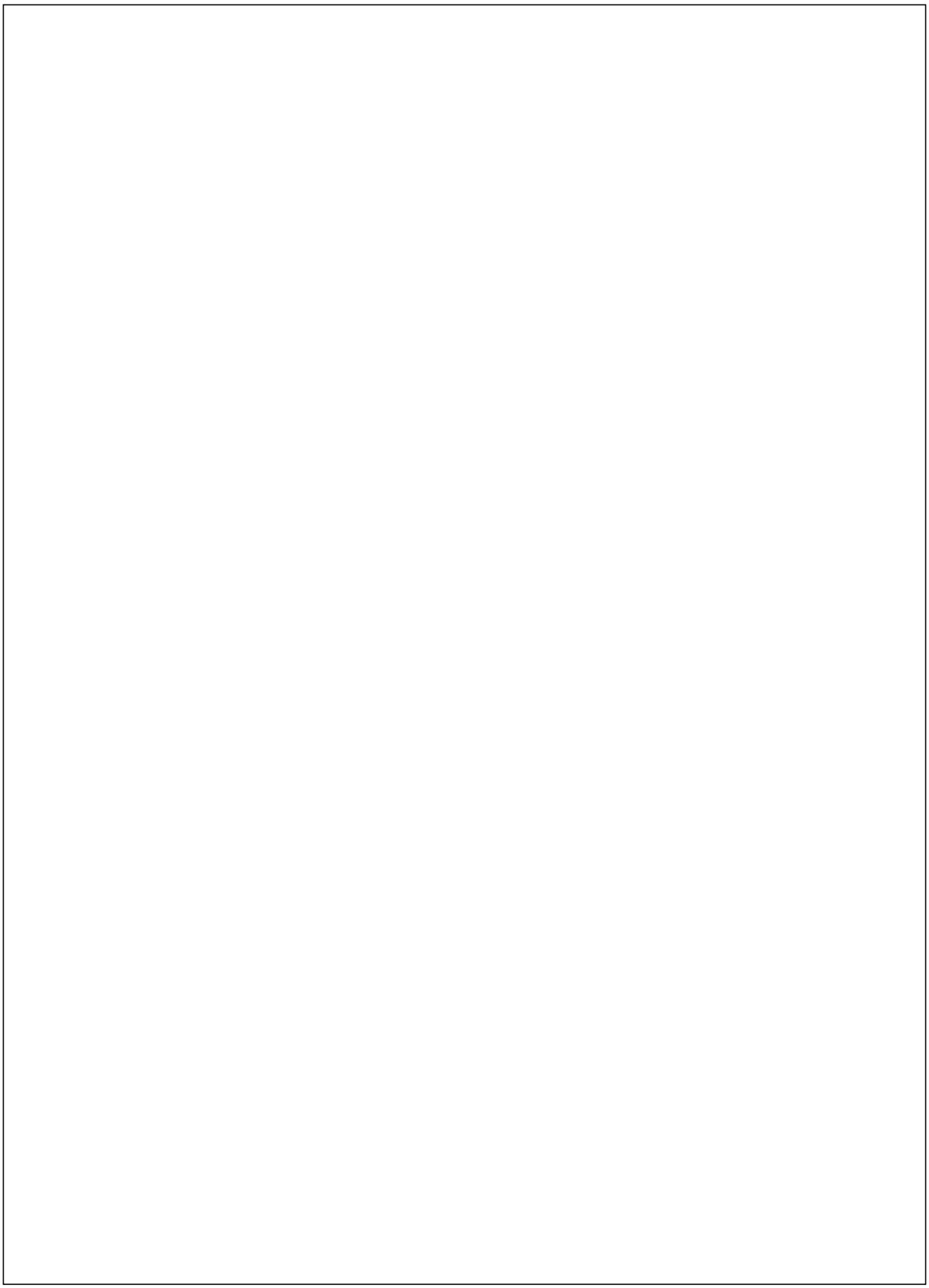
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

MX4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Y	t_{PLH}	0.29	0.24 + 0.023*SL	0.26 + 0.019*SL	0.27 + 0.019*SL
	t_{PHL}	0.53	0.49 + 0.021*SL	0.52 + 0.013*SL	0.58 + 0.009*SL
	t_R	0.21	0.12 + 0.046*SL	0.13 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.20	0.16 + 0.020*SL	0.17 + 0.016*SL	0.18 + 0.016*SL
D1 to Y	t_{PLH}	0.29	0.24 + 0.024*SL	0.26 + 0.019*SL	0.27 + 0.019*SL
	t_{PHL}	0.53	0.49 + 0.019*SL	0.51 + 0.013*SL	0.58 + 0.009*SL
	t_R	0.21	0.12 + 0.046*SL	0.13 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.21	0.17 + 0.018*SL	0.18 + 0.016*SL	0.19 + 0.016*SL
D2 to Y	t_{PLH}	0.34	0.30 + 0.020*SL	0.30 + 0.019*SL	0.32 + 0.019*SL
	t_{PHL}	0.52	0.47 + 0.021*SL	0.50 + 0.012*SL	0.56 + 0.009*SL
	t_R	0.21	0.13 + 0.038*SL	0.12 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.21	0.16 + 0.022*SL	0.18 + 0.016*SL	0.19 + 0.016*SL
D3 to Y	t_{PLH}	0.34	0.30 + 0.023*SL	0.31 + 0.019*SL	0.32 + 0.019*SL
	t_{PHL}	0.52	0.47 + 0.021*SL	0.50 + 0.013*SL	0.56 + 0.009*SL
	t_R	0.21	0.12 + 0.042*SL	0.12 + 0.043*SL	0.10 + 0.044*SL
	t_F	0.21	0.17 + 0.021*SL	0.18 + 0.016*SL	0.19 + 0.016*SL
S0 to Y	t_{PLH}	0.52	0.47 + 0.026*SL	0.49 + 0.019*SL	0.50 + 0.019*SL
	t_{PHL}	0.38	0.34 + 0.020*SL	0.36 + 0.012*SL	0.43 + 0.009*SL
	t_R	0.20	0.12 + 0.040*SL	0.11 + 0.043*SL	0.09 + 0.044*SL
	t_F	0.19	0.14 + 0.026*SL	0.17 + 0.016*SL	0.17 + 0.016*SL
S1 to Y	t_{PLH}	0.45	0.40 + 0.026*SL	0.42 + 0.019*SL	0.42 + 0.019*SL
	t_{PHL}	0.29	0.25 + 0.021*SL	0.27 + 0.012*SL	0.33 + 0.009*SL
	t_R	0.18	0.11 + 0.039*SL	0.09 + 0.044*SL	0.07 + 0.045*SL
	t_F	0.19	0.15 + 0.022*SL	0.16 + 0.017*SL	0.18 + 0.015*SL

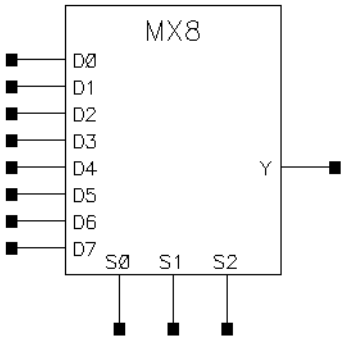
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL



Inputs: D0, D1, D2, D3, D4, D5, D6, D7
S0, S1, S2
Outputs: Y
Input Loading (SL):
- S0: 1
- S2: 2
- D0, D1, D2, D3, D4, D5, D6, D7, S1: 3

Maximum Fanout (Rec. SL):
- MX8: 28
- MX8D2: 56

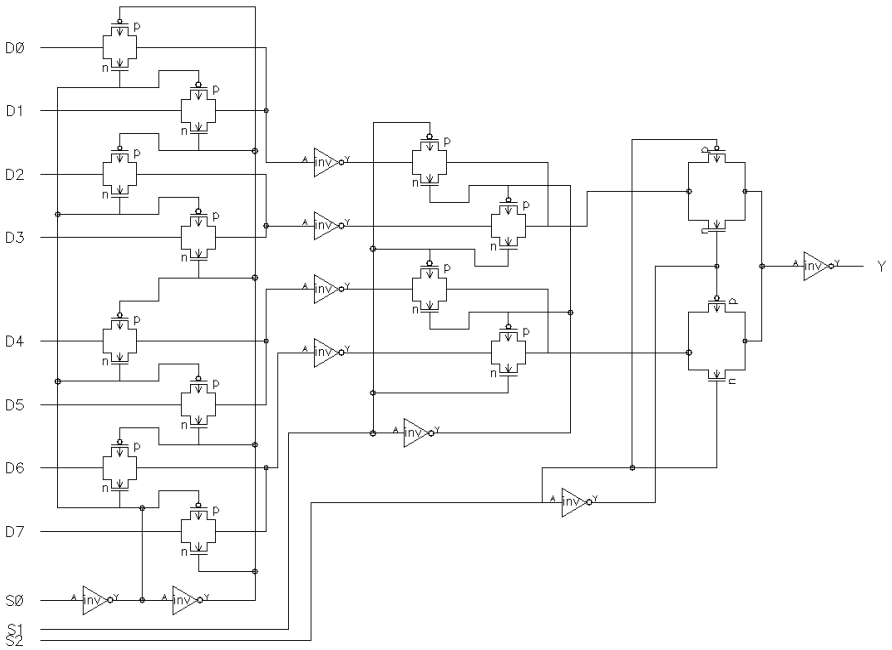
Gate Count: All : 12



Symbol

S2	S1	S0	Y
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

Truth Table



Schematic

MX8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Y	tPLH	0.42	0.34 + 0.041*SL	0.36 + 0.037*SL	0.36 + 0.036*SL
	tPHL	0.57	0.50 + 0.035*SL	0.54 + 0.022*SL	0.64 + 0.017*SL
	tR	0.32	0.16 + 0.082*SL	0.16 + 0.081*SL	0.11 + 0.084*SL
	tF	0.25	0.17 + 0.042*SL	0.20 + 0.032*SL	0.22 + 0.031*SL
D1 to Y	tPLH	0.43	0.34 + 0.041*SL	0.36 + 0.037*SL	0.36 + 0.036*SL
	tPHL	0.57	0.50 + 0.035*SL	0.54 + 0.022*SL	0.64 + 0.017*SL
	tR	0.32	0.16 + 0.082*SL	0.16 + 0.081*SL	0.11 + 0.084*SL
	tF	0.26	0.18 + 0.039*SL	0.20 + 0.032*SL	0.22 + 0.031*SL
D2 to Y	tPLH	0.42	0.34 + 0.040*SL	0.36 + 0.037*SL	0.36 + 0.036*SL
	tPHL	0.57	0.50 + 0.035*SL	0.54 + 0.022*SL	0.64 + 0.017*SL
	tR	0.32	0.16 + 0.082*SL	0.16 + 0.081*SL	0.11 + 0.084*SL
	tF	0.26	0.18 + 0.040*SL	0.20 + 0.032*SL	0.22 + 0.031*SL
D3 to Y	tPLH	0.42	0.34 + 0.040*SL	0.35 + 0.037*SL	0.36 + 0.036*SL
	tPHL	0.57	0.50 + 0.035*SL	0.54 + 0.022*SL	0.64 + 0.017*SL
	tR	0.32	0.16 + 0.083*SL	0.16 + 0.081*SL	0.11 + 0.084*SL
	tF	0.26	0.18 + 0.040*SL	0.20 + 0.032*SL	0.22 + 0.031*SL
D4 to Y	tPLH	0.42	0.34 + 0.040*SL	0.35 + 0.037*SL	0.36 + 0.036*SL
	tPHL	0.57	0.50 + 0.035*SL	0.54 + 0.022*SL	0.64 + 0.017*SL
	tR	0.32	0.16 + 0.083*SL	0.16 + 0.081*SL	0.10 + 0.084*SL
	tF	0.26	0.18 + 0.039*SL	0.20 + 0.032*SL	0.22 + 0.031*SL
D5 to Y	tPLH	0.42	0.34 + 0.040*SL	0.35 + 0.037*SL	0.36 + 0.036*SL
	tPHL	0.57	0.50 + 0.035*SL	0.54 + 0.022*SL	0.64 + 0.017*SL
	tR	0.32	0.16 + 0.083*SL	0.16 + 0.081*SL	0.10 + 0.084*SL
	tF	0.26	0.18 + 0.039*SL	0.20 + 0.032*SL	0.22 + 0.031*SL
D6 to Y	tPLH	0.42	0.34 + 0.040*SL	0.35 + 0.037*SL	0.36 + 0.036*SL
	tPHL	0.57	0.50 + 0.035*SL	0.54 + 0.022*SL	0.64 + 0.017*SL
	tR	0.32	0.16 + 0.083*SL	0.16 + 0.081*SL	0.10 + 0.084*SL
	tF	0.26	0.18 + 0.040*SL	0.20 + 0.032*SL	0.22 + 0.031*SL
D7 to Y	tPLH	0.42	0.34 + 0.040*SL	0.35 + 0.037*SL	0.36 + 0.036*SL
	tPHL	0.57	0.50 + 0.035*SL	0.54 + 0.022*SL	0.64 + 0.017*SL
	tR	0.32	0.16 + 0.083*SL	0.16 + 0.081*SL	0.10 + 0.084*SL
	tF	0.26	0.18 + 0.040*SL	0.20 + 0.032*SL	0.22 + 0.031*SL
S0 to Y	tPLH	0.90	0.82 + 0.038*SL	0.83 + 0.037*SL	0.83 + 0.036*SL
	tPHL	0.68	0.61 + 0.034*SL	0.65 + 0.022*SL	0.74 + 0.017*SL
	tR	0.31	0.14 + 0.082*SL	0.14 + 0.082*SL	0.10 + 0.084*SL
	tF	0.25	0.16 + 0.043*SL	0.20 + 0.032*SL	0.21 + 0.031*SL
S1 to Y	tPLH	0.59	0.51 + 0.039*SL	0.52 + 0.036*SL	0.53 + 0.036*SL
	tPHL	0.36	0.29 + 0.035*SL	0.33 + 0.022*SL	0.42 + 0.017*SL
	tR	0.31	0.16 + 0.078*SL	0.15 + 0.082*SL	0.10 + 0.084*SL
	tF	0.26	0.17 + 0.044*SL	0.21 + 0.032*SL	0.21 + 0.031*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

MX8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S2 to Y	t_{PLH}	0.47	0.38 + 0.042*SL	0.40 + 0.037*SL	0.41 + 0.036*SL
	t_{PHL}	0.25	0.19 + 0.030*SL	0.22 + 0.021*SL	0.29 + 0.017*SL
	t_R	0.30	0.14 + 0.080*SL	0.13 + 0.083*SL	0.10 + 0.084*SL
	t_F	0.22	0.15 + 0.035*SL	0.15 + 0.032*SL	0.16 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

MX8D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Y	t_{PLH}	0.42	0.37 + 0.025*SL	0.38 + 0.019*SL	0.40 + 0.018*SL
	t_{PHL}	0.55	0.50 + 0.025*SL	0.54 + 0.014*SL	0.62 + 0.011*SL
	t_R	0.22	0.13 + 0.046*SL	0.15 + 0.040*SL	0.11 + 0.042*SL
	t_F	0.23	0.19 + 0.018*SL	0.19 + 0.018*SL	0.23 + 0.016*SL
D1 to Y	t_{PLH}	0.42	0.37 + 0.025*SL	0.38 + 0.019*SL	0.40 + 0.018*SL
	t_{PHL}	0.56	0.51 + 0.025*SL	0.54 + 0.015*SL	0.62 + 0.011*SL
	t_R	0.22	0.13 + 0.046*SL	0.15 + 0.040*SL	0.11 + 0.042*SL
	t_F	0.23	0.19 + 0.019*SL	0.19 + 0.018*SL	0.23 + 0.016*SL
D2 to Y	t_{PLH}	0.41	0.36 + 0.025*SL	0.38 + 0.019*SL	0.40 + 0.018*SL
	t_{PHL}	0.56	0.51 + 0.025*SL	0.54 + 0.015*SL	0.62 + 0.011*SL
	t_R	0.22	0.13 + 0.046*SL	0.15 + 0.040*SL	0.11 + 0.042*SL
	t_F	0.23	0.19 + 0.018*SL	0.19 + 0.018*SL	0.23 + 0.016*SL
D3 to Y	t_{PLH}	0.41	0.36 + 0.025*SL	0.38 + 0.019*SL	0.40 + 0.018*SL
	t_{PHL}	0.56	0.51 + 0.025*SL	0.54 + 0.015*SL	0.62 + 0.011*SL
	t_R	0.22	0.13 + 0.046*SL	0.15 + 0.040*SL	0.11 + 0.042*SL
	t_F	0.23	0.19 + 0.018*SL	0.19 + 0.018*SL	0.23 + 0.016*SL
D4 to Y	t_{PLH}	0.41	0.37 + 0.024*SL	0.38 + 0.019*SL	0.40 + 0.018*SL
	t_{PHL}	0.56	0.51 + 0.024*SL	0.54 + 0.015*SL	0.62 + 0.010*SL
	t_R	0.22	0.13 + 0.047*SL	0.15 + 0.040*SL	0.11 + 0.042*SL
	t_F	0.23	0.19 + 0.018*SL	0.19 + 0.018*SL	0.23 + 0.016*SL
D5 to Y	t_{PLH}	0.41	0.36 + 0.024*SL	0.38 + 0.019*SL	0.40 + 0.018*SL
	t_{PHL}	0.55	0.51 + 0.025*SL	0.54 + 0.015*SL	0.62 + 0.010*SL
	t_R	0.22	0.13 + 0.047*SL	0.15 + 0.040*SL	0.11 + 0.042*SL
	t_F	0.23	0.19 + 0.019*SL	0.19 + 0.018*SL	0.23 + 0.016*SL
D6 to Y	t_{PLH}	0.41	0.36 + 0.025*SL	0.38 + 0.019*SL	0.40 + 0.018*SL
	t_{PHL}	0.56	0.51 + 0.025*SL	0.54 + 0.015*SL	0.62 + 0.010*SL
	t_R	0.22	0.13 + 0.047*SL	0.15 + 0.040*SL	0.11 + 0.042*SL
	t_F	0.23	0.19 + 0.018*SL	0.19 + 0.018*SL	0.23 + 0.016*SL
D7 to Y	t_{PLH}	0.41	0.36 + 0.025*SL	0.38 + 0.019*SL	0.40 + 0.018*SL
	t_{PHL}	0.56	0.51 + 0.025*SL	0.54 + 0.015*SL	0.62 + 0.010*SL
	t_R	0.22	0.13 + 0.047*SL	0.15 + 0.040*SL	0.11 + 0.042*SL
	t_F	0.23	0.19 + 0.018*SL	0.19 + 0.018*SL	0.23 + 0.016*SL
S0 to Y	t_{PLH}	0.88	0.84 + 0.022*SL	0.85 + 0.019*SL	0.87 + 0.018*SL
	t_{PHL}	0.67	0.63 + 0.020*SL	0.65 + 0.015*SL	0.73 + 0.010*SL
	t_R	0.22	0.12 + 0.047*SL	0.14 + 0.040*SL	0.11 + 0.042*SL
	t_F	0.22	0.18 + 0.019*SL	0.18 + 0.018*SL	0.23 + 0.016*SL
S1 to Y	t_{PLH}	0.57	0.53 + 0.023*SL	0.54 + 0.019*SL	0.56 + 0.018*SL
	t_{PHL}	0.35	0.31 + 0.024*SL	0.33 + 0.014*SL	0.41 + 0.010*SL
	t_R	0.22	0.16 + 0.034*SL	0.14 + 0.041*SL	0.11 + 0.042*SL
	t_F	0.22	0.16 + 0.028*SL	0.19 + 0.018*SL	0.23 + 0.016*SL

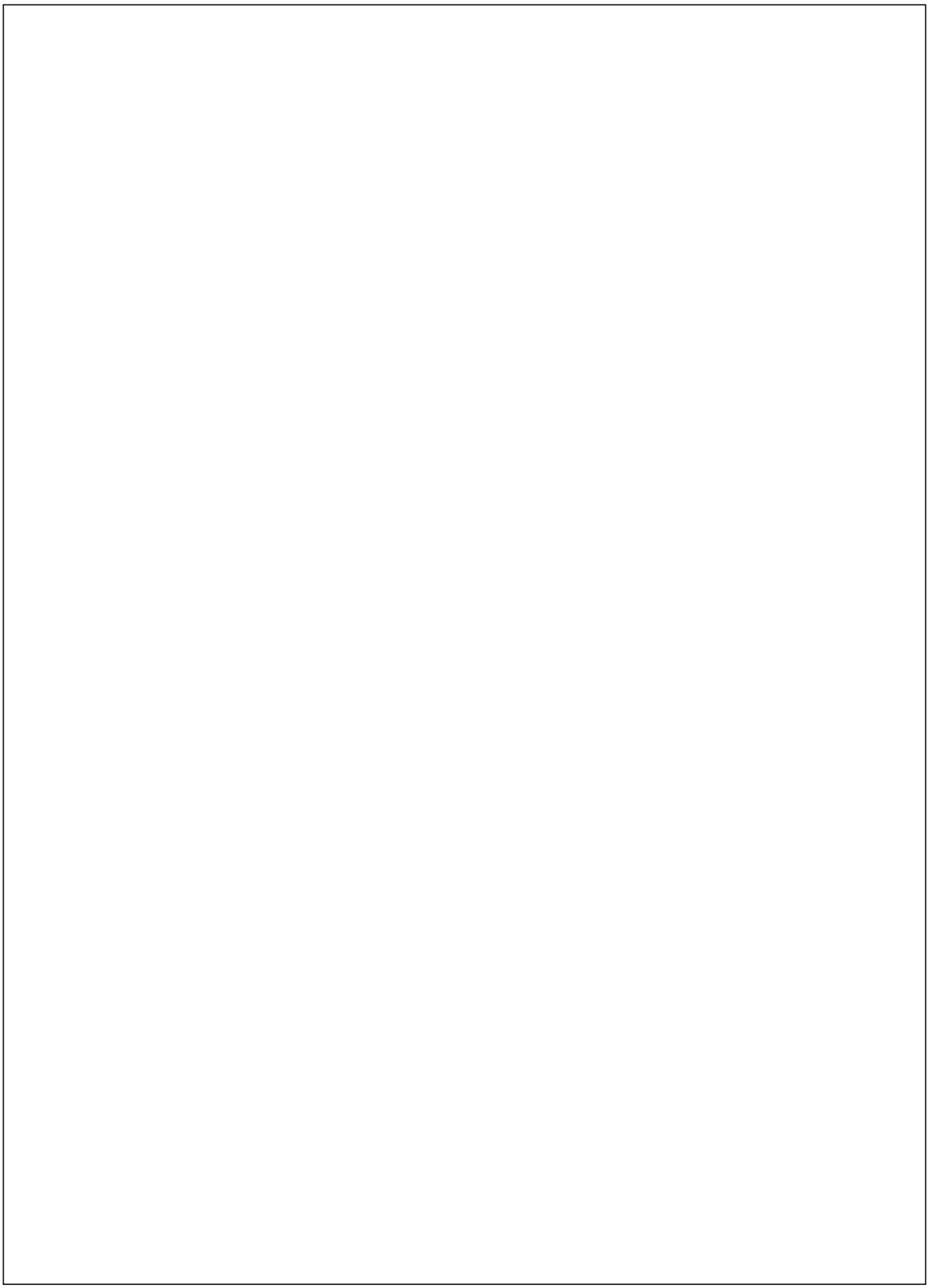
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

MX8D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S2 to Y	tPLH	0.45	0.40 + 0.025*SL	0.41 + 0.019*SL	0.44 + 0.018*SL
	tPHL	0.26	0.22 + 0.020*SL	0.24 + 0.013*SL	0.30 + 0.010*SL
	t_R	0.20	0.12 + 0.041*SL	0.12 + 0.041*SL	0.10 + 0.042*SL
	t_F	0.21	0.17 + 0.018*SL	0.17 + 0.018*SL	0.20 + 0.016*SL

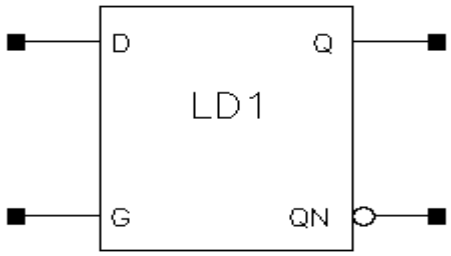
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL



Inputs: D, G
Outputs: Q, QN
Input Loading (SL):
- D: 3
- G: 1

Maximum Fanout (Rec. SL):
- LD1: 28
- LD1D2:56

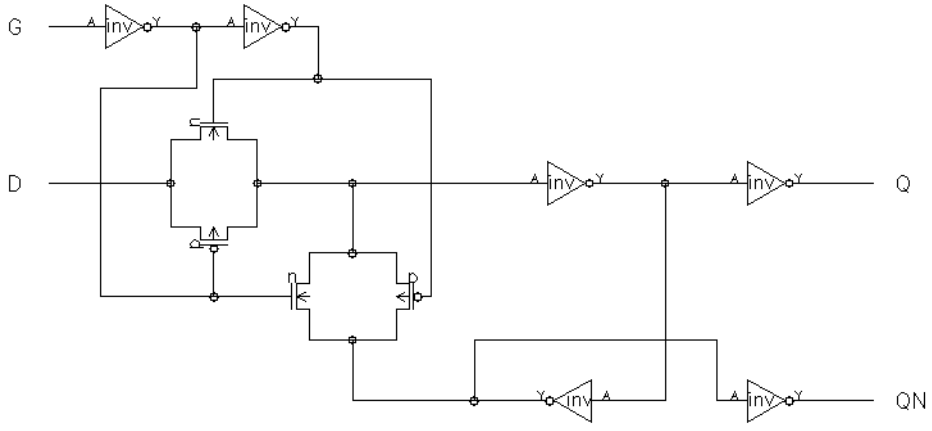
Gate Count: 5



Symbol

D	G	Qn+1	QNn+1
0	1	0	1
1	1	1	0
x	0	Qn	QNn

Truth Table



Schematic

LD1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	t_{PLH}	0.20	0.13 + 0.038*SL	0.13 + 0.036*SL	0.13 + 0.036*SL
	t_{PHL}	0.38	0.33 + 0.025*SL	0.35 + 0.017*SL	0.38 + 0.016*SL
	t_R	0.25	0.09 + 0.081*SL	0.08 + 0.083*SL	0.06 + 0.084*SL
	t_F	0.15	0.09 + 0.033*SL	0.09 + 0.031*SL	0.07 + 0.032*SL
G to Q	t_{PLH}	0.32	0.25 + 0.037*SL	0.25 + 0.037*SL	0.25 + 0.036*SL
	t_{PHL}	0.31	0.27 + 0.024*SL	0.29 + 0.017*SL	0.31 + 0.016*SL
	t_R	0.23	0.07 + 0.083*SL	0.07 + 0.084*SL	0.05 + 0.085*SL
	t_F	0.13	0.06 + 0.034*SL	0.07 + 0.031*SL	0.05 + 0.032*SL
D to QN	t_{PLH}	0.49	0.42 + 0.035*SL	0.41 + 0.036*SL	0.41 + 0.036*SL
	t_{PHL}	0.24	0.20 + 0.022*SL	0.21 + 0.017*SL	0.23 + 0.016*SL
	t_R	0.24	0.08 + 0.078*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.13	0.07 + 0.031*SL	0.07 + 0.031*SL	0.05 + 0.032*SL
G to QN	t_{PLH}	0.42	0.35 + 0.037*SL	0.35 + 0.036*SL	0.34 + 0.037*SL
	t_{PHL}	0.36	0.32 + 0.021*SL	0.33 + 0.017*SL	0.34 + 0.016*SL
	t_R	0.23	0.08 + 0.078*SL	0.06 + 0.084*SL	0.05 + 0.084*SL
	t_F	0.12	0.06 + 0.032*SL	0.06 + 0.032*SL	0.04 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

LD1 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	t_{PWH}	0.000
Input Hold Time (D to G)	t_{HD}	0.000
Input Setup Time (D to G)	t_{SU}	0.000

LD1D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

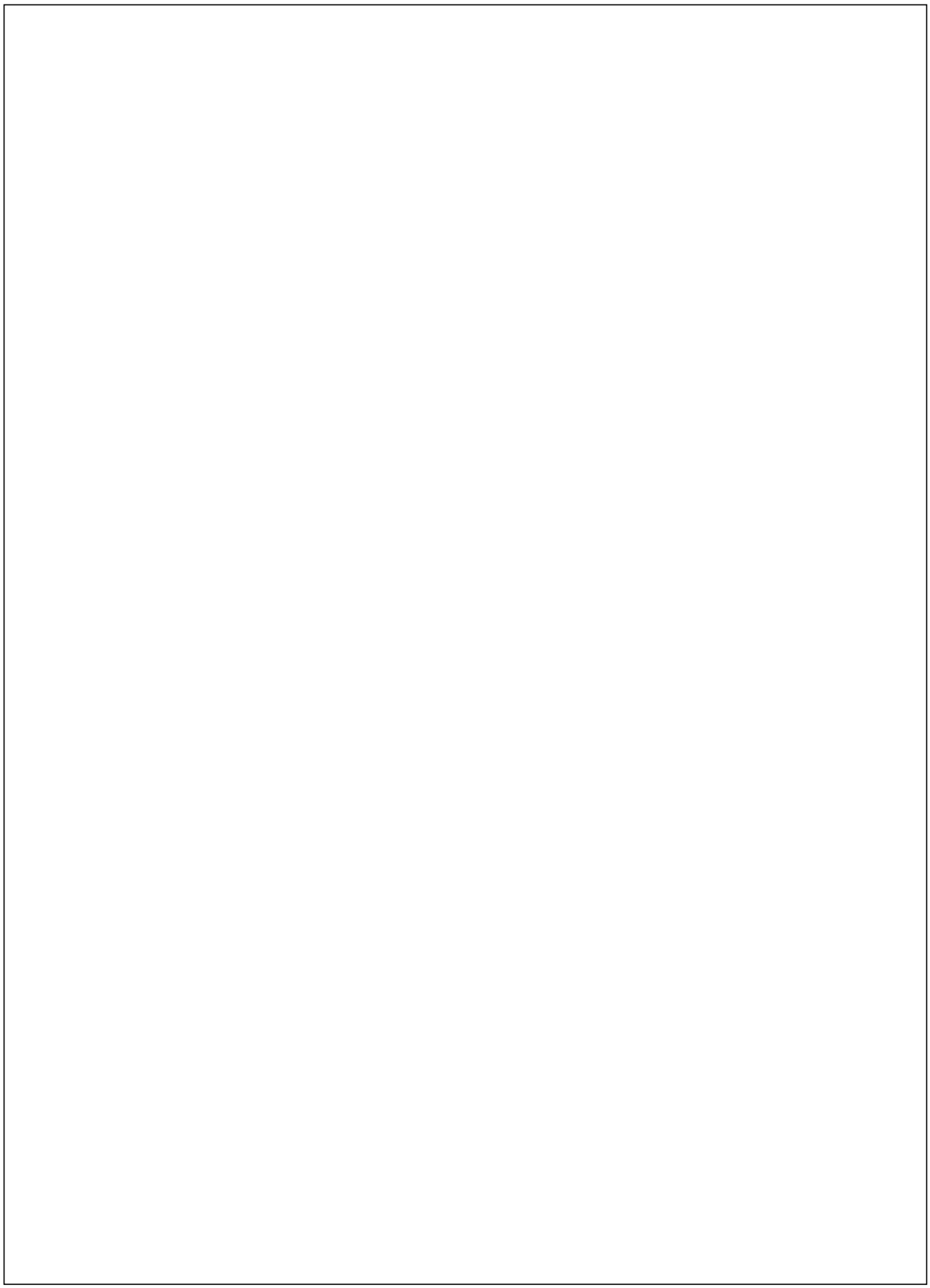
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.20	0.16 + 0.020*SL	0.17 + 0.019*SL	0.17 + 0.018*SL
	tPHL	0.39	0.35 + 0.016*SL	0.37 + 0.010*SL	0.41 + 0.008*SL
	tR	0.17	0.09 + 0.042*SL	0.09 + 0.041*SL	0.06 + 0.043*SL
	tF	0.14	0.11 + 0.017*SL	0.12 + 0.015*SL	0.10 + 0.016*SL
G to Q	tPLH	0.31	0.27 + 0.020*SL	0.27 + 0.019*SL	0.28 + 0.018*SL
	tPHL	0.32	0.29 + 0.015*SL	0.31 + 0.010*SL	0.34 + 0.008*SL
	tR	0.15	0.08 + 0.037*SL	0.06 + 0.043*SL	0.06 + 0.043*SL
	tF	0.12	0.08 + 0.017*SL	0.08 + 0.016*SL	0.09 + 0.016*SL
D to QN	tPLH	0.52	0.49 + 0.018*SL	0.49 + 0.018*SL	0.48 + 0.018*SL
	tPHL	0.29	0.27 + 0.014*SL	0.28 + 0.010*SL	0.31 + 0.008*SL
	tR	0.16	0.10 + 0.034*SL	0.07 + 0.041*SL	0.05 + 0.042*SL
	tF	0.11	0.08 + 0.016*SL	0.08 + 0.016*SL	0.08 + 0.016*SL
G to QN	tPLH	0.45	0.42 + 0.016*SL	0.42 + 0.018*SL	0.41 + 0.018*SL
	tPHL	0.40	0.37 + 0.014*SL	0.39 + 0.009*SL	0.41 + 0.008*SL
	tR	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.05 + 0.042*SL
	tF	0.12	0.07 + 0.022*SL	0.09 + 0.015*SL	0.08 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD1D2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

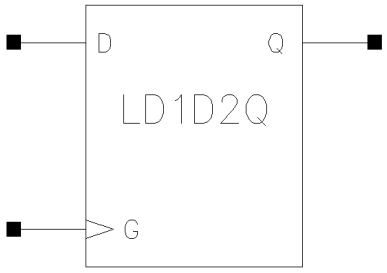
Parameter	Symbol	Value [ns]
Pulse Width High (G)	tPWH	0.000
Input Hold Time (D to G)	tHD	0.000
Input Setup Time (D to G)	tSU	0.000



Inputs: D, G
Outputs: Q
Input Loading (SL):
- LD1D2Q: D: 3, G: 1
- LD1D4Q: D: 3, G: 1

Maximum Fanout (Rec. SL):
- LD1D2Q: 56
- LD1D4Q: 112

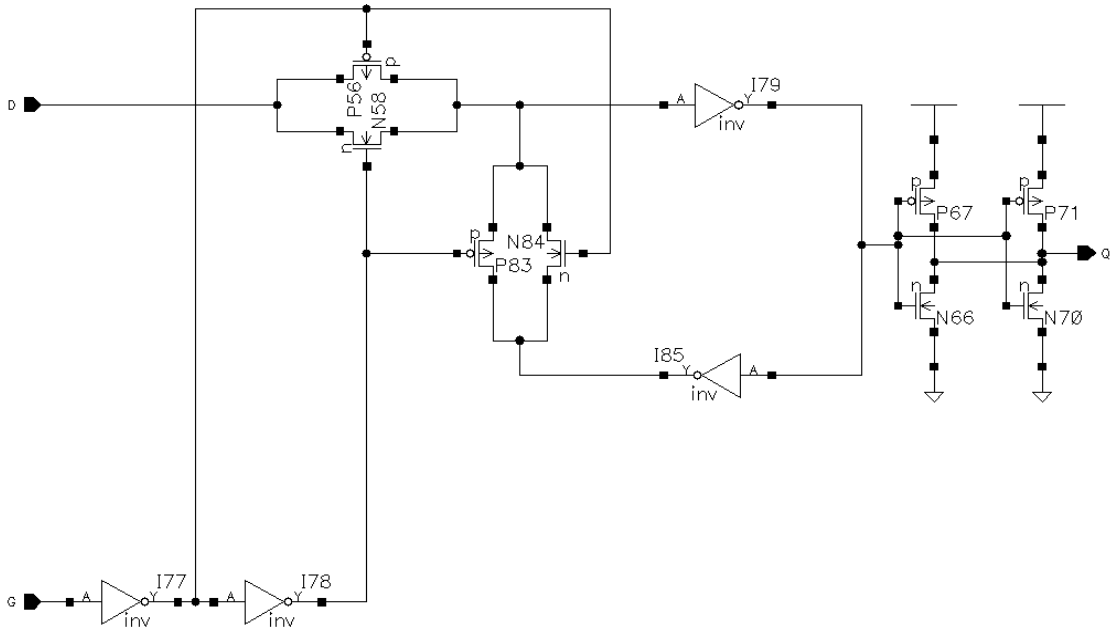
Gate Count:
- LD1D2Q: 4
- LD1D4Q: 5



Symbol

D	G	Qn+1
0	1	0
1	1	1
x	0	Qn

Truth Table



Schematic

LD1D2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	t_{PLH}	0.21	0.17 + 0.020*SL	0.17 + 0.018*SL	0.17 + 0.018*SL
	t_{PHL}	0.39	0.36 + 0.016*SL	0.38 + 0.010*SL	0.42 + 0.008*SL
	t_R	0.18	0.10 + 0.038*SL	0.09 + 0.041*SL	0.06 + 0.043*SL
	t_F	0.15	0.13 + 0.013*SL	0.12 + 0.015*SL	0.11 + 0.016*SL
G to Q	t_{PLH}	0.31	0.27 + 0.021*SL	0.27 + 0.019*SL	0.28 + 0.018*SL
	t_{PHL}	0.33	0.29 + 0.016*SL	0.31 + 0.010*SL	0.35 + 0.008*SL
	t_R	0.16	0.08 + 0.040*SL	0.07 + 0.042*SL	0.06 + 0.043*SL
	t_F	0.12	0.08 + 0.017*SL	0.08 + 0.016*SL	0.09 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

LD1D2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	t_{PWH}	0.000
Input Hold Time (D to G)	t_{HD}	0.000
Input Setup Time (D to G)	t_{SU}	0.000

LD1D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	t_{PLH}	0.26	0.23 + 0.012*SL	0.24 + 0.010*SL	0.25 + 0.009*SL
	t_{PHL}	0.45	0.43 + 0.010*SL	0.44 + 0.007*SL	0.47 + 0.005*SL
	t_R	0.16	0.11 + 0.022*SL	0.11 + 0.021*SL	0.09 + 0.022*SL
	t_F	0.17	0.15 + 0.008*SL	0.15 + 0.008*SL	0.16 + 0.008*SL
G to Q	t_{PLH}	0.34	0.31 + 0.011*SL	0.32 + 0.010*SL	0.33 + 0.009*SL
	t_{PHL}	0.37	0.35 + 0.011*SL	0.36 + 0.007*SL	0.39 + 0.005*SL
	t_R	0.14	0.09 + 0.024*SL	0.09 + 0.022*SL	0.08 + 0.022*SL
	t_F	0.15	0.13 + 0.010*SL	0.13 + 0.009*SL	0.14 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

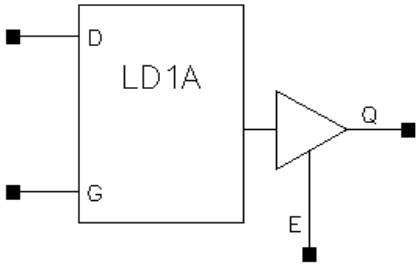
LD1D4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	t_{PWH}	0.000
Input Hold Time (D to G)	t_{HD}	0.000
Input Setup Time (D to G)	t_{SU}	0.000

Inputs: D, G, E
Outputs: Q
Input Loading (SL):
- D: 3
- G: 1
- E: 1.5

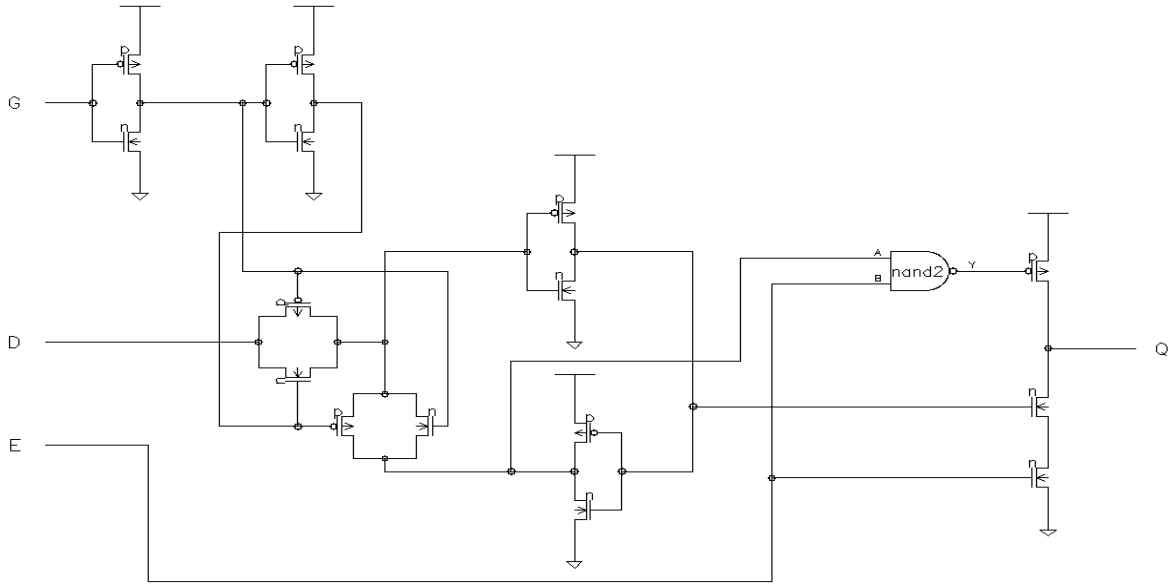
Maximum Fanout (Rec. SL): 28
Gate Count: 5



Symbol

D	G	E	Qn+1
x	x	0	Hi-Z
0	1	1	0
1	1	1	1
x	0	1	Qn

Truth Table



Schematic

LD1A Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
E to Q	t_{PLH}	0.14	0.05 + 0.043*SL	0.07 + 0.037*SL	0.08 + 0.036*SL
	t_{PHL}	0.01	-0.10 + 0.054*SL	-0.03 + 0.030*SL	0.05 + 0.026*SL
	t_R	0.27	0.13 + 0.069*SL	0.09 + 0.082*SL	0.06 + 0.084*SL
	t_F	0.31	0.19 + 0.060*SL	0.21 + 0.053*SL	0.15 + 0.056*SL
	t_{PLZ}	0.40	0.40 + -0.000*SL	0.40 + -0.000*SL	0.40 + -0.000*SL
	t_{PHZ}	0.40	0.40 + -0.000*SL	0.40 + -0.000*SL	0.40 + -0.000*SL
D to Q	t_{PLH}	0.33	0.25 + 0.038*SL	0.26 + 0.037*SL	0.27 + 0.036*SL
	t_{PHL}	0.43	0.38 + 0.024*SL	0.38 + 0.025*SL	0.37 + 0.026*SL
	t_R	0.24	0.07 + 0.085*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.25	0.17 + 0.045*SL	0.14 + 0.054*SL	0.06 + 0.058*SL
G to Q	t_{PLH}	0.46	0.38 + 0.041*SL	0.39 + 0.037*SL	0.40 + 0.036*SL
	t_{PHL}	0.37	0.32 + 0.023*SL	0.32 + 0.025*SL	0.30 + 0.026*SL
	t_R	0.23	0.07 + 0.082*SL	0.06 + 0.084*SL	0.05 + 0.084*SL
	t_F	0.24	0.14 + 0.048*SL	0.12 + 0.055*SL	0.05 + 0.058*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

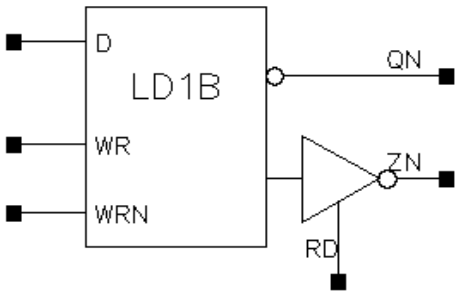
LD1A Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	t_{PWH}	0.000
Input Hold Time (D to G)	t_{HD}	0.000
Input Setup Time (D to G)	t_{SU}	0.000

Inputs: D, WR, WRN, RD
Outputs: QN, ZN
Input Loading (SL):
- D: 3
- WR, WRN: 1
- RD: 1.5

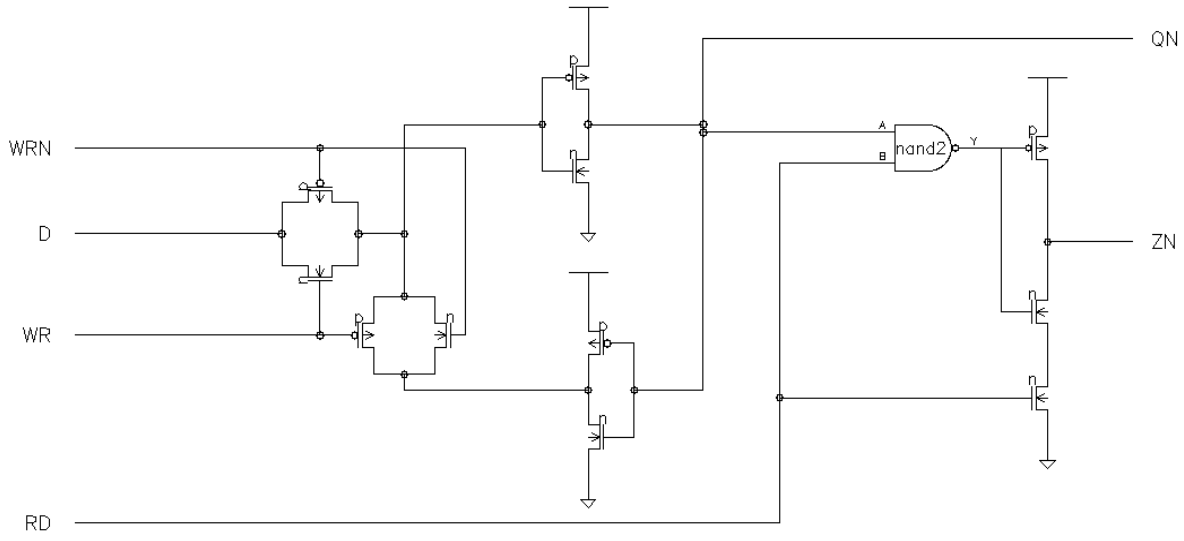
Maximum Fanout (Rec. SL): 14
Gate Count: 4



Symbol

D	WR	WRN	RD	QNn+1	ZNn+1
0	1	0	0	1	Hi-Z
1	1	0	0	0	Hi-Z
0	1	0	1	1	1
1	1	0	1	0	0
x	0	1	0	QNn	Hi-Z
x	0	1	1	QNn	QNn

Truth Table



Schematic

LD1B Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to QN	tPLH	0.40	0.32 + 0.044*SL	0.34 + 0.038*SL	0.33 + 0.038*SL
	tPHL	0.13	0.06 + 0.034*SL	0.09 + 0.022*SL	0.20 + 0.016*SL
	tR	0.52	0.36 + 0.079*SL	0.35 + 0.083*SL	0.26 + 0.088*SL
	tF	0.37	0.30 + 0.033*SL	0.31 + 0.030*SL	0.30 + 0.030*SL
WR to QN	tPLH	0.20	0.12 + 0.041*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
	tPHL	0.29	0.25 + 0.022*SL	0.26 + 0.017*SL	0.28 + 0.016*SL
	tR	0.42	0.25 + 0.086*SL	0.25 + 0.087*SL	0.22 + 0.089*SL
	tF	0.22	0.15 + 0.034*SL	0.16 + 0.032*SL	0.14 + 0.033*SL
WRN to QN	tPLH	0.20	0.12 + 0.041*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
	tPHL	0.29	0.25 + 0.022*SL	0.26 + 0.017*SL	0.28 + 0.016*SL
	tR	0.42	0.25 + 0.086*SL	0.25 + 0.087*SL	0.22 + 0.089*SL
	tF	0.22	0.15 + 0.034*SL	0.16 + 0.032*SL	0.14 + 0.033*SL
RD to ZN	tPLH	0.19	0.11 + 0.039*SL	0.12 + 0.036*SL	0.12 + 0.036*SL
	tPHL	0.01	-0.10 + 0.053*SL	-0.03 + 0.030*SL	0.05 + 0.026*SL
	tR	0.26	0.12 + 0.073*SL	0.09 + 0.082*SL	0.06 + 0.083*SL
	tF	0.30	0.19 + 0.058*SL	0.20 + 0.052*SL	0.15 + 0.055*SL
	tPLZ	0.40	0.40 + -0.000*SL	0.40 + 0.000*SL	0.40 + -0.000*SL
	tPHZ	0.40	0.41 + -0.000*SL	0.40 + 0.000*SL	0.41 + -0.000*SL
D to ZN	tPLH	0.62	0.45 + 0.083*SL	0.48 + 0.074*SL	0.52 + 0.072*SL
	tPHL	0.35	0.21 + 0.071*SL	0.27 + 0.052*SL	0.36 + 0.047*SL
	tR	0.24	0.09 + 0.077*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.19	0.08 + 0.056*SL	0.08 + 0.056*SL	0.05 + 0.057*SL
WR to ZN	tPLH	0.42	0.25 + 0.083*SL	0.28 + 0.074*SL	0.31 + 0.072*SL
	tPHL	0.50	0.38 + 0.058*SL	0.41 + 0.049*SL	0.44 + 0.047*SL
	tR	0.24	0.09 + 0.077*SL	0.07 + 0.084*SL	0.05 + 0.084*SL
	tF	0.18	0.07 + 0.057*SL	0.07 + 0.056*SL	0.05 + 0.057*SL
WRN to ZN	tPLH	0.42	0.25 + 0.083*SL	0.28 + 0.074*SL	0.31 + 0.072*SL
	tPHL	0.50	0.38 + 0.058*SL	0.41 + 0.049*SL	0.44 + 0.047*SL
	tR	0.24	0.09 + 0.077*SL	0.07 + 0.084*SL	0.05 + 0.084*SL
	tF	0.18	0.07 + 0.057*SL	0.07 + 0.056*SL	0.05 + 0.057*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD1B Timing Requirements

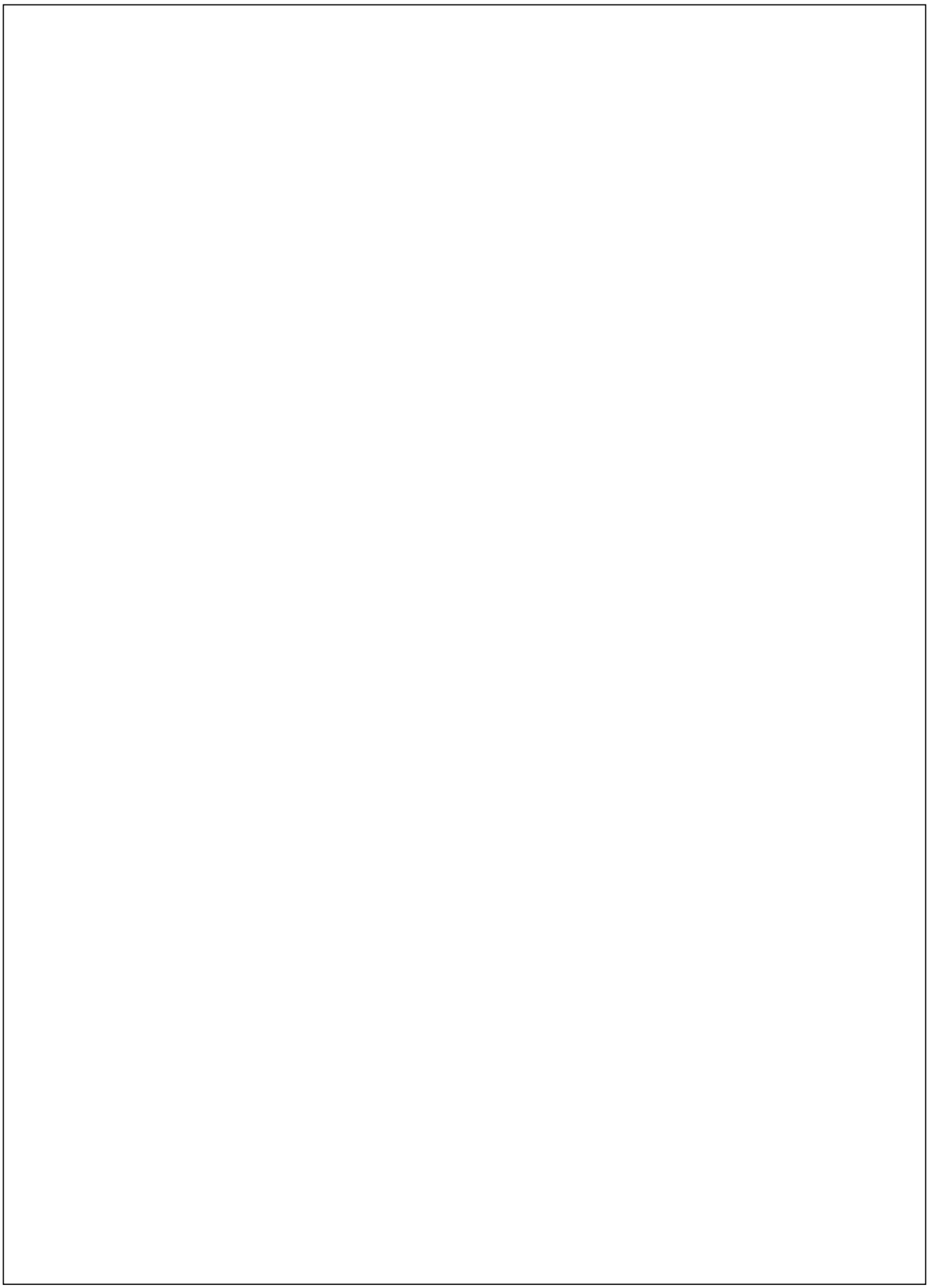
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (WRN)	tPWL	0.000

LD1B Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (WR)	t_{PWH}	0.000
Input Hold Time (D to WR)	t_{HD}	0.000
Input Hold Time (D to WRN)	t_{HD}	0.000
Input Setup Time (D to WR)	t_{SU}	0.000
Input Setup Time (D to WRN)	t_{SU}	0.000

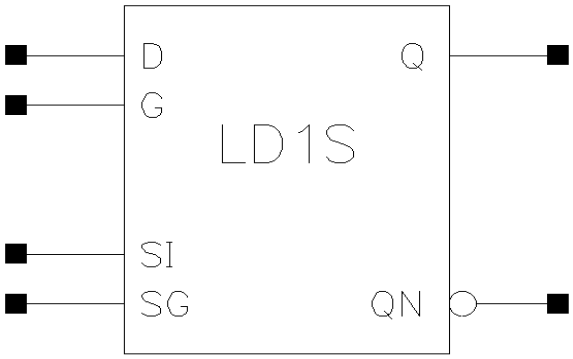


Inputs: D, G, SI, SG
Outputs: Q, QN

Input Loading (SL):
- LD1S: D, SI: All : 1
- LD1SD2: G, SG: All : 2

Maximum Fanout (Rec. SL):
- LD1S: 28
- LD1SD2: 56

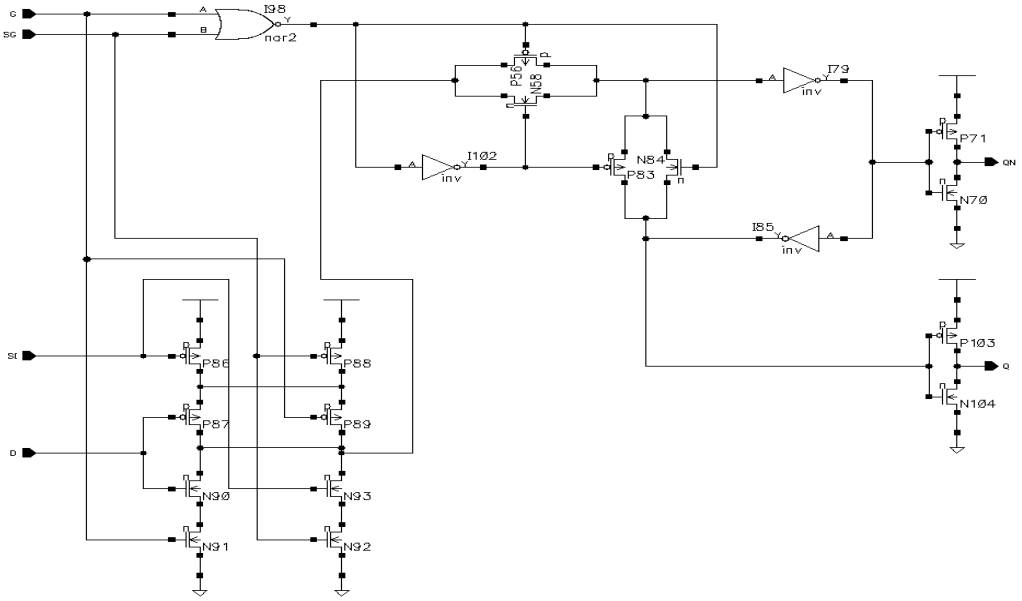
Gate Count:
- LD1S: 7
- LD1SD2: 8



Symbol

D	G	SI	SG	Qn+1	QNn+1
x	0	x	0	Qn	QNn
x	x	1	1	1	0
x	0	0	1	0	1
1	1	x	x	1	0
0	1	x	0	0	1
0	1	0	1	0	1

Truth Table



Schematic

LD1S Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.54	0.47 + 0.036*SL	0.47 + 0.036*SL	0.47 + 0.036*SL
	tPHL	0.78	0.73 + 0.023*SL	0.75 + 0.017*SL	0.76 + 0.016*SL
	tR	0.23	0.07 + 0.082*SL	0.06 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.06 + 0.037*SL	0.08 + 0.031*SL	0.04 + 0.033*SL
G to Q	tPLH	0.47	0.40 + 0.036*SL	0.40 + 0.036*SL	0.40 + 0.036*SL
	tPHL	0.79	0.74 + 0.022*SL	0.76 + 0.016*SL	0.77 + 0.016*SL
	tR	0.23	0.07 + 0.079*SL	0.06 + 0.083*SL	0.05 + 0.084*SL
	tF	0.13	0.06 + 0.035*SL	0.08 + 0.031*SL	0.04 + 0.033*SL
SI to Q	tPLH	0.60	0.52 + 0.037*SL	0.52 + 0.036*SL	0.52 + 0.036*SL
	tPHL	0.77	0.72 + 0.023*SL	0.74 + 0.017*SL	0.75 + 0.016*SL
	tR	0.23	0.06 + 0.085*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.13	0.06 + 0.035*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
SG to Q	tPLH	0.52	0.45 + 0.036*SL	0.45 + 0.036*SL	0.44 + 0.036*SL
	tPHL	0.76	0.72 + 0.021*SL	0.73 + 0.017*SL	0.75 + 0.016*SL
	tR	0.24	0.08 + 0.079*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.13	0.07 + 0.032*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
D to QN	tPLH	0.74	0.66 + 0.039*SL	0.67 + 0.036*SL	0.67 + 0.036*SL
	tPHL	0.44	0.39 + 0.024*SL	0.41 + 0.017*SL	0.43 + 0.016*SL
	tR	0.25	0.09 + 0.083*SL	0.09 + 0.083*SL	0.06 + 0.084*SL
	tF	0.14	0.08 + 0.032*SL	0.08 + 0.031*SL	0.06 + 0.032*SL
G to QN	tPLH	0.75	0.67 + 0.038*SL	0.68 + 0.036*SL	0.68 + 0.036*SL
	tPHL	0.37	0.32 + 0.024*SL	0.34 + 0.017*SL	0.36 + 0.016*SL
	tR	0.25	0.09 + 0.082*SL	0.09 + 0.083*SL	0.06 + 0.084*SL
	tF	0.14	0.08 + 0.033*SL	0.08 + 0.031*SL	0.05 + 0.033*SL
SI to QN	tPLH	0.73	0.65 + 0.038*SL	0.66 + 0.036*SL	0.66 + 0.036*SL
	tPHL	0.49	0.44 + 0.024*SL	0.46 + 0.017*SL	0.49 + 0.016*SL
	tR	0.25	0.10 + 0.079*SL	0.08 + 0.083*SL	0.06 + 0.084*SL
	tF	0.14	0.08 + 0.032*SL	0.08 + 0.031*SL	0.06 + 0.033*SL
SG to QN	tPLH	0.72	0.65 + 0.038*SL	0.65 + 0.036*SL	0.65 + 0.036*SL
	tPHL	0.41	0.36 + 0.024*SL	0.38 + 0.017*SL	0.41 + 0.016*SL
	tR	0.25	0.09 + 0.078*SL	0.07 + 0.084*SL	0.06 + 0.084*SL
	tF	0.15	0.08 + 0.033*SL	0.09 + 0.031*SL	0.06 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

LD1S Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	tPWH	0.000

LD1S Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (SG)	t_{PWH}	0.000
Input Hold Time (D to G)	t_{HD}	0.000
Input Hold Time (SI to SG)	t_{HD}	0.000
Input Setup Time (D to G)	t_{SU}	0.000
Input Setup Time (SI to SG)	t_{SU}	0.000

LD1SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	t_{PLH}	0.58	0.55 + 0.016*SL	0.54 + 0.018*SL	0.54 + 0.018*SL
	t_{PHL}	0.83	0.80 + 0.014*SL	0.81 + 0.010*SL	0.84 + 0.008*SL
	t_R	0.16	0.07 + 0.043*SL	0.08 + 0.041*SL	0.06 + 0.042*SL
	t_F	0.12	0.08 + 0.019*SL	0.09 + 0.016*SL	0.09 + 0.016*SL
G to Q	t_{PLH}	0.50	0.46 + 0.018*SL	0.47 + 0.018*SL	0.46 + 0.018*SL
	t_{PHL}	0.84	0.81 + 0.012*SL	0.82 + 0.010*SL	0.85 + 0.008*SL
	t_R	0.16	0.10 + 0.033*SL	0.07 + 0.041*SL	0.05 + 0.042*SL
	t_F	0.12	0.09 + 0.016*SL	0.09 + 0.016*SL	0.08 + 0.016*SL
SI to Q	t_{PLH}	0.63	0.60 + 0.016*SL	0.59 + 0.018*SL	0.58 + 0.019*SL
	t_{PHL}	0.82	0.79 + 0.013*SL	0.80 + 0.010*SL	0.83 + 0.008*SL
	t_R	0.16	0.09 + 0.037*SL	0.07 + 0.041*SL	0.05 + 0.042*SL
	t_F	0.11	0.08 + 0.016*SL	0.08 + 0.016*SL	0.08 + 0.016*SL
SG to Q	t_{PLH}	0.55	0.52 + 0.017*SL	0.51 + 0.018*SL	0.51 + 0.018*SL
	t_{PHL}	0.81	0.78 + 0.012*SL	0.79 + 0.010*SL	0.82 + 0.008*SL
	t_R	0.17	0.09 + 0.039*SL	0.08 + 0.041*SL	0.05 + 0.042*SL
	t_F	0.12	0.08 + 0.020*SL	0.09 + 0.015*SL	0.08 + 0.016*SL
D to QN	t_{PLH}	0.74	0.70 + 0.021*SL	0.70 + 0.019*SL	0.71 + 0.018*SL
	t_{PHL}	0.45	0.42 + 0.013*SL	0.43 + 0.010*SL	0.47 + 0.008*SL
	t_R	0.17	0.10 + 0.038*SL	0.09 + 0.042*SL	0.06 + 0.043*SL
	t_F	0.13	0.11 + 0.011*SL	0.09 + 0.016*SL	0.09 + 0.016*SL
G to QN	t_{PLH}	0.74	0.70 + 0.020*SL	0.71 + 0.019*SL	0.71 + 0.018*SL
	t_{PHL}	0.37	0.34 + 0.015*SL	0.36 + 0.010*SL	0.39 + 0.008*SL
	t_R	0.17	0.09 + 0.040*SL	0.09 + 0.041*SL	0.06 + 0.043*SL
	t_F	0.13	0.09 + 0.020*SL	0.11 + 0.015*SL	0.08 + 0.016*SL
SI to QN	t_{PLH}	0.72	0.68 + 0.020*SL	0.69 + 0.019*SL	0.69 + 0.018*SL
	t_{PHL}	0.50	0.47 + 0.016*SL	0.48 + 0.010*SL	0.52 + 0.008*SL
	t_R	0.18	0.10 + 0.041*SL	0.09 + 0.041*SL	0.07 + 0.043*SL
	t_F	0.13	0.10 + 0.017*SL	0.10 + 0.016*SL	0.09 + 0.016*SL
SG to QN	t_{PLH}	0.72	0.68 + 0.021*SL	0.68 + 0.019*SL	0.69 + 0.018*SL
	t_{PHL}	0.42	0.39 + 0.014*SL	0.40 + 0.010*SL	0.44 + 0.008*SL
	t_R	0.18	0.09 + 0.044*SL	0.10 + 0.041*SL	0.07 + 0.043*SL
	t_F	0.13	0.11 + 0.013*SL	0.10 + 0.016*SL	0.09 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

LD1SD2 Timing Requirements

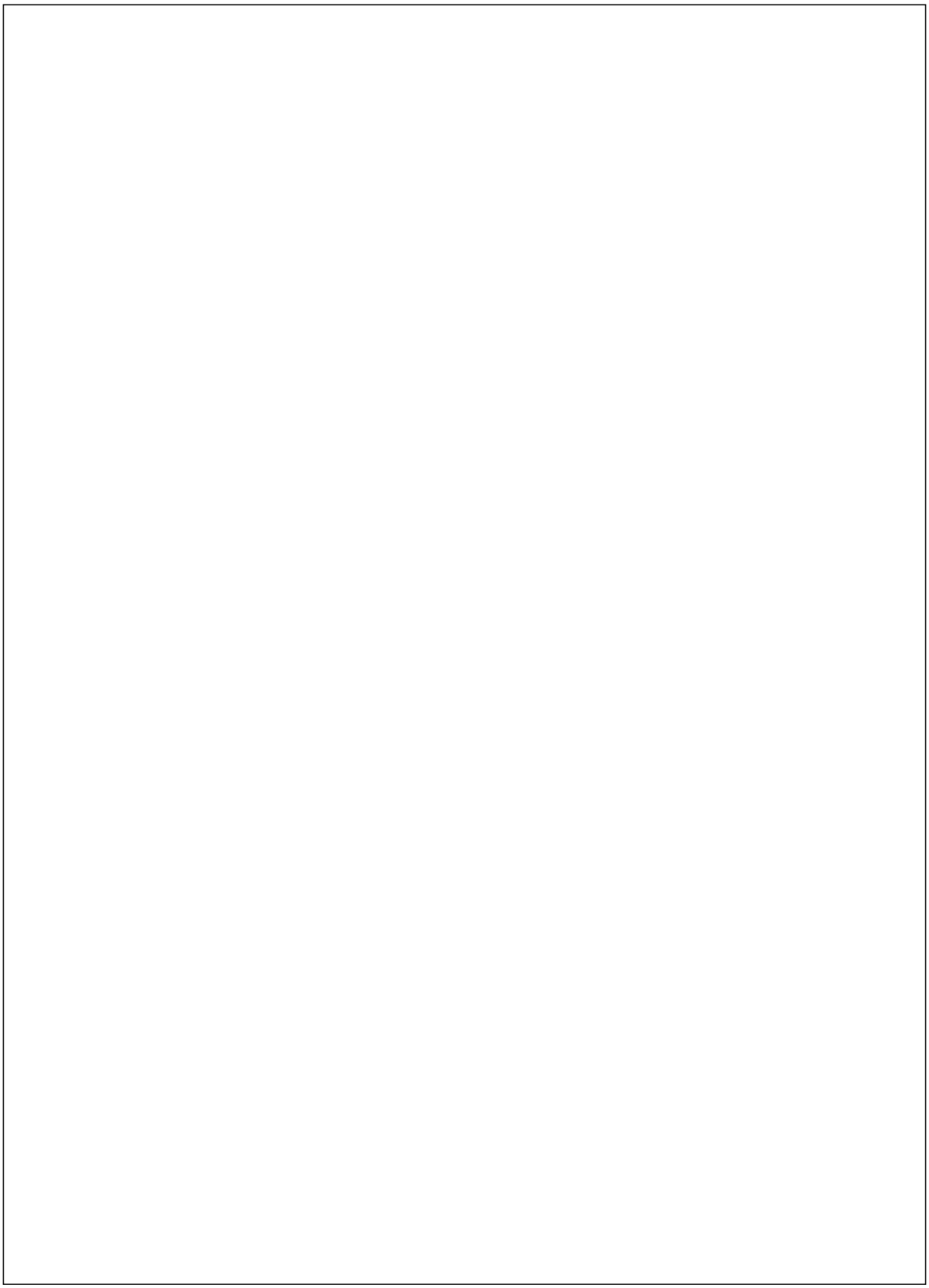
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	t_{PWH}	0.000

LD1SD2 Timing Requirements

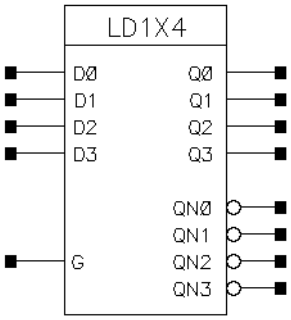
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (SG)	t_{PWH}	0.000
Input Hold Time (D to G)	t_{HD}	0.000
Input Hold Time (SI to SG)	t_{HD}	0.000
Input Setup Time (D to G)	t_{SU}	0.000
Input Setup Time (SI to SG)	t_{SU}	0.000



Inputs: D0, D1, D2, D3, G
Outputs: Q0, Q1, Q2, Q3
QN0, QN1, QN2, QN3
Input Loading (SL):
- D0, DI, D2, D3: 3
- G: 1

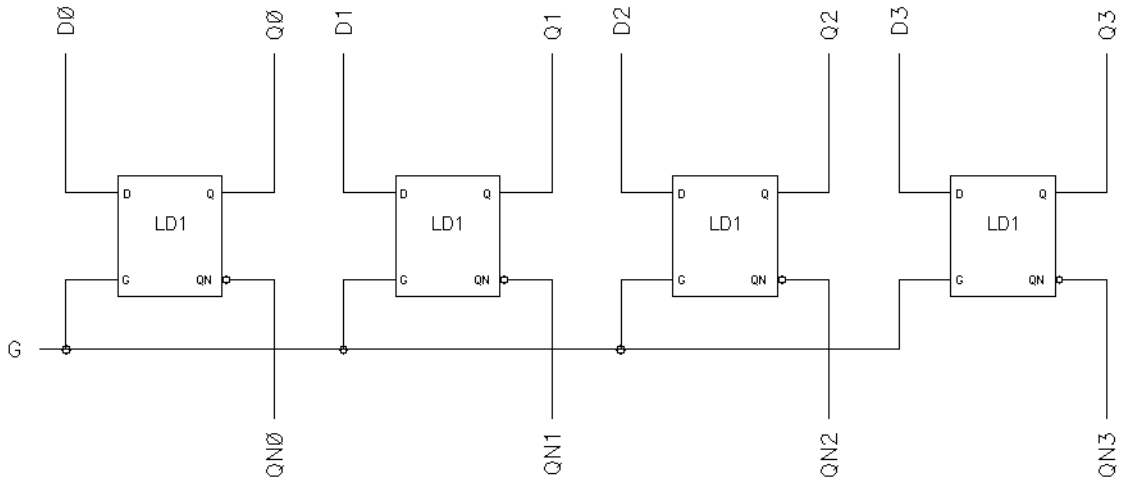
Maximum Fanout (Rec. SL): All : 28
Gate Count: 13



Symbol

D	G	Qn+1	QNn+1
0	1	0	1
1	1	1	0
x	0	Qn	QNn

Truth Table



Schematic

LD1X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Q0	t_{PLH}	0.21	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
	t_{PHL}	0.38	0.33 + 0.025*SL	0.35 + 0.018*SL	0.38 + 0.017*SL
	t_R	0.26	0.10 + 0.083*SL	0.08 + 0.087*SL	0.06 + 0.088*SL
	t_F	0.16	0.09 + 0.035*SL	0.10 + 0.032*SL	0.07 + 0.034*SL
G to Q0	t_{PLH}	0.41	0.33 + 0.040*SL	0.34 + 0.038*SL	0.34 + 0.038*SL
	t_{PHL}	0.48	0.43 + 0.024*SL	0.45 + 0.018*SL	0.47 + 0.017*SL
	t_R	0.25	0.07 + 0.086*SL	0.07 + 0.088*SL	0.05 + 0.089*SL
	t_F	0.13	0.06 + 0.035*SL	0.07 + 0.033*SL	0.06 + 0.034*SL
D1 to Q1	t_{PLH}	0.20	0.13 + 0.038*SL	0.13 + 0.036*SL	0.13 + 0.036*SL
	t_{PHL}	0.38	0.33 + 0.024*SL	0.35 + 0.017*SL	0.38 + 0.016*SL
	t_R	0.25	0.09 + 0.080*SL	0.08 + 0.083*SL	0.06 + 0.084*SL
	t_F	0.16	0.09 + 0.034*SL	0.10 + 0.031*SL	0.06 + 0.032*SL
G to Q1	t_{PLH}	0.41	0.33 + 0.038*SL	0.34 + 0.036*SL	0.34 + 0.036*SL
	t_{PHL}	0.48	0.43 + 0.024*SL	0.45 + 0.017*SL	0.47 + 0.016*SL
	t_R	0.24	0.07 + 0.081*SL	0.07 + 0.084*SL	0.05 + 0.085*SL
	t_F	0.13	0.06 + 0.034*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
D2 to Q2	t_{PLH}	0.21	0.13 + 0.039*SL	0.13 + 0.038*SL	0.13 + 0.038*SL
	t_{PHL}	0.38	0.33 + 0.025*SL	0.35 + 0.018*SL	0.38 + 0.017*SL
	t_R	0.26	0.10 + 0.083*SL	0.08 + 0.087*SL	0.06 + 0.088*SL
	t_F	0.16	0.09 + 0.035*SL	0.10 + 0.032*SL	0.07 + 0.034*SL
G to Q2	t_{PLH}	0.41	0.33 + 0.040*SL	0.34 + 0.038*SL	0.34 + 0.038*SL
	t_{PHL}	0.48	0.43 + 0.024*SL	0.45 + 0.018*SL	0.47 + 0.017*SL
	t_R	0.25	0.07 + 0.086*SL	0.07 + 0.088*SL	0.05 + 0.089*SL
	t_F	0.13	0.07 + 0.034*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
D3 to Q3	t_{PLH}	0.20	0.13 + 0.038*SL	0.13 + 0.036*SL	0.13 + 0.036*SL
	t_{PHL}	0.38	0.33 + 0.024*SL	0.35 + 0.017*SL	0.38 + 0.016*SL
	t_R	0.25	0.09 + 0.080*SL	0.08 + 0.083*SL	0.06 + 0.084*SL
	t_F	0.16	0.09 + 0.034*SL	0.10 + 0.031*SL	0.06 + 0.032*SL
G to Q3	t_{PLH}	0.41	0.33 + 0.038*SL	0.34 + 0.036*SL	0.34 + 0.036*SL
	t_{PHL}	0.48	0.43 + 0.024*SL	0.45 + 0.017*SL	0.47 + 0.016*SL
	t_R	0.24	0.07 + 0.081*SL	0.07 + 0.084*SL	0.05 + 0.084*SL
	t_F	0.13	0.07 + 0.032*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
D0 to QN0	t_{PLH}	0.49	0.42 + 0.036*SL	0.41 + 0.037*SL	0.41 + 0.038*SL
	t_{PHL}	0.25	0.20 + 0.022*SL	0.22 + 0.017*SL	0.23 + 0.016*SL
	t_R	0.24	0.08 + 0.081*SL	0.06 + 0.088*SL	0.05 + 0.089*SL
	t_F	0.14	0.07 + 0.032*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
G to QN0	t_{PLH}	0.58	0.51 + 0.037*SL	0.51 + 0.038*SL	0.51 + 0.038*SL
	t_{PHL}	0.45	0.40 + 0.023*SL	0.42 + 0.017*SL	0.43 + 0.017*SL
	t_R	0.24	0.07 + 0.086*SL	0.06 + 0.088*SL	0.05 + 0.089*SL
	t_F	0.14	0.06 + 0.036*SL	0.08 + 0.033*SL	0.04 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD1X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D1 to QN1	tPLH	0.49	0.42 + 0.034*SL	0.41 + 0.036*SL	0.41 + 0.036*SL
	tPHL	0.24	0.20 + 0.022*SL	0.22 + 0.017*SL	0.23 + 0.016*SL
	tR	0.24	0.08 + 0.078*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.13	0.07 + 0.031*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
G to QN1	tPLH	0.58	0.51 + 0.036*SL	0.51 + 0.036*SL	0.51 + 0.036*SL
	tPHL	0.45	0.40 + 0.023*SL	0.42 + 0.017*SL	0.43 + 0.016*SL
	tR	0.23	0.06 + 0.083*SL	0.06 + 0.084*SL	0.05 + 0.084*SL
	tF	0.13	0.06 + 0.036*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
D2 to QN2	tPLH	0.49	0.42 + 0.036*SL	0.41 + 0.037*SL	0.41 + 0.038*SL
	tPHL	0.25	0.20 + 0.022*SL	0.22 + 0.017*SL	0.23 + 0.016*SL
	tR	0.25	0.08 + 0.081*SL	0.06 + 0.088*SL	0.05 + 0.089*SL
	tF	0.14	0.07 + 0.032*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
G to QN2	tPLH	0.58	0.51 + 0.037*SL	0.51 + 0.038*SL	0.51 + 0.038*SL
	tPHL	0.45	0.40 + 0.023*SL	0.42 + 0.017*SL	0.43 + 0.017*SL
	tR	0.24	0.07 + 0.084*SL	0.06 + 0.088*SL	0.05 + 0.089*SL
	tF	0.14	0.06 + 0.036*SL	0.08 + 0.033*SL	0.05 + 0.034*SL
D3 to QN3	tPLH	0.49	0.42 + 0.034*SL	0.41 + 0.036*SL	0.41 + 0.036*SL
	tPHL	0.24	0.20 + 0.022*SL	0.22 + 0.017*SL	0.23 + 0.016*SL
	tR	0.24	0.08 + 0.078*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.13	0.07 + 0.031*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
G to QN3	tPLH	0.58	0.51 + 0.037*SL	0.51 + 0.036*SL	0.51 + 0.036*SL
	tPHL	0.45	0.40 + 0.023*SL	0.42 + 0.017*SL	0.43 + 0.016*SL
	tR	0.23	0.06 + 0.085*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.13	0.06 + 0.036*SL	0.07 + 0.031*SL	0.04 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD1X4 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	tPWH	0.000
Input Hold Time (D0 to G)	tHD	0.000
Input Hold Time (D1 to G)	tHD	0.000
Input Hold Time (D2 to G)	tHD	0.000
Input Hold Time (D3 to G)	tHD	0.000

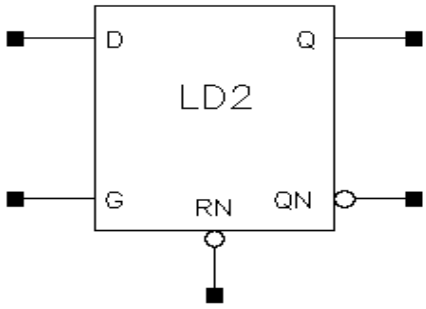
LD1X4 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Input Setup Time (D0 to G)	t_{SU}	0.000
Input Setup Time (D1 to G)	t_{SU}	0.000
Input Setup Time (D2 to G)	t_{SU}	0.000
Input Setup Time (D3 to G)	t_{SU}	0.000

Inputs: D, G, RN
Outputs: Q, QN
Input Loading (SL):
- D: 3
- G, RN: 1

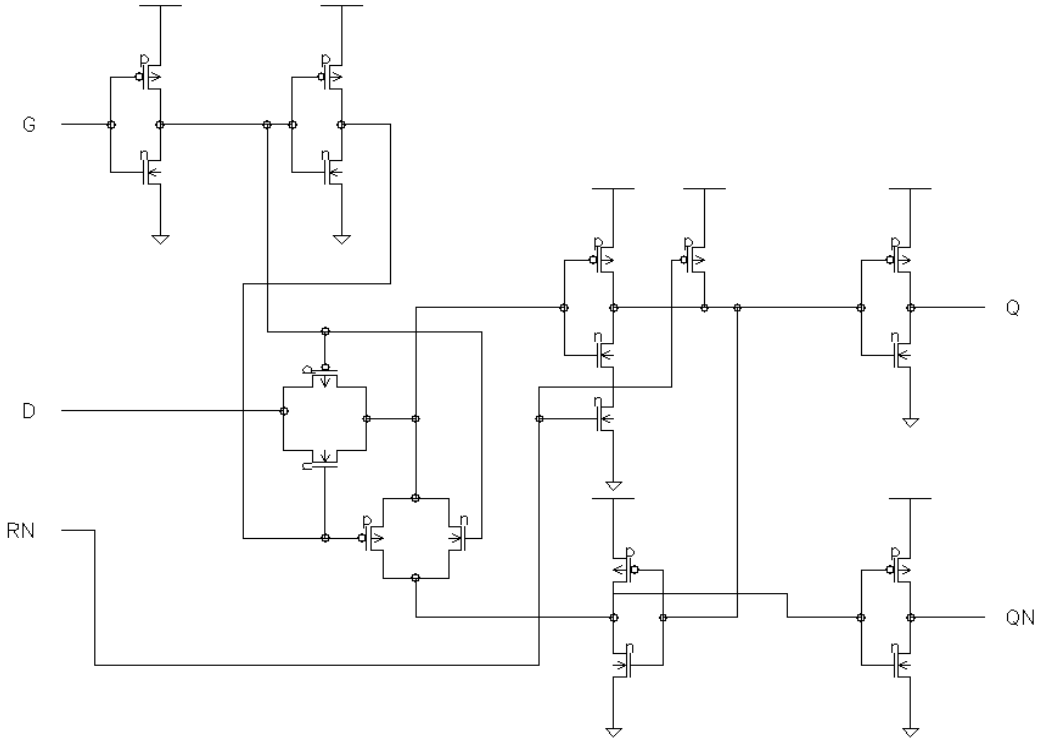
Maximum Fanout (Rec. SL): All : 28
Gate Count: 5



Symbol

D	G	RN	Qn+1	QNn+1
0	1	1	0	1
1	1	1	1	0
x	0	1	Qn	QNn
x	x	0	0	1

Truth Table



Schematic

LD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	t_{PLH}	0.23	0.14 + 0.042*SL	0.16 + 0.037*SL	0.17 + 0.036*SL
	t_{PHL}	0.39	0.33 + 0.028*SL	0.36 + 0.018*SL	0.40 + 0.016*SL
	t_R	0.27	0.11 + 0.081*SL	0.10 + 0.082*SL	0.07 + 0.084*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.030*SL	0.08 + 0.032*SL
D to Q	t_{PLH}	0.30	0.21 + 0.041*SL	0.23 + 0.037*SL	0.23 + 0.036*SL
	t_{PHL}	0.37	0.32 + 0.025*SL	0.34 + 0.018*SL	0.38 + 0.016*SL
	t_R	0.27	0.11 + 0.081*SL	0.10 + 0.083*SL	0.07 + 0.084*SL
	t_F	0.16	0.10 + 0.032*SL	0.11 + 0.031*SL	0.07 + 0.032*SL
G to Q	t_{PLH}	0.38	0.30 + 0.041*SL	0.31 + 0.037*SL	0.32 + 0.036*SL
	t_{PHL}	0.33	0.28 + 0.024*SL	0.30 + 0.017*SL	0.33 + 0.016*SL
	t_R	0.25	0.08 + 0.084*SL	0.09 + 0.083*SL	0.06 + 0.084*SL
	t_F	0.13	0.07 + 0.034*SL	0.07 + 0.032*SL	0.06 + 0.033*SL
RN to QN	t_{PLH}	0.50	0.43 + 0.035*SL	0.43 + 0.036*SL	0.43 + 0.036*SL
	t_{PHL}	0.27	0.23 + 0.022*SL	0.24 + 0.017*SL	0.25 + 0.016*SL
	t_R	0.24	0.08 + 0.078*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.14	0.07 + 0.033*SL	0.08 + 0.031*SL	0.05 + 0.033*SL
D to QN	t_{PLH}	0.48	0.41 + 0.035*SL	0.41 + 0.036*SL	0.41 + 0.036*SL
	t_{PHL}	0.34	0.29 + 0.023*SL	0.31 + 0.017*SL	0.32 + 0.016*SL
	t_R	0.24	0.08 + 0.079*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.14	0.07 + 0.037*SL	0.09 + 0.031*SL	0.04 + 0.033*SL
G to QN	t_{PLH}	0.44	0.37 + 0.035*SL	0.36 + 0.036*SL	0.36 + 0.036*SL
	t_{PHL}	0.42	0.38 + 0.022*SL	0.39 + 0.017*SL	0.41 + 0.016*SL
	t_R	0.23	0.07 + 0.080*SL	0.06 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.14	0.07 + 0.035*SL	0.08 + 0.031*SL	0.04 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

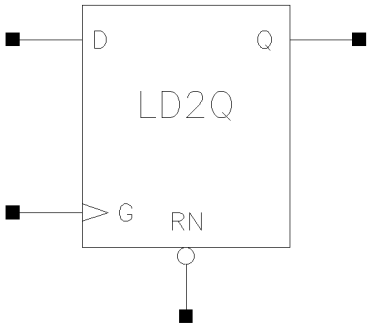
LD2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	t_{PWL}	0.000
Pulse Width High (G)	t_{PWH}	0.000
Input Hold Time (D to G)	t_{HD}	0.000
Input Setup Time (D to G)	t_{SU}	0.000
Recovery Time (RN)	t_{RC}	0.000

Inputs: D, G, RN
OutPUT: Q
Input Loading (SL): All: D: 3, G,RN: 1
Maximum Fanout (Rec. SL):
- LD2Q: 28
- LD2D3Q: 84

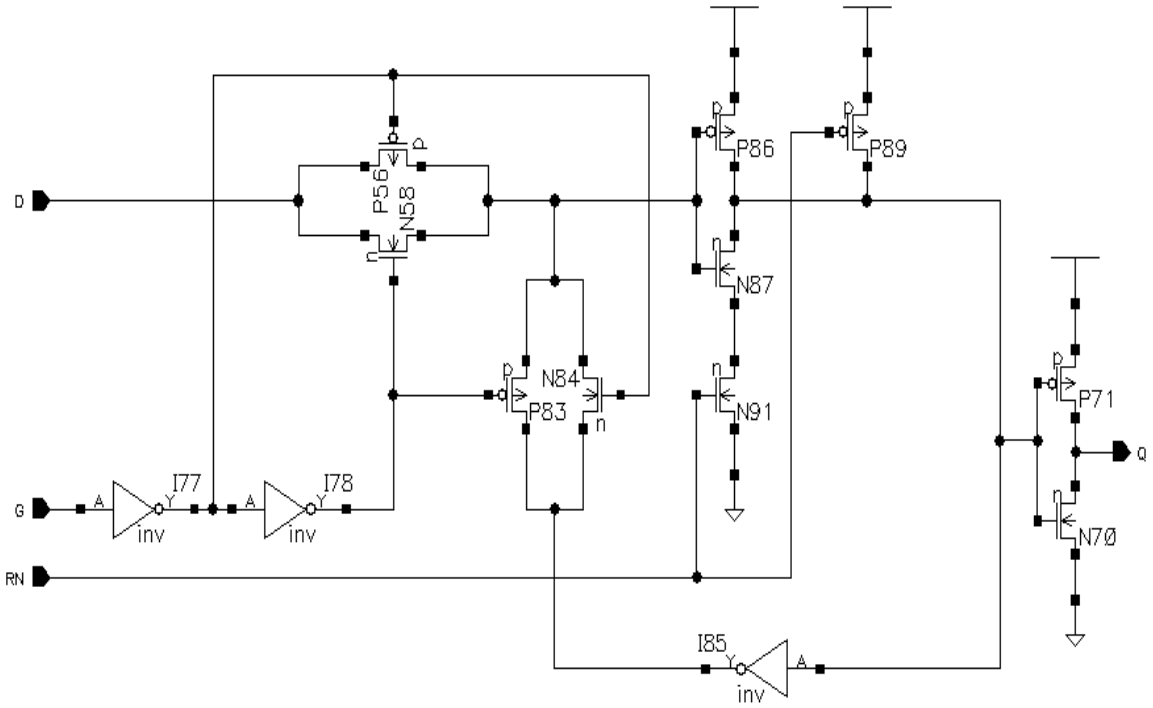
Gate Count:
- LD2Q: 4
- LD2D3Q: 5



Symbol

D	G	RN	Qn+1
0	1	1	0
1	1	1	1
x	0	1	Qn
x	x	0	0

Truth Table



Schematic

LD2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	t_{PLH}	0.24	0.15 + 0.043*SL	0.17 + 0.038*SL	0.17 + 0.038*SL
	t_{PHL}	0.40	0.34 + 0.029*SL	0.37 + 0.018*SL	0.40 + 0.016*SL
	t_R	0.28	0.11 + 0.083*SL	0.10 + 0.086*SL	0.06 + 0.088*SL
	t_F	0.19	0.12 + 0.035*SL	0.13 + 0.031*SL	0.07 + 0.034*SL
D to Q	t_{PLH}	0.30	0.22 + 0.043*SL	0.23 + 0.038*SL	0.24 + 0.038*SL
	t_{PHL}	0.38	0.32 + 0.028*SL	0.35 + 0.018*SL	0.38 + 0.016*SL
	t_R	0.28	0.11 + 0.086*SL	0.11 + 0.086*SL	0.07 + 0.088*SL
	t_F	0.17	0.11 + 0.034*SL	0.12 + 0.031*SL	0.06 + 0.034*SL
G to Q	t_{PLH}	0.39	0.30 + 0.043*SL	0.32 + 0.038*SL	0.32 + 0.038*SL
	t_{PHL}	0.33	0.28 + 0.025*SL	0.31 + 0.018*SL	0.33 + 0.016*SL
	t_R	0.27	0.11 + 0.081*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
	t_F	0.14	0.07 + 0.037*SL	0.08 + 0.033*SL	0.05 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	t_{PWL}	0.000
Pulse Width High (G)	t_{PWH}	0.000
Input Hold Time (D to G)	t_{HD}	0.000
Input Setup Time (D to G)	t_{SU}	0.000
Recovery Time (RN)	t_{RC}	0.000

LD2D3Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

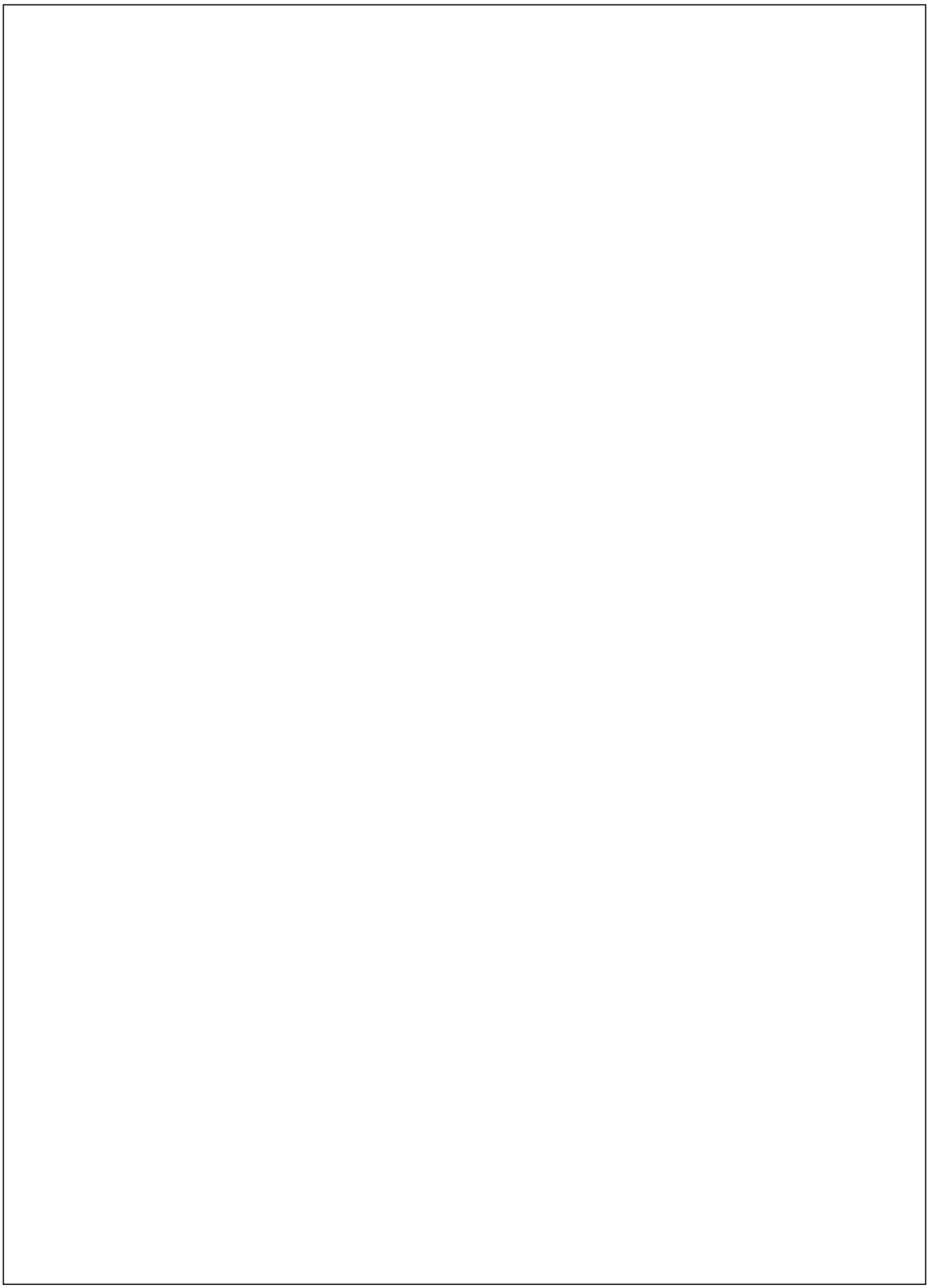
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	t_{PLH}	0.25	0.22 + 0.016*SL	0.23 + 0.014*SL	0.25 + 0.013*SL
	t_{PHL}	0.42	0.39 + 0.016*SL	0.41 + 0.009*SL	0.46 + 0.006*SL
	t_R	0.18	0.13 + 0.028*SL	0.12 + 0.029*SL	0.11 + 0.029*SL
	t_F	0.17	0.14 + 0.016*SL	0.16 + 0.010*SL	0.15 + 0.010*SL
D to Q	t_{PLH}	0.34	0.31 + 0.015*SL	0.31 + 0.013*SL	0.33 + 0.013*SL
	t_{PHL}	0.42	0.39 + 0.013*SL	0.40 + 0.008*SL	0.44 + 0.006*SL
	t_R	0.19	0.13 + 0.027*SL	0.13 + 0.028*SL	0.11 + 0.029*SL
	t_F	0.17	0.15 + 0.011*SL	0.15 + 0.010*SL	0.14 + 0.011*SL
G to Q	t_{PLH}	0.39	0.36 + 0.016*SL	0.37 + 0.014*SL	0.39 + 0.013*SL
	t_{PHL}	0.36	0.33 + 0.013*SL	0.35 + 0.008*SL	0.38 + 0.006*SL
	t_R	0.17	0.12 + 0.028*SL	0.12 + 0.028*SL	0.09 + 0.030*SL
	t_F	0.13	0.10 + 0.014*SL	0.11 + 0.011*SL	0.13 + 0.011*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

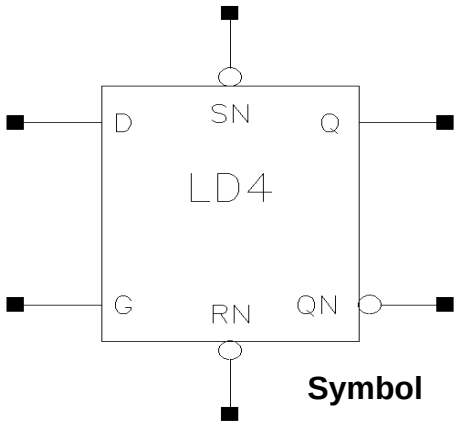
LD2D3Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	t_{PWL}	0.000
Pulse Width High (G)	t_{PWH}	0.000
Input Hold Time (D to G)	t_{HD}	0.000
Input Setup Time (D to G)	t_{SU}	0.000
Recovery Time (RN)	t_{RC}	0.000



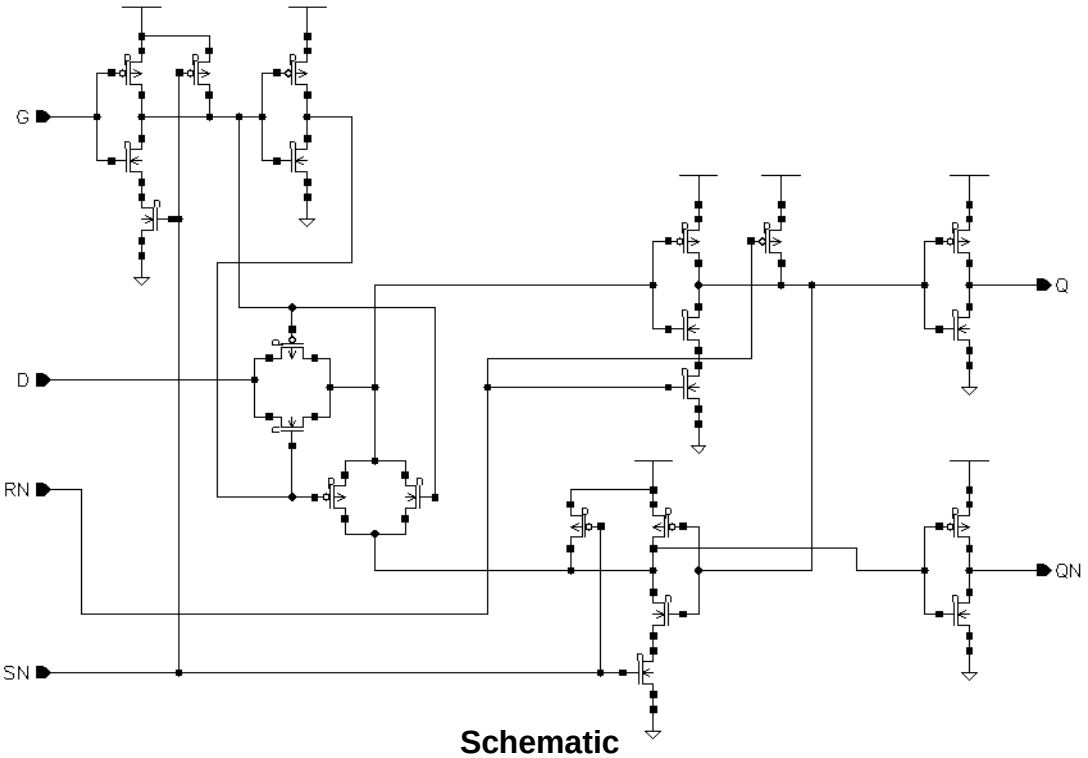
Inputs: D, G, RN, SN
OutPUT: Q, QN
Input Loading (SL): D,: 3, G, RN : 1
SN : 2
Maximum Fanout (Rec. SL): 28
Gate Count: 6



Symbol

D	G	RN	SN	Qn+1	QNn+1
0	1	1	1	0	1
1	1	1	1	1	0
x	x	0	0	0	1
x	x	0	1	0	1
x	x	1	0	1	0
x	0	1	1	Qn	QNn

Truth Table



Schematic

LD4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.23	0.14 + 0.042*SL	0.16 + 0.037*SL	0.17 + 0.036*SL
	tPHL	0.38	0.33 + 0.027*SL	0.36 + 0.018*SL	0.39 + 0.016*SL
	tR	0.27	0.11 + 0.078*SL	0.10 + 0.083*SL	0.07 + 0.084*SL
	tF	0.18	0.11 + 0.033*SL	0.12 + 0.030*SL	0.08 + 0.032*SL
SN to Q	tPLH	0.75	0.67 + 0.037*SL	0.67 + 0.036*SL	0.67 + 0.036*SL
	tPHL	0.37	0.33 + 0.024*SL	0.34 + 0.017*SL	0.37 + 0.016*SL
	tR	0.26	0.10 + 0.079*SL	0.09 + 0.083*SL	0.06 + 0.084*SL
	tF	0.13	0.07 + 0.035*SL	0.07 + 0.032*SL	0.06 + 0.033*SL
D to Q	tPLH	0.30	0.21 + 0.041*SL	0.23 + 0.037*SL	0.23 + 0.036*SL
	tPHL	0.37	0.32 + 0.025*SL	0.34 + 0.018*SL	0.37 + 0.016*SL
	tR	0.27	0.11 + 0.081*SL	0.10 + 0.083*SL	0.07 + 0.084*SL
	tF	0.17	0.11 + 0.030*SL	0.10 + 0.031*SL	0.07 + 0.032*SL
G to Q	tPLH	0.46	0.38 + 0.041*SL	0.39 + 0.037*SL	0.40 + 0.036*SL
	tPHL	0.41	0.36 + 0.023*SL	0.38 + 0.017*SL	0.40 + 0.016*SL
	tR	0.25	0.09 + 0.081*SL	0.08 + 0.083*SL	0.06 + 0.084*SL
	tF	0.14	0.06 + 0.037*SL	0.08 + 0.032*SL	0.06 + 0.033*SL
RN to QN	tPLH	0.56	0.48 + 0.037*SL	0.49 + 0.036*SL	0.48 + 0.036*SL
	tPHL	0.28	0.23 + 0.024*SL	0.25 + 0.017*SL	0.27 + 0.016*SL
	tR	0.25	0.09 + 0.080*SL	0.09 + 0.082*SL	0.05 + 0.084*SL
	tF	0.14	0.07 + 0.035*SL	0.08 + 0.031*SL	0.06 + 0.032*SL
SN to QN	tPLH	0.28	0.19 + 0.042*SL	0.21 + 0.036*SL	0.21 + 0.036*SL
	tPHL	0.37	0.32 + 0.025*SL	0.34 + 0.018*SL	0.37 + 0.016*SL
	tR	0.26	0.10 + 0.081*SL	0.10 + 0.082*SL	0.06 + 0.084*SL
	tF	0.16	0.11 + 0.025*SL	0.09 + 0.031*SL	0.07 + 0.032*SL
D to QN	tPLH	0.54	0.46 + 0.036*SL	0.46 + 0.036*SL	0.46 + 0.036*SL
	tPHL	0.34	0.30 + 0.024*SL	0.32 + 0.017*SL	0.33 + 0.016*SL
	tR	0.25	0.08 + 0.081*SL	0.08 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.06 + 0.040*SL	0.09 + 0.031*SL	0.05 + 0.032*SL
G to QN	tPLH	0.57	0.49 + 0.037*SL	0.50 + 0.036*SL	0.50 + 0.036*SL
	tPHL	0.52	0.47 + 0.023*SL	0.49 + 0.017*SL	0.50 + 0.016*SL
	tR	0.25	0.09 + 0.077*SL	0.08 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.07 + 0.038*SL	0.09 + 0.031*SL	0.05 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD4 Timing Requirements

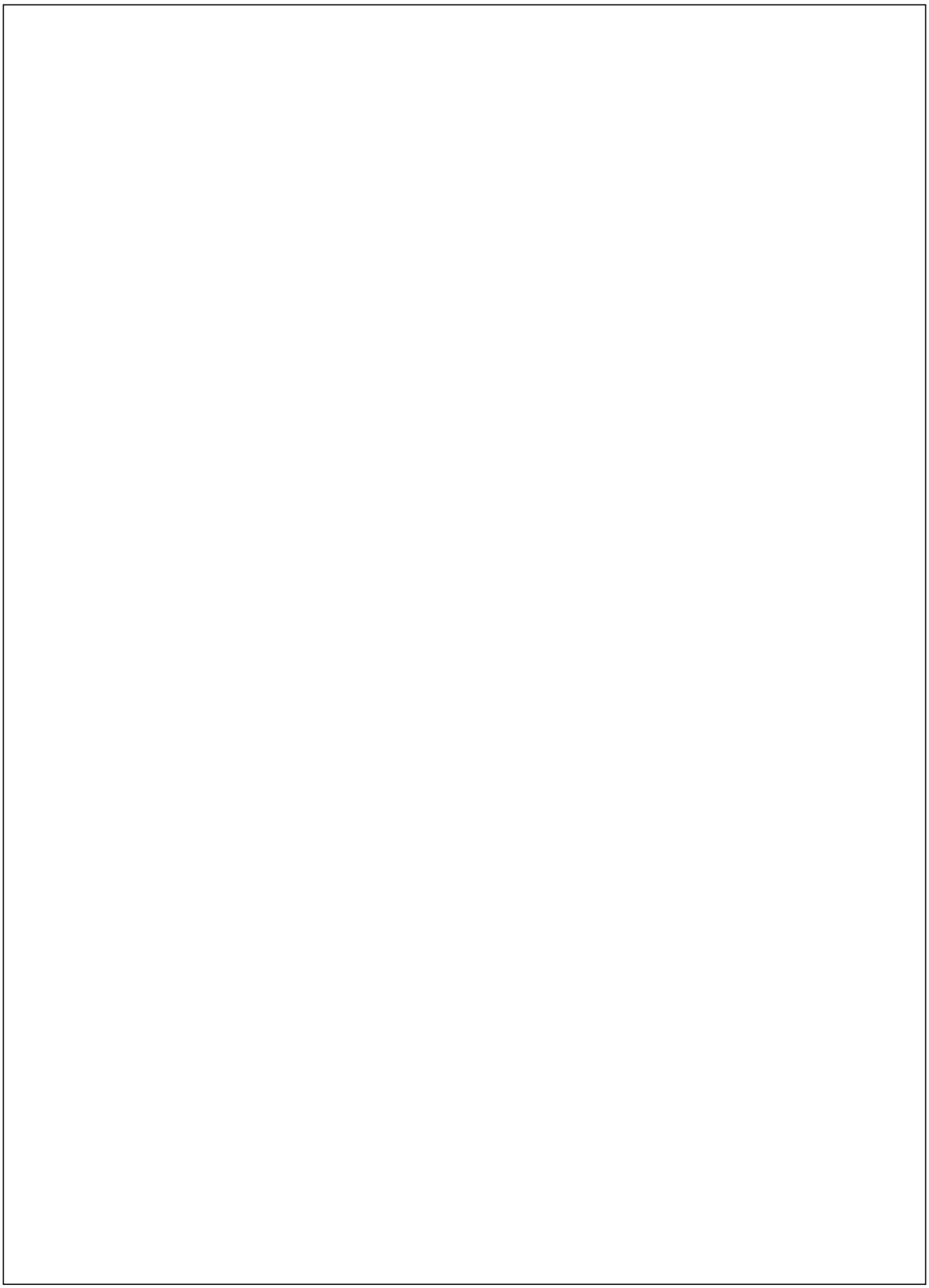
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	tPWL	0.000

LD4 Timing Requirements

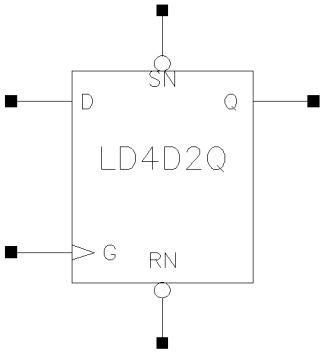
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (SN)	t_{PWL}	0.000
Pulse Width High (G)	t_{PWH}	0.000
Input Hold Time (D to G)	t_{HD}	0.000
Input Setup Time (D to G)	t_{SU}	0.000
Recovery Time (RN)	t_{RC}	0.000
Recovery Time (SN)	t_{RC}	0.000



Inputs: D, G, RN, SN
OutPUT: Q
Input Loading (SL): All: D: 3, G, RN: 1,
SN: 2
Maximum Fanout (Rec. SL):
- LD4D2Q: 56
- LD4D4Q: 144

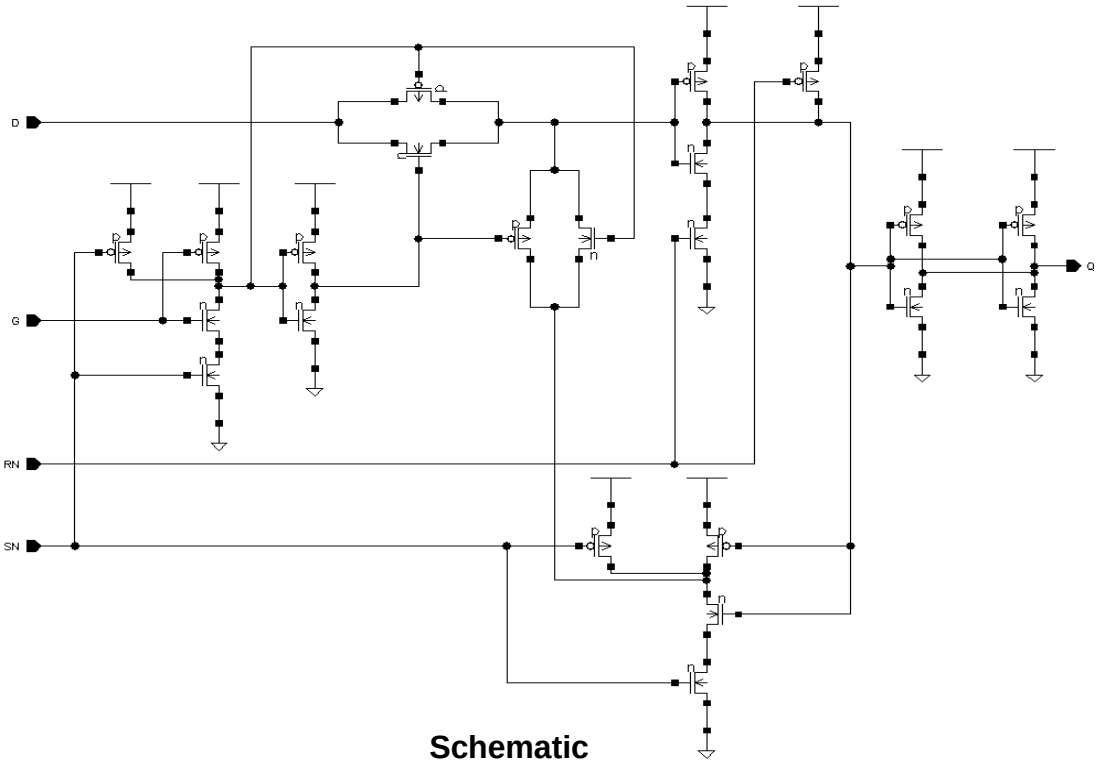
Gate Count:
- LD4D2Q: 6
- LD4D4Q: 7



Symbol

D	G	RN	SN	Qn+1
0	1	1	1	0
1	1	1	1	1
x	x	0	0	0
x	x	0	1	0
x	x	1	0	1
x	0	1	1	Qn

Truth Table



Schematic

LD4D2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.23	0.18 + 0.024*SL	0.19 + 0.020*SL	0.21 + 0.019*SL
	tPHL	0.39	0.36 + 0.017*SL	0.38 + 0.011*SL	0.43 + 0.009*SL
	tR	0.20	0.12 + 0.039*SL	0.11 + 0.044*SL	0.09 + 0.045*SL
	tF	0.17	0.14 + 0.017*SL	0.14 + 0.016*SL	0.12 + 0.017*SL
SN to Q	tPLH	0.72	0.68 + 0.023*SL	0.69 + 0.019*SL	0.70 + 0.019*SL
	tPHL	0.38	0.35 + 0.016*SL	0.37 + 0.010*SL	0.40 + 0.009*SL
	tR	0.19	0.11 + 0.041*SL	0.10 + 0.044*SL	0.08 + 0.045*SL
	tF	0.12	0.09 + 0.017*SL	0.09 + 0.017*SL	0.09 + 0.017*SL
D to Q	tPLH	0.31	0.26 + 0.023*SL	0.27 + 0.020*SL	0.29 + 0.019*SL
	tPHL	0.38	0.35 + 0.017*SL	0.37 + 0.011*SL	0.41 + 0.009*SL
	tR	0.20	0.11 + 0.047*SL	0.12 + 0.043*SL	0.09 + 0.045*SL
	tF	0.16	0.12 + 0.017*SL	0.12 + 0.016*SL	0.12 + 0.016*SL
G to Q	tPLH	0.46	0.42 + 0.022*SL	0.42 + 0.020*SL	0.44 + 0.019*SL
	tPHL	0.41	0.38 + 0.015*SL	0.40 + 0.011*SL	0.44 + 0.009*SL
	tR	0.19	0.10 + 0.044*SL	0.10 + 0.044*SL	0.08 + 0.045*SL
	tF	0.12	0.09 + 0.018*SL	0.09 + 0.017*SL	0.09 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD4D2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	tPWL	0.000
Pulse Width Low (SN)	tPWL	0.000
Pulse Width High (G)	tPWH	0.000
Input Hold Time (D to G)	tHD	0.000
Input Setup Time (D to G)	tSU	0.000
Recovery Time (RN)	tRC	0.000
Recovery Time (SN)	tRC	0.000

LD4D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

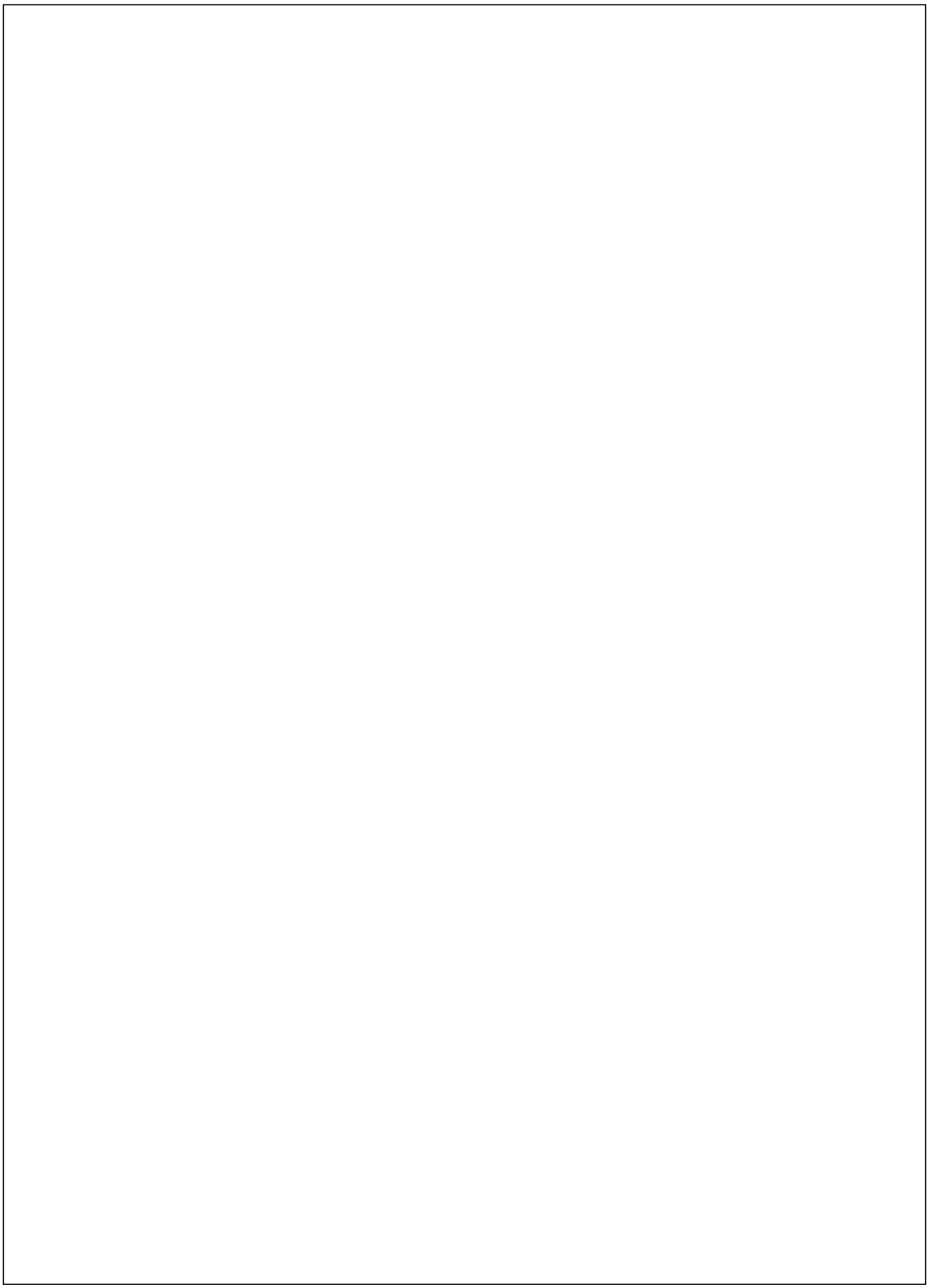
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	t_{PLH}	0.28	0.26 + 0.011*SL	0.26 + 0.011*SL	0.29 + 0.010*SL
	t_{PHL}	0.44	0.43 + 0.010*SL	0.43 + 0.007*SL	0.47 + 0.005*SL
	t_R	0.19	0.14 + 0.024*SL	0.15 + 0.021*SL	0.13 + 0.022*SL
	t_F	0.19	0.17 + 0.011*SL	0.18 + 0.008*SL	0.18 + 0.008*SL
SN to Q	t_{PLH}	0.77	0.75 + 0.014*SL	0.76 + 0.010*SL	0.77 + 0.010*SL
	t_{PHL}	0.43	0.41 + 0.009*SL	0.42 + 0.007*SL	0.45 + 0.005*SL
	t_R	0.17	0.12 + 0.025*SL	0.13 + 0.021*SL	0.12 + 0.022*SL
	t_F	0.14	0.13 + 0.009*SL	0.13 + 0.009*SL	0.14 + 0.008*SL
D to Q	t_{PLH}	0.37	0.35 + 0.012*SL	0.35 + 0.011*SL	0.38 + 0.010*SL
	t_{PHL}	0.44	0.41 + 0.012*SL	0.43 + 0.007*SL	0.46 + 0.005*SL
	t_R	0.18	0.15 + 0.015*SL	0.13 + 0.022*SL	0.13 + 0.022*SL
	t_F	0.18	0.15 + 0.010*SL	0.16 + 0.008*SL	0.16 + 0.008*SL
G to Q	t_{PLH}	0.50	0.48 + 0.013*SL	0.48 + 0.011*SL	0.50 + 0.010*SL
	t_{PHL}	0.45	0.43 + 0.013*SL	0.45 + 0.007*SL	0.48 + 0.005*SL
	t_R	0.16	0.12 + 0.021*SL	0.12 + 0.022*SL	0.11 + 0.022*SL
	t_F	0.14	0.12 + 0.012*SL	0.13 + 0.009*SL	0.14 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

LD4D4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

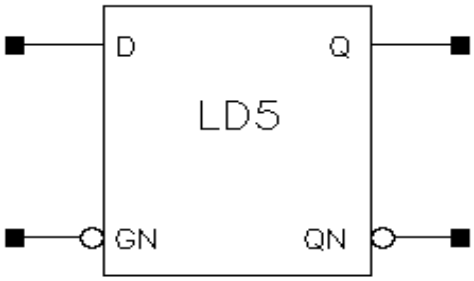
Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	t_{PWL}	0.000
Pulse Width Low (SN)	t_{PWL}	0.000
Pulse Width High (G)	t_{PWH}	0.000
Input Hold Time (D to G)	t_{HD}	0.000
Input Setup Time (D to G)	t_{SU}	0.000
Recovery Time (RN)	t_{RC}	0.000
Recovery Time (SN)	t_{RC}	0.000



Inputs: D, GN
Outputs: Q, QN
Input Loading (SL):
- D: 3
- GN: 1

Maximum Fanout (Rec. SL):
- LD5: All : 28
- LD5D2: All: 56

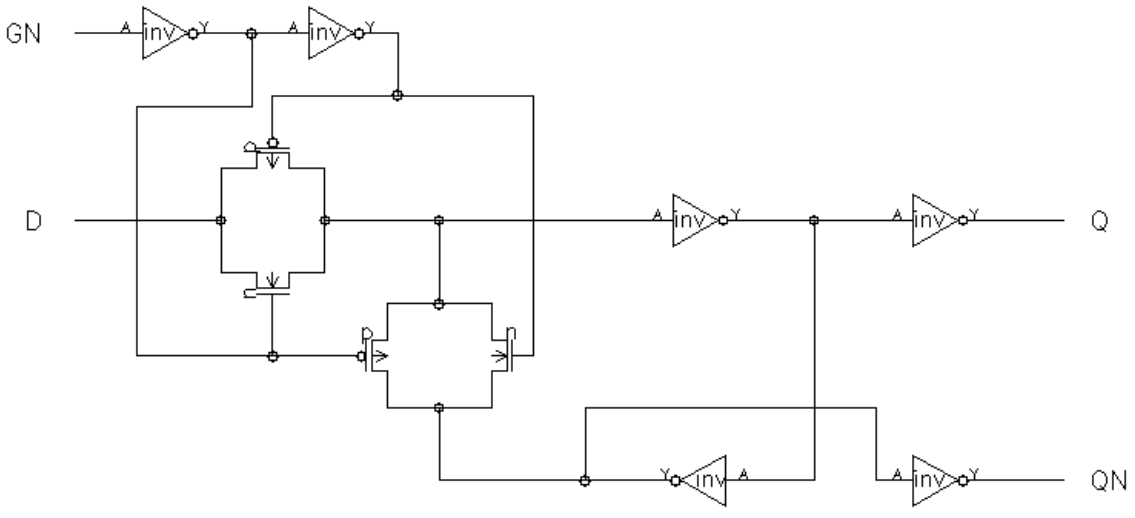
Gate Count:
- LD5: 4
- LD5D2: 5



Symbol

D	GN	Qn+1	QNn+1
0	0	0	1
1	0	1	0
X	1	Qn	QNn

Truth Table



Schematic

LD5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	t_{PLH}	0.21	0.13 + 0.038*SL	0.13 + 0.036*SL	0.14 + 0.036*SL
	t_{PHL}	0.38	0.33 + 0.025*SL	0.35 + 0.017*SL	0.38 + 0.016*SL
	t_R	0.25	0.09 + 0.080*SL	0.08 + 0.083*SL	0.06 + 0.084*SL
	t_F	0.16	0.09 + 0.034*SL	0.10 + 0.031*SL	0.07 + 0.032*SL
GN to Q	t_{PLH}	0.54	0.47 + 0.039*SL	0.47 + 0.037*SL	0.48 + 0.036*SL
	t_{PHL}	0.52	0.47 + 0.024*SL	0.49 + 0.017*SL	0.51 + 0.016*SL
	t_R	0.24	0.07 + 0.084*SL	0.07 + 0.084*SL	0.05 + 0.085*SL
	t_F	0.13	0.07 + 0.033*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
D to QN	t_{PLH}	0.49	0.42 + 0.034*SL	0.41 + 0.036*SL	0.41 + 0.036*SL
	t_{PHL}	0.24	0.20 + 0.022*SL	0.22 + 0.017*SL	0.23 + 0.016*SL
	t_R	0.24	0.08 + 0.077*SL	0.06 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.13	0.07 + 0.031*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
GN to QN	t_{PLH}	0.62	0.55 + 0.036*SL	0.55 + 0.036*SL	0.55 + 0.036*SL
	t_{PHL}	0.58	0.54 + 0.022*SL	0.55 + 0.017*SL	0.57 + 0.016*SL
	t_R	0.23	0.07 + 0.084*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.13	0.06 + 0.035*SL	0.07 + 0.031*SL	0.04 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD5 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	t_{PWL}	0.000
Input Hold Time (D to GN)	t_{HD}	0.000
Input Setup Time (D to GN)	t_{SU}	0.000

LD5D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

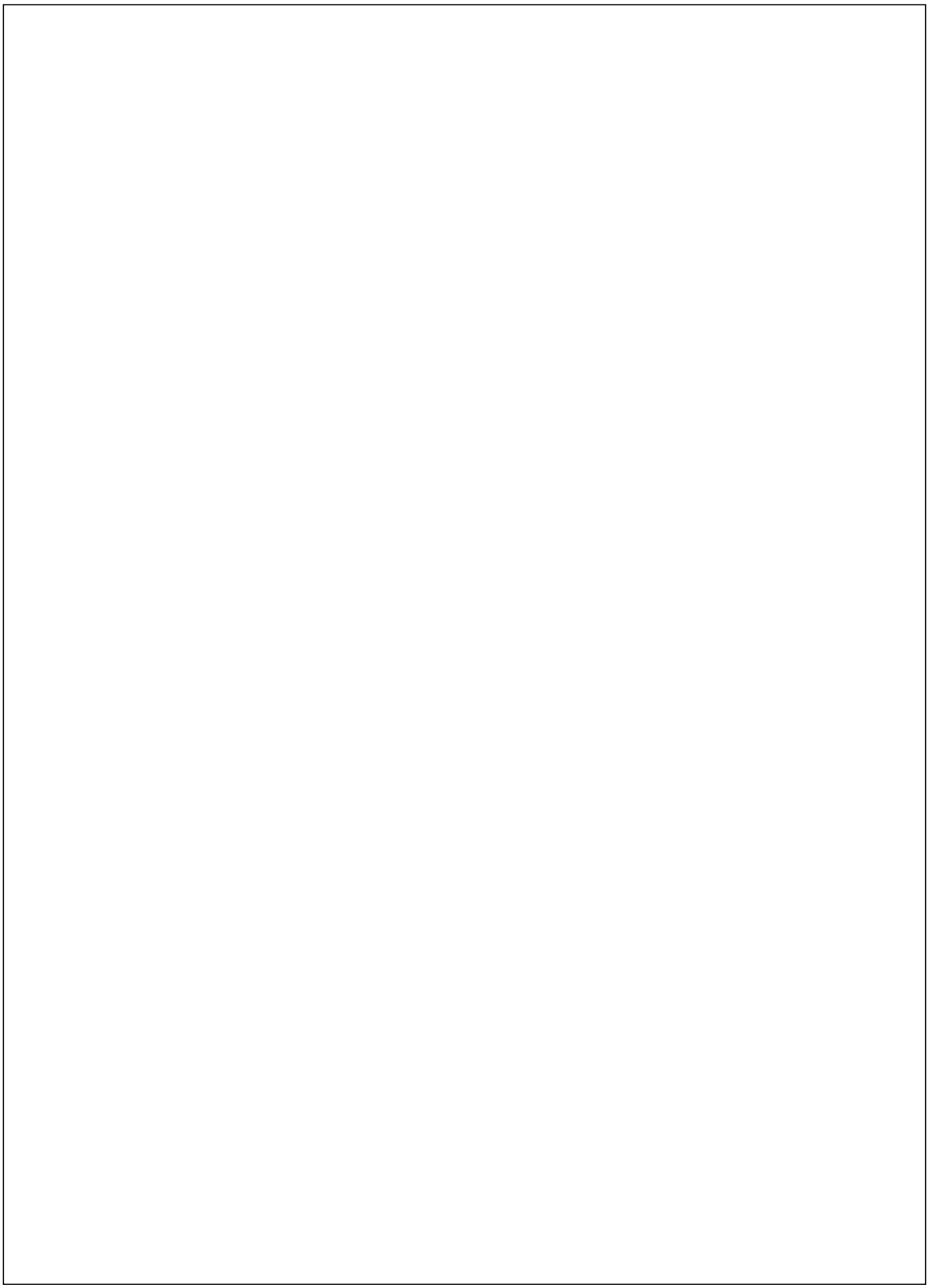
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	t_{PLH}	0.20	0.16 + 0.020*SL	0.17 + 0.019*SL	0.18 + 0.018*SL
	t_{PHL}	0.39	0.36 + 0.016*SL	0.37 + 0.010*SL	0.41 + 0.008*SL
	t_R	0.18	0.10 + 0.040*SL	0.09 + 0.041*SL	0.06 + 0.043*SL
	t_F	0.15	0.11 + 0.016*SL	0.12 + 0.015*SL	0.10 + 0.016*SL
GN to Q	t_{PLH}	0.53	0.49 + 0.020*SL	0.49 + 0.019*SL	0.50 + 0.018*SL
	t_{PHL}	0.52	0.49 + 0.015*SL	0.51 + 0.010*SL	0.54 + 0.008*SL
	t_R	0.15	0.08 + 0.038*SL	0.06 + 0.042*SL	0.06 + 0.043*SL
	t_F	0.12	0.08 + 0.018*SL	0.09 + 0.016*SL	0.08 + 0.016*SL
D to QN	t_{PLH}	0.52	0.49 + 0.017*SL	0.49 + 0.018*SL	0.48 + 0.018*SL
	t_{PHL}	0.30	0.27 + 0.013*SL	0.28 + 0.010*SL	0.31 + 0.008*SL
	t_R	0.16	0.09 + 0.036*SL	0.07 + 0.041*SL	0.05 + 0.042*SL
	t_F	0.11	0.08 + 0.017*SL	0.08 + 0.016*SL	0.08 + 0.016*SL
GN to QN	t_{PLH}	0.65	0.62 + 0.017*SL	0.61 + 0.018*SL	0.61 + 0.018*SL
	t_{PHL}	0.62	0.59 + 0.014*SL	0.60 + 0.009*SL	0.63 + 0.008*SL
	t_R	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.05 + 0.042*SL
	t_F	0.11	0.07 + 0.020*SL	0.09 + 0.016*SL	0.08 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD5D2 Timing Requirements

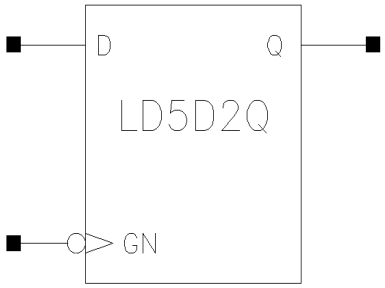
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	t_{PWL}	0.000
Input Hold Time (D to GN)	t_{HD}	0.000
Input Setup Time (D to GN)	t_{SU}	0.000



Inputs: D, GN
Outputs: Q
Input Loading (SL): All : D: 3, GN: 1
Maximum Fanout (Rec. SL):
- LD5D2Q: 56
- LD5D4Q: 112

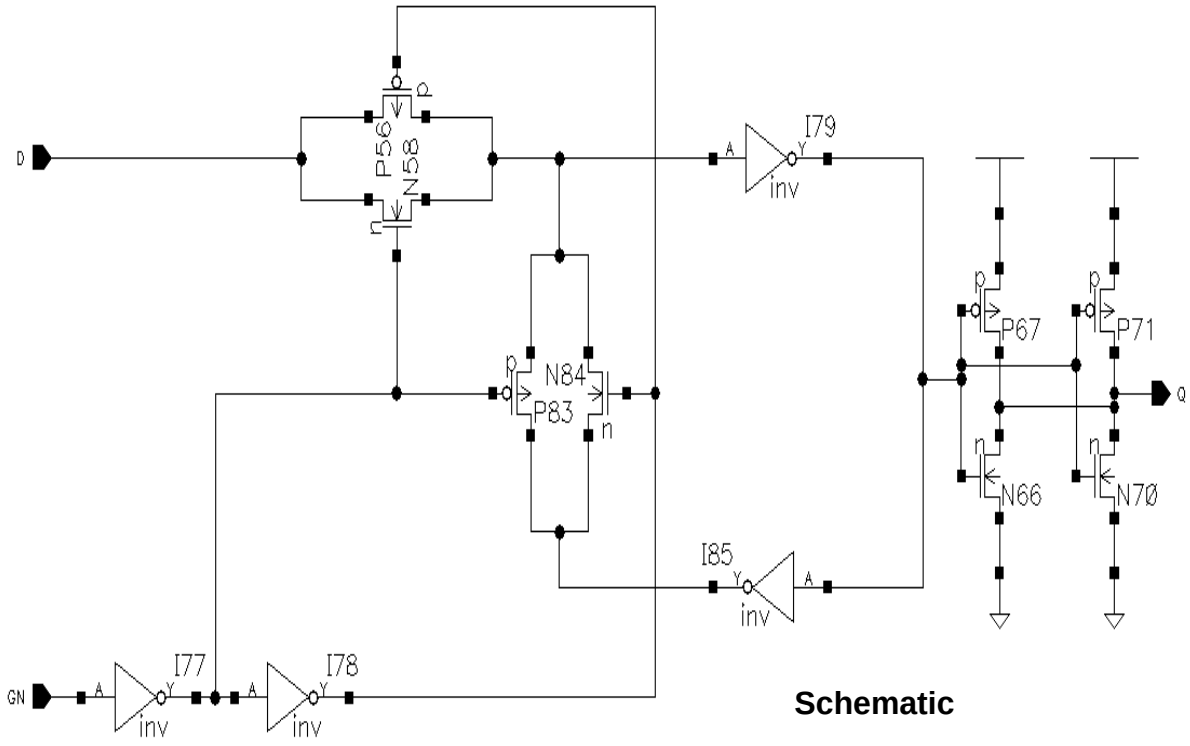
Gate Count:
- LD5D2Q: 4
- LD5D24Q: 5



Symbol

D	GN	Qn+1
0	0	0
1	0	1
X	1	Qn

Truth Table



Schematic

LD5D2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.21	0.16 + 0.022*SL	0.17 + 0.019*SL	0.18 + 0.019*SL
	tPHL	0.39	0.36 + 0.016*SL	0.38 + 0.011*SL	0.42 + 0.009*SL
	tR	0.18	0.10 + 0.043*SL	0.10 + 0.044*SL	0.07 + 0.045*SL
	tF	0.15	0.13 + 0.013*SL	0.12 + 0.016*SL	0.11 + 0.016*SL
GN to Q	tPLH	0.53	0.49 + 0.021*SL	0.50 + 0.019*SL	0.50 + 0.019*SL
	tPHL	0.53	0.49 + 0.016*SL	0.51 + 0.010*SL	0.55 + 0.008*SL
	tR	0.16	0.08 + 0.043*SL	0.07 + 0.044*SL	0.05 + 0.046*SL
	tF	0.13	0.09 + 0.017*SL	0.09 + 0.017*SL	0.09 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

LD5D2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.000
Input Hold Time (D to GN)	tHD	0.000
Input Setup Time (D to GN)	tSU	0.000

LD5D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.26	0.23 + 0.012*SL	0.24 + 0.010*SL	0.25 + 0.009*SL
	tPHL	0.45	0.43 + 0.011*SL	0.44 + 0.007*SL	0.47 + 0.005*SL
	tR	0.16	0.11 + 0.022*SL	0.11 + 0.021*SL	0.09 + 0.022*SL
	tF	0.17	0.15 + 0.010*SL	0.15 + 0.008*SL	0.16 + 0.008*SL
GN to Q	tPLH	0.55	0.53 + 0.011*SL	0.53 + 0.010*SL	0.55 + 0.009*SL
	tPHL	0.57	0.55 + 0.013*SL	0.57 + 0.007*SL	0.60 + 0.005*SL
	tR	0.14	0.09 + 0.021*SL	0.09 + 0.022*SL	0.08 + 0.022*SL
	tF	0.16	0.14 + 0.009*SL	0.14 + 0.008*SL	0.15 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

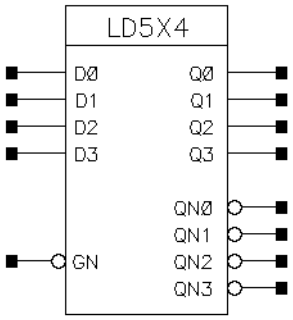
LD5D4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.000
Input Hold Time (D to GN)	tHD	0.000
Input Setup Time (D to GN)	tSU	0.000

Inputs: D0, D1, D2, D3, GN
Outputs: Q0, Q1, Q2, Q3
QN0, QN1, QN2, QN3
Input Loading (SL):
- D0, D1, D2, D3: 3
- GN: 1

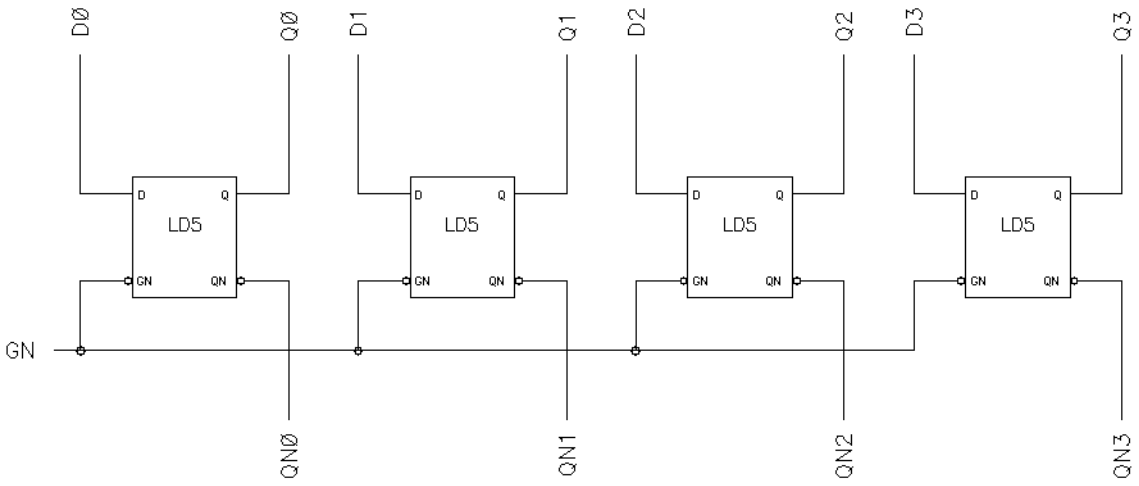
Maximum Fanout (Rec. SL): All : 28
Gate Count: 13



Symbol

D	GN	Qn+1	QNn+1
0	0	0	1
1	0	1	0
x	1	Qn	QNn

Truth Table



Schematic

LD5X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Q0	tPLH	0.21	0.13 + 0.039*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
	tPHL	0.38	0.33 + 0.025*SL	0.35 + 0.018*SL	0.38 + 0.017*SL
	tR	0.26	0.10 + 0.082*SL	0.08 + 0.087*SL	0.06 + 0.088*SL
	tF	0.16	0.09 + 0.035*SL	0.10 + 0.033*SL	0.07 + 0.034*SL
GN to Q0	tPLH	0.70	0.62 + 0.039*SL	0.62 + 0.038*SL	0.63 + 0.038*SL
	tPHL	0.61	0.56 + 0.024*SL	0.58 + 0.018*SL	0.60 + 0.017*SL
	tR	0.24	0.06 + 0.090*SL	0.07 + 0.088*SL	0.05 + 0.089*SL
	tF	0.14	0.06 + 0.036*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
D1 to Q1	tPLH	0.20	0.13 + 0.038*SL	0.13 + 0.036*SL	0.13 + 0.036*SL
	tPHL	0.38	0.33 + 0.024*SL	0.35 + 0.017*SL	0.38 + 0.016*SL
	tR	0.25	0.09 + 0.080*SL	0.08 + 0.083*SL	0.06 + 0.084*SL
	tF	0.16	0.09 + 0.034*SL	0.10 + 0.031*SL	0.06 + 0.032*SL
GN to Q1	tPLH	0.70	0.62 + 0.038*SL	0.62 + 0.037*SL	0.63 + 0.036*SL
	tPHL	0.60	0.56 + 0.024*SL	0.58 + 0.017*SL	0.60 + 0.016*SL
	tR	0.23	0.06 + 0.087*SL	0.07 + 0.084*SL	0.05 + 0.085*SL
	tF	0.13	0.06 + 0.034*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
D2 to Q2	tPLH	0.21	0.13 + 0.039*SL	0.14 + 0.038*SL	0.14 + 0.038*SL
	tPHL	0.38	0.33 + 0.025*SL	0.35 + 0.018*SL	0.38 + 0.016*SL
	tR	0.26	0.10 + 0.083*SL	0.08 + 0.087*SL	0.06 + 0.088*SL
	tF	0.16	0.09 + 0.035*SL	0.10 + 0.033*SL	0.07 + 0.034*SL
GN to Q2	tPLH	0.70	0.62 + 0.039*SL	0.62 + 0.038*SL	0.63 + 0.038*SL
	tPHL	0.61	0.56 + 0.024*SL	0.58 + 0.018*SL	0.60 + 0.017*SL
	tR	0.24	0.06 + 0.090*SL	0.07 + 0.088*SL	0.05 + 0.089*SL
	tF	0.14	0.06 + 0.036*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
D3 to Q3	tPLH	0.20	0.13 + 0.038*SL	0.13 + 0.036*SL	0.13 + 0.036*SL
	tPHL	0.38	0.33 + 0.024*SL	0.35 + 0.017*SL	0.38 + 0.016*SL
	tR	0.25	0.09 + 0.080*SL	0.08 + 0.083*SL	0.06 + 0.084*SL
	tF	0.16	0.09 + 0.035*SL	0.10 + 0.031*SL	0.06 + 0.032*SL
GN to Q3	tPLH	0.69	0.62 + 0.038*SL	0.62 + 0.037*SL	0.63 + 0.036*SL
	tPHL	0.60	0.56 + 0.024*SL	0.57 + 0.017*SL	0.60 + 0.016*SL
	tR	0.23	0.06 + 0.087*SL	0.07 + 0.084*SL	0.05 + 0.085*SL
	tF	0.13	0.06 + 0.034*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
D0 to QN0	tPLH	0.49	0.42 + 0.036*SL	0.41 + 0.037*SL	0.41 + 0.037*SL
	tPHL	0.25	0.20 + 0.023*SL	0.22 + 0.017*SL	0.23 + 0.016*SL
	tR	0.25	0.08 + 0.082*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	tF	0.14	0.07 + 0.032*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
GN to QN0	tPLH	0.72	0.64 + 0.038*SL	0.64 + 0.038*SL	0.64 + 0.037*SL
	tPHL	0.74	0.69 + 0.021*SL	0.71 + 0.017*SL	0.72 + 0.017*SL
	tR	0.24	0.07 + 0.086*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	tF	0.14	0.07 + 0.034*SL	0.07 + 0.033*SL	0.05 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD5X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D1 to QN1	t_{PLH}	0.49	0.42 + 0.034*SL	0.41 + 0.036*SL	0.41 + 0.036*SL
	t_{PHL}	0.24	0.20 + 0.022*SL	0.22 + 0.017*SL	0.23 + 0.016*SL
	t_R	0.24	0.08 + 0.078*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.13	0.07 + 0.031*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
GN to QN1	t_{PLH}	0.71	0.64 + 0.036*SL	0.64 + 0.036*SL	0.63 + 0.036*SL
	t_{PHL}	0.73	0.69 + 0.021*SL	0.71 + 0.017*SL	0.72 + 0.016*SL
	t_R	0.24	0.09 + 0.075*SL	0.06 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.13	0.07 + 0.033*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
D2 to QN2	t_{PLH}	0.49	0.42 + 0.036*SL	0.41 + 0.037*SL	0.42 + 0.037*SL
	t_{PHL}	0.25	0.20 + 0.023*SL	0.22 + 0.017*SL	0.23 + 0.016*SL
	t_R	0.25	0.08 + 0.083*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	t_F	0.14	0.07 + 0.032*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
GN to QN2	t_{PLH}	0.72	0.64 + 0.038*SL	0.64 + 0.038*SL	0.65 + 0.037*SL
	t_{PHL}	0.74	0.69 + 0.022*SL	0.71 + 0.017*SL	0.72 + 0.017*SL
	t_R	0.24	0.08 + 0.082*SL	0.06 + 0.086*SL	0.05 + 0.087*SL
	t_F	0.13	0.07 + 0.034*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
D3 to QN3	t_{PLH}	0.49	0.42 + 0.034*SL	0.41 + 0.036*SL	0.41 + 0.036*SL
	t_{PHL}	0.24	0.20 + 0.022*SL	0.22 + 0.017*SL	0.23 + 0.016*SL
	t_R	0.24	0.08 + 0.078*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.13	0.07 + 0.031*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
GN to QN3	t_{PLH}	0.71	0.64 + 0.036*SL	0.64 + 0.036*SL	0.63 + 0.036*SL
	t_{PHL}	0.73	0.69 + 0.021*SL	0.71 + 0.017*SL	0.72 + 0.016*SL
	t_R	0.24	0.08 + 0.078*SL	0.06 + 0.084*SL	0.05 + 0.084*SL
	t_F	0.13	0.07 + 0.033*SL	0.07 + 0.031*SL	0.04 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

LD5X4 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	t_{PWL}	0.000
Input Hold Time (D0 to GN)	t_{HD}	0.000
Input Hold Time (D1 to GN)	t_{HD}	0.000
Input Hold Time (D2 to GN)	t_{HD}	0.000
Input Hold Time (D3 to GN)	t_{HD}	0.000
Input Setup Time (D0 to GN)	t_{SU}	0.000

LD5X4 Timing Requirements

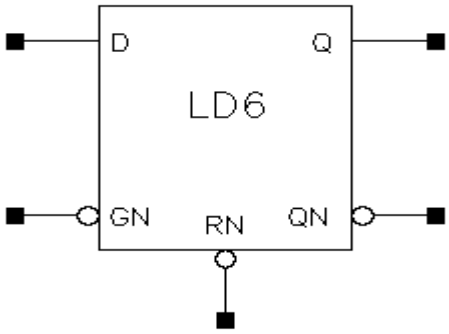
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Input Setup Time (D1 to GN)	t_{SU}	0.000
Input Setup Time (D2 to GN)	t_{SU}	0.000
Input Setup Time (D3 to GN)	t_{SU}	0.000

Inputs: D, GN, RN
Outputs: Q, QN
Input Loading (SL):
- D: 3
- GN, RN: 1

Maximum Fanout (Rec. SL):
- LD6: All: 28
- LD6D2: All: 56

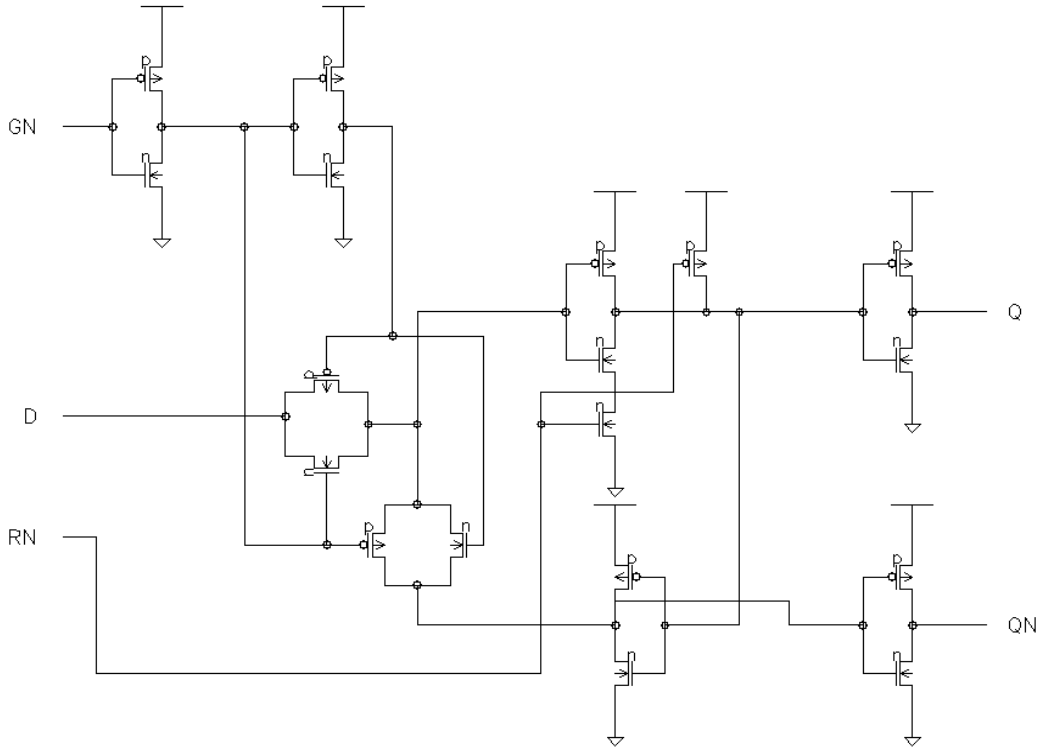
Gate Count:
- LD6: 5
- LD6D2: 6



Symbol

D	GN	RN	Qn+1	QNn+1
0	0	1	0	1
1	0	1	1	0
x	1	1	Qn	QNn
x	x	0	0	1

Truth Table



Schematic

LD6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.23	0.14 + 0.042*SL	0.16 + 0.037*SL	0.17 + 0.036*SL
	tPHL	0.39	0.33 + 0.028*SL	0.36 + 0.018*SL	0.40 + 0.016*SL
	tR	0.27	0.11 + 0.081*SL	0.10 + 0.082*SL	0.07 + 0.084*SL
	tF	0.18	0.12 + 0.032*SL	0.12 + 0.030*SL	0.08 + 0.032*SL
D to Q	tPLH	0.30	0.21 + 0.041*SL	0.23 + 0.037*SL	0.23 + 0.036*SL
	tPHL	0.37	0.32 + 0.025*SL	0.34 + 0.018*SL	0.38 + 0.016*SL
	tR	0.27	0.11 + 0.081*SL	0.10 + 0.083*SL	0.07 + 0.084*SL
	tF	0.17	0.10 + 0.033*SL	0.11 + 0.031*SL	0.07 + 0.032*SL
GN to Q	tPLH	0.60	0.51 + 0.041*SL	0.53 + 0.037*SL	0.53 + 0.036*SL
	tPHL	0.53	0.48 + 0.025*SL	0.50 + 0.017*SL	0.53 + 0.016*SL
	tR	0.25	0.08 + 0.083*SL	0.08 + 0.083*SL	0.06 + 0.084*SL
	tF	0.14	0.07 + 0.035*SL	0.08 + 0.032*SL	0.06 + 0.033*SL
RN to QN	tPLH	0.50	0.43 + 0.035*SL	0.43 + 0.036*SL	0.43 + 0.036*SL
	tPHL	0.27	0.23 + 0.022*SL	0.24 + 0.017*SL	0.25 + 0.016*SL
	tR	0.24	0.08 + 0.078*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.07 + 0.033*SL	0.08 + 0.031*SL	0.05 + 0.033*SL
D to QN	tPLH	0.48	0.42 + 0.034*SL	0.41 + 0.036*SL	0.41 + 0.036*SL
	tPHL	0.34	0.29 + 0.023*SL	0.31 + 0.017*SL	0.32 + 0.016*SL
	tR	0.24	0.07 + 0.080*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.07 + 0.037*SL	0.09 + 0.031*SL	0.04 + 0.033*SL
GN to QN	tPLH	0.64	0.57 + 0.036*SL	0.57 + 0.036*SL	0.57 + 0.036*SL
	tPHL	0.64	0.60 + 0.022*SL	0.61 + 0.017*SL	0.62 + 0.016*SL
	tR	0.23	0.06 + 0.085*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.06 + 0.038*SL	0.08 + 0.031*SL	0.04 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

LD6 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.000
Pulse Width Low (RN)	tPWL	0.000
Input Hold Time (D to GN)	tHD	0.000
Input Setup Time (D to GN)	tSU	0.000
Recovery Time (RN)	tRC	0.000

LD6D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

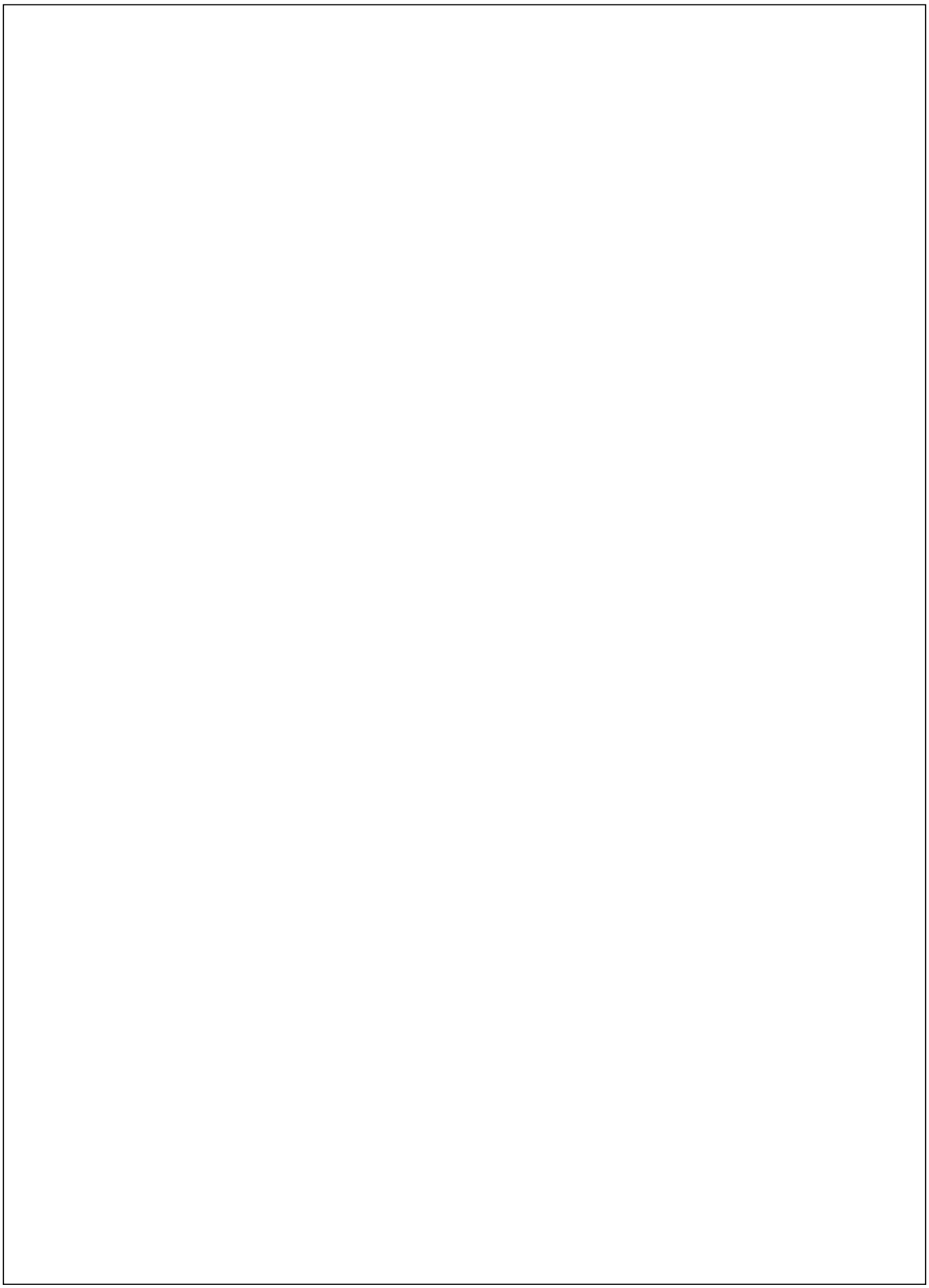
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.23	0.18 + 0.022*SL	0.19 + 0.019*SL	0.21 + 0.018*SL
	tPHL	0.39	0.36 + 0.016*SL	0.38 + 0.011*SL	0.43 + 0.008*SL
	tR	0.19	0.11 + 0.041*SL	0.11 + 0.041*SL	0.09 + 0.042*SL
	tF	0.16	0.14 + 0.013*SL	0.13 + 0.015*SL	0.13 + 0.016*SL
D to Q	tPLH	0.30	0.26 + 0.021*SL	0.27 + 0.019*SL	0.28 + 0.018*SL
	tPHL	0.38	0.35 + 0.015*SL	0.37 + 0.011*SL	0.41 + 0.008*SL
	tR	0.20	0.11 + 0.046*SL	0.12 + 0.041*SL	0.09 + 0.042*SL
	tF	0.15	0.13 + 0.012*SL	0.12 + 0.015*SL	0.12 + 0.016*SL
GN to Q	tPLH	0.59	0.54 + 0.022*SL	0.55 + 0.019*SL	0.57 + 0.018*SL
	tPHL	0.54	0.51 + 0.015*SL	0.52 + 0.010*SL	0.56 + 0.008*SL
	tR	0.18	0.09 + 0.043*SL	0.10 + 0.041*SL	0.08 + 0.043*SL
	tF	0.12	0.09 + 0.018*SL	0.09 + 0.016*SL	0.09 + 0.016*SL
RN to QN	tPLH	0.54	0.50 + 0.016*SL	0.50 + 0.018*SL	0.49 + 0.018*SL
	tPHL	0.32	0.30 + 0.013*SL	0.31 + 0.010*SL	0.34 + 0.008*SL
	tR	0.16	0.08 + 0.038*SL	0.07 + 0.041*SL	0.05 + 0.042*SL
	tF	0.12	0.10 + 0.012*SL	0.08 + 0.016*SL	0.09 + 0.016*SL
D to QN	tPLH	0.52	0.49 + 0.016*SL	0.49 + 0.018*SL	0.48 + 0.018*SL
	tPHL	0.40	0.38 + 0.010*SL	0.39 + 0.010*SL	0.41 + 0.008*SL
	tR	0.16	0.09 + 0.039*SL	0.08 + 0.041*SL	0.06 + 0.042*SL
	tF	0.13	0.09 + 0.018*SL	0.10 + 0.015*SL	0.08 + 0.016*SL
GN to QN	tPLH	0.67	0.63 + 0.017*SL	0.63 + 0.018*SL	0.63 + 0.018*SL
	tPHL	0.69	0.66 + 0.015*SL	0.68 + 0.009*SL	0.70 + 0.008*SL
	tR	0.16	0.09 + 0.038*SL	0.08 + 0.041*SL	0.05 + 0.043*SL
	tF	0.13	0.09 + 0.022*SL	0.11 + 0.015*SL	0.09 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

LD6D2 Timing Requirements

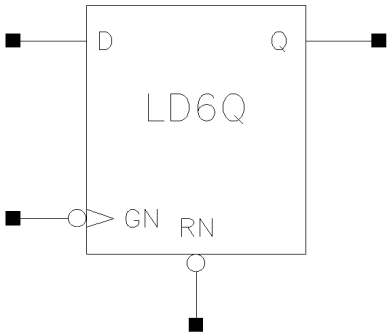
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.000
Pulse Width Low (RN)	tPWL	0.000
Input Hold Time (D to GN)	tHD	0.000
Input Setup Time (D to GN)	tSU	0.000
Recovery Time (RN)	tRC	0.000



Inputs: D, GN, RN
Outputs: Q,
Input Loading (SL): All : D: 3, GN, RN: 1
Maximum Fanout (Rec. SL):
- LD6Q: 28
- LD6D3Q: 84

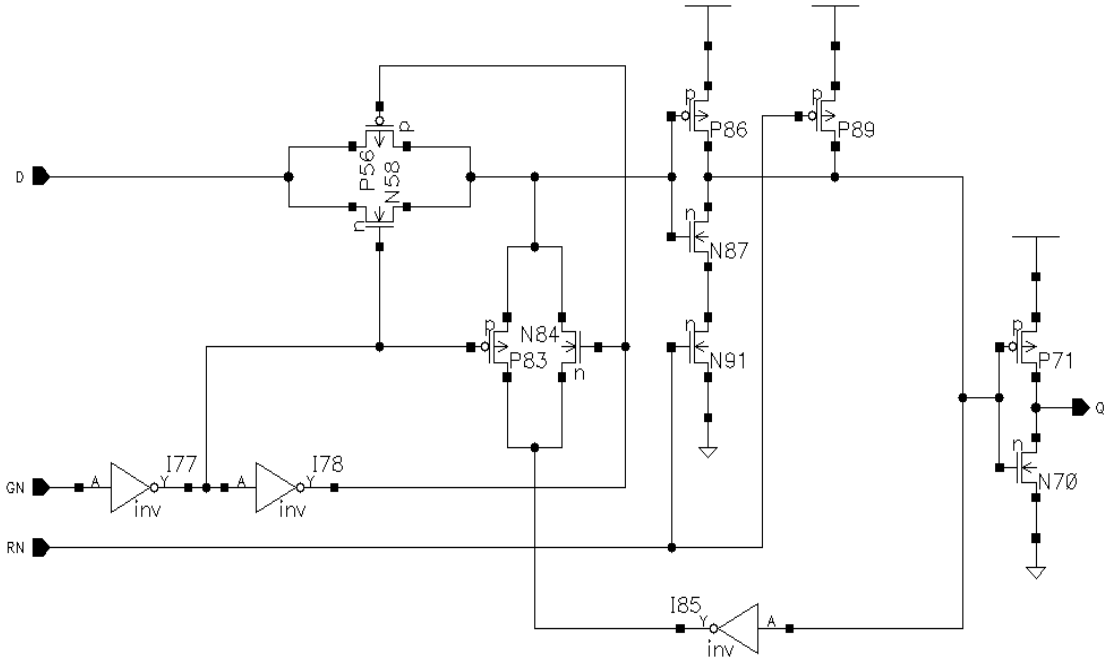
Gate Count:
- LD6Q: 4
- LD6D3Q: 5



Symbol

D	GN	RN	Qn+1
0	0	1	0
1	0	1	1
x	1	1	Qn
x	x	0	0

Truth Table



Schematic

LD6Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	t_{PLH}	0.24	0.15 + 0.043*SL	0.17 + 0.038*SL	0.17 + 0.038*SL
	t_{PHL}	0.40	0.34 + 0.029*SL	0.37 + 0.018*SL	0.40 + 0.016*SL
	t_R	0.28	0.11 + 0.083*SL	0.10 + 0.086*SL	0.06 + 0.088*SL
	t_F	0.19	0.12 + 0.035*SL	0.13 + 0.031*SL	0.07 + 0.034*SL
D to Q	t_{PLH}	0.31	0.22 + 0.043*SL	0.23 + 0.038*SL	0.24 + 0.038*SL
	t_{PHL}	0.38	0.32 + 0.028*SL	0.35 + 0.018*SL	0.38 + 0.016*SL
	t_R	0.28	0.10 + 0.087*SL	0.11 + 0.086*SL	0.07 + 0.088*SL
	t_F	0.17	0.11 + 0.033*SL	0.11 + 0.031*SL	0.06 + 0.034*SL
GN to Q	t_{PLH}	0.60	0.52 + 0.043*SL	0.53 + 0.038*SL	0.54 + 0.038*SL
	t_{PHL}	0.53	0.48 + 0.026*SL	0.50 + 0.018*SL	0.53 + 0.016*SL
	t_R	0.26	0.10 + 0.083*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
	t_F	0.14	0.07 + 0.036*SL	0.08 + 0.033*SL	0.05 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD6Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	t_{PWL}	0.000
Pulse Width Low (RN)	t_{PWL}	0.000
Input Hold Time (D to GN)	t_{HD}	0.000
Input Setup Time (D to GN)	t_{SU}	0.000
Recovery Time (RN)	t_{RC}	0.000

LD6D3Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

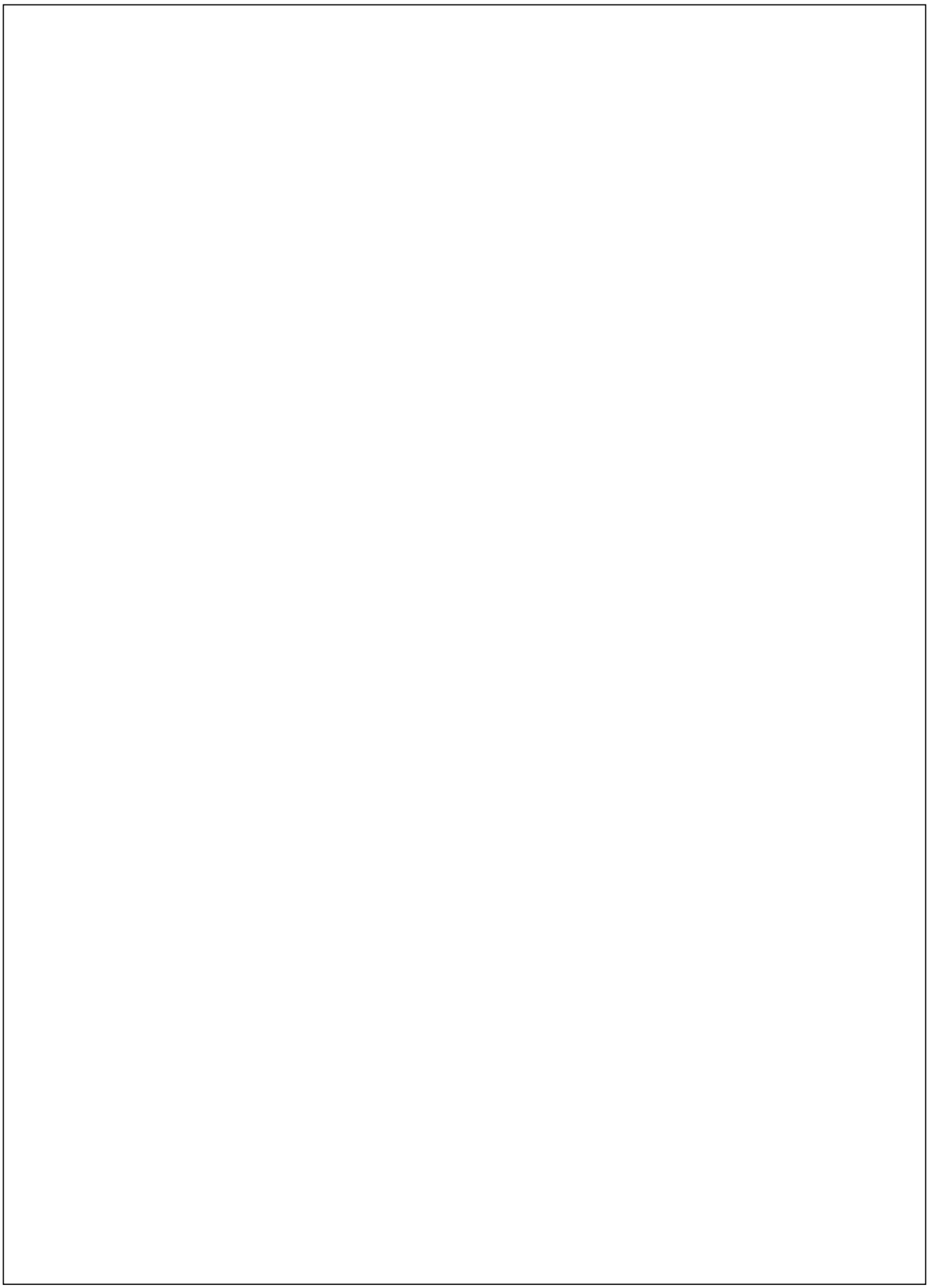
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.25	0.22 + 0.016*SL	0.23 + 0.014*SL	0.25 + 0.013*SL
	tPHL	0.42	0.39 + 0.016*SL	0.41 + 0.009*SL	0.46 + 0.006*SL
	tR	0.18	0.13 + 0.028*SL	0.12 + 0.029*SL	0.11 + 0.029*SL
	tF	0.17	0.14 + 0.016*SL	0.16 + 0.010*SL	0.15 + 0.010*SL
D to Q	tPLH	0.34	0.30 + 0.017*SL	0.31 + 0.013*SL	0.33 + 0.013*SL
	tPHL	0.42	0.39 + 0.013*SL	0.41 + 0.008*SL	0.44 + 0.006*SL
	tR	0.18	0.12 + 0.030*SL	0.13 + 0.028*SL	0.11 + 0.029*SL
	tF	0.17	0.15 + 0.010*SL	0.15 + 0.010*SL	0.15 + 0.010*SL
GN to Q	tPLH	0.61	0.58 + 0.016*SL	0.59 + 0.014*SL	0.61 + 0.013*SL
	tPHL	0.56	0.53 + 0.012*SL	0.55 + 0.008*SL	0.58 + 0.006*SL
	tR	0.17	0.12 + 0.027*SL	0.11 + 0.029*SL	0.10 + 0.029*SL
	tF	0.13	0.11 + 0.013*SL	0.11 + 0.012*SL	0.13 + 0.011*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

LD6D3Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

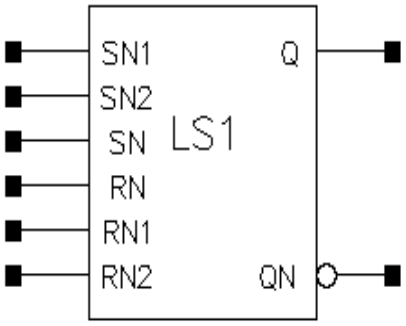
Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.000
Pulse Width Low (RN)	tPWL	0.000
Input Hold Time (D to GN)	tHD	0.000
Input Setup Time (D to GN)	tSU	0.000
Recovery Time (RN)	tRC	0.000



Inputs: SN1, SN2, SN, RN, RN1, RN2
Outputs: Q, QN
Input Loading (SL):
- LS1: All: 1
- LS1D3: All: 1

Maximum Fanout (Rec. SL):
- LS1: 14
- LS1D3: 84

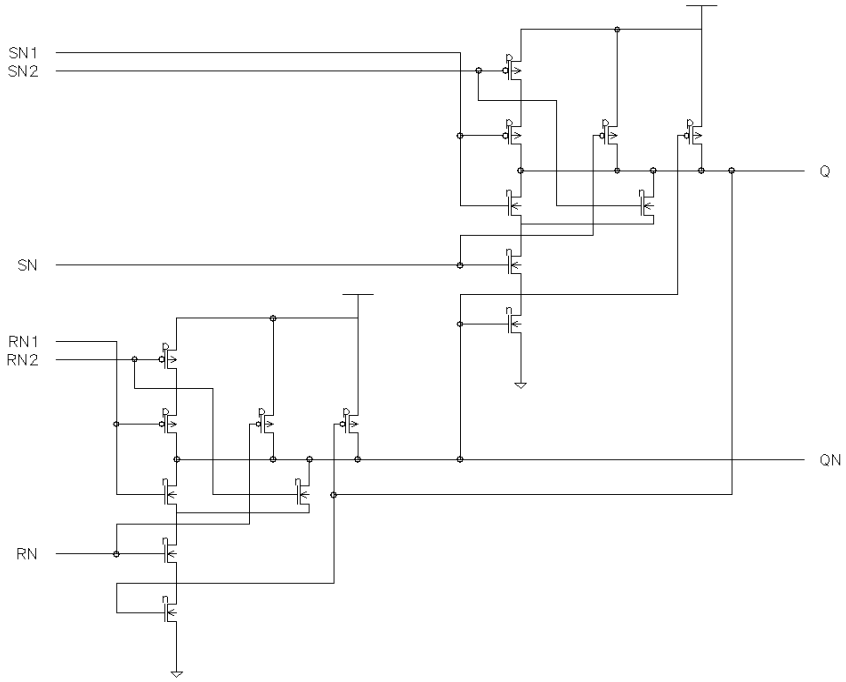
Gate Count:
- LS1: 4
- LS1D3:



Symbol

SN1/SN2	RN1/RN2	SN	RN	Qn+1	QNn+1
x	1	0	1	1	0
1	x	1	0	0	1
x	x	0	0	1	1
1	1	1	1	Qn	QNn
1	0	1	1	0	1
0	1	1	1	1	0
0	0	1	1	1	1

Truth Table



Schematic

LS1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	t_{PHL}	0.58	0.43 + 0.076*SL	0.45 + 0.070*SL	0.45 + 0.070*SL
	t_F	0.42	0.26 + 0.078*SL	0.26 + 0.079*SL	0.23 + 0.080*SL
RN1 to Q	t_{PHL}	0.67	0.46 + 0.105*SL	0.47 + 0.102*SL	0.46 + 0.102*SL
	t_F	0.44	0.27 + 0.084*SL	0.26 + 0.089*SL	0.24 + 0.090*SL
RN2 to Q	t_{PHL}	0.63	0.43 + 0.102*SL	0.43 + 0.102*SL	0.43 + 0.102*SL
	t_F	0.44	0.27 + 0.084*SL	0.26 + 0.089*SL	0.24 + 0.090*SL
SN to Q	t_{PLH}	0.41	0.33 + 0.040*SL	0.34 + 0.037*SL	0.34 + 0.037*SL
	t_{PHL}	0.21	0.13 + 0.041*SL	0.16 + 0.032*SL	0.19 + 0.030*SL
	t_R	0.58	0.44 + 0.070*SL	0.40 + 0.083*SL	0.31 + 0.087*SL
	t_F	0.52	0.40 + 0.060*SL	0.38 + 0.067*SL	0.29 + 0.071*SL
SN1 to Q	t_{PLH}	0.50	0.35 + 0.072*SL	0.36 + 0.070*SL	0.34 + 0.070*SL
	t_{PHL}	0.23	0.13 + 0.052*SL	0.17 + 0.039*SL	0.20 + 0.037*SL
	t_R	0.79	0.49 + 0.146*SL	0.45 + 0.161*SL	0.37 + 0.165*SL
	t_F	0.55	0.39 + 0.081*SL	0.39 + 0.081*SL	0.29 + 0.086*SL
SN2 to Q	t_{PLH}	0.46	0.32 + 0.070*SL	0.32 + 0.070*SL	0.31 + 0.070*SL
	t_{PHL}	0.26	0.17 + 0.049*SL	0.20 + 0.038*SL	0.23 + 0.037*SL
	t_R	0.78	0.48 + 0.148*SL	0.44 + 0.162*SL	0.37 + 0.165*SL
	t_F	0.61	0.46 + 0.077*SL	0.45 + 0.080*SL	0.33 + 0.086*SL
RN to QN	t_{PLH}	0.41	0.33 + 0.041*SL	0.34 + 0.037*SL	0.33 + 0.037*SL
	t_{PHL}	0.21	0.13 + 0.041*SL	0.15 + 0.032*SL	0.19 + 0.030*SL
	t_R	0.57	0.43 + 0.071*SL	0.40 + 0.082*SL	0.30 + 0.087*SL
	t_F	0.52	0.40 + 0.060*SL	0.38 + 0.067*SL	0.29 + 0.071*SL
RN1 to QN	t_{PLH}	0.49	0.35 + 0.072*SL	0.36 + 0.070*SL	0.34 + 0.070*SL
	t_{PHL}	0.23	0.12 + 0.053*SL	0.17 + 0.039*SL	0.20 + 0.037*SL
	t_R	0.78	0.49 + 0.146*SL	0.44 + 0.161*SL	0.36 + 0.165*SL
	t_F	0.55	0.39 + 0.081*SL	0.39 + 0.081*SL	0.29 + 0.086*SL
RN2 to QN	t_{PLH}	0.46	0.31 + 0.070*SL	0.32 + 0.070*SL	0.31 + 0.070*SL
	t_{PHL}	0.26	0.16 + 0.049*SL	0.20 + 0.038*SL	0.22 + 0.037*SL
	t_R	0.77	0.48 + 0.148*SL	0.43 + 0.162*SL	0.36 + 0.165*SL
	t_F	0.61	0.45 + 0.076*SL	0.44 + 0.080*SL	0.33 + 0.086*SL
SN to QN	t_{PHL}	0.58	0.43 + 0.076*SL	0.45 + 0.070*SL	0.45 + 0.070*SL
	t_F	0.41	0.26 + 0.078*SL	0.26 + 0.079*SL	0.23 + 0.080*SL
SN1 to QN	t_{PHL}	0.67	0.46 + 0.105*SL	0.47 + 0.102*SL	0.46 + 0.102*SL
	t_F	0.44	0.27 + 0.087*SL	0.26 + 0.089*SL	0.24 + 0.090*SL
SN2 to QN	t_{PHL}	0.64	0.43 + 0.102*SL	0.43 + 0.102*SL	0.43 + 0.102*SL
	t_F	0.44	0.27 + 0.084*SL	0.26 + 0.089*SL	0.24 + 0.090*SL

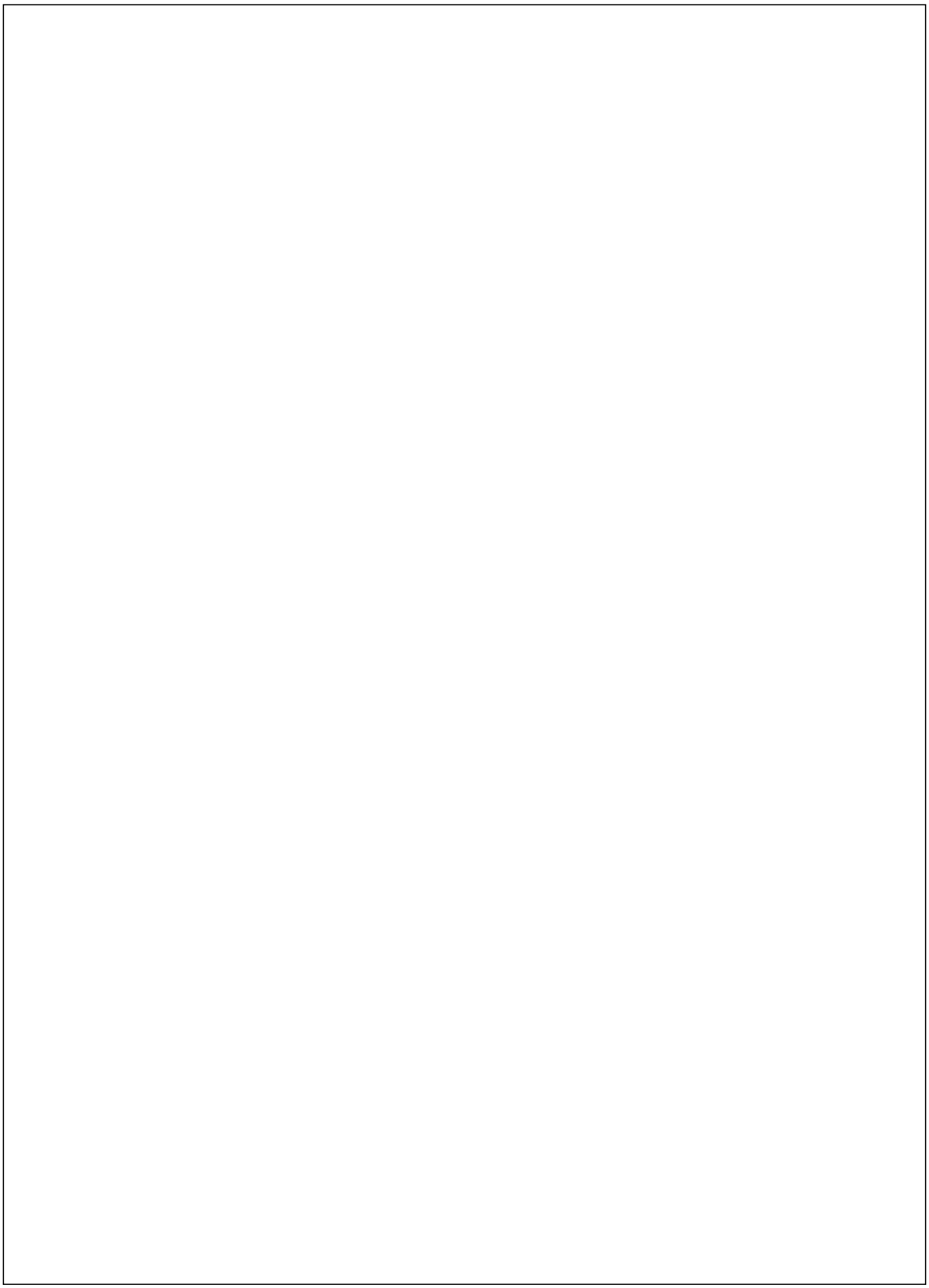
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

LS1D3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	t_{PHL}	0.74	0.71 + 0.011*SL	0.72 + 0.007*SL	0.76 + 0.006*SL
	t_F	0.12	0.10 + 0.012*SL	0.10 + 0.011*SL	0.09 + 0.011*SL
RN1 to Q	t_{PHL}	0.79	0.76 + 0.011*SL	0.77 + 0.008*SL	0.81 + 0.006*SL
	t_F	0.13	0.10 + 0.013*SL	0.11 + 0.011*SL	0.10 + 0.011*SL
RN2 to Q	t_{PHL}	0.76	0.74 + 0.010*SL	0.74 + 0.007*SL	0.77 + 0.006*SL
	t_F	0.13	0.10 + 0.013*SL	0.11 + 0.010*SL	0.10 + 0.011*SL
SN to Q	t_{PLH}	0.52	0.49 + 0.014*SL	0.50 + 0.013*SL	0.50 + 0.013*SL
	t_{PHL}	0.41	0.39 + 0.010*SL	0.40 + 0.007*SL	0.43 + 0.006*SL
	t_R	0.15	0.09 + 0.029*SL	0.09 + 0.028*SL	0.06 + 0.030*SL
	t_F	0.13	0.10 + 0.013*SL	0.11 + 0.011*SL	0.11 + 0.011*SL
SN1 to Q	t_{PLH}	0.58	0.55 + 0.014*SL	0.56 + 0.013*SL	0.56 + 0.013*SL
	t_{PHL}	0.41	0.39 + 0.011*SL	0.40 + 0.007*SL	0.43 + 0.006*SL
	t_R	0.14	0.08 + 0.031*SL	0.09 + 0.029*SL	0.07 + 0.030*SL
	t_F	0.13	0.10 + 0.013*SL	0.11 + 0.011*SL	0.11 + 0.011*SL
SN2 to Q	t_{PLH}	0.55	0.52 + 0.014*SL	0.52 + 0.013*SL	0.53 + 0.012*SL
	t_{PHL}	0.47	0.45 + 0.009*SL	0.45 + 0.007*SL	0.48 + 0.006*SL
	t_R	0.16	0.10 + 0.027*SL	0.10 + 0.028*SL	0.06 + 0.030*SL
	t_F	0.14	0.12 + 0.010*SL	0.11 + 0.011*SL	0.10 + 0.011*SL
RN to QN	t_{PLH}	0.52	0.49 + 0.014*SL	0.50 + 0.013*SL	0.50 + 0.013*SL
	t_{PHL}	0.41	0.39 + 0.011*SL	0.40 + 0.007*SL	0.43 + 0.006*SL
	t_R	0.15	0.09 + 0.028*SL	0.09 + 0.028*SL	0.06 + 0.030*SL
	t_F	0.13	0.11 + 0.011*SL	0.11 + 0.011*SL	0.11 + 0.011*SL
RN1 to QN	t_{PLH}	0.58	0.55 + 0.014*SL	0.55 + 0.013*SL	0.56 + 0.013*SL
	t_{PHL}	0.41	0.39 + 0.011*SL	0.40 + 0.007*SL	0.43 + 0.006*SL
	t_R	0.15	0.09 + 0.027*SL	0.09 + 0.029*SL	0.07 + 0.030*SL
	t_F	0.13	0.10 + 0.014*SL	0.11 + 0.011*SL	0.11 + 0.011*SL
RN2 to QN	t_{PLH}	0.55	0.52 + 0.014*SL	0.52 + 0.013*SL	0.52 + 0.012*SL
	t_{PHL}	0.47	0.45 + 0.009*SL	0.45 + 0.007*SL	0.48 + 0.006*SL
	t_R	0.16	0.11 + 0.026*SL	0.10 + 0.028*SL	0.06 + 0.030*SL
	t_F	0.14	0.12 + 0.010*SL	0.12 + 0.010*SL	0.10 + 0.011*SL
SN to QN	t_{PHL}	0.73	0.71 + 0.011*SL	0.72 + 0.007*SL	0.75 + 0.006*SL
	t_F	0.13	0.10 + 0.014*SL	0.11 + 0.010*SL	0.09 + 0.011*SL
SN1 to QN	t_{PHL}	0.79	0.76 + 0.012*SL	0.77 + 0.008*SL	0.82 + 0.006*SL
	t_F	0.13	0.10 + 0.011*SL	0.11 + 0.011*SL	0.10 + 0.011*SL
SN2 to QN	t_{PHL}	0.76	0.74 + 0.010*SL	0.74 + 0.007*SL	0.77 + 0.006*SL
	t_F	0.13	0.11 + 0.012*SL	0.11 + 0.011*SL	0.11 + 0.011*SL

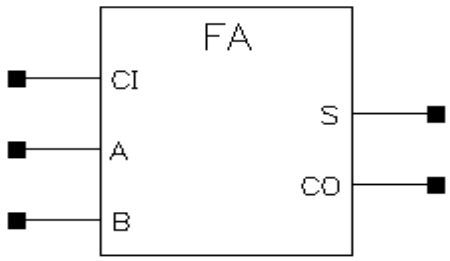
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL



Inputs: C1, A, B
Outputs: S, C0
Input Loading (SL):
- FA: CI: 2, B: 2, A: 1
- FAD2: CI: 2,, B: 2, A: 1
- FAD4: CI: 2, B: 2, A: 1
- FAD6:CI: 2, B: 2, A: 1

Maximum Fanout (Rec. SL):
- FA: 14
- FAD2: 56
- FAD4: 112
- FAD6: 168

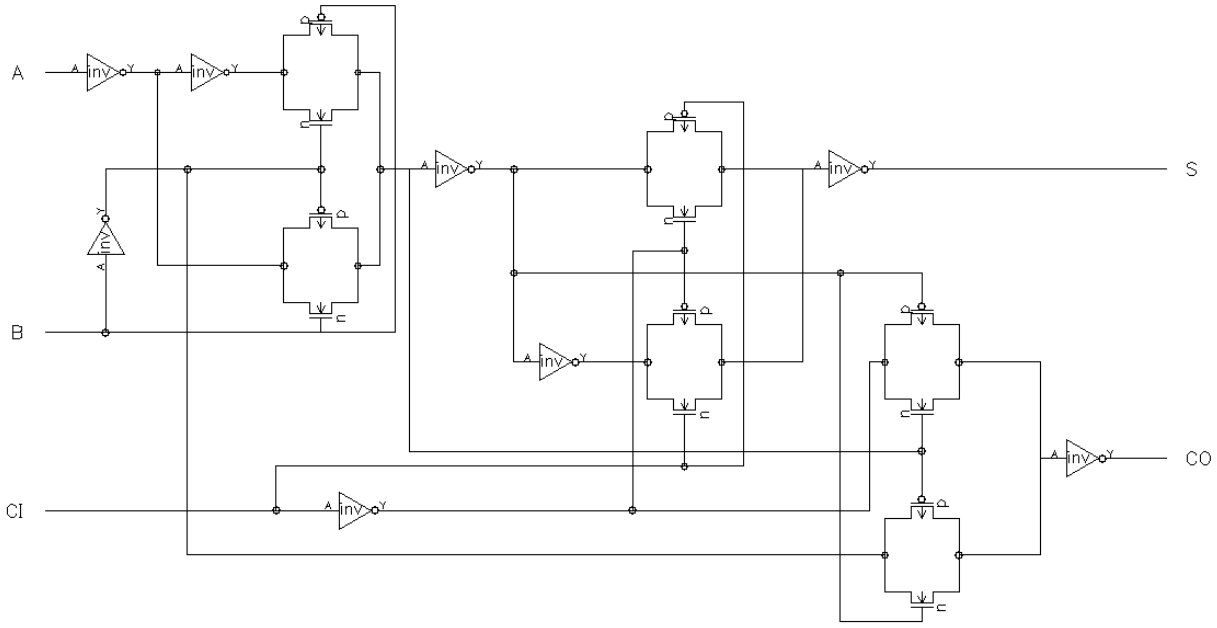
Gate Count:
- FA: 7
- FAD2: 8
- FAD4: 10
- FAD6: 12



Symbol

A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table



Schematic

FA Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	t_{PLH}	0.58	0.49 + 0.041*SL	0.50 + 0.037*SL	0.50 + 0.038*SL
	t_{PHL}	0.73	0.67 + 0.030*SL	0.70 + 0.020*SL	0.76 + 0.017*SL
	t_R	0.27	0.11 + 0.082*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
	t_F	0.19	0.12 + 0.038*SL	0.13 + 0.033*SL	0.11 + 0.034*SL
B to CO	t_{PLH}	0.50	0.42 + 0.040*SL	0.42 + 0.037*SL	0.42 + 0.038*SL
	t_{PHL}	0.48	0.38 + 0.047*SL	0.46 + 0.021*SL	0.53 + 0.017*SL
	t_R	0.27	0.10 + 0.085*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
	t_F	0.27	0.19 + 0.041*SL	0.22 + 0.030*SL	0.16 + 0.033*SL
CI to CO	t_{PLH}	0.28	0.20 + 0.042*SL	0.21 + 0.038*SL	0.22 + 0.038*SL
	t_{PHL}	0.45	0.39 + 0.031*SL	0.42 + 0.021*SL	0.50 + 0.017*SL
	t_R	0.28	0.11 + 0.083*SL	0.10 + 0.087*SL	0.07 + 0.088*SL
	t_F	0.21	0.12 + 0.045*SL	0.15 + 0.033*SL	0.14 + 0.034*SL
A to S	t_{PLH}	0.57	0.48 + 0.042*SL	0.50 + 0.037*SL	0.50 + 0.037*SL
	t_{PHL}	0.74	0.69 + 0.028*SL	0.71 + 0.019*SL	0.77 + 0.016*SL
	t_R	0.26	0.10 + 0.078*SL	0.08 + 0.085*SL	0.05 + 0.087*SL
	t_F	0.17	0.10 + 0.037*SL	0.12 + 0.031*SL	0.10 + 0.032*SL
B to S	t_{PLH}	0.48	0.40 + 0.041*SL	0.41 + 0.037*SL	0.41 + 0.037*SL
	t_{PHL}	0.68	0.62 + 0.029*SL	0.66 + 0.018*SL	0.70 + 0.016*SL
	t_R	0.26	0.09 + 0.083*SL	0.08 + 0.085*SL	0.05 + 0.087*SL
	t_F	0.18	0.10 + 0.037*SL	0.12 + 0.031*SL	0.10 + 0.032*SL
CI to S	t_{PLH}	0.20	0.12 + 0.041*SL	0.13 + 0.037*SL	0.13 + 0.037*SL
	t_{PHL}	0.38	0.32 + 0.028*SL	0.35 + 0.019*SL	0.40 + 0.016*SL
	t_R	0.27	0.11 + 0.079*SL	0.10 + 0.085*SL	0.06 + 0.086*SL
	t_F	0.18	0.10 + 0.039*SL	0.13 + 0.031*SL	0.10 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FAD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	0.59	0.55 + 0.022*SL	0.56 + 0.019*SL	0.56 + 0.019*SL
	tPHL	0.73	0.70 + 0.019*SL	0.72 + 0.013*SL	0.78 + 0.009*SL
	tR	0.20	0.12 + 0.038*SL	0.10 + 0.044*SL	0.08 + 0.045*SL
	tF	0.18	0.13 + 0.022*SL	0.15 + 0.017*SL	0.16 + 0.017*SL
B to CO	tPLH	0.51	0.47 + 0.021*SL	0.48 + 0.019*SL	0.48 + 0.019*SL
	tPHL	0.51	0.46 + 0.026*SL	0.50 + 0.013*SL	0.57 + 0.009*SL
	tR	0.20	0.10 + 0.047*SL	0.12 + 0.043*SL	0.08 + 0.045*SL
	tF	0.28	0.24 + 0.018*SL	0.25 + 0.015*SL	0.26 + 0.015*SL
CI to CO	tPLH	0.28	0.24 + 0.020*SL	0.24 + 0.020*SL	0.26 + 0.019*SL
	tPHL	0.46	0.42 + 0.019*SL	0.44 + 0.013*SL	0.51 + 0.010*SL
	tR	0.20	0.12 + 0.038*SL	0.11 + 0.044*SL	0.09 + 0.045*SL
	tF	0.18	0.14 + 0.021*SL	0.15 + 0.018*SL	0.17 + 0.017*SL
A to S	tPLH	0.55	0.51 + 0.020*SL	0.52 + 0.019*SL	0.53 + 0.018*SL
	tPHL	0.75	0.71 + 0.020*SL	0.73 + 0.012*SL	0.79 + 0.009*SL
	tR	0.18	0.10 + 0.042*SL	0.10 + 0.041*SL	0.07 + 0.042*SL
	tF	0.15	0.10 + 0.024*SL	0.13 + 0.016*SL	0.15 + 0.015*SL
B to S	tPLH	0.47	0.42 + 0.022*SL	0.43 + 0.019*SL	0.44 + 0.018*SL
	tPHL	0.68	0.65 + 0.018*SL	0.67 + 0.012*SL	0.72 + 0.009*SL
	tR	0.18	0.10 + 0.039*SL	0.09 + 0.041*SL	0.07 + 0.042*SL
	tF	0.15	0.11 + 0.024*SL	0.13 + 0.016*SL	0.14 + 0.016*SL
CI to S	tPLH	0.21	0.17 + 0.021*SL	0.18 + 0.019*SL	0.19 + 0.018*SL
	tPHL	0.39	0.35 + 0.018*SL	0.37 + 0.012*SL	0.43 + 0.009*SL
	tR	0.20	0.13 + 0.032*SL	0.10 + 0.041*SL	0.09 + 0.042*SL
	tF	0.15	0.10 + 0.027*SL	0.13 + 0.017*SL	0.15 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FAD4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	0.68	0.67 + 0.010*SL	0.66 + 0.010*SL	0.68 + 0.009*SL
	tPHL	0.78	0.75 + 0.012*SL	0.76 + 0.009*SL	0.81 + 0.006*SL
	tR	0.19	0.14 + 0.022*SL	0.15 + 0.021*SL	0.12 + 0.022*SL
	tF	0.19	0.16 + 0.016*SL	0.18 + 0.010*SL	0.20 + 0.009*SL
B to CO	tPLH	0.61	0.59 + 0.008*SL	0.59 + 0.010*SL	0.60 + 0.009*SL
	tPHL	0.58	0.55 + 0.014*SL	0.57 + 0.009*SL	0.61 + 0.006*SL
	tR	0.19	0.17 + 0.011*SL	0.14 + 0.022*SL	0.14 + 0.022*SL
	tF	0.28	0.26 + 0.012*SL	0.27 + 0.008*SL	0.27 + 0.008*SL
CI to CO	tPLH	0.34	0.31 + 0.013*SL	0.32 + 0.010*SL	0.33 + 0.010*SL
	tPHL	0.51	0.49 + 0.014*SL	0.50 + 0.008*SL	0.55 + 0.006*SL
	tR	0.18	0.13 + 0.027*SL	0.15 + 0.021*SL	0.13 + 0.022*SL
	tF	0.20	0.18 + 0.010*SL	0.18 + 0.010*SL	0.20 + 0.009*SL
A to S	tPLH	0.60	0.57 + 0.013*SL	0.58 + 0.010*SL	0.60 + 0.010*SL
	tPHL	0.79	0.77 + 0.013*SL	0.78 + 0.008*SL	0.83 + 0.006*SL
	tR	0.16	0.13 + 0.017*SL	0.12 + 0.022*SL	0.11 + 0.022*SL
	tF	0.19	0.16 + 0.014*SL	0.17 + 0.010*SL	0.20 + 0.008*SL
B to S	tPLH	0.51	0.49 + 0.012*SL	0.49 + 0.010*SL	0.51 + 0.010*SL
	tPHL	0.74	0.71 + 0.012*SL	0.72 + 0.008*SL	0.77 + 0.006*SL
	tR	0.16	0.13 + 0.018*SL	0.12 + 0.022*SL	0.12 + 0.022*SL
	tF	0.19	0.16 + 0.015*SL	0.17 + 0.010*SL	0.20 + 0.008*SL
CI to S	tPLH	0.28	0.25 + 0.013*SL	0.26 + 0.010*SL	0.28 + 0.010*SL
	tPHL	0.42	0.40 + 0.013*SL	0.41 + 0.008*SL	0.45 + 0.006*SL
	tR	0.18	0.14 + 0.018*SL	0.13 + 0.022*SL	0.14 + 0.022*SL
	tF	0.17	0.14 + 0.012*SL	0.15 + 0.010*SL	0.17 + 0.009*SL

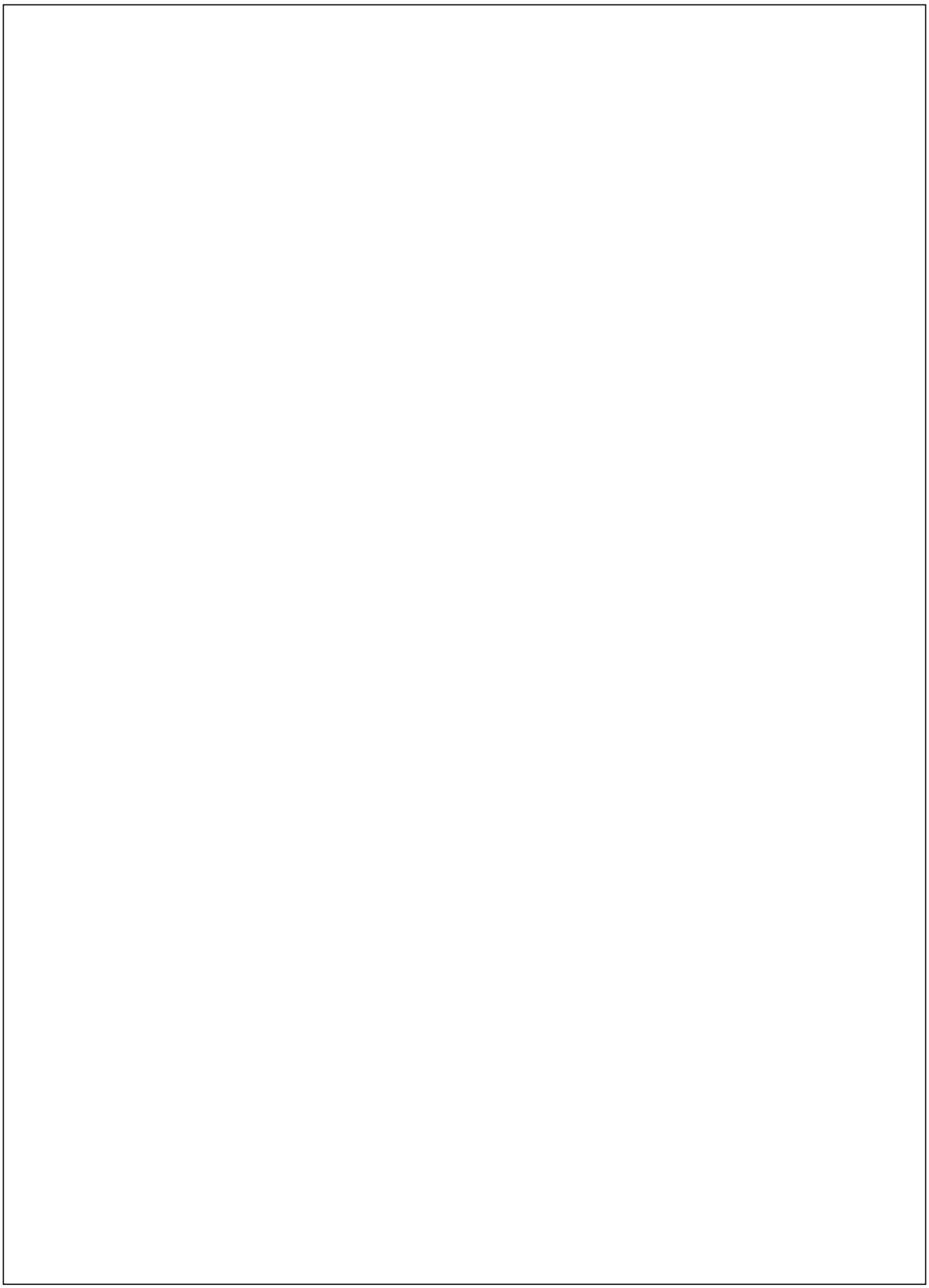
*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FAD6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	0.79	0.78 + 0.003*SL	0.77 + 0.007*SL	0.79 + 0.006*SL
	tPHL	0.82	0.80 + 0.009*SL	0.81 + 0.007*SL	0.84 + 0.005*SL
	tR	0.22	0.21 + 0.006*SL	0.18 + 0.014*SL	0.18 + 0.014*SL
	tF	0.23	0.19 + 0.019*SL	0.23 + 0.007*SL	0.23 + 0.006*SL
B to CO	tPLH	0.71	0.70 + 0.005*SL	0.70 + 0.007*SL	0.71 + 0.006*SL
	tPHL	0.62	0.60 + 0.011*SL	0.61 + 0.007*SL	0.65 + 0.005*SL
	tR	0.22	0.20 + 0.006*SL	0.18 + 0.014*SL	0.19 + 0.014*SL
	tF	0.29	0.28 + 0.006*SL	0.27 + 0.007*SL	0.30 + 0.006*SL
CI to CO	tPLH	0.39	0.37 + 0.010*SL	0.38 + 0.008*SL	0.40 + 0.007*SL
	tPHL	0.57	0.56 + 0.009*SL	0.56 + 0.007*SL	0.60 + 0.005*SL
	tR	0.20	0.17 + 0.014*SL	0.17 + 0.014*SL	0.15 + 0.014*SL
	tF	0.23	0.21 + 0.010*SL	0.22 + 0.007*SL	0.23 + 0.006*SL
A to S	tPLH	0.65	0.63 + 0.010*SL	0.64 + 0.007*SL	0.65 + 0.007*SL
	tPHL	0.86	0.84 + 0.007*SL	0.84 + 0.007*SL	0.88 + 0.005*SL
	tR	0.18	0.17 + 0.009*SL	0.15 + 0.014*SL	0.16 + 0.014*SL
	tF	0.22	0.19 + 0.016*SL	0.22 + 0.006*SL	0.21 + 0.006*SL
B to S	tPLH	0.57	0.55 + 0.009*SL	0.55 + 0.007*SL	0.57 + 0.007*SL
	tPHL	0.80	0.77 + 0.013*SL	0.79 + 0.007*SL	0.82 + 0.005*SL
	tR	0.18	0.15 + 0.013*SL	0.15 + 0.015*SL	0.16 + 0.014*SL
	tF	0.22	0.21 + 0.004*SL	0.20 + 0.007*SL	0.22 + 0.006*SL
CI to S	tPLH	0.34	0.32 + 0.010*SL	0.33 + 0.008*SL	0.35 + 0.007*SL
	tPHL	0.47	0.45 + 0.008*SL	0.46 + 0.007*SL	0.50 + 0.005*SL
	tR	0.21	0.19 + 0.009*SL	0.18 + 0.013*SL	0.16 + 0.014*SL
	tF	0.21	0.17 + 0.017*SL	0.20 + 0.006*SL	0.20 + 0.007*SL

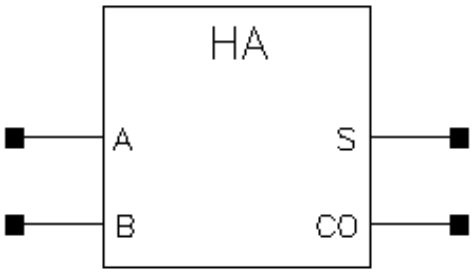
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: A, B
Outputs: S, C0
Input Loading (SL):
- HA: A: 2, B: 3
-HAD2: A: 2, B: 3
- HAD4:A: 2, B: 3

Maximum Fanout (Rec. SL):
- HAl: 28
- HAD2: 56
- HAD4: 112

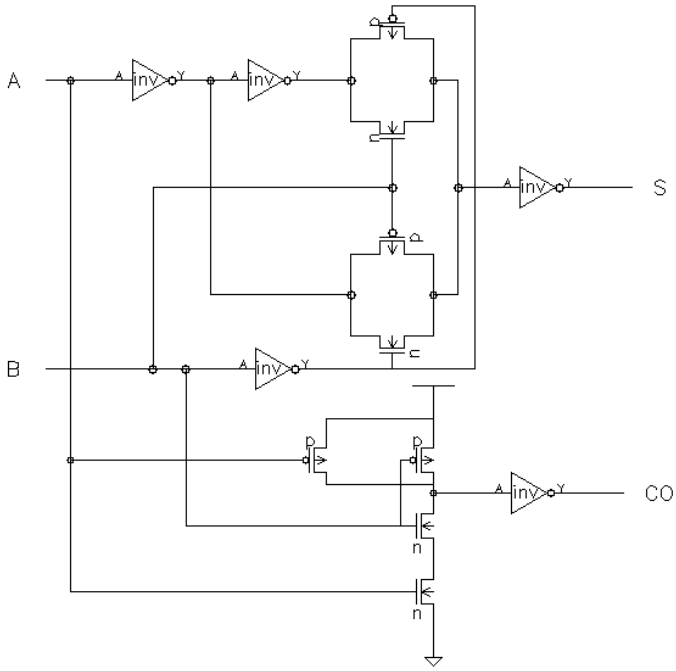
Gate Count:
- HA: 5
- HAD2: 6
- HAD4: 8



Symbol

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table



Schematic

HA Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	0.18	0.11 + 0.039*SL	0.11 + 0.036*SL	0.12 + 0.036*SL
	tPHL	0.35	0.30 + 0.025*SL	0.32 + 0.017*SL	0.34 + 0.016*SL
	tR	0.26	0.11 + 0.077*SL	0.09 + 0.082*SL	0.06 + 0.084*SL
	tF	0.16	0.11 + 0.027*SL	0.09 + 0.032*SL	0.05 + 0.034*SL
B to CO	tPLH	0.21	0.13 + 0.038*SL	0.14 + 0.036*SL	0.14 + 0.036*SL
	tPHL	0.29	0.25 + 0.023*SL	0.26 + 0.017*SL	0.28 + 0.016*SL
	tR	0.26	0.10 + 0.078*SL	0.09 + 0.082*SL	0.06 + 0.084*SL
	tF	0.15	0.08 + 0.031*SL	0.08 + 0.033*SL	0.05 + 0.034*SL
A to S	tPLH	0.53	0.45 + 0.038*SL	0.45 + 0.037*SL	0.45 + 0.037*SL
	tPHL	0.28	0.23 + 0.028*SL	0.25 + 0.019*SL	0.30 + 0.017*SL
	tR	0.28	0.13 + 0.076*SL	0.10 + 0.086*SL	0.09 + 0.087*SL
	tF	0.19	0.11 + 0.037*SL	0.13 + 0.032*SL	0.10 + 0.033*SL
B to S	tPLH	0.44	0.37 + 0.039*SL	0.37 + 0.037*SL	0.37 + 0.037*SL
	tPHL	0.22	0.17 + 0.026*SL	0.19 + 0.019*SL	0.23 + 0.017*SL
	tR	0.28	0.11 + 0.086*SL	0.11 + 0.085*SL	0.09 + 0.087*SL
	tF	0.18	0.11 + 0.034*SL	0.12 + 0.032*SL	0.10 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

HAD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	0.19	0.14 + 0.022*SL	0.15 + 0.019*SL	0.16 + 0.018*SL
	tPHL	0.36	0.32 + 0.017*SL	0.35 + 0.010*SL	0.38 + 0.008*SL
	tR	0.19	0.11 + 0.039*SL	0.10 + 0.041*SL	0.07 + 0.042*SL
	tF	0.14	0.11 + 0.017*SL	0.11 + 0.015*SL	0.11 + 0.015*SL
B to CO	tPLH	0.22	0.18 + 0.021*SL	0.19 + 0.019*SL	0.19 + 0.018*SL
	tPHL	0.32	0.29 + 0.014*SL	0.30 + 0.010*SL	0.34 + 0.008*SL
	tR	0.18	0.10 + 0.041*SL	0.10 + 0.041*SL	0.08 + 0.042*SL
	tF	0.13	0.10 + 0.014*SL	0.10 + 0.016*SL	0.10 + 0.016*SL
A to S	tPLH	0.50	0.45 + 0.025*SL	0.47 + 0.019*SL	0.48 + 0.018*SL
	tPHL	0.27	0.24 + 0.020*SL	0.26 + 0.012*SL	0.31 + 0.009*SL
	tR	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.07 + 0.043*SL
	tF	0.15	0.11 + 0.022*SL	0.12 + 0.018*SL	0.16 + 0.015*SL
B to S	tPLH	0.42	0.38 + 0.022*SL	0.38 + 0.019*SL	0.39 + 0.018*SL
	tPHL	0.23	0.19 + 0.018*SL	0.21 + 0.012*SL	0.26 + 0.009*SL
	tR	0.18	0.10 + 0.041*SL	0.10 + 0.042*SL	0.07 + 0.043*SL
	tF	0.16	0.12 + 0.021*SL	0.14 + 0.016*SL	0.15 + 0.016*SL

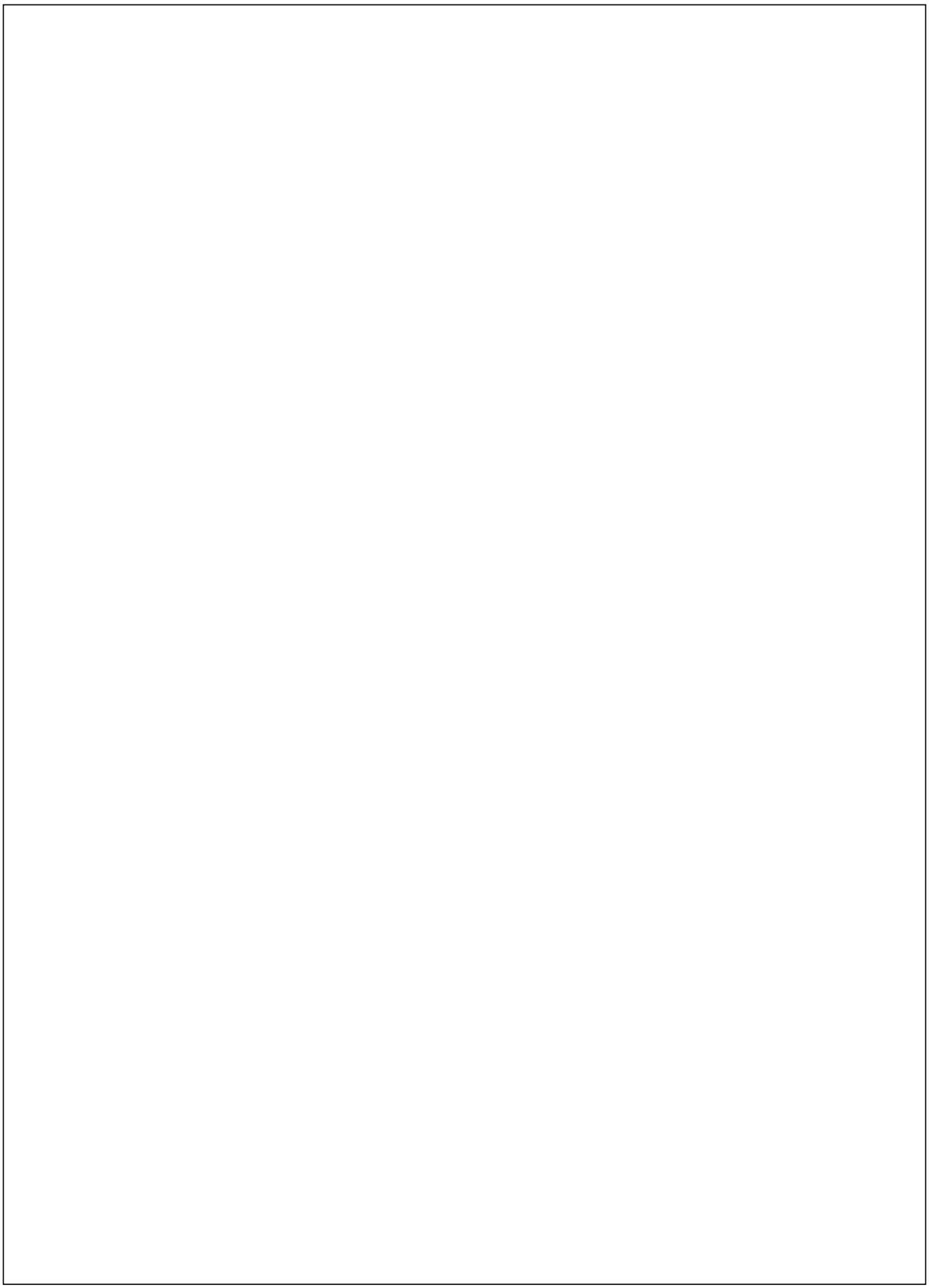
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

HAD4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	t_{PLH}	0.25	0.22 + 0.012*SL	0.23 + 0.010*SL	0.24 + 0.010*SL
	t_{PHL}	0.41	0.39 + 0.011*SL	0.40 + 0.007*SL	0.44 + 0.005*SL
	t_R	0.18	0.15 + 0.016*SL	0.13 + 0.021*SL	0.10 + 0.022*SL
	t_F	0.16	0.13 + 0.012*SL	0.15 + 0.008*SL	0.15 + 0.008*SL
B to CO	t_{PLH}	0.29	0.27 + 0.011*SL	0.27 + 0.010*SL	0.29 + 0.009*SL
	t_{PHL}	0.39	0.37 + 0.010*SL	0.38 + 0.006*SL	0.41 + 0.005*SL
	t_R	0.17	0.12 + 0.025*SL	0.13 + 0.022*SL	0.12 + 0.022*SL
	t_F	0.16	0.13 + 0.012*SL	0.15 + 0.008*SL	0.13 + 0.008*SL
A to S	t_{PLH}	0.54	0.52 + 0.011*SL	0.52 + 0.010*SL	0.54 + 0.009*SL
	t_{PHL}	0.32	0.30 + 0.010*SL	0.31 + 0.008*SL	0.35 + 0.006*SL
	t_R	0.16	0.12 + 0.019*SL	0.11 + 0.022*SL	0.11 + 0.022*SL
	t_F	0.18	0.15 + 0.014*SL	0.16 + 0.011*SL	0.21 + 0.008*SL
B to S	t_{PLH}	0.46	0.43 + 0.013*SL	0.44 + 0.010*SL	0.46 + 0.010*SL
	t_{PHL}	0.28	0.26 + 0.011*SL	0.27 + 0.008*SL	0.31 + 0.006*SL
	t_R	0.16	0.11 + 0.024*SL	0.12 + 0.022*SL	0.11 + 0.022*SL
	t_F	0.20	0.18 + 0.008*SL	0.17 + 0.010*SL	0.20 + 0.008*SL

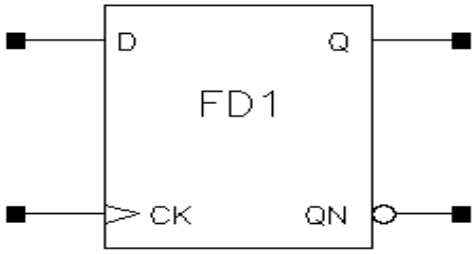
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL



Inputs: D, CK
Outputs: Q, QN
Input Loading (SL):
- D: 3
- CK: 1

Maximum Fanout (Rec. SL): All :
- FD1: 28
- FD1D2:56

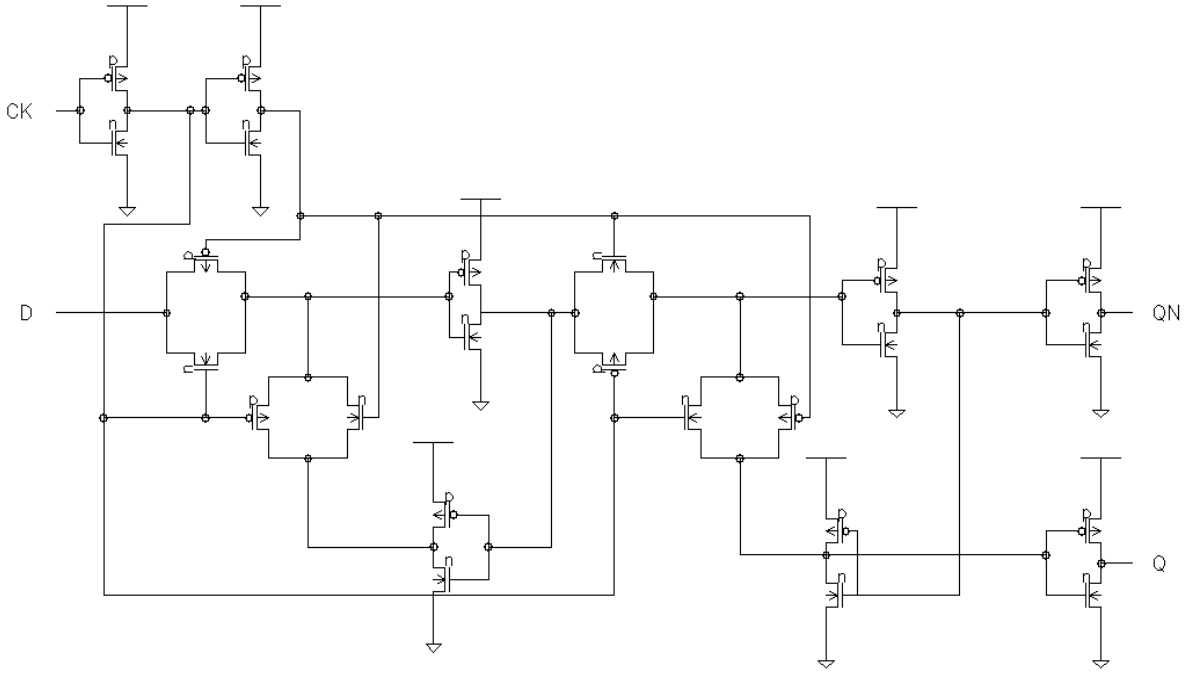
Gate Count:
- FD1: 6
- FD1D2:7



Symbol

D	CK	Qn+1	QNn+1
0	↑	0	1
1	↑	1	0
x	↓	Qn	QNn

Truth Table



Schematic

FD1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.52	0.44 + 0.037*SL	0.44 + 0.037*SL	0.44 + 0.037*SL
	t_{PHL}	0.45	0.41 + 0.021*SL	0.42 + 0.017*SL	0.44 + 0.016*SL
	t_R	0.24	0.08 + 0.081*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	t_F	0.13	0.06 + 0.034*SL	0.07 + 0.032*SL	0.04 + 0.034*SL
CK to QN	t_{PLH}	0.42	0.34 + 0.039*SL	0.34 + 0.038*SL	0.35 + 0.038*SL
	t_{PHL}	0.41	0.36 + 0.024*SL	0.38 + 0.018*SL	0.40 + 0.016*SL
	t_R	0.25	0.08 + 0.086*SL	0.07 + 0.087*SL	0.05 + 0.088*SL
	t_F	0.14	0.07 + 0.036*SL	0.08 + 0.033*SL	0.05 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD1 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.178
Input Setup Time (D to CK)	t_{SU}	0.287

FD1D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.55	0.51 + 0.019*SL	0.51 + 0.018*SL	0.51 + 0.018*SL
	t_{PHL}	0.49	0.46 + 0.014*SL	0.48 + 0.010*SL	0.51 + 0.008*SL
	t_R	0.16	0.08 + 0.042*SL	0.08 + 0.041*SL	0.05 + 0.042*SL
	t_F	0.11	0.08 + 0.018*SL	0.08 + 0.016*SL	0.09 + 0.016*SL
CK to QN	t_{PLH}	0.40	0.36 + 0.020*SL	0.37 + 0.019*SL	0.37 + 0.019*SL
	t_{PHL}	0.42	0.39 + 0.015*SL	0.40 + 0.010*SL	0.44 + 0.008*SL
	t_R	0.17	0.07 + 0.048*SL	0.08 + 0.043*SL	0.05 + 0.045*SL
	t_F	0.12	0.09 + 0.016*SL	0.09 + 0.017*SL	0.09 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

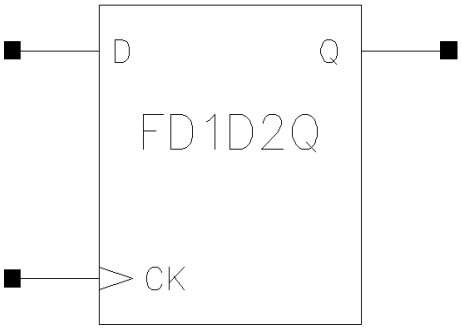
FD1D2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.178
Input Setup Time (D to CK)	t_{SU}	0.287

Inputs: D, CK
Output: Q
Input Loading (SL): All: D: 3, CK: 1
Maximum Fanout (Rec. SL):
- FD1D2Q: 56
- FD1D4Q: 112

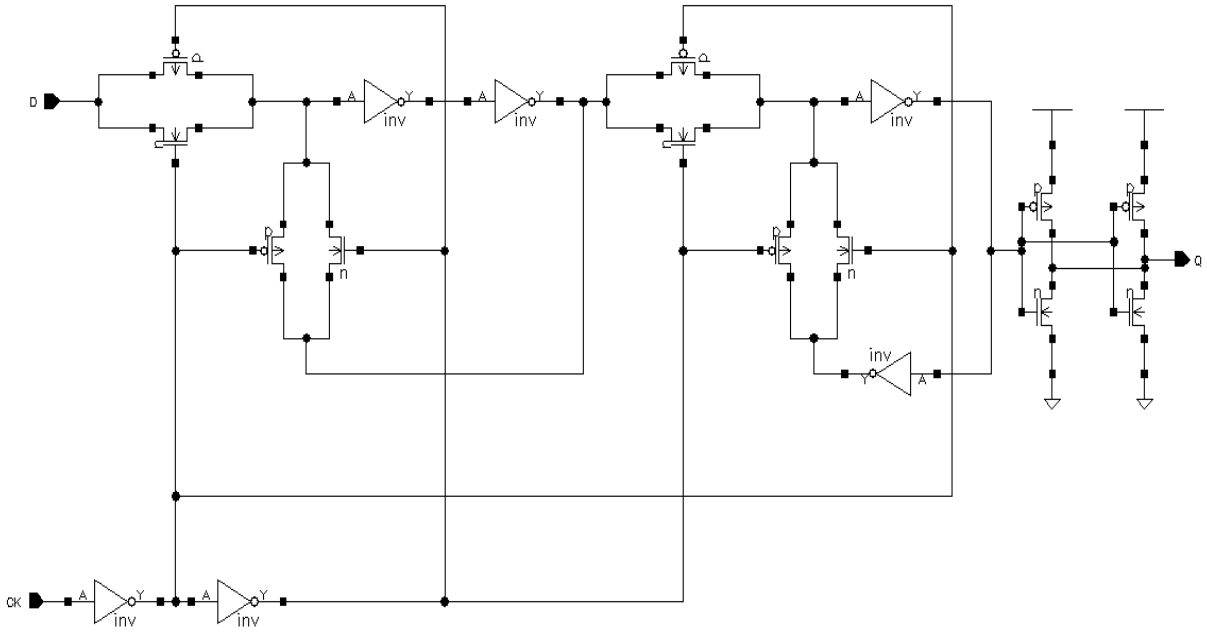
Gate Count:
- FD1D2Q: 6
- FD1D4Q: 7



Symbol

D	CK	Qn+1
0	↑	0
1	↑	1
x	↓	Qn

Truth Table



Schematic

FD1D2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.37	0.33 + 0.023*SL	0.33 + 0.020*SL	0.35 + 0.019*SL
	tPHL	0.33	0.29 + 0.020*SL	0.31 + 0.013*SL	0.38 + 0.010*SL
	tR	0.19	0.10 + 0.043*SL	0.10 + 0.044*SL	0.08 + 0.045*SL
	tF	0.16	0.11 + 0.026*SL	0.13 + 0.019*SL	0.17 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD1D2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.178
Input Setup Time (D to CK)	tSU	0.342

FD1D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.40	0.38 + 0.013*SL	0.38 + 0.011*SL	0.40 + 0.010*SL
	tPHL	0.36	0.34 + 0.014*SL	0.35 + 0.009*SL	0.40 + 0.006*SL
	tR	0.17	0.13 + 0.020*SL	0.13 + 0.022*SL	0.12 + 0.022*SL
	tF	0.17	0.15 + 0.011*SL	0.15 + 0.012*SL	0.19 + 0.009*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD1D4Q Timing Requirements

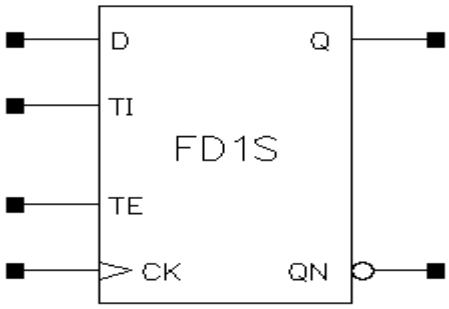
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.233
Input Setup Time (D to CK)	tSU	0.342

Inputs: D, TI, TE, CK
Outputs: Q, QN
Input Loading (SL):
- D, TI, CK: 1
- TE: 2

Maximum Fanout (Rec. SL): All :
- FD1S: 28
- FD1SD2: 56

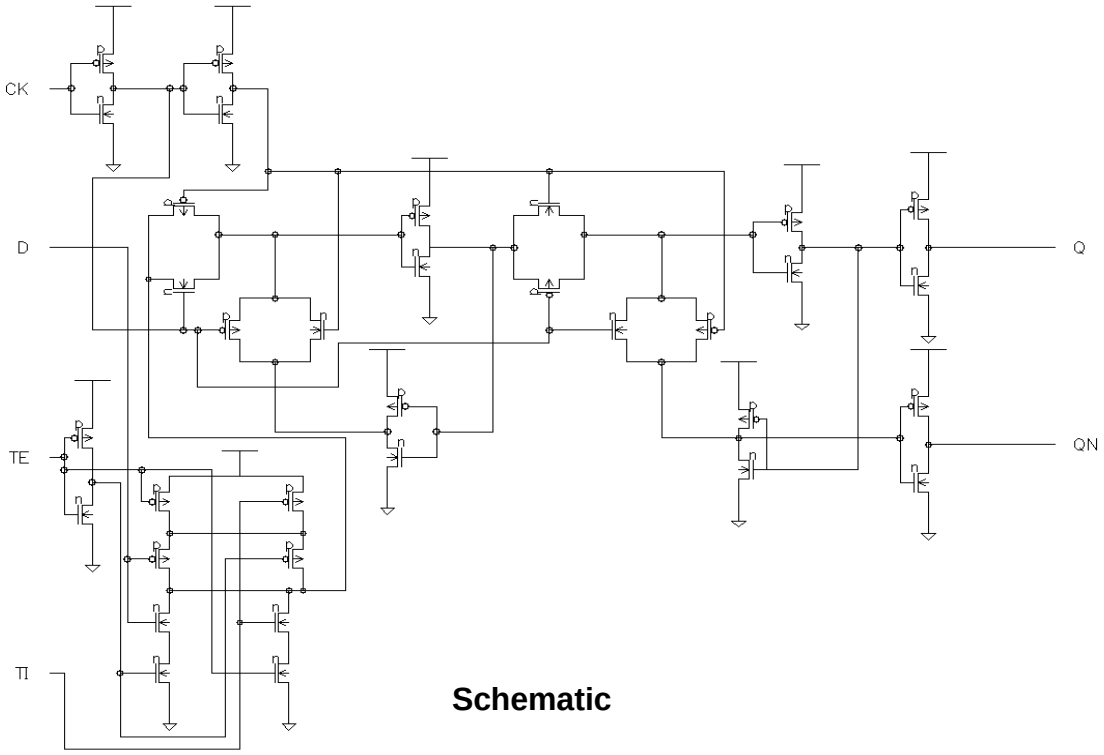
Gate Count:
- FD1S: 9
- FD1SD2: 10



Symbol

D	TI	TE	CK	Qn+1	QNn+1
0	x	0	↑	0	1
1	x	0	↑	1	0
x	0	1	↑	0	1
x	1	1	↑	1	0
x	x	x	↓	Qn	QNn

Truth Table



Schematic

FD1S Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.41	0.34 + 0.039*SL	0.34 + 0.038*SL	0.34 + 0.038*SL
	tPHL	0.41	0.36 + 0.024*SL	0.38 + 0.018*SL	0.40 + 0.016*SL
	tR	0.25	0.08 + 0.084*SL	0.07 + 0.088*SL	0.05 + 0.088*SL
	tF	0.14	0.06 + 0.038*SL	0.08 + 0.033*SL	0.06 + 0.034*SL
CK to QN	tPLH	0.52	0.44 + 0.037*SL	0.44 + 0.037*SL	0.44 + 0.037*SL
	tPHL	0.45	0.41 + 0.022*SL	0.42 + 0.017*SL	0.43 + 0.016*SL
	tR	0.24	0.07 + 0.085*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	tF	0.13	0.06 + 0.034*SL	0.07 + 0.032*SL	0.04 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD1S Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.506
Input Setup Time (TE to CK)	tSU	0.616
Input Setup Time (TI to CK)	tSU	0.561

FD1SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

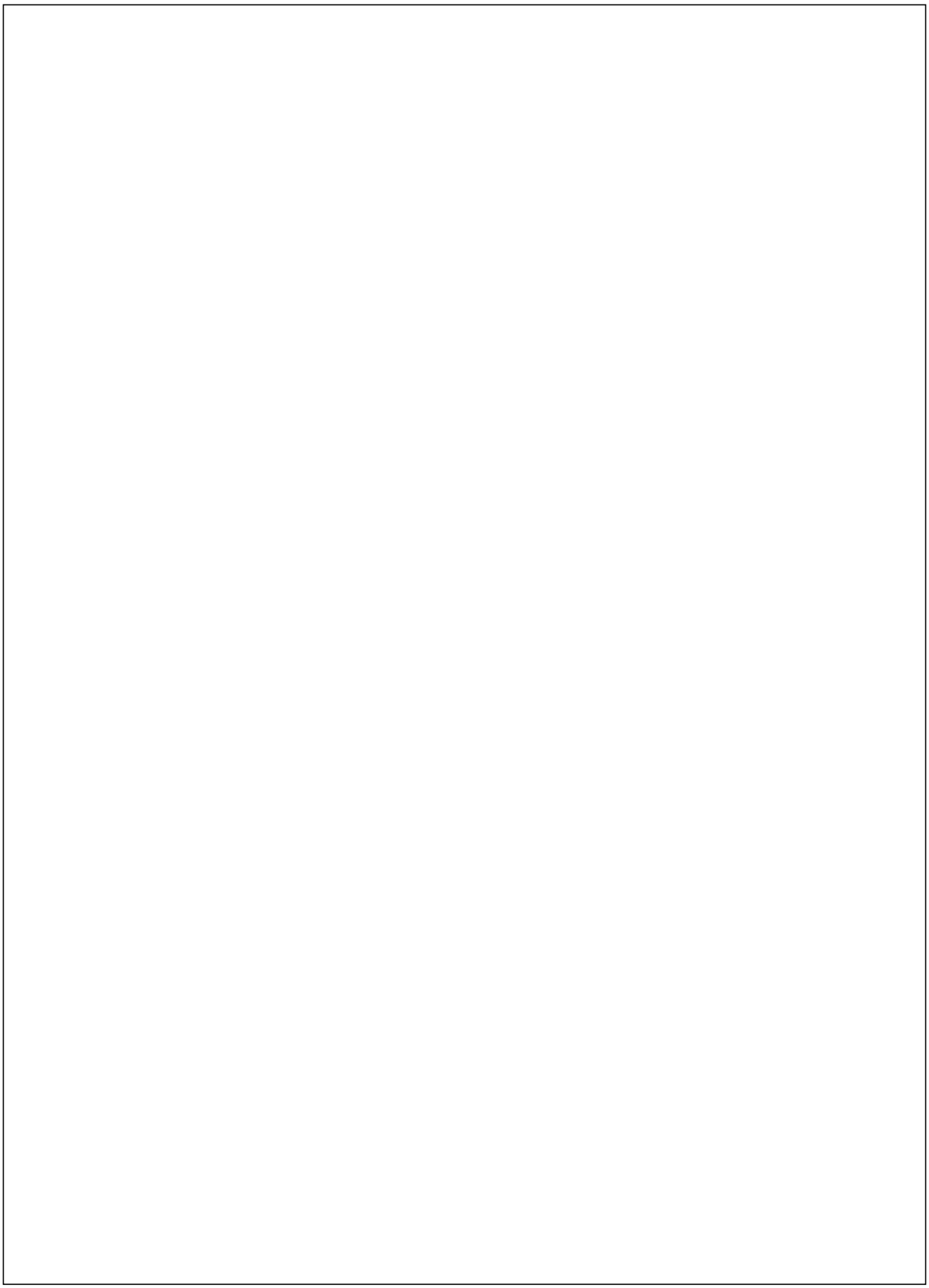
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.40	0.36 + 0.021*SL	0.36 + 0.019*SL	0.37 + 0.019*SL
	t_{PHL}	0.42	0.39 + 0.015*SL	0.40 + 0.010*SL	0.43 + 0.008*SL
	t_R	0.17	0.08 + 0.045*SL	0.09 + 0.043*SL	0.06 + 0.045*SL
	t_F	0.12	0.09 + 0.015*SL	0.09 + 0.017*SL	0.09 + 0.017*SL
CK to QN	t_{PLH}	0.54	0.51 + 0.016*SL	0.51 + 0.018*SL	0.50 + 0.018*SL
	t_{PHL}	0.49	0.46 + 0.014*SL	0.47 + 0.010*SL	0.50 + 0.008*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.041*SL	0.05 + 0.042*SL
	t_F	0.11	0.07 + 0.019*SL	0.09 + 0.015*SL	0.07 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD1SD2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

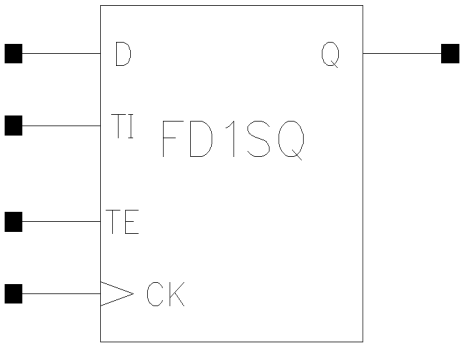
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.000
Input Hold Time (TE to CK)	t_{HD}	0.000
Input Hold Time (TI to CK)	t_{HD}	0.000
Input Setup Time (D to CK)	t_{SU}	0.506
Input Setup Time (TE to CK)	t_{SU}	0.616
Input Setup Time (TI to CK)	t_{SU}	0.561



Inputs: D, TI, TE, CK
Output: Q
Input Loading (SL):
- FD1SD2Q: D: 1,CK: 1,TI: 1, TE: 2
- FD1SD4Q: D: 1,CK: 1, TI: 1,TE:2

Maximum Fanout (Rec. SL):
- FD1SD2Q: 56
- FD1SD4Q: 112

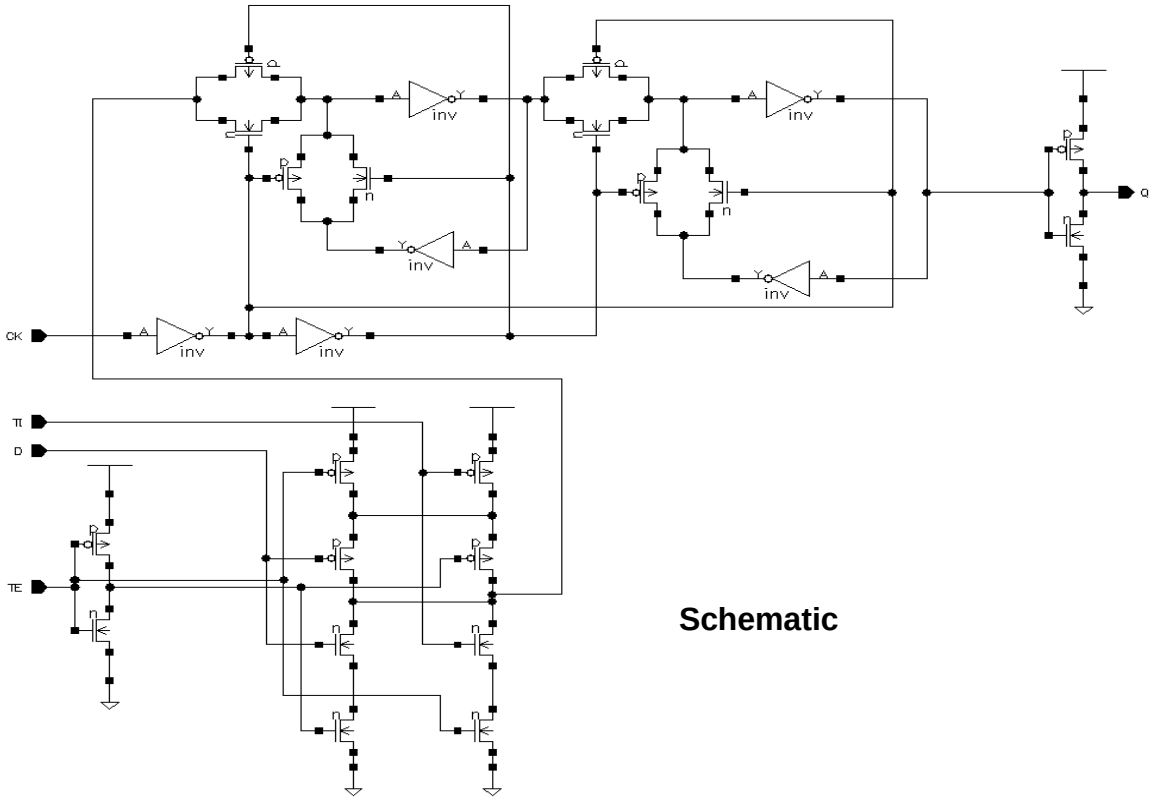
Gate Count:
- FD1SD2Q: 9
- FD1SD4Q: 10



Symbol

D	TI	TE	CK	Qn+1
0	x	0	↑	0
1	x	0	↑	1
x	0	1	↑	0
x	1	1	↑	1
x	x	x	↓	Qn

Truth Table



Schematic

FD1SD2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.40	0.36 + 0.021*SL	0.36 + 0.019*SL	0.37 + 0.019*SL
	tPHL	0.41	0.38 + 0.015*SL	0.40 + 0.010*SL	0.43 + 0.008*SL
	tR	0.17	0.10 + 0.039*SL	0.08 + 0.044*SL	0.06 + 0.045*SL
	tF	0.13	0.10 + 0.016*SL	0.10 + 0.017*SL	0.09 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD1SD2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.506
Input Setup Time (TE to CK)	tSU	0.616
Input Setup Time (TI to CK)	tSU	0.561

FD1SD4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.43	0.41 + 0.012*SL	0.41 + 0.010*SL	0.42 + 0.009*SL
	tPHL	0.45	0.43 + 0.011*SL	0.44 + 0.007*SL	0.48 + 0.005*SL
	tR	0.13	0.08 + 0.025*SL	0.09 + 0.022*SL	0.09 + 0.022*SL
	tF	0.14	0.12 + 0.010*SL	0.13 + 0.009*SL	0.15 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

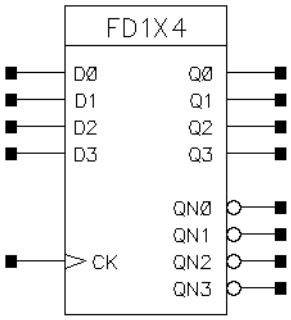
FD1SD4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.506
Input Setup Time (TE to CK)	tSU	0.670
Input Setup Time (TI to CK)	tSU	0.561

Inputs: D0, D1, D2, D3, CK
Outputs: Q0, Q1, Q2, Q3,
QN0, QN1, QN2, QN3
Input Loading (SL):
- D0, D1, D2, D3: 3
- CK: 1

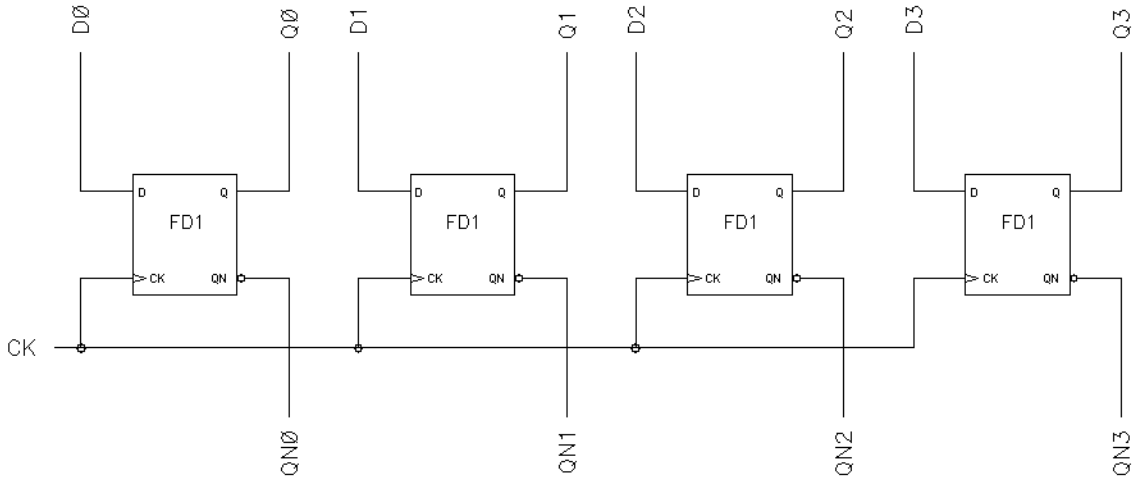
Maximum Fanout (Rec. SL): All : 28
Gate Count: 21



Symbol

D	CK	Qn+1	QNn+1
0	↑	0	1
1	↑	1	0
x	↓	Qn	QNn

Truth Table



Schematic

FD1X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	t_{PLH}	0.80	0.72 + 0.038*SL	0.72 + 0.037*SL	0.72 + 0.037*SL
	t_{PHL}	0.61	0.56 + 0.022*SL	0.58 + 0.017*SL	0.59 + 0.016*SL
	t_R	0.24	0.07 + 0.083*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	t_F	0.13	0.07 + 0.033*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
CK to Q1	t_{PLH}	0.80	0.73 + 0.037*SL	0.73 + 0.038*SL	0.73 + 0.038*SL
	t_{PHL}	0.61	0.56 + 0.022*SL	0.58 + 0.017*SL	0.59 + 0.016*SL
	t_R	0.24	0.07 + 0.087*SL	0.06 + 0.088*SL	0.05 + 0.089*SL
	t_F	0.13	0.07 + 0.032*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
CK to Q2	t_{PLH}	0.80	0.73 + 0.037*SL	0.73 + 0.038*SL	0.72 + 0.038*SL
	t_{PHL}	0.61	0.56 + 0.021*SL	0.58 + 0.017*SL	0.59 + 0.016*SL
	t_R	0.24	0.07 + 0.085*SL	0.06 + 0.088*SL	0.05 + 0.089*SL
	t_F	0.13	0.06 + 0.034*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
CK to Q3	t_{PLH}	0.80	0.72 + 0.038*SL	0.72 + 0.037*SL	0.72 + 0.037*SL
	t_{PHL}	0.61	0.56 + 0.021*SL	0.58 + 0.017*SL	0.59 + 0.016*SL
	t_R	0.24	0.07 + 0.083*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	t_F	0.13	0.06 + 0.034*SL	0.07 + 0.031*SL	0.05 + 0.033*SL
CK to QN0	t_{PLH}	0.57	0.49 + 0.039*SL	0.50 + 0.038*SL	0.50 + 0.038*SL
	t_{PHL}	0.69	0.64 + 0.024*SL	0.66 + 0.017*SL	0.69 + 0.016*SL
	t_R	0.25	0.08 + 0.083*SL	0.07 + 0.088*SL	0.05 + 0.088*SL
	t_F	0.14	0.07 + 0.036*SL	0.08 + 0.032*SL	0.05 + 0.033*SL
CK to QN1	t_{PLH}	0.57	0.50 + 0.039*SL	0.50 + 0.038*SL	0.50 + 0.038*SL
	t_{PHL}	0.69	0.64 + 0.024*SL	0.67 + 0.017*SL	0.69 + 0.016*SL
	t_R	0.25	0.09 + 0.083*SL	0.07 + 0.088*SL	0.06 + 0.089*SL
	t_F	0.14	0.07 + 0.034*SL	0.08 + 0.032*SL	0.06 + 0.033*SL
CK to QN2	t_{PLH}	0.57	0.50 + 0.039*SL	0.50 + 0.038*SL	0.50 + 0.038*SL
	t_{PHL}	0.69	0.65 + 0.024*SL	0.67 + 0.017*SL	0.69 + 0.016*SL
	t_R	0.25	0.09 + 0.081*SL	0.07 + 0.088*SL	0.06 + 0.089*SL
	t_F	0.14	0.07 + 0.033*SL	0.08 + 0.032*SL	0.06 + 0.033*SL
CK to QN3	t_{PLH}	0.57	0.49 + 0.039*SL	0.50 + 0.038*SL	0.50 + 0.038*SL
	t_{PHL}	0.69	0.64 + 0.024*SL	0.66 + 0.017*SL	0.69 + 0.016*SL
	t_R	0.25	0.08 + 0.082*SL	0.06 + 0.088*SL	0.06 + 0.088*SL
	t_F	0.14	0.07 + 0.036*SL	0.08 + 0.032*SL	0.05 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD1X4 Timing Requirements

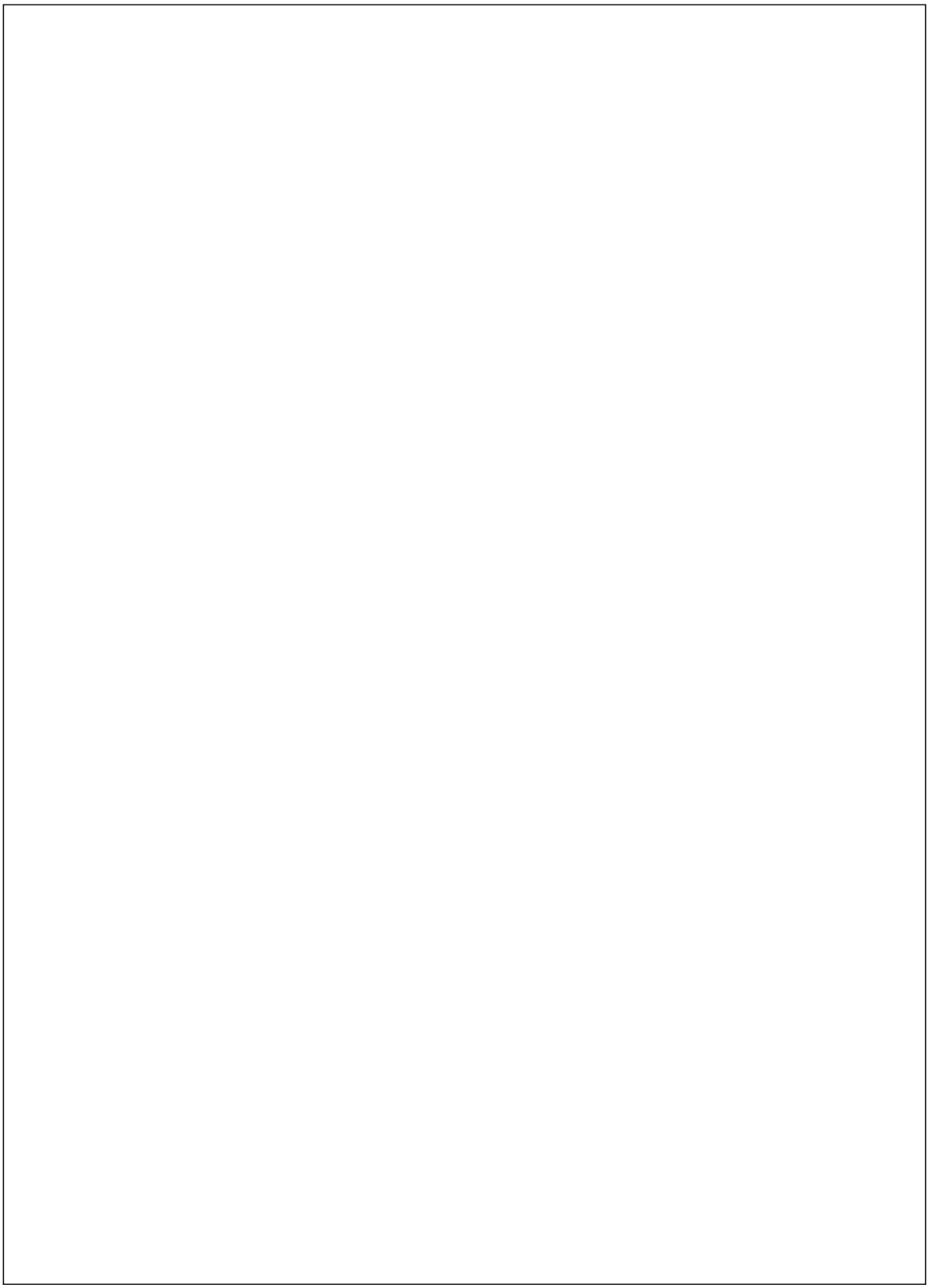
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920

FD1X4 Timing Requirements

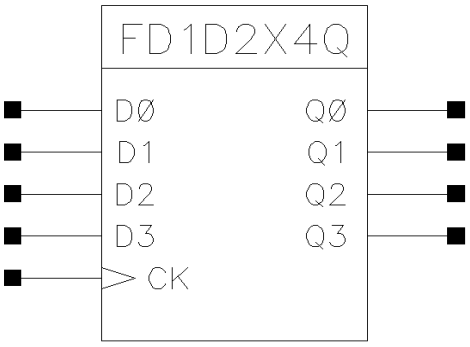
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D0 to CK)	t_{HD}	0.342
Input Hold Time (D1 to CK)	t_{HD}	0.397
Input Hold Time (D2 to CK)	t_{HD}	0.342
Input Hold Time (D3 to CK)	t_{HD}	0.342
Input Setup Time (D0 to CK)	t_{SU}	0.233
Input Setup Time (D1 to CK)	t_{SU}	0.233
Input Setup Time (D2 to CK)	t_{SU}	0.233
Input Setup Time (D3 to CK)	t_{SU}	0.233



Inputs: D0, D1, D2, D3, CK
Output: Q0, Q1, Q2, Q3
Input Loading (SL): All: DO, D1, D2, D3: 3
CK: 1
Maximum Fanout (Rec. SL):
- FD1D2XQ: 56
- FD1D4XQ: 112

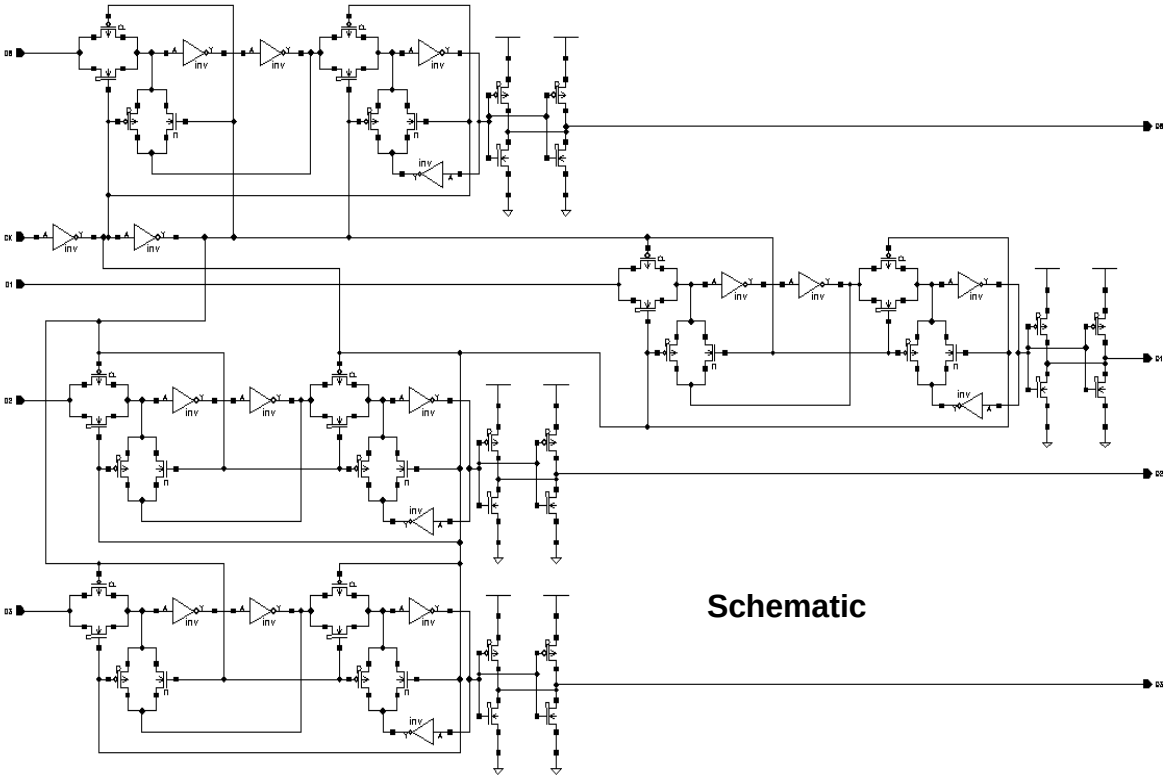
Gate Count:
- FD1D2X4Q: 21
- FD1D4X4Q: 25



Symbol

D	CK	Qn+1
0	↑	0
1	↑	1
x	↓	Qn

Truth Table



Schematic

FD1D2X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	tPLH	0.67	0.62 + 0.023*SL	0.63 + 0.020*SL	0.65 + 0.019*SL
	tPHL	0.54	0.50 + 0.021*SL	0.53 + 0.013*SL	0.60 + 0.010*SL
	tR	0.21	0.13 + 0.040*SL	0.12 + 0.044*SL	0.10 + 0.045*SL
	tF	0.19	0.15 + 0.022*SL	0.16 + 0.018*SL	0.17 + 0.017*SL
CK to Q1	tPLH	0.67	0.62 + 0.021*SL	0.63 + 0.019*SL	0.65 + 0.018*SL
	tPHL	0.54	0.50 + 0.021*SL	0.53 + 0.013*SL	0.59 + 0.010*SL
	tR	0.20	0.11 + 0.047*SL	0.12 + 0.042*SL	0.09 + 0.044*SL
	tF	0.19	0.15 + 0.021*SL	0.16 + 0.017*SL	0.18 + 0.016*SL
CK to Q2	tPLH	0.67	0.62 + 0.021*SL	0.63 + 0.019*SL	0.65 + 0.018*SL
	tPHL	0.54	0.50 + 0.021*SL	0.52 + 0.013*SL	0.59 + 0.010*SL
	tR	0.20	0.11 + 0.047*SL	0.12 + 0.042*SL	0.09 + 0.043*SL
	tF	0.19	0.15 + 0.021*SL	0.16 + 0.017*SL	0.18 + 0.016*SL
CK to Q3	tPLH	0.67	0.63 + 0.022*SL	0.63 + 0.020*SL	0.65 + 0.019*SL
	tPHL	0.54	0.50 + 0.021*SL	0.52 + 0.013*SL	0.59 + 0.010*SL
	tR	0.20	0.11 + 0.047*SL	0.12 + 0.044*SL	0.09 + 0.045*SL
	tF	0.19	0.15 + 0.022*SL	0.16 + 0.017*SL	0.17 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD1D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D0 to CK)	tHD	0.397
Input Hold Time (D1 to CK)	tHD	0.397
Input Hold Time (D2 to CK)	tHD	0.397
Input Hold Time (D3 to CK)	tHD	0.397
Input Setup Time (D0 to CK)	tSU	0.233
Input Setup Time (D1 to CK)	tSU	0.233
Input Setup Time (D2 to CK)	tSU	0.233
Input Setup Time (D3 to CK)	tSU	0.233

FD1D4X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

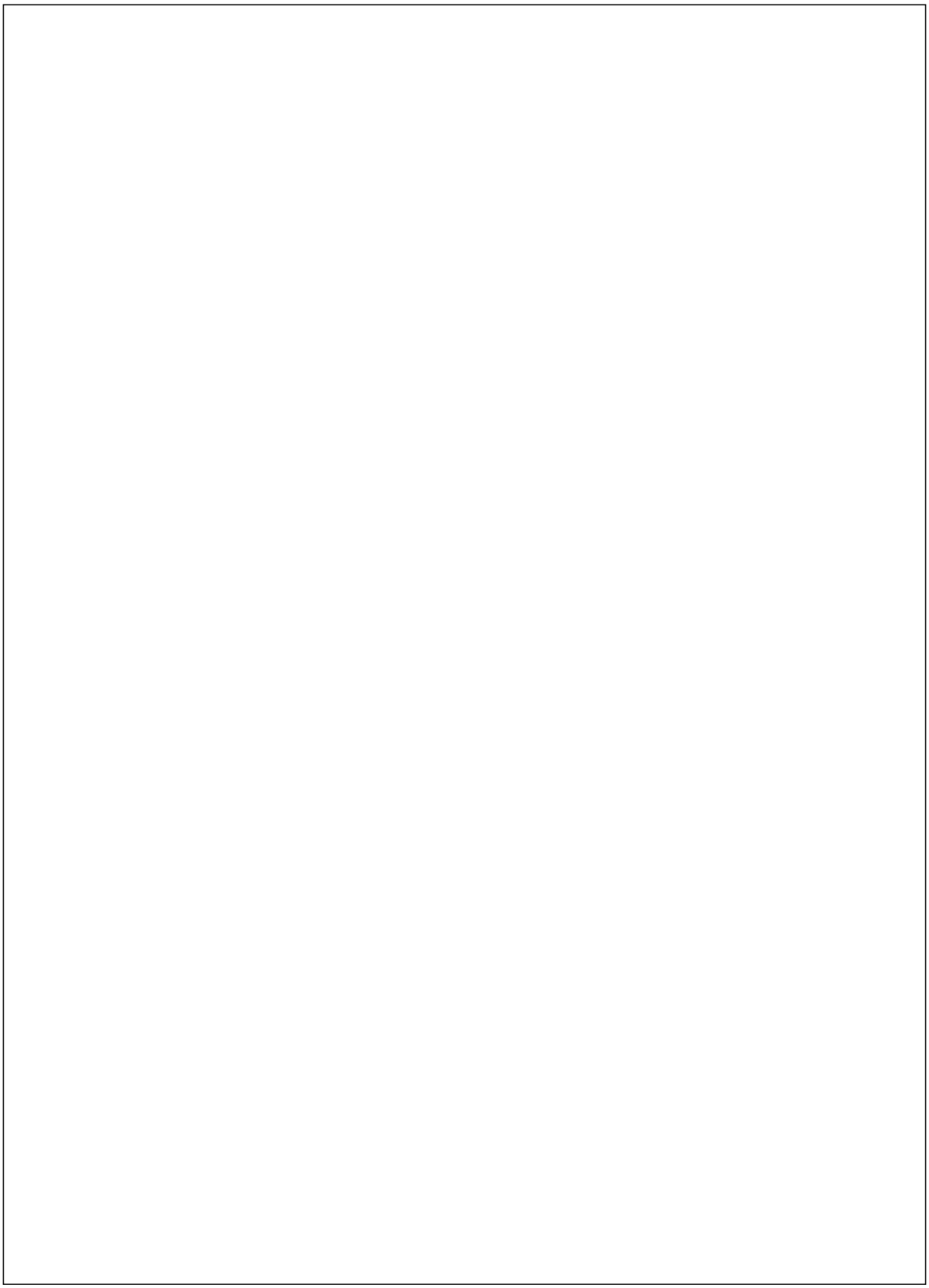
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	t_{PLH}	0.72	0.69 + 0.012*SL	0.70 + 0.011*SL	0.72 + 0.010*SL
	t_{PHL}	0.63	0.60 + 0.016*SL	0.62 + 0.009*SL	0.67 + 0.006*SL
	t_R	0.18	0.14 + 0.021*SL	0.14 + 0.022*SL	0.13 + 0.022*SL
	t_F	0.23	0.21 + 0.010*SL	0.21 + 0.010*SL	0.24 + 0.009*SL
CK to Q1	t_{PLH}	0.72	0.69 + 0.012*SL	0.70 + 0.010*SL	0.72 + 0.009*SL
	t_{PHL}	0.63	0.61 + 0.013*SL	0.62 + 0.009*SL	0.68 + 0.006*SL
	t_R	0.18	0.14 + 0.020*SL	0.14 + 0.021*SL	0.13 + 0.021*SL
	t_F	0.23	0.21 + 0.010*SL	0.21 + 0.010*SL	0.24 + 0.009*SL
CK to Q2	t_{PLH}	0.72	0.69 + 0.012*SL	0.70 + 0.010*SL	0.72 + 0.009*SL
	t_{PHL}	0.63	0.61 + 0.013*SL	0.62 + 0.009*SL	0.67 + 0.006*SL
	t_R	0.18	0.14 + 0.020*SL	0.14 + 0.021*SL	0.13 + 0.021*SL
	t_F	0.23	0.21 + 0.010*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
CK to Q3	t_{PLH}	0.72	0.69 + 0.012*SL	0.70 + 0.011*SL	0.71 + 0.010*SL
	t_{PHL}	0.63	0.59 + 0.016*SL	0.62 + 0.009*SL	0.67 + 0.006*SL
	t_R	0.18	0.14 + 0.021*SL	0.14 + 0.021*SL	0.13 + 0.022*SL
	t_F	0.23	0.21 + 0.009*SL	0.21 + 0.010*SL	0.24 + 0.009*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD1D4X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

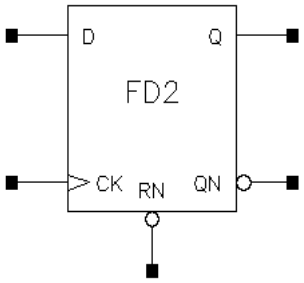
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D0 to CK)	t_{HD}	0.342
Input Hold Time (D1 to CK)	t_{HD}	0.342
Input Hold Time (D2 to CK)	t_{HD}	0.342
Input Hold Time (D3 to CK)	t_{HD}	0.342
Input Setup Time (D0 to CK)	t_{SU}	0.233
Input Setup Time (D1 to CK)	t_{SU}	0.233
Input Setup Time (D2 to CK)	t_{SU}	0.233
Input Setup Time (D3 to CK)	t_{SU}	0.233



Inputs: D, CK, RN
Outputs: Q, QN
Input Loading (SL):
- D: 3
- CK: 1
- RN: 2

Maximum Fanout (Rec. SL):
- FD2: All : 28
- FD2D2: All : 56

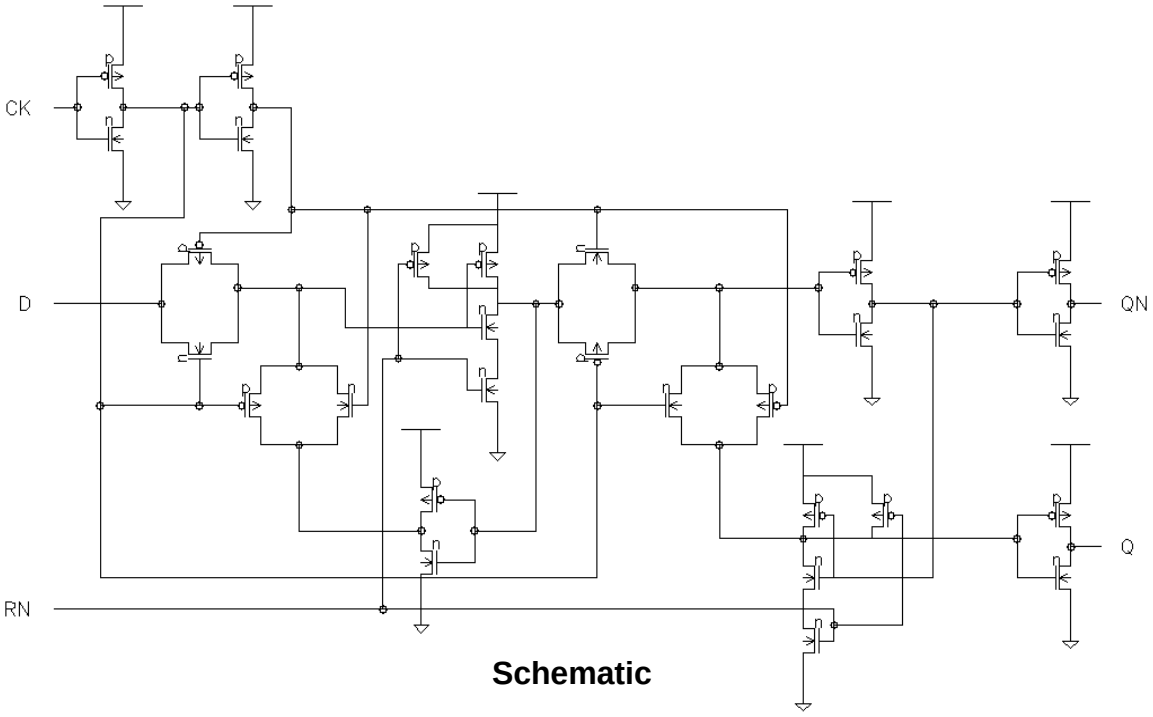
Gate Count:
- FD2: 7
- FD2D2: 8



Symbol

D	RN	CK	Qn+1	QNn+1
0	1	↑	0	1
1	1	↑	1	0
x	0	x	0	1
x	1	↓	Qn	QNn

Truth Table



Schematic

FD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.60	0.53 + 0.036*SL	0.53 + 0.036*SL	0.52 + 0.036*SL
	t_{PHL}	0.46	0.42 + 0.021*SL	0.43 + 0.017*SL	0.45 + 0.016*SL
	t_R	0.25	0.10 + 0.079*SL	0.08 + 0.083*SL	0.05 + 0.085*SL
	t_F	0.14	0.07 + 0.035*SL	0.08 + 0.031*SL	0.05 + 0.032*SL
RN to Q	t_{PHL}	0.37	0.32 + 0.027*SL	0.35 + 0.017*SL	0.37 + 0.016*SL
	t_F	0.17	0.10 + 0.034*SL	0.11 + 0.030*SL	0.06 + 0.032*SL
CK to QN	t_{PLH}	0.41	0.34 + 0.038*SL	0.34 + 0.036*SL	0.35 + 0.036*SL
	t_{PHL}	0.44	0.39 + 0.022*SL	0.41 + 0.017*SL	0.44 + 0.016*SL
	t_R	0.24	0.08 + 0.081*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.14	0.09 + 0.025*SL	0.07 + 0.032*SL	0.06 + 0.032*SL
RN to QN	t_{PLH}	0.63	0.56 + 0.036*SL	0.56 + 0.036*SL	0.56 + 0.036*SL
	t_R	0.25	0.09 + 0.081*SL	0.08 + 0.083*SL	0.05 + 0.084*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.123
Input Setup Time (D to CK)	t_{SU}	0.287
Recovery Time (RN)	t_{RC}	0.139

FD2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

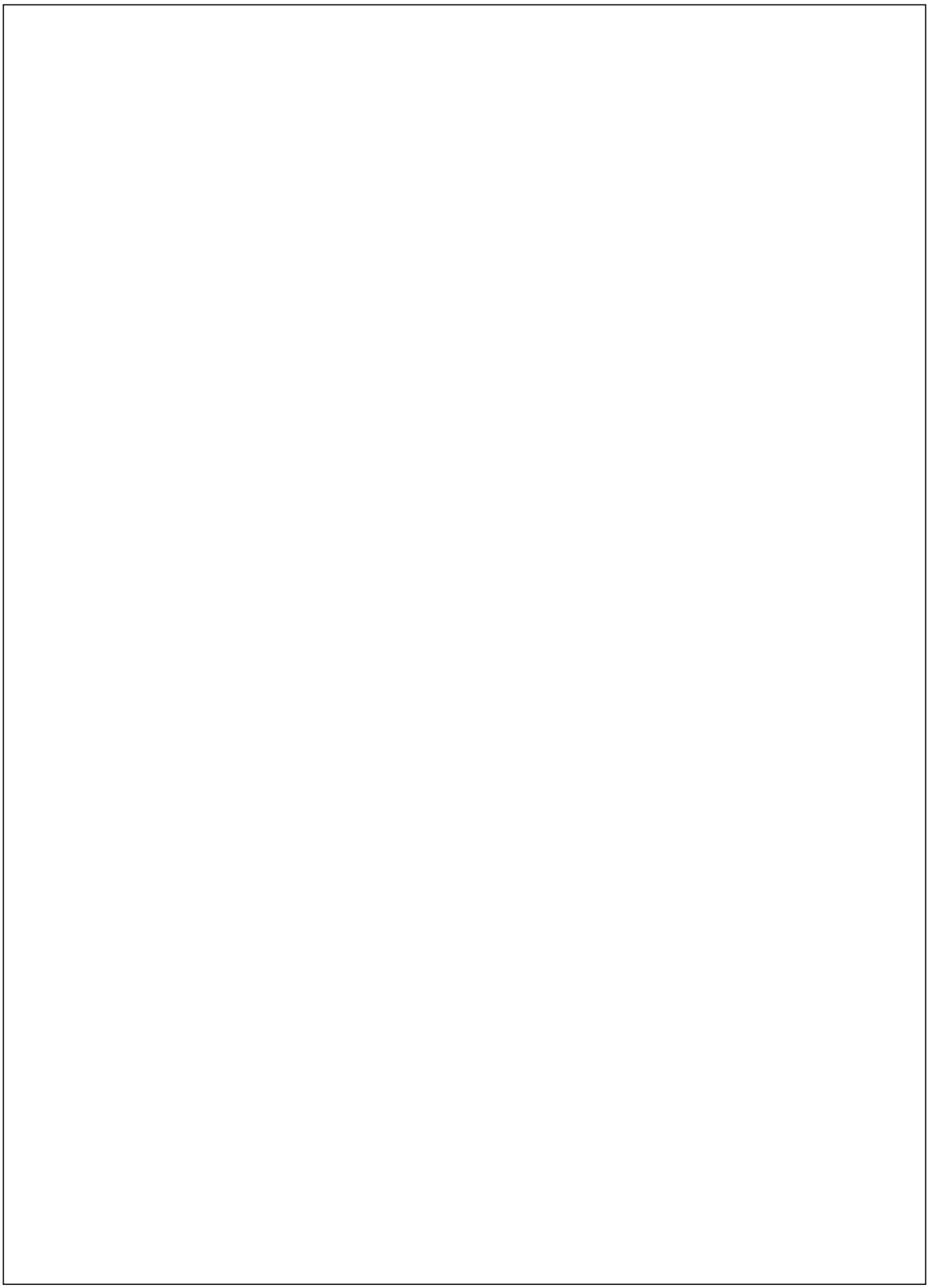
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.65	0.61 + 0.016*SL	0.61 + 0.018*SL	0.61 + 0.018*SL
	t_{PHL}	0.50	0.47 + 0.015*SL	0.49 + 0.010*SL	0.52 + 0.008*SL
	t_R	0.18	0.11 + 0.035*SL	0.09 + 0.042*SL	0.07 + 0.043*SL
	t_F	0.12	0.08 + 0.023*SL	0.10 + 0.015*SL	0.08 + 0.016*SL
RN to Q	t_{PHL}	0.38	0.35 + 0.016*SL	0.36 + 0.010*SL	0.40 + 0.008*SL
	t_F	0.15	0.13 + 0.014*SL	0.12 + 0.015*SL	0.13 + 0.015*SL
CK to QN	t_{PLH}	0.40	0.36 + 0.020*SL	0.37 + 0.019*SL	0.38 + 0.018*SL
	t_{PHL}	0.45	0.42 + 0.016*SL	0.44 + 0.010*SL	0.47 + 0.008*SL
	t_R	0.16	0.08 + 0.042*SL	0.08 + 0.041*SL	0.06 + 0.042*SL
	t_F	0.13	0.09 + 0.017*SL	0.10 + 0.016*SL	0.10 + 0.016*SL
RN to QN	t_{PLH}	0.62	0.59 + 0.018*SL	0.59 + 0.018*SL	0.59 + 0.018*SL
	t_R	0.17	0.11 + 0.032*SL	0.08 + 0.041*SL	0.06 + 0.042*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD2D2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

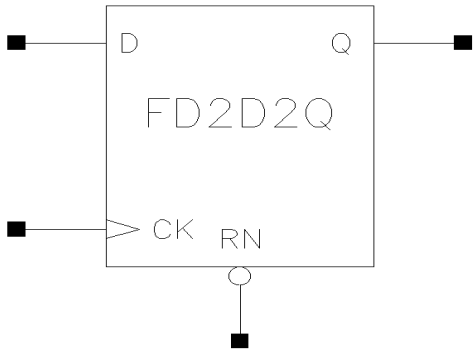
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.178
Input Setup Time (D to CK)	t_{SU}	0.287
Recovery Time (RN)	t_{RC}	0.139



Inputs: D, CK, RN
Output: Q
Input Loading (SL):
- FD2D2Q: D: 3, CK: 1, RN: 2
- FD2D4Q: D: 3, CK: 1, RN: 2

Maximum Fanout (Rec. SL):
- FD2D2Q: 56
- FD2D4Q: 112

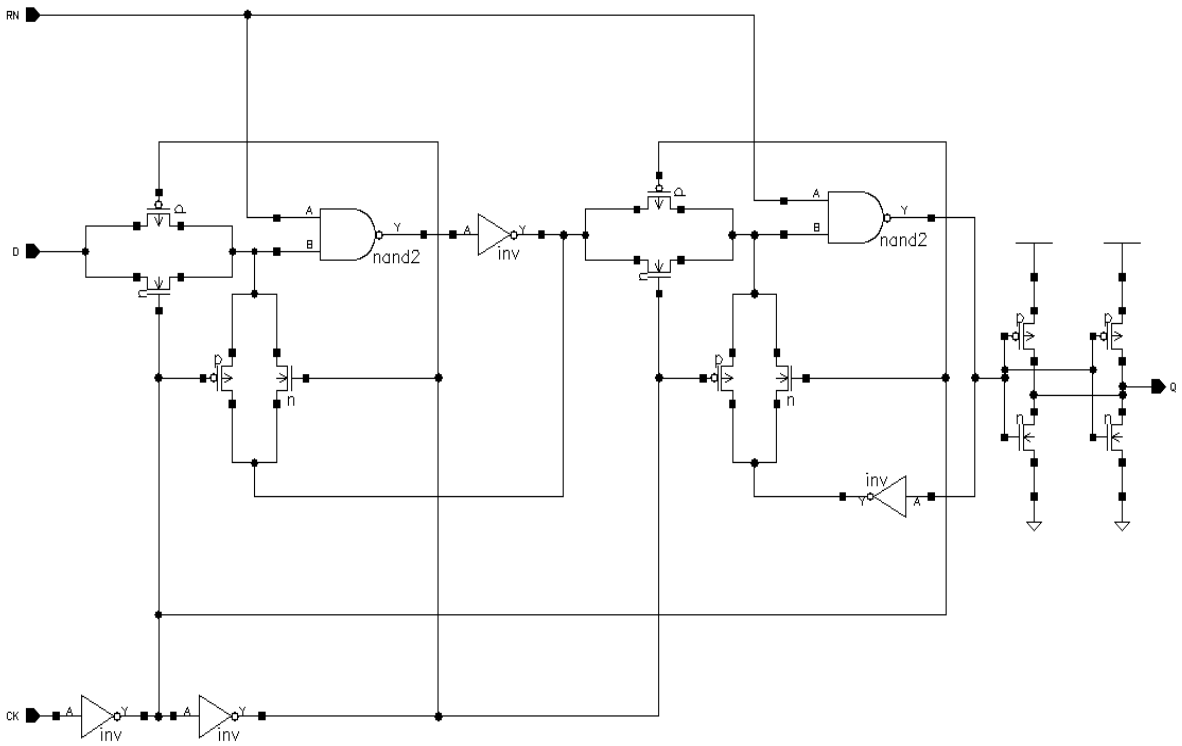
Gate Count:
- FD2D2Q: 7
- FD2D4Q: 8



Symbol

D	RN	CK	Qn+1
0	1	↑	0
1	1	↑	1
x	0	x	0
x	1	↓	Qn

Truth Table



Schematic

FD2D2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.42	0.37 + 0.025*SL	0.38 + 0.020*SL	0.42 + 0.019*SL
	t_{PHL}	0.33	0.29 + 0.020*SL	0.31 + 0.013*SL	0.38 + 0.010*SL
	t_R	0.22	0.12 + 0.047*SL	0.14 + 0.042*SL	0.12 + 0.043*SL
	t_F	0.16	0.11 + 0.025*SL	0.13 + 0.018*SL	0.17 + 0.016*SL
RN to Q	t_{PHL}	0.54	0.49 + 0.023*SL	0.52 + 0.013*SL	0.60 + 0.009*SL
	t_F	0.23	0.19 + 0.017*SL	0.20 + 0.016*SL	0.20 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD2D2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.178
Input Setup Time (D to CK)	t_{SU}	0.342
Recovery Time (RN)	t_{RC}	0.139

FD2D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.47	0.45 + 0.014*SL	0.45 + 0.011*SL	0.48 + 0.010*SL
	t_{PHL}	0.36	0.34 + 0.013*SL	0.35 + 0.009*SL	0.40 + 0.006*SL
	t_R	0.22	0.18 + 0.018*SL	0.17 + 0.021*SL	0.17 + 0.021*SL
	t_F	0.17	0.14 + 0.014*SL	0.15 + 0.011*SL	0.20 + 0.009*SL
RN to Q	t_{PHL}	0.59	0.56 + 0.012*SL	0.57 + 0.009*SL	0.63 + 0.006*SL
	t_F	0.23	0.21 + 0.013*SL	0.22 + 0.009*SL	0.24 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD2D4Q Timing Requirements

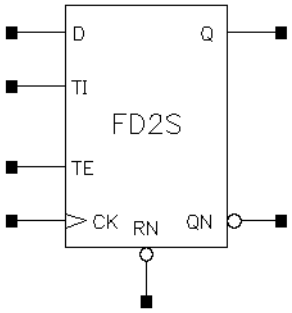
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.178
Input Setup Time (D to CK)	t_{SU}	0.342
Recovery Time (RN)	t_{RC}	0.139

Inputs: D, TI, TE, CK, RN
Outputs: Q, QN
Input Loading (SL):
- D, TI, CK: 1
- TE, RN: 2

Maximum Fanout (Rec. SL):
- FD2S: All : 28
- D2SD2: All : 56

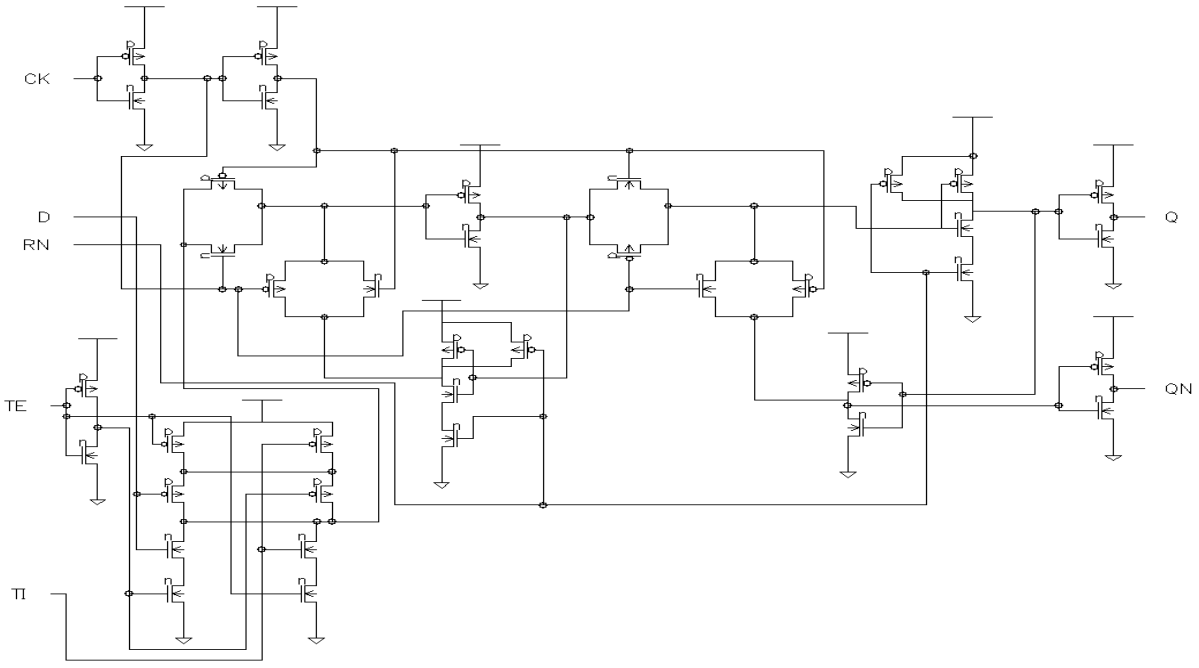
Gate Count:
- FD2S: 10
- FD2SD2: 10



Symbol

D	RN	TI	TE	CK	Qn+1	QNn+1
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	1	0	1	↑	0	1
x	1	1	1	↑	1	0
x	0	x	x	x	0	1
x	1	x	x	↓	Qn	QNn

Truth Table



Schematic

FD2S Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.46	0.38 + 0.041*SL	0.39 + 0.036*SL	0.40 + 0.036*SL
	t_{PHL}	0.42	0.37 + 0.025*SL	0.39 + 0.018*SL	0.42 + 0.016*SL
	t_R	0.25	0.09 + 0.081*SL	0.09 + 0.082*SL	0.06 + 0.083*SL
	t_F	0.14	0.08 + 0.031*SL	0.08 + 0.033*SL	0.06 + 0.034*SL
RN to Q	t_{PHL}	0.39	0.34 + 0.028*SL	0.37 + 0.018*SL	0.40 + 0.016*SL
	t_F	0.18	0.11 + 0.035*SL	0.12 + 0.031*SL	0.08 + 0.033*SL
CK to QN	t_{PLH}	0.53	0.45 + 0.038*SL	0.46 + 0.036*SL	0.45 + 0.036*SL
	t_{PHL}	0.51	0.46 + 0.022*SL	0.48 + 0.017*SL	0.49 + 0.017*SL
	t_R	0.23	0.07 + 0.083*SL	0.07 + 0.082*SL	0.05 + 0.083*SL
	t_F	0.14	0.07 + 0.037*SL	0.08 + 0.032*SL	0.05 + 0.033*SL
RN to QN	t_{PLH}	0.50	0.43 + 0.035*SL	0.43 + 0.036*SL	0.42 + 0.036*SL
	t_R	0.23	0.07 + 0.083*SL	0.07 + 0.082*SL	0.05 + 0.083*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD2S Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.000
Input Hold Time (TE to CK)	t_{HD}	0.000
Input Hold Time (TI to CK)	t_{HD}	0.000
Input Setup Time (D to CK)	t_{SU}	0.506
Input Setup Time (TE to CK)	t_{SU}	0.616
Input Setup Time (TI to CK)	t_{SU}	0.561
Recovery Time (RN)	t_{RC}	0.139

FD2SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

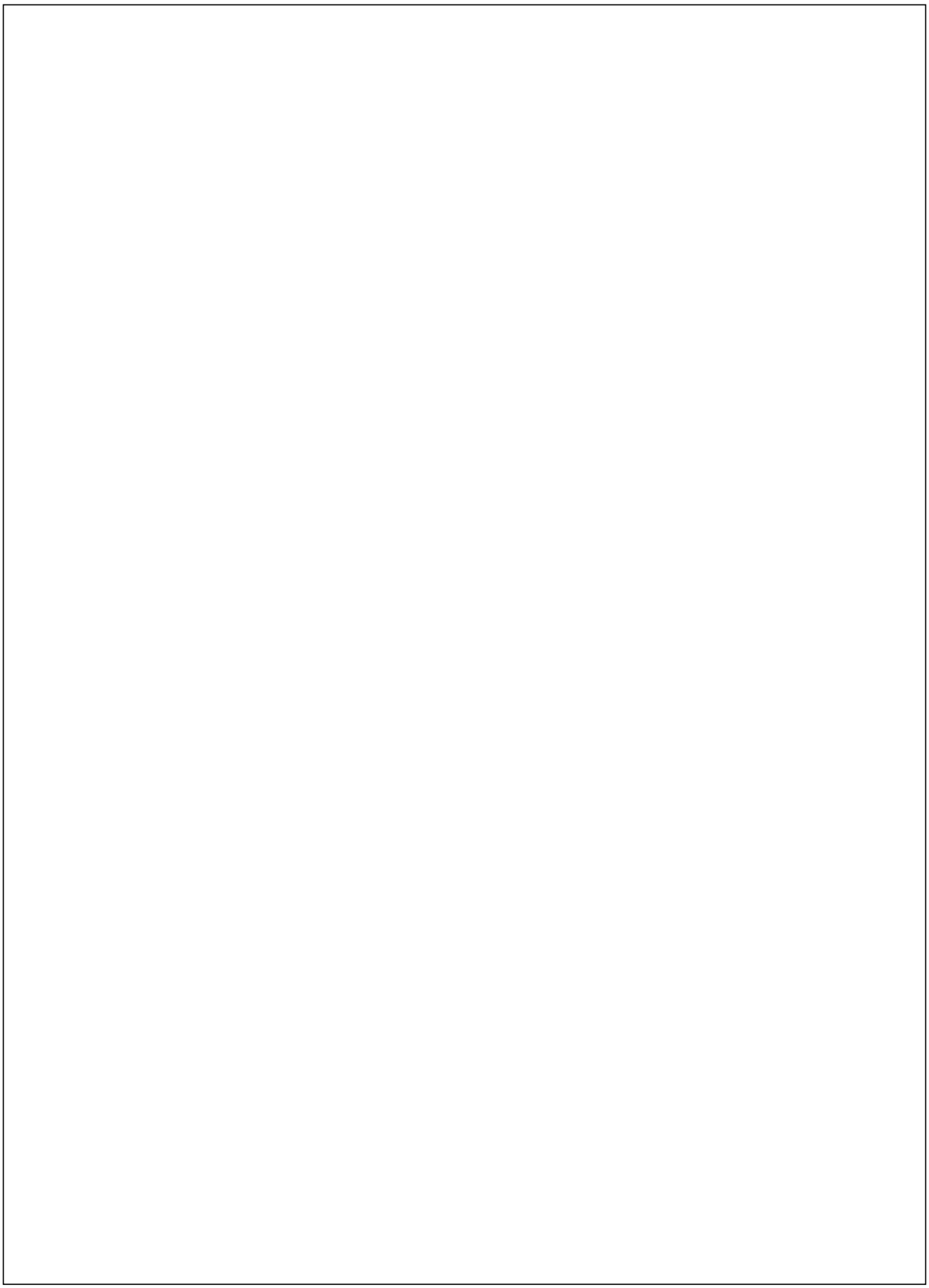
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.46	0.42 + 0.022*SL	0.43 + 0.019*SL	0.44 + 0.018*SL
	tPHL	0.43	0.40 + 0.015*SL	0.41 + 0.010*SL	0.45 + 0.009*SL
	tR	0.18	0.09 + 0.043*SL	0.10 + 0.041*SL	0.08 + 0.042*SL
	tF	0.12	0.09 + 0.016*SL	0.09 + 0.017*SL	0.09 + 0.017*SL
RN to Q	tPHL	0.40	0.36 + 0.017*SL	0.38 + 0.011*SL	0.43 + 0.008*SL
	tF	0.16	0.13 + 0.017*SL	0.13 + 0.016*SL	0.13 + 0.016*SL
CK to QN	tPLH	0.56	0.52 + 0.017*SL	0.52 + 0.018*SL	0.51 + 0.018*SL
	tPHL	0.56	0.53 + 0.013*SL	0.54 + 0.010*SL	0.57 + 0.008*SL
	tR	0.16	0.09 + 0.037*SL	0.08 + 0.041*SL	0.05 + 0.042*SL
	tF	0.12	0.08 + 0.018*SL	0.09 + 0.016*SL	0.09 + 0.016*SL
RN to QN	tPLH	0.54	0.50 + 0.016*SL	0.50 + 0.018*SL	0.50 + 0.018*SL
	tR	0.16	0.08 + 0.040*SL	0.08 + 0.041*SL	0.06 + 0.042*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD2SD2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

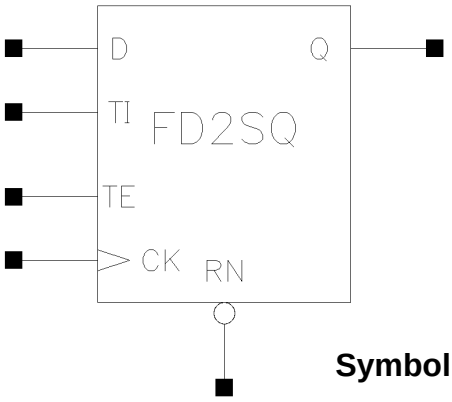
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.506
Input Setup Time (TE to CK)	tSU	0.616
Input Setup Time (TI to CK)	tSU	0.561
Recovery Time (RN)	tRC	0.139



Inputs: D, TI, TE, CK, RN
Output: Q
Input Loading (SL):
- FD2SD2Q: D: 1,CK: 1,RN: 2,
  TI: 1,TE: 2
- FD2SD4Q: D: 1,CK: 1, RN: 2, TI: 1
  TE: 2

Maximum Fanout (Rec. SL):
- FD2SD2Q: 56
- FD2SD4Q: 112

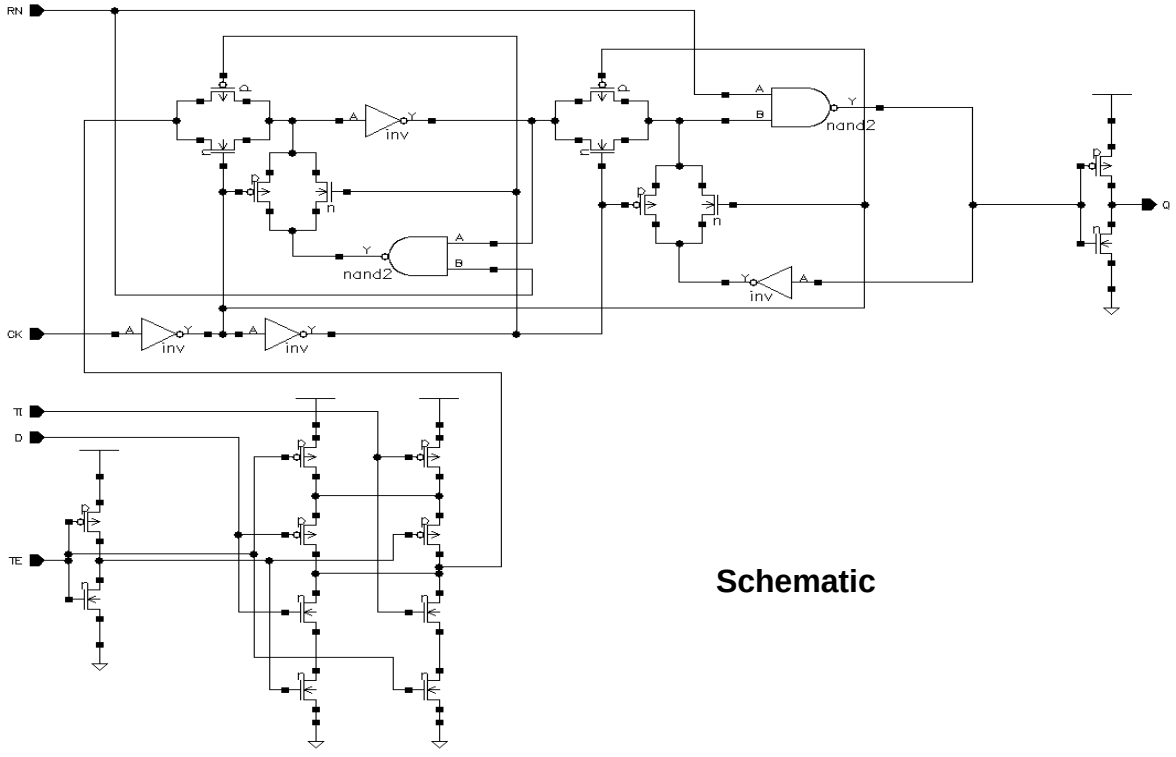
Gate Count:
- FD2SD2Q: 10
- FD2SD4Q: 11



Symbol

D	RN	TI	TE	CK	Qn+1
0	1	x	0	↑	0
1	1	x	0	↑	1
x	1	0	1	↑	0
x	1	1	1	↑	1
x	0	x	x	x	0
x	1	x	x	↓	Qn

Truth Table



Schematic

FD2SD2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.46	0.42 + 0.022*SL	0.42 + 0.019*SL	0.44 + 0.018*SL
	t_{PHL}	0.43	0.40 + 0.015*SL	0.41 + 0.010*SL	0.45 + 0.008*SL
	t_R	0.19	0.10 + 0.045*SL	0.11 + 0.041*SL	0.08 + 0.043*SL
	t_F	0.13	0.10 + 0.015*SL	0.10 + 0.016*SL	0.11 + 0.016*SL
RN to Q	t_{PHL}	0.40	0.36 + 0.018*SL	0.39 + 0.011*SL	0.44 + 0.008*SL
	t_F	0.17	0.13 + 0.020*SL	0.14 + 0.015*SL	0.13 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD2SD2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.000
Input Hold Time (TE to CK)	t_{HD}	0.000
Input Hold Time (TI to CK)	t_{HD}	0.000
Input Setup Time (D to CK)	t_{SU}	0.506
Input Setup Time (TE to CK)	t_{SU}	0.616
Input Setup Time (TI to CK)	t_{SU}	0.561
Recovery Time (RN)	t_{RC}	0.139

FD2SD4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

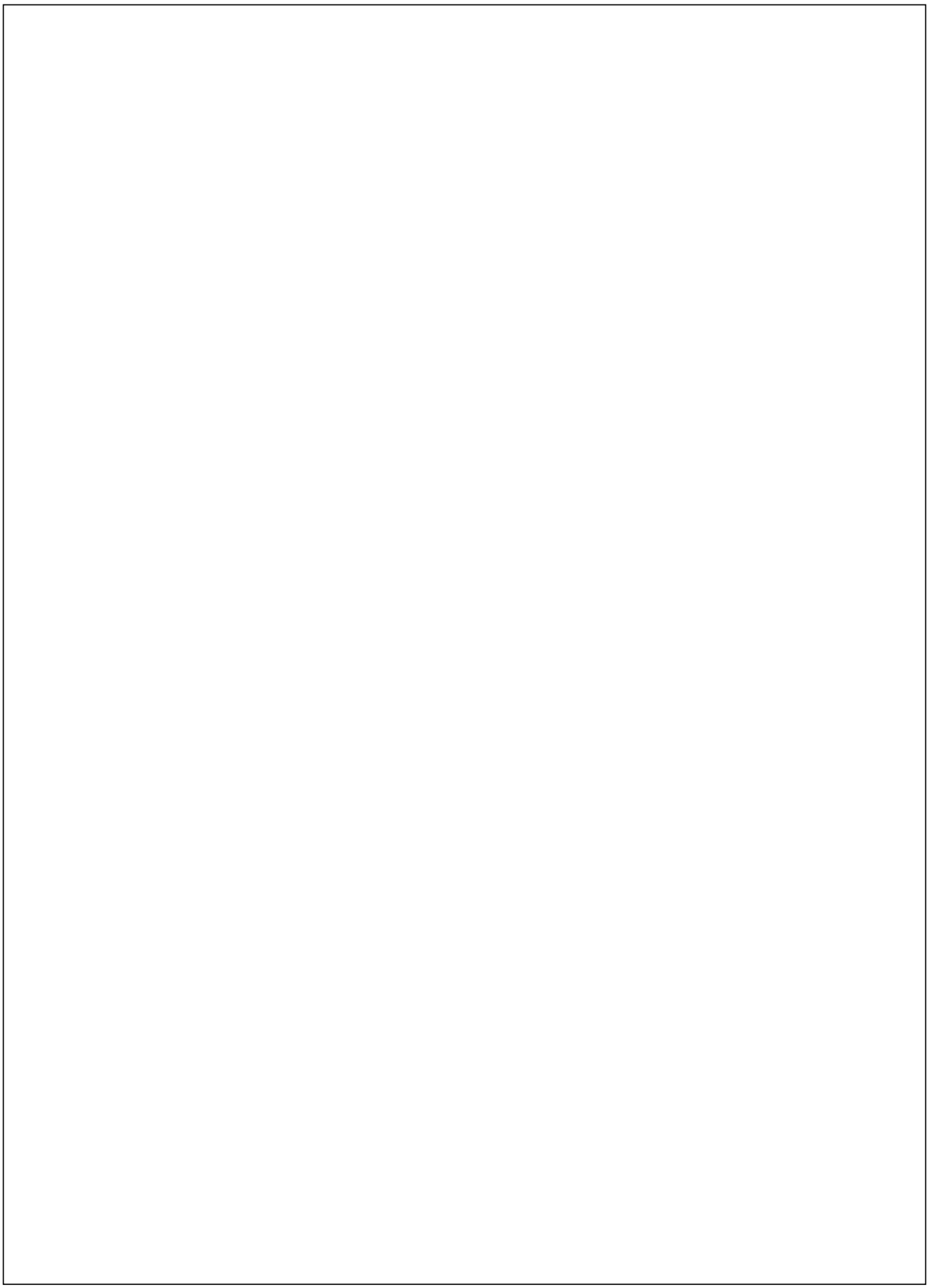
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.51	0.49 + 0.009*SL	0.49 + 0.011*SL	0.51 + 0.009*SL
	tPHL	0.47	0.45 + 0.010*SL	0.46 + 0.007*SL	0.50 + 0.005*SL
	tR	0.18	0.15 + 0.016*SL	0.13 + 0.020*SL	0.12 + 0.021*SL
	tF	0.15	0.12 + 0.010*SL	0.13 + 0.009*SL	0.15 + 0.008*SL
RN to Q	tPHL	0.45	0.43 + 0.011*SL	0.44 + 0.007*SL	0.49 + 0.005*SL
	tF	0.18	0.16 + 0.010*SL	0.17 + 0.007*SL	0.17 + 0.007*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD2SD4Q Timing Requirements

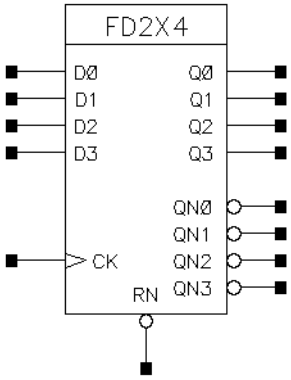
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.506
Input Setup Time (TE to CK)	tSU	0.616
Input Setup Time (TI to CK)	tSU	0.561
Recovery Time (RN)	tRC	0.139



Inputs: D0, D1, D2, D3, CK, RN
Outputs: Q0, Q1, Q2, Q3
QN0, QN1, QN2, QN3
Input Loading (SL):
- D0, D1, D2, D3: 3
- CK: 1
- RN: 8

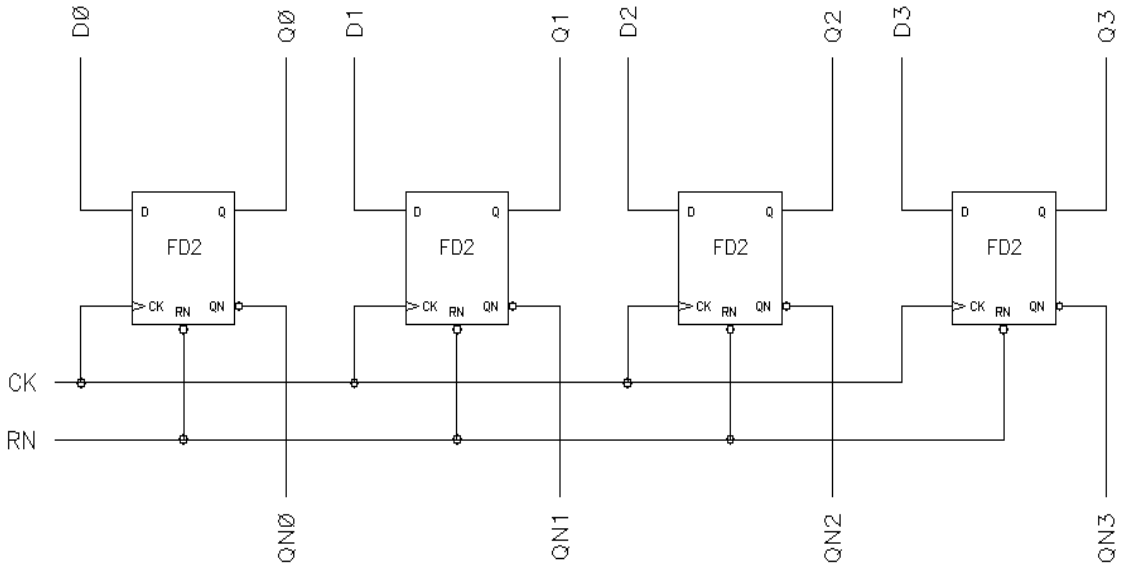
Maximum Fanout (Rec. SL): All : 28
Gate Count: 25



Symbol

D	RN	CK	Qn+1	QNn+1
0	1	↑	0	1
1	1	↑	1	0
x	0	x	0	1
x	1	↓	Qn	QNn

Truth Table



Schematic

FD2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q0	tPHL	0.37	0.32 + 0.025*SL	0.34 + 0.017*SL	0.37 + 0.016*SL
	tF	0.16	0.10 + 0.032*SL	0.11 + 0.030*SL	0.06 + 0.032*SL
CK to Q0	tPLH	0.90	0.83 + 0.037*SL	0.83 + 0.036*SL	0.83 + 0.036*SL
	tPHL	0.64	0.59 + 0.022*SL	0.61 + 0.017*SL	0.62 + 0.016*SL
	tR	0.25	0.08 + 0.083*SL	0.08 + 0.083*SL	0.05 + 0.085*SL
	tF	0.13	0.07 + 0.030*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
RN to Q1	tPHL	0.37	0.32 + 0.026*SL	0.34 + 0.018*SL	0.37 + 0.017*SL
	tF	0.17	0.10 + 0.034*SL	0.11 + 0.032*SL	0.06 + 0.034*SL
CK to Q1	tPLH	0.91	0.83 + 0.037*SL	0.83 + 0.037*SL	0.82 + 0.038*SL
	tPHL	0.63	0.59 + 0.022*SL	0.60 + 0.017*SL	0.62 + 0.017*SL
	tR	0.26	0.10 + 0.083*SL	0.08 + 0.087*SL	0.05 + 0.089*SL
	tF	0.14	0.07 + 0.032*SL	0.07 + 0.033*SL	0.04 + 0.034*SL
RN to Q2	tPHL	0.37	0.32 + 0.026*SL	0.34 + 0.018*SL	0.37 + 0.017*SL
	tF	0.17	0.10 + 0.034*SL	0.11 + 0.032*SL	0.06 + 0.034*SL
CK to Q2	tPLH	0.90	0.83 + 0.037*SL	0.83 + 0.037*SL	0.82 + 0.038*SL
	tPHL	0.63	0.59 + 0.022*SL	0.60 + 0.017*SL	0.62 + 0.017*SL
	tR	0.26	0.10 + 0.083*SL	0.08 + 0.087*SL	0.05 + 0.089*SL
	tF	0.14	0.07 + 0.032*SL	0.07 + 0.033*SL	0.04 + 0.034*SL
RN to Q3	tPHL	0.37	0.32 + 0.025*SL	0.34 + 0.017*SL	0.37 + 0.016*SL
	tF	0.16	0.10 + 0.032*SL	0.11 + 0.030*SL	0.06 + 0.032*SL
CK to Q3	tPLH	0.90	0.83 + 0.035*SL	0.83 + 0.036*SL	0.83 + 0.036*SL
	tPHL	0.63	0.59 + 0.022*SL	0.60 + 0.017*SL	0.62 + 0.016*SL
	tR	0.25	0.09 + 0.082*SL	0.08 + 0.083*SL	0.05 + 0.085*SL
	tF	0.13	0.07 + 0.031*SL	0.07 + 0.031*SL	0.05 + 0.032*SL
RN to QN0	tPLH	0.63	0.55 + 0.036*SL	0.55 + 0.036*SL	0.55 + 0.036*SL
	tR	0.25	0.09 + 0.079*SL	0.08 + 0.083*SL	0.05 + 0.084*SL
CK to QN0	tPLH	0.59	0.51 + 0.037*SL	0.51 + 0.036*SL	0.52 + 0.036*SL
	tPHL	0.74	0.70 + 0.023*SL	0.71 + 0.017*SL	0.74 + 0.016*SL
	tR	0.24	0.07 + 0.083*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.08 + 0.031*SL	0.08 + 0.031*SL	0.06 + 0.032*SL
RN to QN1	tPLH	0.62	0.55 + 0.037*SL	0.55 + 0.037*SL	0.54 + 0.037*SL
	tR	0.25	0.09 + 0.083*SL	0.08 + 0.087*SL	0.05 + 0.089*SL
CK to QN1	tPLH	0.59	0.51 + 0.039*SL	0.51 + 0.038*SL	0.52 + 0.038*SL
	tPHL	0.74	0.70 + 0.024*SL	0.71 + 0.018*SL	0.74 + 0.017*SL
	tR	0.25	0.07 + 0.086*SL	0.07 + 0.088*SL	0.05 + 0.088*SL
	tF	0.14	0.08 + 0.032*SL	0.08 + 0.033*SL	0.07 + 0.033*SL
RN to QN2	tPLH	0.62	0.55 + 0.037*SL	0.55 + 0.037*SL	0.54 + 0.037*SL
	tR	0.25	0.09 + 0.083*SL	0.08 + 0.087*SL	0.05 + 0.089*SL
CK to QN2	tPLH	0.58	0.51 + 0.039*SL	0.51 + 0.038*SL	0.51 + 0.038*SL
	tPHL	0.74	0.70 + 0.023*SL	0.71 + 0.018*SL	0.74 + 0.017*SL
	tR	0.25	0.07 + 0.086*SL	0.07 + 0.088*SL	0.05 + 0.088*SL
	tF	0.14	0.08 + 0.032*SL	0.08 + 0.033*SL	0.07 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

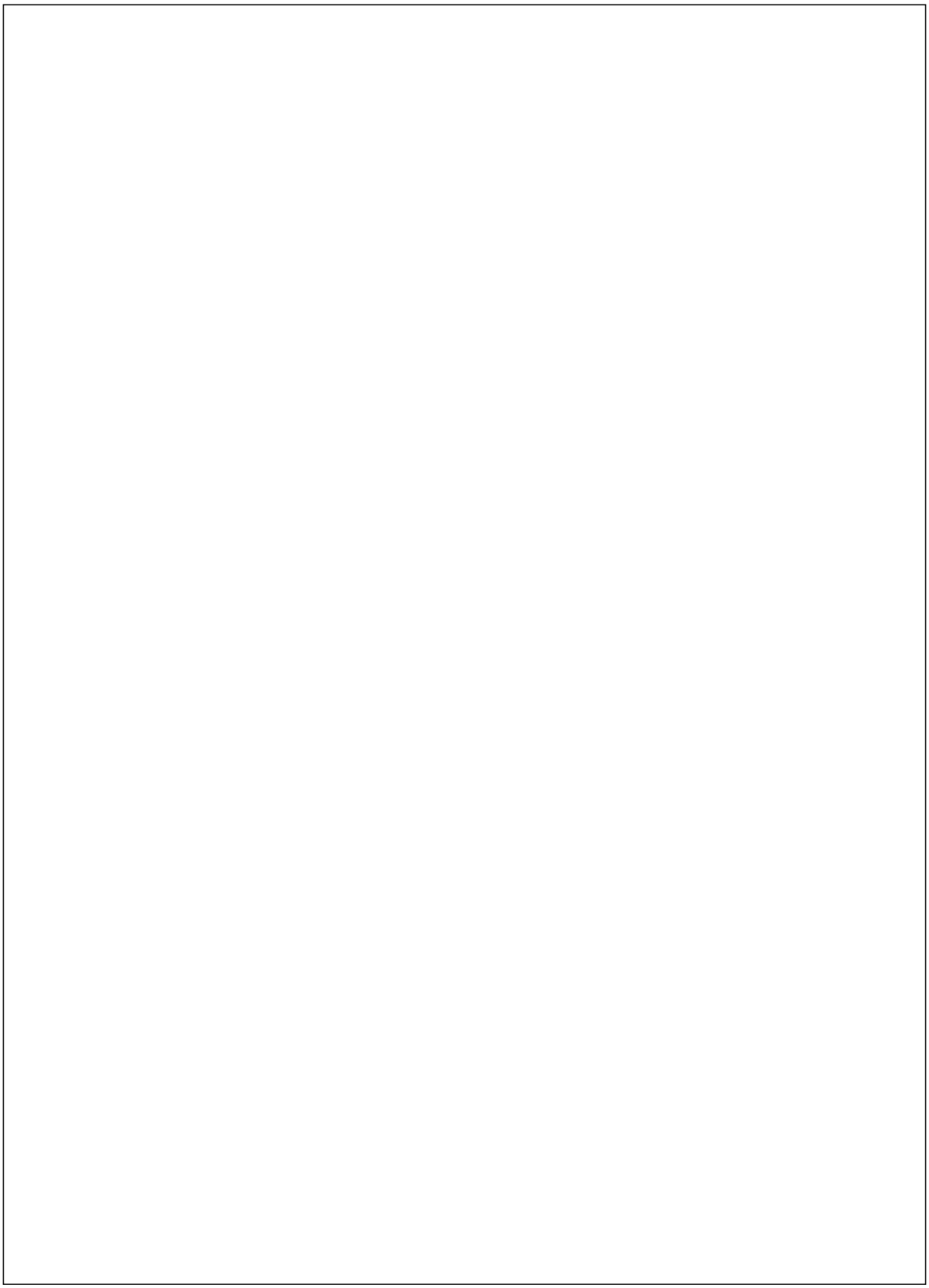
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to QN3	t_{PLH}	0.62	0.55 + 0.036*SL	0.55 + 0.036*SL	0.55 + 0.036*SL
	t_R	0.25	0.09 + 0.079*SL	0.08 + 0.083*SL	0.05 + 0.084*SL
CK to QN3	t_{PLH}	0.58	0.51 + 0.038*SL	0.51 + 0.037*SL	0.51 + 0.036*SL
	t_{PHL}	0.74	0.70 + 0.023*SL	0.71 + 0.017*SL	0.74 + 0.016*SL
	t_R	0.24	0.07 + 0.082*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.14	0.08 + 0.030*SL	0.08 + 0.031*SL	0.06 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD2X4 Timing Requirements

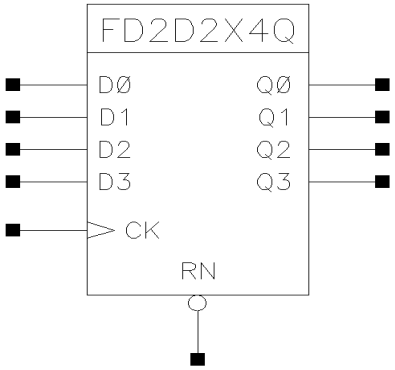
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D0 to CK)	t_{HD}	0.342
Input Hold Time (D1 to CK)	t_{HD}	0.342
Input Hold Time (D2 to CK)	t_{HD}	0.342
Input Hold Time (D3 to CK)	t_{HD}	0.342
Input Setup Time (D0 to CK)	t_{SU}	0.233
Input Setup Time (D1 to CK)	t_{SU}	0.233
Input Setup Time (D2 to CK)	t_{SU}	0.233
Input Setup Time (D3 to CK)	t_{SU}	0.233
Recovery Time (RN)	t_{RC}	0.139



Inputs: D0, D1,D2,D3, CK, RN
Output: Q
Input Loading (SL): All: D0,D1,D2,D3: 3,
CK: 1, RN: 8
Maximum Fanout (Rec. SL):
- FD2D2X4Q: 56
- FD2D4X4Q: 112

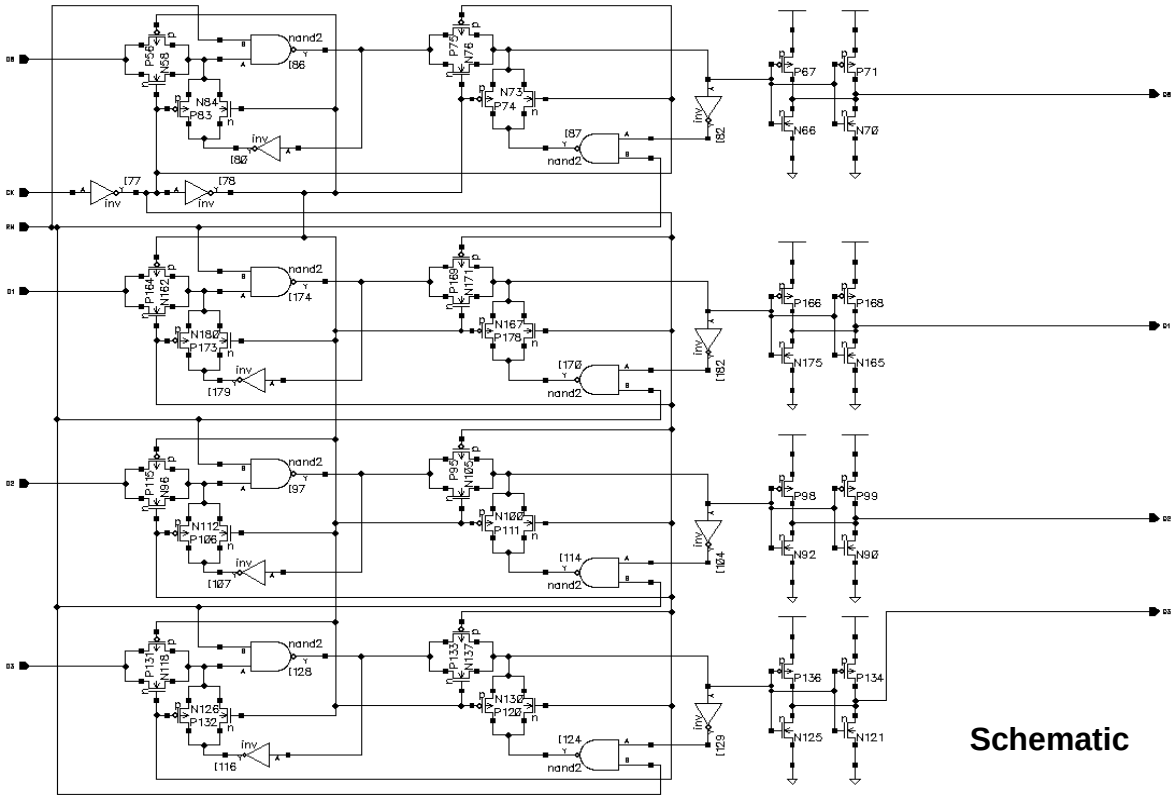
Gate Count:
- FD2D2X4Q: 25
- FD2D4X4Q: 29



Symbol

D	RN	CK	Qn+1
0	1	↑	0
1	1	↑	1
x	0	x	0
x	1	↓	Qn

Truth Table



Schematic

FD2D2X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q0	t_{PHL}	0.54	0.49 + 0.023*SL	0.52 + 0.013*SL	0.60 + 0.009*SL
	t_F	0.23	0.19 + 0.017*SL	0.20 + 0.016*SL	0.21 + 0.015*SL
CK to Q0	t_{PLH}	0.74	0.69 + 0.025*SL	0.70 + 0.020*SL	0.73 + 0.019*SL
	t_{PHL}	0.55	0.51 + 0.021*SL	0.53 + 0.013*SL	0.60 + 0.010*SL
	t_R	0.23	0.14 + 0.043*SL	0.14 + 0.042*SL	0.13 + 0.043*SL
	t_F	0.19	0.15 + 0.023*SL	0.16 + 0.017*SL	0.19 + 0.016*SL
RN to Q1	t_{PHL}	0.54	0.49 + 0.024*SL	0.52 + 0.014*SL	0.60 + 0.010*SL
	t_F	0.23	0.20 + 0.018*SL	0.20 + 0.017*SL	0.21 + 0.016*SL
CK to Q1	t_{PLH}	0.73	0.68 + 0.025*SL	0.70 + 0.020*SL	0.73 + 0.019*SL
	t_{PHL}	0.54	0.50 + 0.021*SL	0.53 + 0.013*SL	0.60 + 0.010*SL
	t_R	0.23	0.14 + 0.045*SL	0.14 + 0.043*SL	0.13 + 0.044*SL
	t_F	0.20	0.15 + 0.023*SL	0.17 + 0.018*SL	0.19 + 0.017*SL
RN to Q2	t_{PHL}	0.54	0.49 + 0.024*SL	0.52 + 0.014*SL	0.60 + 0.010*SL
	t_F	0.23	0.20 + 0.018*SL	0.20 + 0.017*SL	0.21 + 0.016*SL
CK to Q2	t_{PLH}	0.73	0.68 + 0.025*SL	0.70 + 0.020*SL	0.73 + 0.019*SL
	t_{PHL}	0.55	0.50 + 0.021*SL	0.53 + 0.013*SL	0.60 + 0.010*SL
	t_R	0.23	0.14 + 0.045*SL	0.14 + 0.043*SL	0.13 + 0.044*SL
	t_F	0.20	0.15 + 0.023*SL	0.17 + 0.018*SL	0.19 + 0.017*SL
RN to Q3	t_{PHL}	0.54	0.49 + 0.023*SL	0.52 + 0.013*SL	0.60 + 0.009*SL
	t_F	0.23	0.19 + 0.017*SL	0.20 + 0.016*SL	0.21 + 0.015*SL
CK to Q3	t_{PLH}	0.74	0.69 + 0.025*SL	0.70 + 0.020*SL	0.73 + 0.019*SL
	t_{PHL}	0.55	0.51 + 0.021*SL	0.53 + 0.013*SL	0.60 + 0.010*SL
	t_R	0.22	0.14 + 0.044*SL	0.14 + 0.042*SL	0.13 + 0.042*SL
	t_F	0.19	0.15 + 0.024*SL	0.17 + 0.017*SL	0.19 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD2D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D0 to CK)	t_{HD}	0.397
Input Hold Time (D1 to CK)	t_{HD}	0.397
Input Hold Time (D2 to CK)	t_{HD}	0.397

FD2D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Input Hold Time (D3 to CK)	t_{HD}	0.397
Input Setup Time (D0 to CK)	t_{SU}	0.233
Input Setup Time (D1 to CK)	t_{SU}	0.233
Input Setup Time (D2 to CK)	t_{SU}	0.233
Input Setup Time (D3 to CK)	t_{SU}	0.233
Recovery Time (RN)	t_{RC}	0.139

FD2D4X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q0	tPHL	0.59	0.56 + 0.013*SL	0.57 + 0.009*SL	0.63 + 0.006*SL
	tF	0.23	0.21 + 0.014*SL	0.22 + 0.009*SL	0.26 + 0.008*SL
CK to Q0	tPLH	0.80	0.77 + 0.014*SL	0.78 + 0.011*SL	0.81 + 0.010*SL
	tPHL	0.64	0.60 + 0.016*SL	0.63 + 0.009*SL	0.68 + 0.006*SL
	tR	0.22	0.19 + 0.017*SL	0.18 + 0.021*SL	0.18 + 0.021*SL
	tF	0.23	0.21 + 0.014*SL	0.22 + 0.010*SL	0.24 + 0.008*SL
RN to Q1	tPHL	0.58	0.56 + 0.013*SL	0.57 + 0.009*SL	0.63 + 0.006*SL
	tF	0.24	0.21 + 0.013*SL	0.22 + 0.010*SL	0.26 + 0.008*SL
CK to Q1	tPLH	0.79	0.76 + 0.014*SL	0.77 + 0.011*SL	0.80 + 0.010*SL
	tPHL	0.63	0.60 + 0.015*SL	0.62 + 0.009*SL	0.67 + 0.006*SL
	tR	0.23	0.19 + 0.018*SL	0.18 + 0.021*SL	0.17 + 0.021*SL
	tF	0.24	0.21 + 0.014*SL	0.22 + 0.010*SL	0.25 + 0.008*SL
RN to Q2	tPHL	0.58	0.56 + 0.013*SL	0.57 + 0.009*SL	0.63 + 0.006*SL
	tF	0.24	0.21 + 0.013*SL	0.22 + 0.010*SL	0.26 + 0.008*SL
CK to Q2	tPLH	0.79	0.76 + 0.014*SL	0.77 + 0.011*SL	0.80 + 0.010*SL
	tPHL	0.63	0.60 + 0.015*SL	0.62 + 0.009*SL	0.67 + 0.006*SL
	tR	0.23	0.19 + 0.018*SL	0.18 + 0.021*SL	0.17 + 0.021*SL
	tF	0.24	0.21 + 0.014*SL	0.22 + 0.010*SL	0.26 + 0.008*SL
RN to Q3	tPHL	0.59	0.56 + 0.013*SL	0.57 + 0.009*SL	0.63 + 0.006*SL
	tF	0.23	0.21 + 0.014*SL	0.22 + 0.009*SL	0.26 + 0.008*SL
CK to Q3	tPLH	0.80	0.77 + 0.014*SL	0.78 + 0.011*SL	0.81 + 0.010*SL
	tPHL	0.64	0.61 + 0.016*SL	0.63 + 0.009*SL	0.68 + 0.006*SL
	tR	0.22	0.18 + 0.019*SL	0.18 + 0.021*SL	0.18 + 0.021*SL
	tF	0.23	0.21 + 0.014*SL	0.22 + 0.010*SL	0.24 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD2D4X4Q Timing Requirements

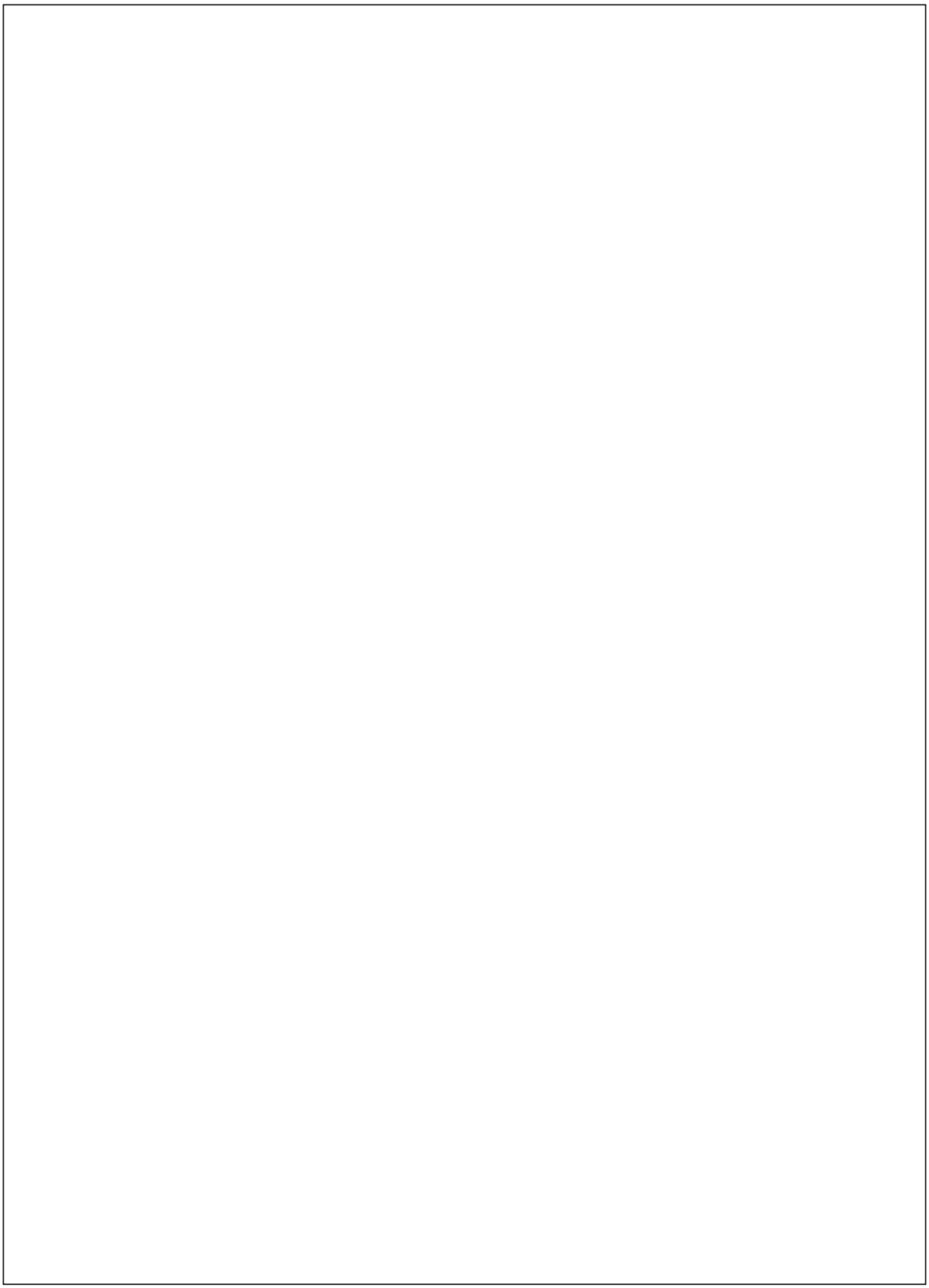
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D0 to CK)	t_{HD}	0.342
Input Hold Time (D1 to CK)	t_{HD}	0.342
Input Hold Time (D2 to CK)	t_{HD}	0.342
Input Hold Time (D3 to CK)	t_{HD}	0.342
Input Setup Time (D0 to CK)	t_{SU}	0.233

FD2D4X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

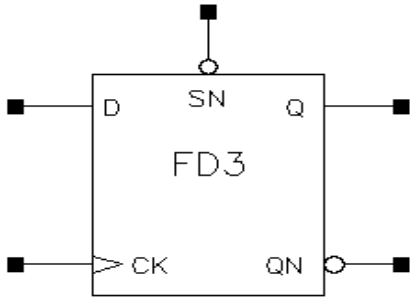
Parameter	Symbol	Value [ns]
Input Setup Time (D1 to CK)	t_{SU}	0.233
Input Setup Time (D2 to CK)	t_{SU}	0.233
Input Setup Time (D3 to CK)	t_{SU}	0.233
Recovery Time (RN)	t_{RC}	0.139



Inputs: D, CK, SN
Outputs: Q, QN
Input Loading (SL):
- D: 3
- CK: 1
- SN: 2

Maximum Fanout (Rec. SL):
- FD3: All : 28
- FD3D2: All : 56

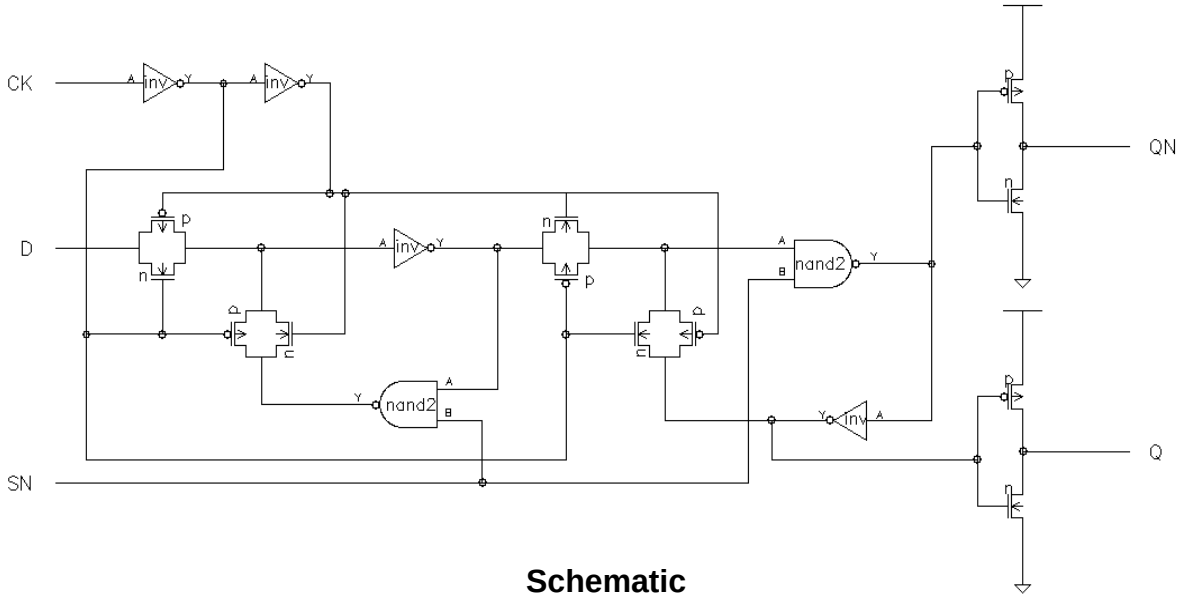
Gate Count:
- FD3: 7
- FD3D2: 8



Symbol

D	SN	CK	Qn+1	QNn+1
0	1	⎍	0	1
1	1	⎍	1	0
x	0	x	1	0
x	1	⎎	Qn	QNn

Truth Table



Schematic

FD3 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	t_{PLH}	0.50	0.43 + 0.035*SL	0.43 + 0.036*SL	0.42 + 0.036*SL
	t_R	0.23	0.07 + 0.083*SL	0.07 + 0.082*SL	0.05 + 0.083*SL
CK to Q	t_{PLH}	0.53	0.45 + 0.035*SL	0.45 + 0.036*SL	0.45 + 0.036*SL
	t_{PHL}	0.51	0.47 + 0.022*SL	0.48 + 0.017*SL	0.49 + 0.016*SL
	t_R	0.23	0.06 + 0.083*SL	0.07 + 0.083*SL	0.05 + 0.083*SL
	t_F	0.14	0.06 + 0.038*SL	0.08 + 0.032*SL	0.05 + 0.033*SL
SN to QN	t_{PHL}	0.39	0.34 + 0.028*SL	0.37 + 0.018*SL	0.40 + 0.016*SL
	t_F	0.18	0.11 + 0.035*SL	0.12 + 0.031*SL	0.08 + 0.033*SL
CK to QN	t_{PLH}	0.47	0.39 + 0.040*SL	0.40 + 0.036*SL	0.41 + 0.036*SL
	t_{PHL}	0.42	0.37 + 0.025*SL	0.39 + 0.018*SL	0.42 + 0.016*SL
	t_R	0.25	0.09 + 0.080*SL	0.09 + 0.082*SL	0.06 + 0.083*SL
	t_F	0.14	0.07 + 0.034*SL	0.07 + 0.033*SL	0.05 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD3 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.178
Input Setup Time (D to CK)	t_{SU}	0.342
Recovery Time (SN)	t_{RC}	0.139

FD3SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

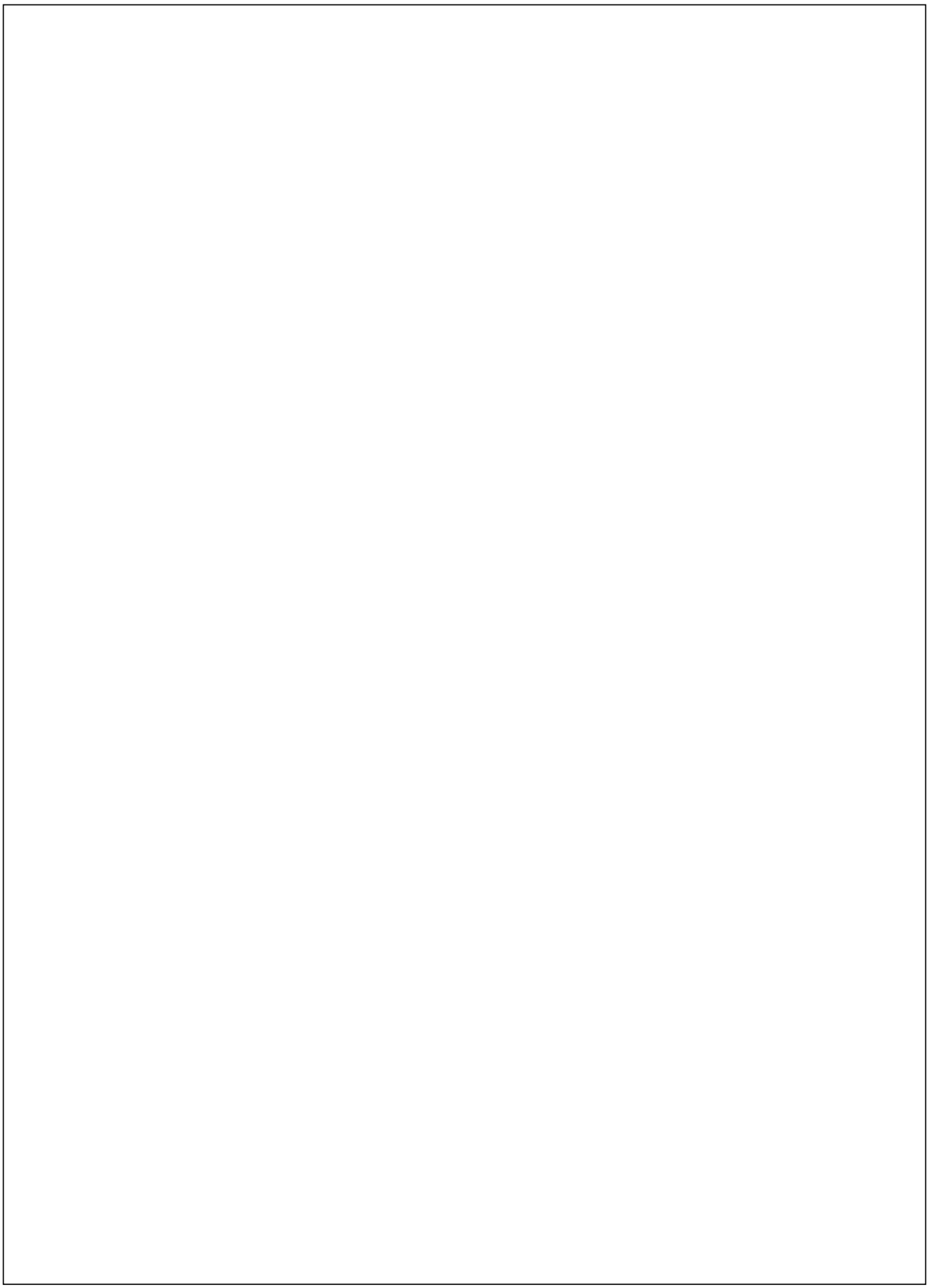
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.62	0.59 + 0.018*SL	0.59 + 0.018*SL	0.59 + 0.018*SL
	tR	0.17	0.10 + 0.034*SL	0.08 + 0.041*SL	0.06 + 0.042*SL
CK to Q	tPLH	0.40	0.36 + 0.020*SL	0.36 + 0.019*SL	0.37 + 0.018*SL
	tPHL	0.44	0.41 + 0.015*SL	0.43 + 0.010*SL	0.47 + 0.008*SL
	tR	0.16	0.08 + 0.043*SL	0.08 + 0.041*SL	0.06 + 0.042*SL
	tF	0.13	0.09 + 0.018*SL	0.10 + 0.016*SL	0.10 + 0.016*SL
SN to QN	tPHL	0.38	0.35 + 0.016*SL	0.36 + 0.010*SL	0.40 + 0.008*SL
	tF	0.16	0.12 + 0.017*SL	0.13 + 0.015*SL	0.13 + 0.015*SL
CK to QN	tPLH	0.64	0.61 + 0.017*SL	0.61 + 0.018*SL	0.60 + 0.018*SL
	tPHL	0.50	0.47 + 0.013*SL	0.48 + 0.010*SL	0.51 + 0.008*SL
	tR	0.18	0.12 + 0.032*SL	0.09 + 0.042*SL	0.07 + 0.043*SL
	tF	0.12	0.08 + 0.017*SL	0.09 + 0.015*SL	0.08 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD3SD2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

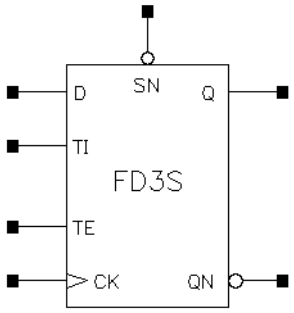
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.616
Input Setup Time (TE to CK)	tSU	0.725
Input Setup Time (TI to CK)	tSU	0.616
Recovery Time (SN)	tRC	0.139



Inputs: D, TI, TE, CK, SN
Outputs: Q, QN
Input Loading (SL):
- D, TI, CK: 1
- TE, SN: 2

Maximum Fanout (Rec. SL):
- FD3S: All : 28
- FD3SD2: All : 56

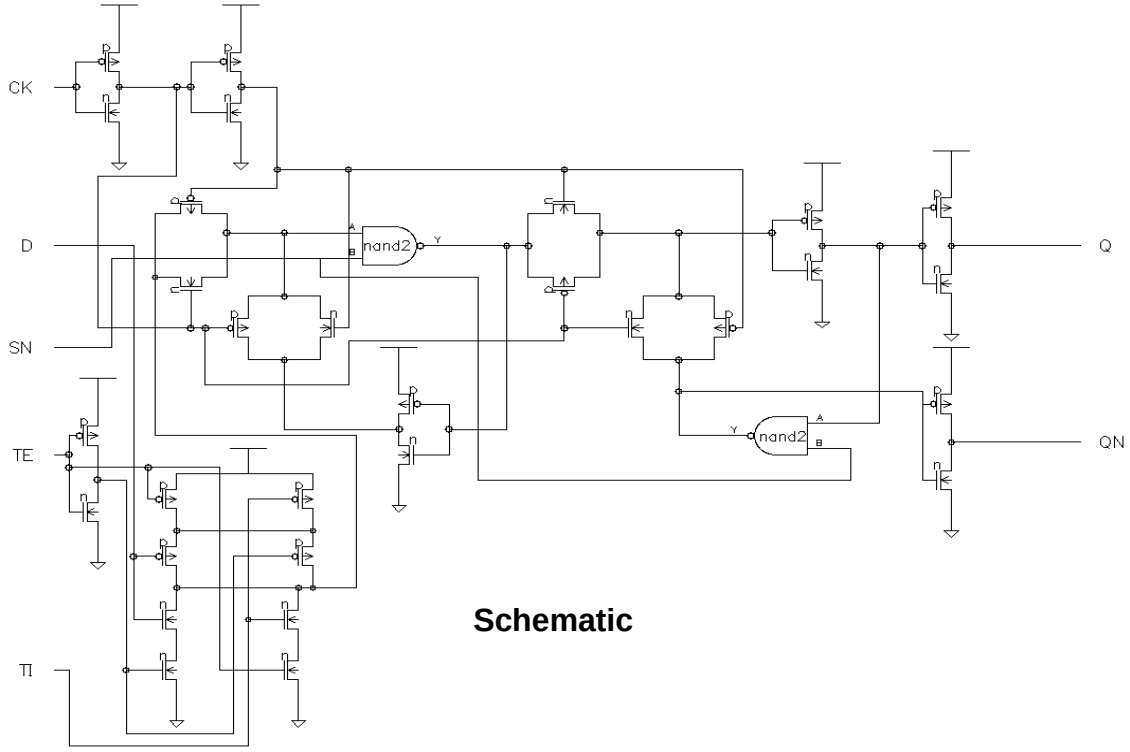
Gate Count:
- FD3S: 10
- FD3SD2: 11



Symbol

D	SN	TI	TE	CK	Qn+1	QNn+1
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	1	0	1	↑	0	1
x	1	1	1	↑	1	0
x	0	x	x	x	1	0
x	1	x	x	↓	Qn	QNn

Truth Table



Schematic

FD3S Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	t_{PLH}	0.63	0.56 + 0.035*SL	0.55 + 0.037*SL	0.56 + 0.036*SL
	t_R	0.24	0.09 + 0.077*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
CK to Q	t_{PLH}	0.42	0.34 + 0.038*SL	0.34 + 0.036*SL	0.35 + 0.036*SL
	t_{PHL}	0.44	0.39 + 0.022*SL	0.41 + 0.017*SL	0.44 + 0.016*SL
	t_R	0.24	0.08 + 0.082*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.14	0.09 + 0.025*SL	0.07 + 0.031*SL	0.06 + 0.032*SL
SN to QN	t_{PHL}	0.37	0.32 + 0.025*SL	0.34 + 0.017*SL	0.37 + 0.016*SL
	t_F	0.17	0.10 + 0.034*SL	0.11 + 0.030*SL	0.06 + 0.032*SL
CK to QN	t_{PLH}	0.60	0.53 + 0.036*SL	0.53 + 0.036*SL	0.52 + 0.036*SL
	t_{PHL}	0.47	0.42 + 0.022*SL	0.44 + 0.017*SL	0.45 + 0.016*SL
	t_R	0.25	0.10 + 0.079*SL	0.08 + 0.083*SL	0.05 + 0.085*SL
	t_F	0.13	0.06 + 0.034*SL	0.07 + 0.031*SL	0.05 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD3S Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.000
Input Hold Time (TE to CK)	t_{HD}	0.000
Input Hold Time (TI to CK)	t_{HD}	0.000
Input Setup Time (D to CK)	t_{SU}	0.616
Input Setup Time (TE to CK)	t_{SU}	0.725
Input Setup Time (TI to CK)	t_{SU}	0.616
Recovery Time (SN)	t_{RC}	0.139

FD3SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

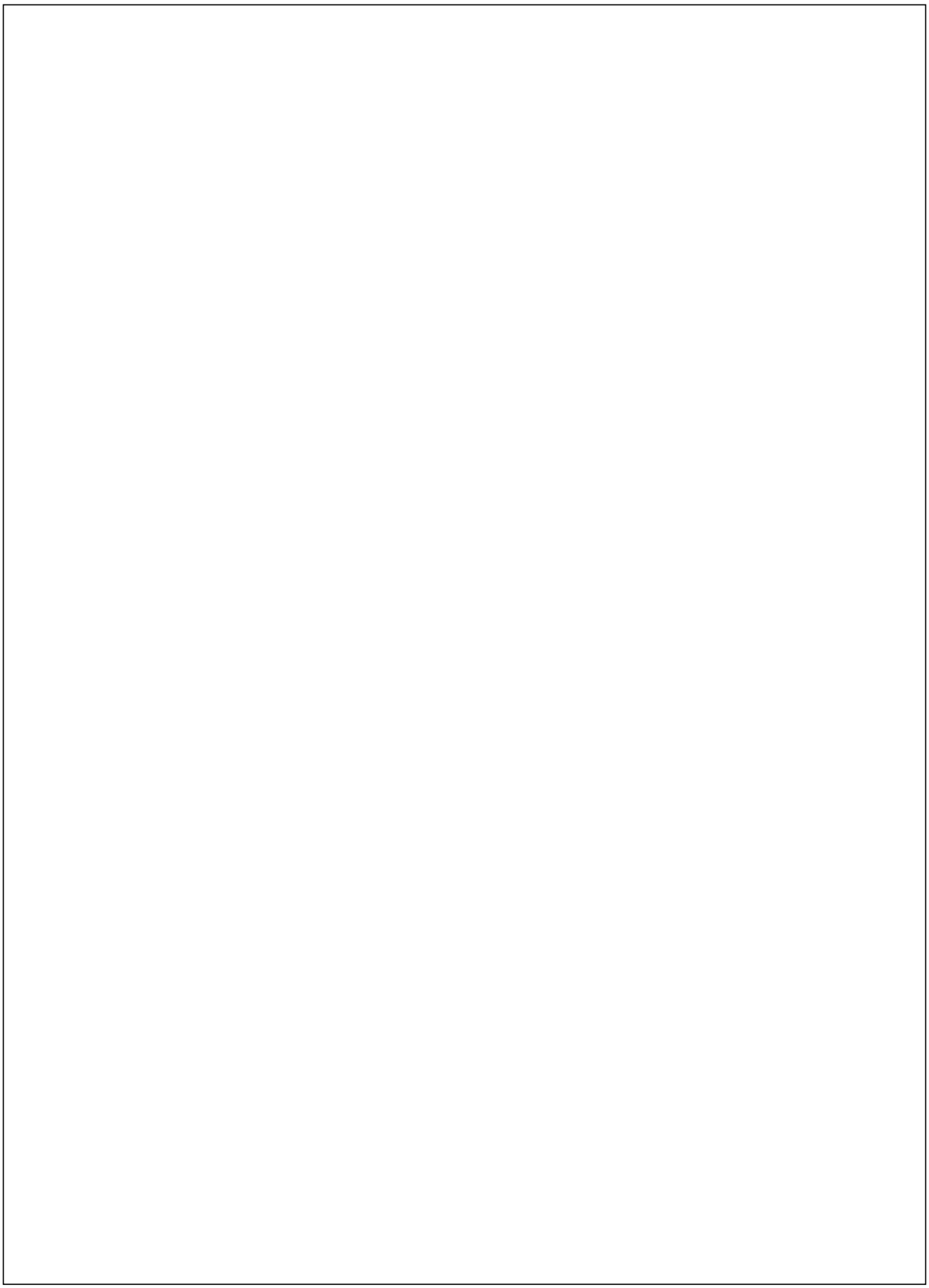
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	t_{PLH}	0.62	0.59 + 0.018*SL	0.59 + 0.018*SL	0.59 + 0.018*SL
	t_R	0.17	0.10 + 0.034*SL	0.08 + 0.041*SL	0.06 + 0.042*SL
CK to Q	t_{PLH}	0.40	0.36 + 0.020*SL	0.36 + 0.019*SL	0.37 + 0.018*SL
	t_{PHL}	0.44	0.41 + 0.015*SL	0.43 + 0.010*SL	0.47 + 0.008*SL
	t_R	0.16	0.08 + 0.043*SL	0.08 + 0.041*SL	0.06 + 0.042*SL
	t_F	0.13	0.09 + 0.018*SL	0.10 + 0.016*SL	0.10 + 0.016*SL
SN to QN	t_{PHL}	0.38	0.35 + 0.016*SL	0.36 + 0.010*SL	0.40 + 0.008*SL
	t_F	0.16	0.12 + 0.017*SL	0.13 + 0.015*SL	0.13 + 0.015*SL
CK to QN	t_{PLH}	0.64	0.61 + 0.017*SL	0.61 + 0.018*SL	0.60 + 0.018*SL
	t_{PHL}	0.50	0.47 + 0.013*SL	0.48 + 0.010*SL	0.51 + 0.008*SL
	t_R	0.18	0.12 + 0.032*SL	0.09 + 0.042*SL	0.07 + 0.043*SL
	t_F	0.12	0.08 + 0.017*SL	0.09 + 0.015*SL	0.08 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD3SD2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

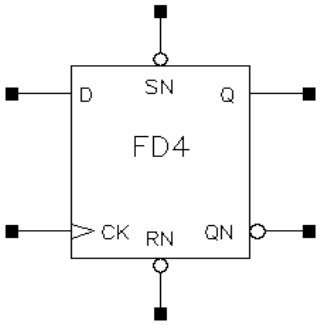
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.000
Input Hold Time (TE to CK)	t_{HD}	0.000
Input Hold Time (TI to CK)	t_{HD}	0.000
Input Setup Time (D to CK)	t_{SU}	0.616
Input Setup Time (TE to CK)	t_{SU}	0.725
Input Setup Time (TI to CK)	t_{SU}	0.616
Recovery Time (SN)	t_{RC}	0.139



Inputs: D, CK, SN, RN
Outputs: Q, QN
Input Loading (SL):
- D: 3
- CK: 1
- SN, RN: 2

Maximum Fanout (Rec. SL):
- FD4: All : 28
- FD4D2: All : 56

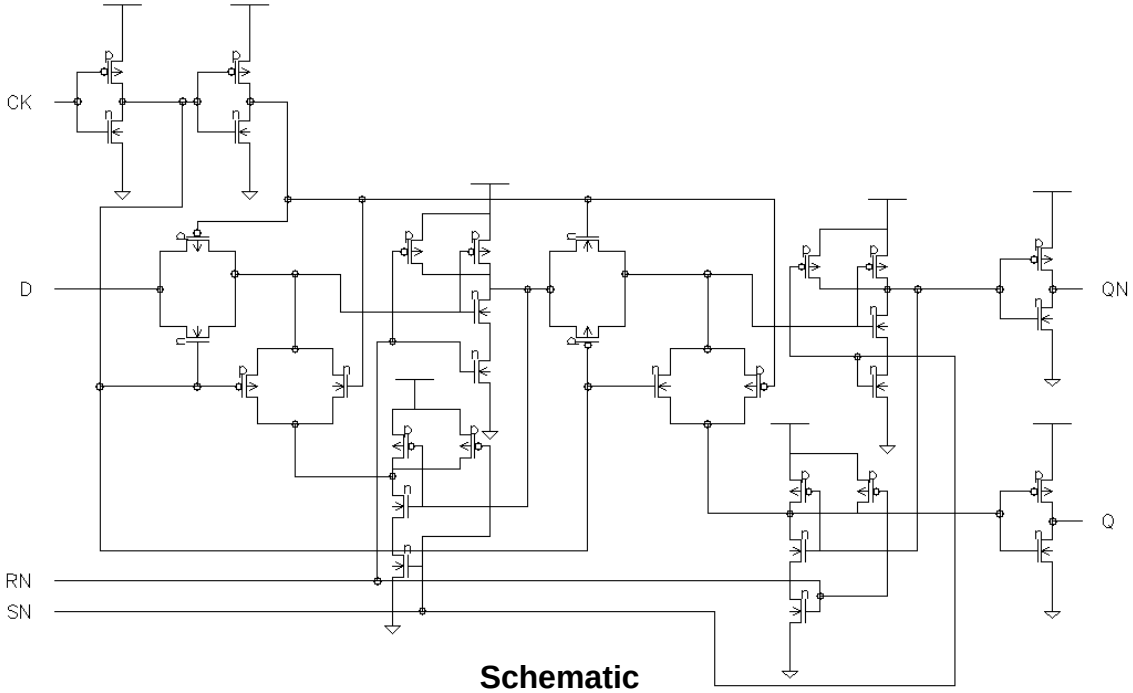
Gate Count:
- FD4: 8
- FD4D2: 9



Symbol

D	SN	RN	CK	Qn+1	QNn+1
0	1	1	↑	0	1
1	1	1	↑	1	0
x	0	1	x	1	0
x	1	0	x	0	1
x	0	0	x	0	0
x	1	1	↓	Qn	QNn

Truth Table



Schematic

FD4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.61	0.54 + 0.038*SL	0.54 + 0.037*SL	0.54 + 0.037*SL
	t_{PHL}	0.52	0.47 + 0.023*SL	0.49 + 0.017*SL	0.51 + 0.016*SL
	t_R	0.26	0.09 + 0.083*SL	0.08 + 0.085*SL	0.06 + 0.087*SL
	t_F	0.15	0.07 + 0.037*SL	0.09 + 0.030*SL	0.05 + 0.032*SL
RN to Q	t_{PLH}	0.22	0.13 + 0.042*SL	0.15 + 0.037*SL	0.15 + 0.037*SL
	t_{PHL}	0.37	0.32 + 0.027*SL	0.35 + 0.017*SL	0.37 + 0.016*SL
	t_R	0.27	0.11 + 0.082*SL	0.10 + 0.084*SL	0.06 + 0.086*SL
	t_F	0.17	0.10 + 0.033*SL	0.11 + 0.030*SL	0.07 + 0.032*SL
SN to Q	t_{PLH}	0.56	0.49 + 0.035*SL	0.48 + 0.037*SL	0.49 + 0.037*SL
	t_R	0.26	0.10 + 0.081*SL	0.08 + 0.085*SL	0.06 + 0.087*SL
CK to QN	t_{PLH}	0.47	0.39 + 0.042*SL	0.40 + 0.038*SL	0.41 + 0.038*SL
	t_{PHL}	0.45	0.40 + 0.023*SL	0.42 + 0.018*SL	0.45 + 0.016*SL
	t_R	0.26	0.10 + 0.084*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
	t_F	0.14	0.08 + 0.031*SL	0.08 + 0.031*SL	0.06 + 0.032*SL
RN to QN	t_{PLH}	0.68	0.60 + 0.040*SL	0.61 + 0.037*SL	0.61 + 0.038*SL
	t_R	0.27	0.11 + 0.078*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
SN to QN	t_{PLH}	0.22	0.14 + 0.042*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
	t_{PHL}	0.39	0.33 + 0.025*SL	0.36 + 0.018*SL	0.40 + 0.016*SL
	t_R	0.28	0.11 + 0.084*SL	0.11 + 0.086*SL	0.06 + 0.088*SL
	t_F	0.18	0.11 + 0.035*SL	0.12 + 0.030*SL	0.08 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD4 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.178
Input Setup Time (D to CK)	t_{SU}	0.342
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139

FD4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

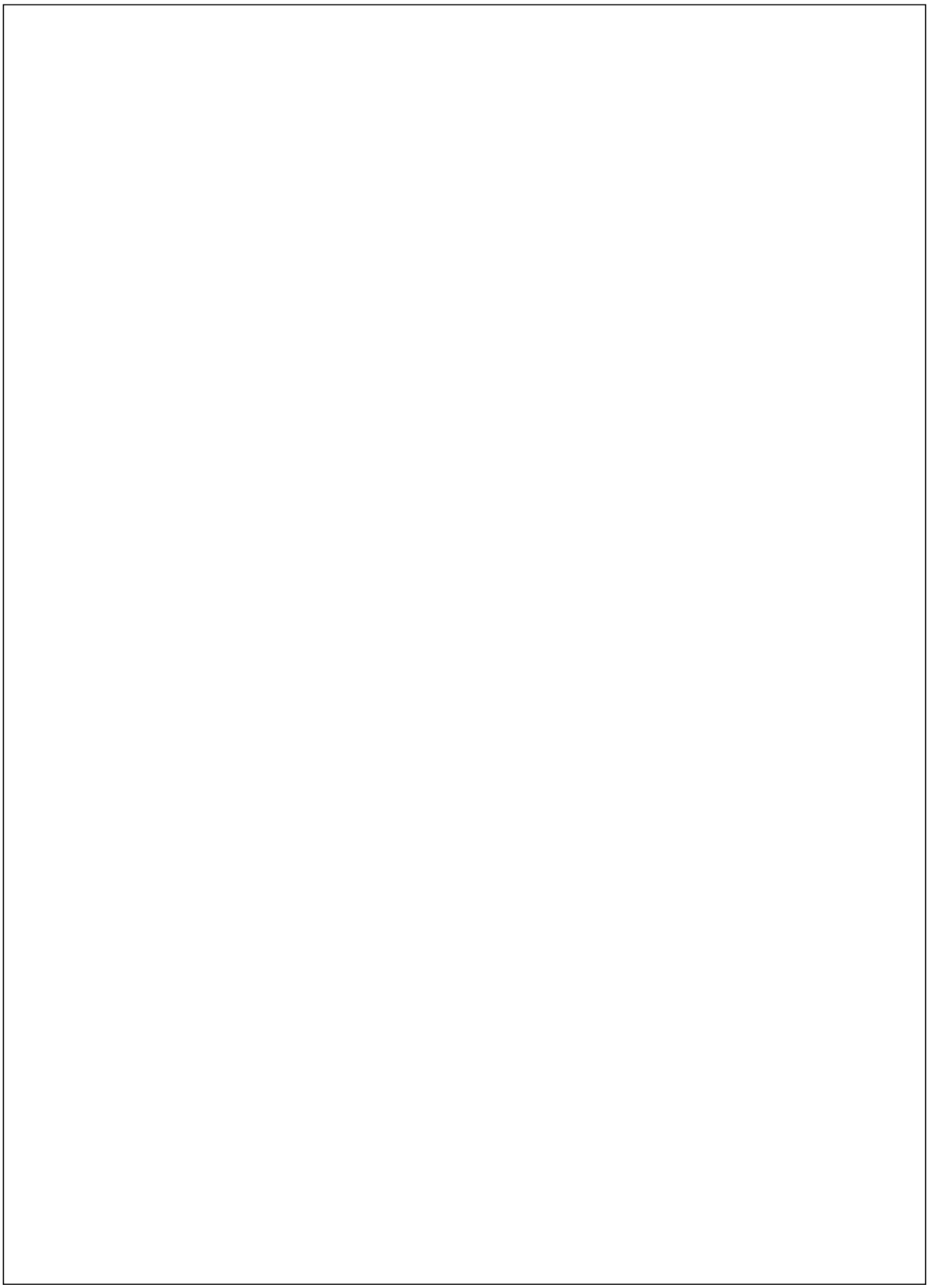
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.66	0.62 + 0.019*SL	0.62 + 0.018*SL	0.62 + 0.018*SL
	tPHL	0.57	0.54 + 0.016*SL	0.56 + 0.010*SL	0.58 + 0.008*SL
	tR	0.18	0.11 + 0.035*SL	0.09 + 0.041*SL	0.07 + 0.042*SL
	tF	0.13	0.08 + 0.026*SL	0.11 + 0.016*SL	0.09 + 0.017*SL
RN to Q	tPLH	0.21	0.17 + 0.022*SL	0.18 + 0.019*SL	0.19 + 0.018*SL
	tPHL	0.38	0.35 + 0.016*SL	0.37 + 0.010*SL	0.41 + 0.009*SL
	tR	0.20	0.13 + 0.033*SL	0.11 + 0.040*SL	0.09 + 0.042*SL
	tF	0.16	0.12 + 0.017*SL	0.13 + 0.016*SL	0.12 + 0.016*SL
SN to Q	tPLH	0.61	0.57 + 0.017*SL	0.57 + 0.018*SL	0.57 + 0.018*SL
	tR	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.07 + 0.042*SL
CK to QN	tPLH	0.46	0.42 + 0.022*SL	0.43 + 0.019*SL	0.44 + 0.018*SL
	tPHL	0.46	0.42 + 0.019*SL	0.45 + 0.010*SL	0.48 + 0.009*SL
	tR	0.18	0.10 + 0.040*SL	0.09 + 0.041*SL	0.08 + 0.042*SL
	tF	0.13	0.09 + 0.019*SL	0.10 + 0.016*SL	0.12 + 0.015*SL
RN to QN	tPLH	0.68	0.64 + 0.023*SL	0.65 + 0.019*SL	0.66 + 0.018*SL
	tR	0.19	0.11 + 0.038*SL	0.10 + 0.040*SL	0.08 + 0.042*SL
SN to QN	tPLH	0.22	0.18 + 0.020*SL	0.18 + 0.019*SL	0.20 + 0.018*SL
	tPHL	0.40	0.36 + 0.017*SL	0.38 + 0.011*SL	0.42 + 0.008*SL
	tR	0.20	0.13 + 0.034*SL	0.11 + 0.040*SL	0.09 + 0.041*SL
	tF	0.16	0.13 + 0.016*SL	0.13 + 0.015*SL	0.13 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD4D2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

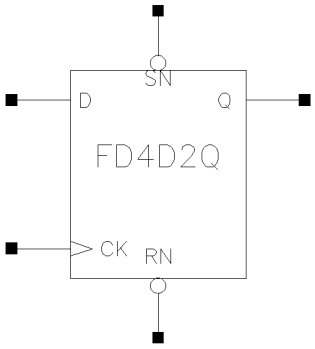
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.178
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



Inputs: D, CK, RN, SN
Output: Q
Input Loading (SL):
- FD4D2Q: CK: 1, RN, SN: 2
  D: 3
- FD4D4Q: CK: 1, RN, SN: 2
  D: 3

Maximum Fanout (Rec. SL):
- FD4D2Q: 56
- FD4D4Q: 112

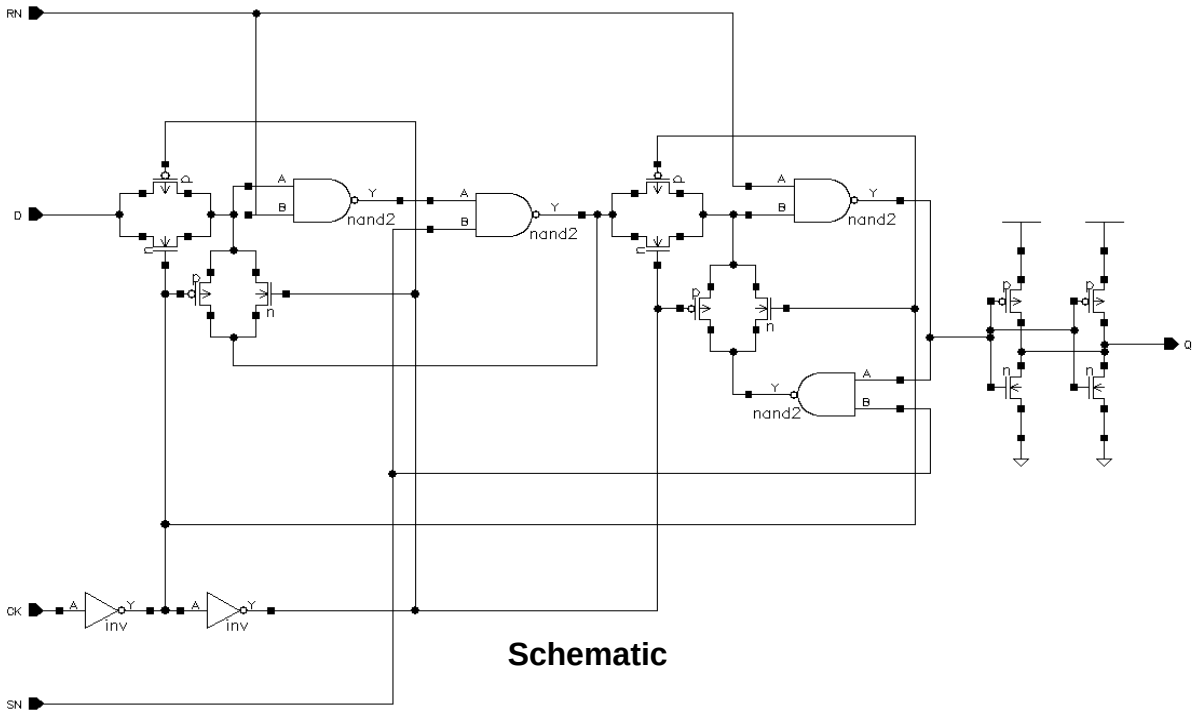
Gate Count:
- FD4D2Q: 8
- FD4D4Q: 9



Symbol

D	SN	RN	CK	Qn+1
0	1	1	↑	0
1	1	1	↑	1
x	0	1	x	1
x	1	0	x	0
x	0	0	x	0
x	1	1	↓	Qn

Truth Table



Schematic

FD4D2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.42	0.37 + 0.025*SL	0.38 + 0.020*SL	0.42 + 0.019*SL
	t_{PHL}	0.32	0.28 + 0.020*SL	0.30 + 0.013*SL	0.37 + 0.010*SL
	t_R	0.21	0.12 + 0.045*SL	0.13 + 0.042*SL	0.12 + 0.043*SL
	t_F	0.15	0.11 + 0.021*SL	0.11 + 0.019*SL	0.17 + 0.016*SL
RN to Q	t_{PLH}	0.38	0.33 + 0.024*SL	0.35 + 0.020*SL	0.37 + 0.019*SL
	t_{PHL}	0.53	0.49 + 0.021*SL	0.51 + 0.014*SL	0.59 + 0.010*SL
	t_R	0.25	0.18 + 0.037*SL	0.16 + 0.040*SL	0.12 + 0.043*SL
	t_F	0.21	0.17 + 0.022*SL	0.19 + 0.017*SL	0.22 + 0.015*SL
SN to Q	t_{PLH}	0.81	0.76 + 0.025*SL	0.78 + 0.020*SL	0.80 + 0.019*SL
	t_R	0.23	0.14 + 0.042*SL	0.15 + 0.041*SL	0.12 + 0.042*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD4D2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.178
Input Setup Time (D to CK)	t_{SU}	0.342
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139

FD4D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

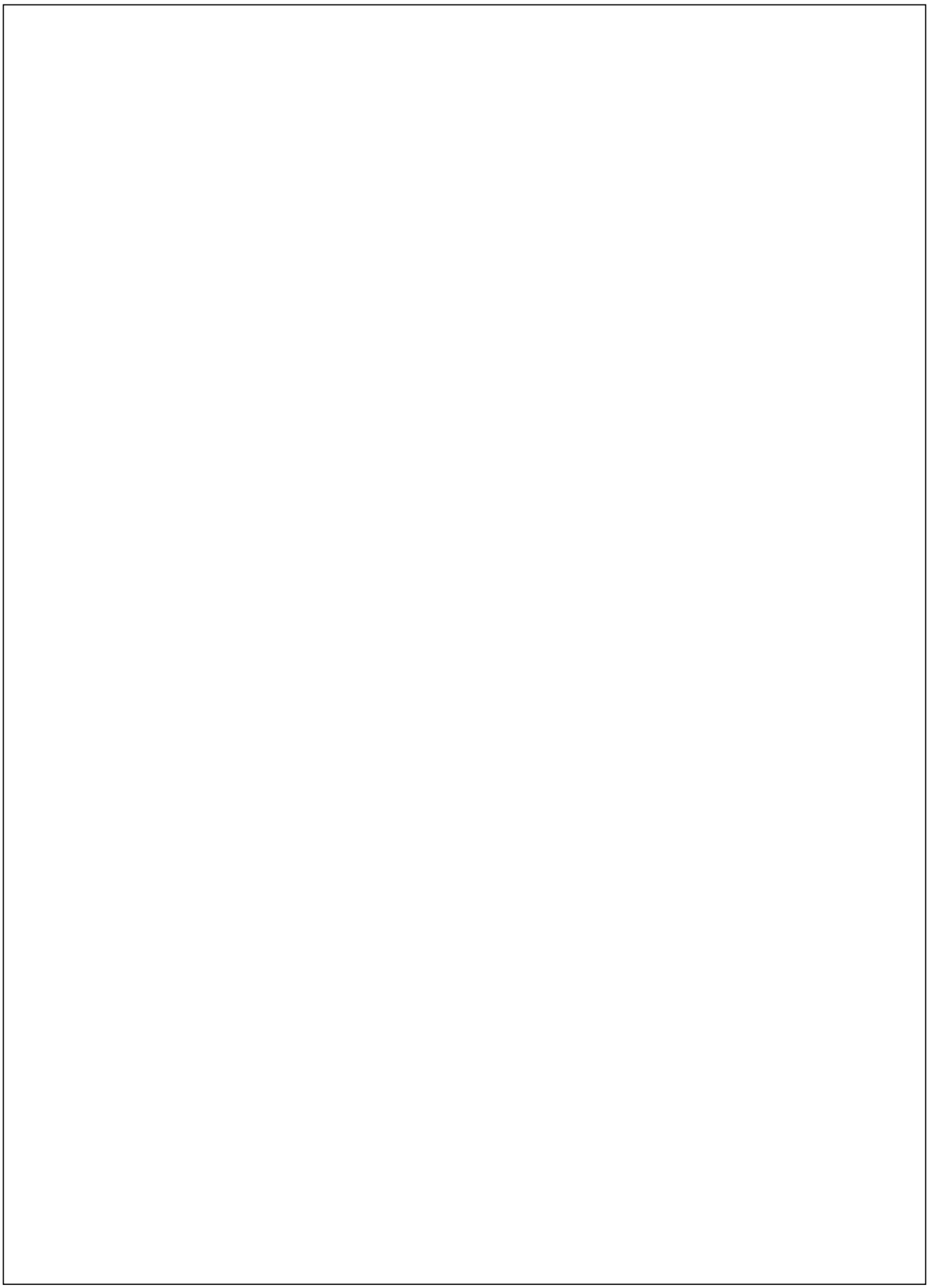
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.47	0.44 + 0.014*SL	0.45 + 0.011*SL	0.48 + 0.010*SL
	tPHL	0.35	0.33 + 0.014*SL	0.34 + 0.009*SL	0.39 + 0.006*SL
	tR	0.22	0.18 + 0.017*SL	0.17 + 0.021*SL	0.17 + 0.021*SL
	tF	0.17	0.13 + 0.016*SL	0.15 + 0.011*SL	0.19 + 0.009*SL
RN to Q	tPLH	0.44	0.42 + 0.014*SL	0.42 + 0.011*SL	0.45 + 0.010*SL
	tPHL	0.58	0.55 + 0.014*SL	0.56 + 0.009*SL	0.62 + 0.006*SL
	tR	0.23	0.18 + 0.024*SL	0.19 + 0.020*SL	0.17 + 0.021*SL
	tF	0.23	0.20 + 0.014*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
SN to Q	tPLH	0.87	0.84 + 0.014*SL	0.85 + 0.011*SL	0.87 + 0.010*SL
	tR	0.23	0.20 + 0.012*SL	0.18 + 0.021*SL	0.19 + 0.020*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD4D4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

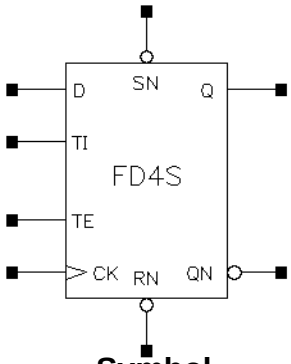
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.178
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



Inputs: D, TI, TE, CK, SN, RN
Outputs: Q, QN
Input Loading (SL):
- D, TI, CK: 1
- TE, SN, RN: 2

Maximum Fanout (Rec. SL):
- FD4S: All : 28
- FD4SD2: All : 56

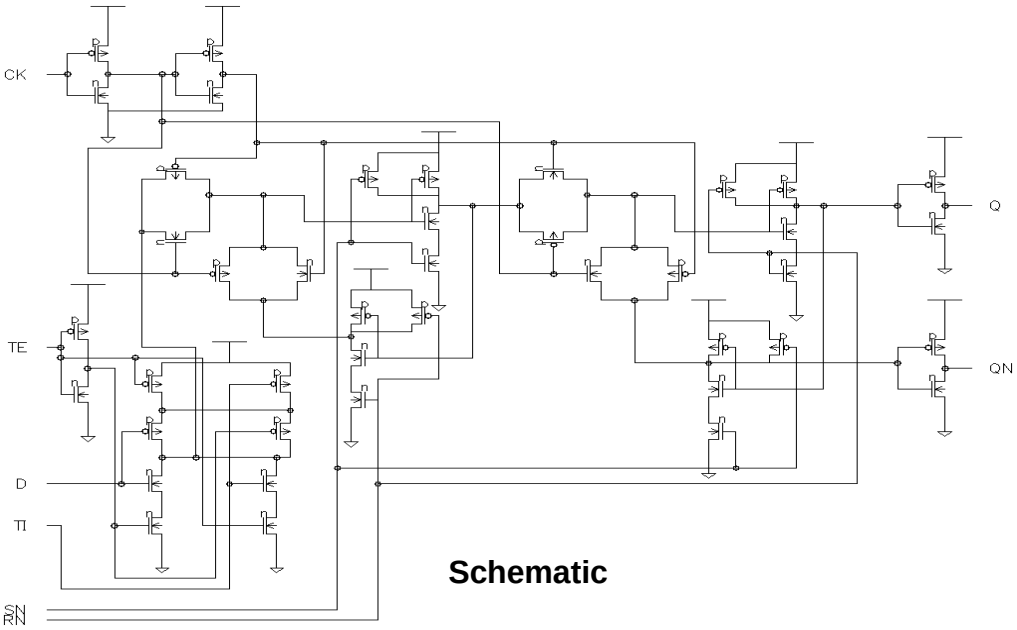
Gate Count:
- FD4S: 11
- FD4SD2: 12



Symbol

D	SN	RN	TI	TE	CK	Qn+1	QNn+1
0	1	1	x	0	↑	0	1
1	1	1	x	0	↑	1	0
x	1	1	0	1	↑	0	1
x	1	1	1	1	↑	1	0
x	0	1	x	x	x	1	0
x	1	0	x	x	x	0	1
x	0	0	x	x	x	0	0
x	1	1	x	x	↓	Qn	QNn

Truth Table



Schematic

FD4S Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	t_{PLH}	0.68	0.60 + 0.041*SL	0.61 + 0.037*SL	0.61 + 0.038*SL
	t_R	0.27	0.11 + 0.078*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
RN to Q	t_{PLH}	0.22	0.14 + 0.042*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
	t_{PHL}	0.39	0.33 + 0.027*SL	0.36 + 0.018*SL	0.40 + 0.016*SL
	t_R	0.28	0.12 + 0.083*SL	0.11 + 0.086*SL	0.06 + 0.088*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.030*SL	0.08 + 0.032*SL
CK to Q	t_{PLH}	0.47	0.39 + 0.042*SL	0.40 + 0.038*SL	0.40 + 0.038*SL
	t_{PHL}	0.45	0.40 + 0.023*SL	0.42 + 0.017*SL	0.45 + 0.016*SL
	t_R	0.26	0.10 + 0.084*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
	t_F	0.14	0.08 + 0.029*SL	0.08 + 0.032*SL	0.07 + 0.032*SL
SN to QN	t_{PLH}	0.22	0.13 + 0.042*SL	0.15 + 0.037*SL	0.15 + 0.037*SL
	t_{PHL}	0.37	0.32 + 0.027*SL	0.35 + 0.017*SL	0.37 + 0.016*SL
	t_R	0.27	0.11 + 0.082*SL	0.10 + 0.084*SL	0.06 + 0.086*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.030*SL	0.07 + 0.032*SL
RN to QN	t_{PLH}	0.56	0.49 + 0.038*SL	0.49 + 0.037*SL	0.49 + 0.037*SL
	t_R	0.26	0.09 + 0.082*SL	0.09 + 0.085*SL	0.06 + 0.087*SL
CK to QN	t_{PLH}	0.61	0.54 + 0.038*SL	0.54 + 0.037*SL	0.54 + 0.037*SL
	t_{PHL}	0.52	0.47 + 0.024*SL	0.49 + 0.017*SL	0.50 + 0.016*SL
	t_R	0.25	0.08 + 0.086*SL	0.08 + 0.085*SL	0.06 + 0.087*SL
	t_F	0.14	0.07 + 0.036*SL	0.09 + 0.030*SL	0.05 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD4S Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.000
Input Hold Time (TE to CK)	t_{HD}	0.000
Input Hold Time (TI to CK)	t_{HD}	0.000
Input Setup Time (D to CK)	t_{SU}	0.561
Input Setup Time (TE to CK)	t_{SU}	0.725
Input Setup Time (TI to CK)	t_{SU}	0.616

FD4S Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139

FD4SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.68	0.64 + 0.021*SL	0.65 + 0.019*SL	0.66 + 0.019*SL
	tR	0.19	0.12 + 0.035*SL	0.09 + 0.044*SL	0.08 + 0.044*SL
RN to Q	tPLH	0.22	0.18 + 0.020*SL	0.18 + 0.019*SL	0.19 + 0.019*SL
	tPHL	0.39	0.36 + 0.017*SL	0.38 + 0.011*SL	0.42 + 0.008*SL
	tR	0.21	0.13 + 0.039*SL	0.12 + 0.043*SL	0.08 + 0.044*SL
	tF	0.16	0.13 + 0.018*SL	0.13 + 0.015*SL	0.13 + 0.015*SL
CK to Q	tPLH	0.47	0.42 + 0.023*SL	0.43 + 0.019*SL	0.44 + 0.019*SL
	tPHL	0.45	0.42 + 0.017*SL	0.44 + 0.010*SL	0.48 + 0.008*SL
	tR	0.18	0.10 + 0.040*SL	0.09 + 0.044*SL	0.08 + 0.045*SL
	tF	0.13	0.09 + 0.017*SL	0.10 + 0.016*SL	0.10 + 0.016*SL
SN to QN	tPLH	0.21	0.17 + 0.022*SL	0.18 + 0.019*SL	0.19 + 0.018*SL
	tPHL	0.38	0.35 + 0.015*SL	0.37 + 0.010*SL	0.41 + 0.008*SL
	tR	0.20	0.13 + 0.034*SL	0.11 + 0.041*SL	0.09 + 0.042*SL
	tF	0.16	0.12 + 0.016*SL	0.13 + 0.015*SL	0.12 + 0.015*SL
RN to QN	tPLH	0.61	0.57 + 0.018*SL	0.57 + 0.018*SL	0.57 + 0.018*SL
	tR	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.07 + 0.042*SL
CK to QN	tPLH	0.66	0.62 + 0.017*SL	0.62 + 0.018*SL	0.62 + 0.018*SL
	tPHL	0.57	0.54 + 0.015*SL	0.56 + 0.010*SL	0.58 + 0.008*SL
	tR	0.18	0.11 + 0.036*SL	0.09 + 0.041*SL	0.07 + 0.042*SL
	tF	0.13	0.08 + 0.025*SL	0.11 + 0.015*SL	0.09 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD4SD2 Timing Requirements

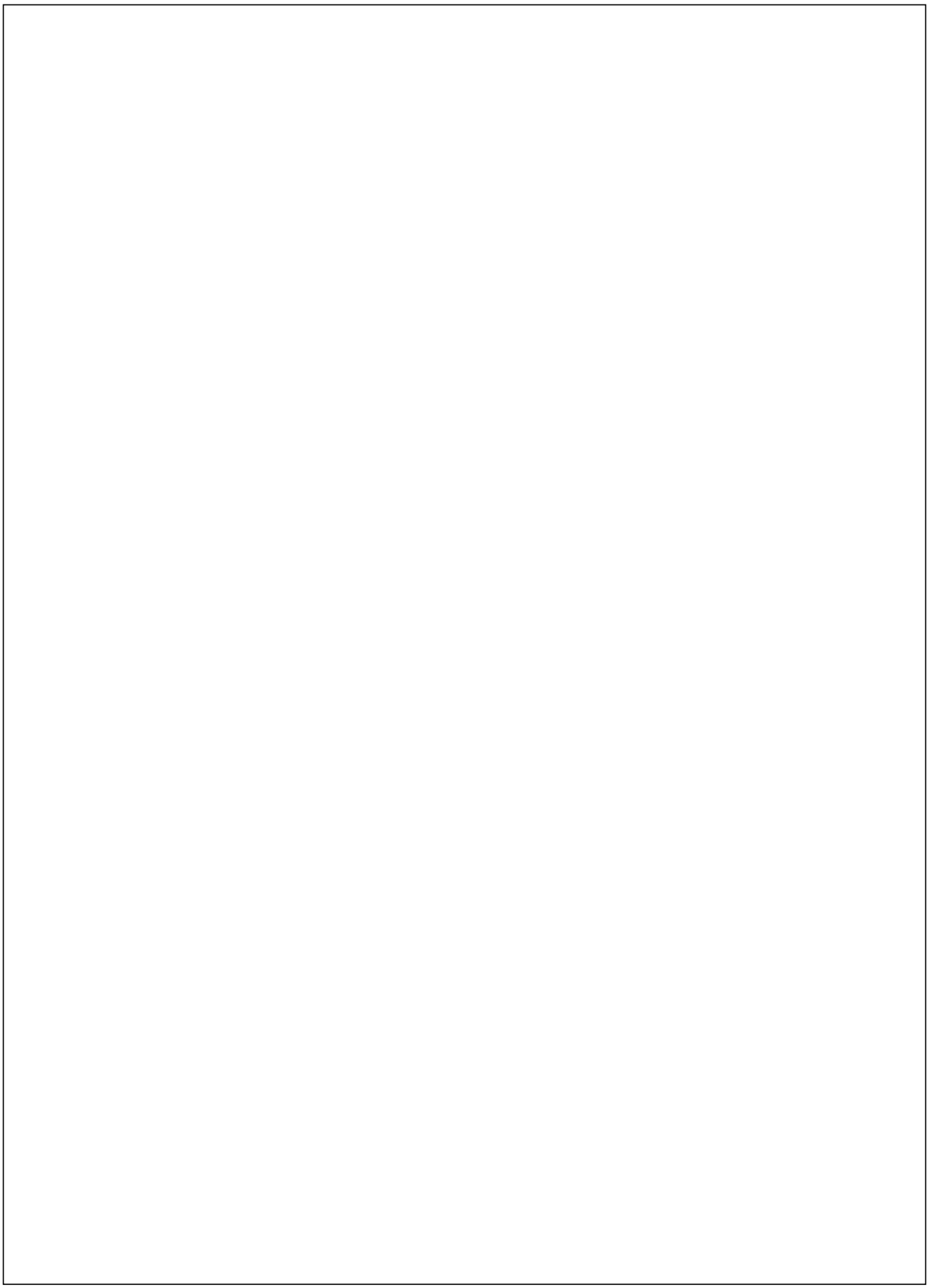
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.561
Input Setup Time (TE to CK)	tSU	0.725
Input Setup Time (TI to CK)	tSU	0.616

FD4SD2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

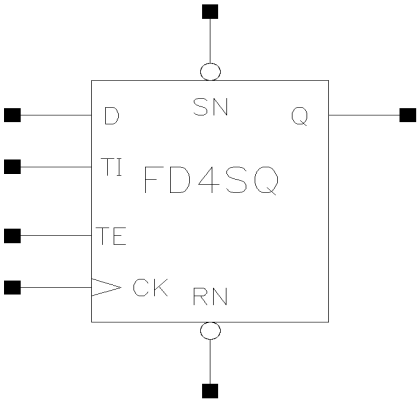
Parameter	Symbol	Value [ns]
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139



Inputs: D, TI, TE, CK, SN, RN
Output: Q
Input Loading (SL):
- FD4SD2Q: D, CK, TI: 1
  RN, SN, TE: 2
- FD4SD4Q: D, CK, TI: 1
  RN, SN, TE: 2

Maximum Fanout (Rec. SL):
- FD4SD2Q: 56
- FD4SD4Q: 112

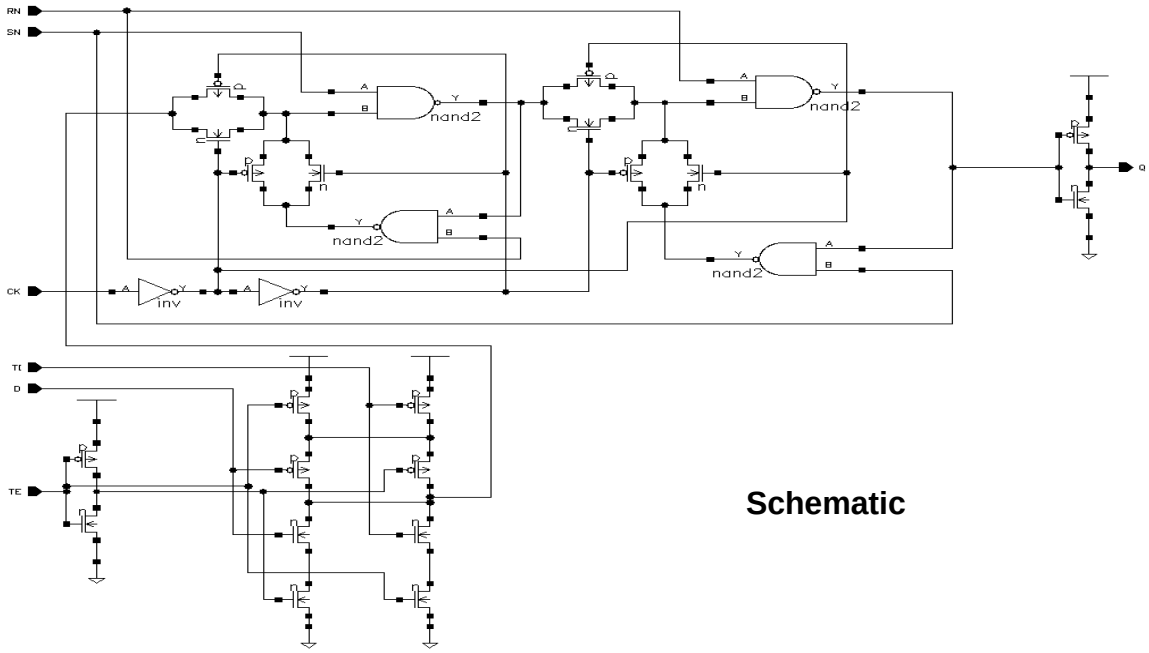
Gate Count:
- FD4SD2Q: 11
- FD4SD4Q: 12



Symbol

D	SN	RN	TI	TE	CK	Qn+1
0	1	1	x	0	⎍	0
1	1	1	x	0	⎍	1
x	1	1	0	1	⎍	0
x	1	1	1	1	⎍	1
x	0	1	x	x	x	1
x	1	0	x	x	x	0
x	0	0	x	x	x	0
x	1	1	x	x	⎎	Qn

Truth Table



Schematic

FD4SD2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	t_{PLH}	0.68	0.64 + 0.020*SL	0.64 + 0.019*SL	0.65 + 0.018*SL
	t_R	0.19	0.12 + 0.035*SL	0.10 + 0.042*SL	0.08 + 0.043*SL
RN to Q	t_{PLH}	0.22	0.18 + 0.021*SL	0.18 + 0.019*SL	0.19 + 0.018*SL
	t_{PHL}	0.39	0.36 + 0.018*SL	0.38 + 0.011*SL	0.43 + 0.008*SL
	t_R	0.20	0.13 + 0.034*SL	0.11 + 0.042*SL	0.08 + 0.043*SL
	t_F	0.16	0.12 + 0.023*SL	0.14 + 0.014*SL	0.12 + 0.016*SL
CK to Q	t_{PLH}	0.47	0.42 + 0.022*SL	0.43 + 0.019*SL	0.44 + 0.019*SL
	t_{PHL}	0.45	0.42 + 0.017*SL	0.44 + 0.010*SL	0.48 + 0.008*SL
	t_R	0.19	0.11 + 0.041*SL	0.11 + 0.042*SL	0.08 + 0.043*SL
	t_F	0.13	0.09 + 0.017*SL	0.10 + 0.016*SL	0.09 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD4SD2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.000
Input Hold Time (TE to CK)	t_{HD}	0.000
Input Hold Time (TI to CK)	t_{HD}	0.000
Input Setup Time (D to CK)	t_{SU}	0.561
Input Setup Time (TE to CK)	t_{SU}	0.725
Input Setup Time (TI to CK)	t_{SU}	0.616
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139

FD4SD4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

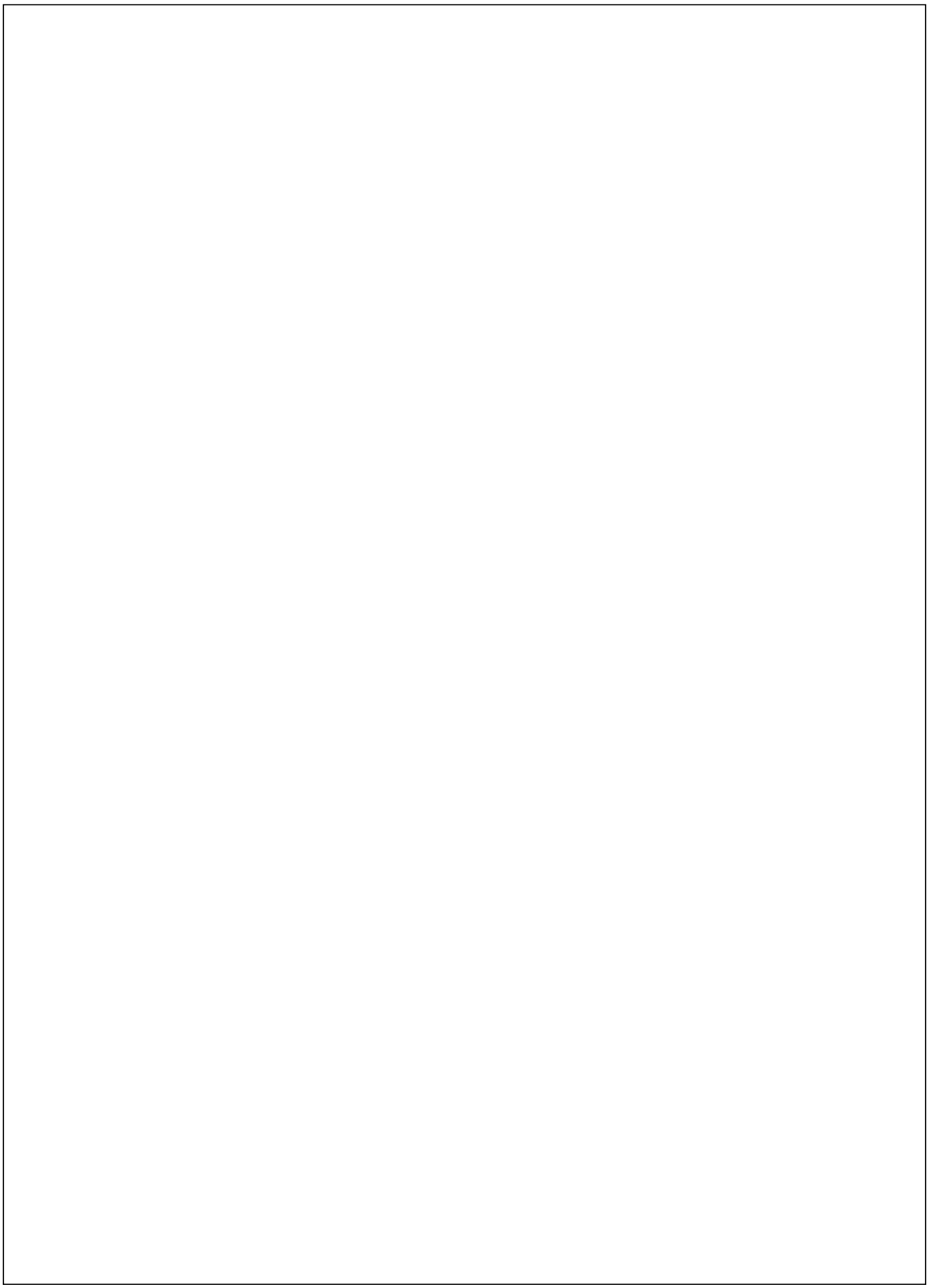
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	t_{PLH}	0.73	0.71 + 0.013*SL	0.72 + 0.010*SL	0.74 + 0.009*SL
	t_R	0.17	0.13 + 0.019*SL	0.12 + 0.021*SL	0.13 + 0.021*SL
RN to Q	t_{PLH}	0.27	0.25 + 0.012*SL	0.25 + 0.010*SL	0.27 + 0.009*SL
	t_{PHL}	0.44	0.42 + 0.010*SL	0.43 + 0.007*SL	0.47 + 0.005*SL
	t_R	0.18	0.15 + 0.015*SL	0.13 + 0.021*SL	0.13 + 0.020*SL
	t_F	0.18	0.16 + 0.012*SL	0.17 + 0.007*SL	0.17 + 0.007*SL
CK to Q	t_{PLH}	0.52	0.49 + 0.012*SL	0.50 + 0.010*SL	0.52 + 0.009*SL
	t_{PHL}	0.51	0.48 + 0.011*SL	0.50 + 0.007*SL	0.53 + 0.005*SL
	t_R	0.17	0.14 + 0.017*SL	0.12 + 0.021*SL	0.12 + 0.021*SL
	t_F	0.16	0.15 + 0.005*SL	0.14 + 0.008*SL	0.14 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD4SD4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

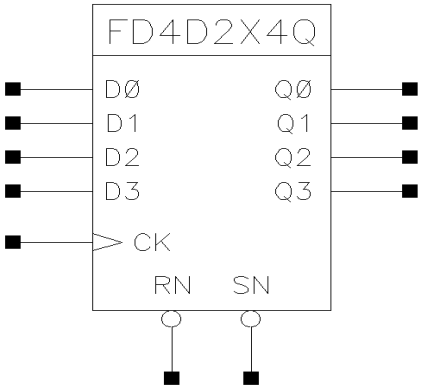
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.000
Input Hold Time (TE to CK)	t_{HD}	0.000
Input Hold Time (TI to CK)	t_{HD}	0.000
Input Setup Time (D to CK)	t_{SU}	0.561
Input Setup Time (TE to CK)	t_{SU}	0.725
Input Setup Time (TI to CK)	t_{SU}	0.616
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139



Inputs: D0, D1, D2, D3,, CK, RN, SN
Outputs: Q, Q1, Q2, Q3
Input Loading (SL):
- FD4D2X4Q: CK: 1, RN, SN: 8
  D0, D1, D2, D3: 3
- FD4D4X4Q: CK: 1, RN, SN: 8
  D0, D1, D2, D3: 3

Maximum Fanout (Rec. SL):
- FD4D2X4Q: 56
- FD4D4X4Q: 112

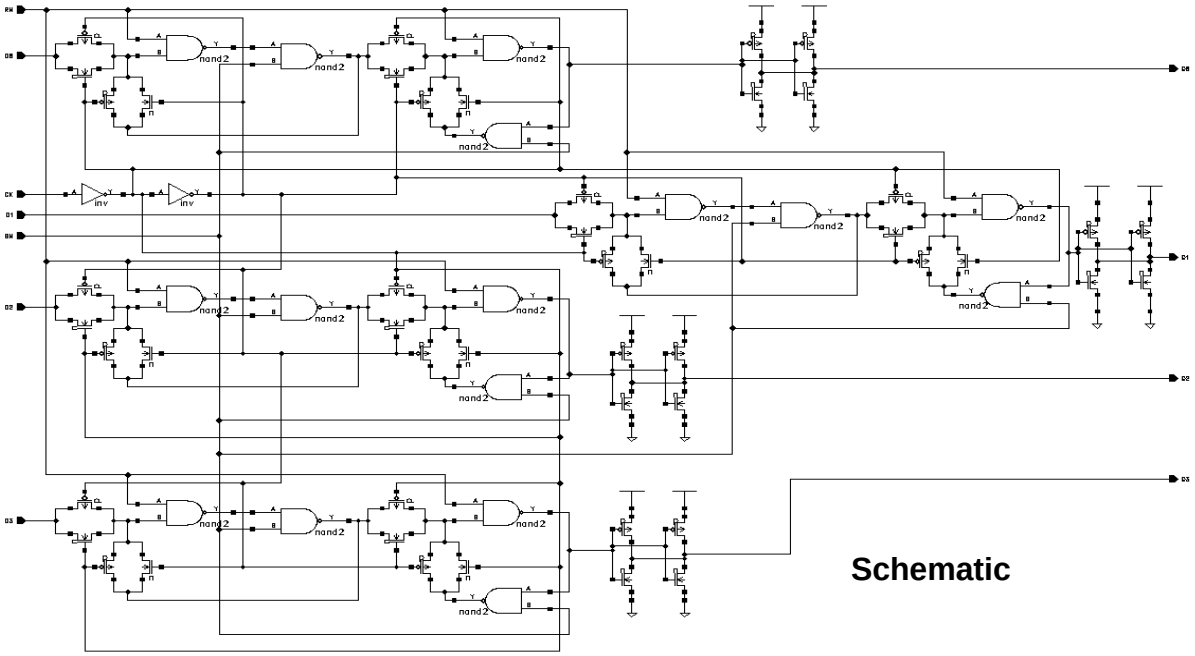
Gate Count:
- FD4D2X4Q: 29
- FD4D4X4Q: 33



Symbol

D	SN	RN	CK	Qn+1
0	1	1	↑	0
1	1	1	↑	1
x	0	1	x	1
x	1	0	x	0
x	0	0	x	0
x	1	1	↓	Qn

Truth Table



Schematic

FD4D2X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.73 + 0.019*SL
	t_{PHL}	0.54	0.49 + 0.025*SL	0.53 + 0.013*SL	0.59 + 0.010*SL
	t_R	0.22	0.14 + 0.044*SL	0.14 + 0.042*SL	0.13 + 0.043*SL
	t_F	0.18	0.14 + 0.021*SL	0.15 + 0.017*SL	0.18 + 0.016*SL
RN to Q0	t_{PLH}	0.38	0.34 + 0.023*SL	0.34 + 0.020*SL	0.37 + 0.019*SL
	t_{PHL}	0.53	0.48 + 0.022*SL	0.51 + 0.014*SL	0.59 + 0.010*SL
	t_R	0.24	0.15 + 0.049*SL	0.17 + 0.040*SL	0.12 + 0.043*SL
	t_F	0.21	0.16 + 0.024*SL	0.18 + 0.017*SL	0.21 + 0.015*SL
SN to Q0	t_{PLH}	0.81	0.76 + 0.026*SL	0.78 + 0.020*SL	0.80 + 0.019*SL
	t_R	0.23	0.14 + 0.046*SL	0.15 + 0.041*SL	0.12 + 0.043*SL
CK to Q1	t_{PLH}	0.74	0.69 + 0.024*SL	0.70 + 0.020*SL	0.73 + 0.019*SL
	t_{PHL}	0.54	0.49 + 0.025*SL	0.53 + 0.013*SL	0.59 + 0.010*SL
	t_R	0.23	0.14 + 0.045*SL	0.14 + 0.043*SL	0.13 + 0.044*SL
	t_F	0.19	0.15 + 0.020*SL	0.15 + 0.018*SL	0.18 + 0.016*SL
RN to Q1	t_{PLH}	0.38	0.33 + 0.023*SL	0.34 + 0.020*SL	0.37 + 0.019*SL
	t_{PHL}	0.52	0.48 + 0.022*SL	0.50 + 0.014*SL	0.58 + 0.010*SL
	t_R	0.25	0.15 + 0.050*SL	0.17 + 0.041*SL	0.12 + 0.044*SL
	t_F	0.21	0.16 + 0.024*SL	0.19 + 0.017*SL	0.21 + 0.016*SL
SN to Q1	t_{PLH}	0.81	0.77 + 0.024*SL	0.78 + 0.020*SL	0.80 + 0.019*SL
	t_R	0.24	0.17 + 0.035*SL	0.15 + 0.042*SL	0.12 + 0.044*SL
CK to Q2	t_{PLH}	0.74	0.69 + 0.025*SL	0.70 + 0.020*SL	0.74 + 0.019*SL
	t_{PHL}	0.54	0.49 + 0.025*SL	0.53 + 0.013*SL	0.59 + 0.010*SL
	t_R	0.23	0.14 + 0.044*SL	0.14 + 0.043*SL	0.13 + 0.044*SL
	t_F	0.19	0.15 + 0.020*SL	0.15 + 0.018*SL	0.18 + 0.016*SL
RN to Q2	t_{PLH}	0.38	0.33 + 0.023*SL	0.34 + 0.020*SL	0.37 + 0.019*SL
	t_{PHL}	0.52	0.48 + 0.022*SL	0.50 + 0.014*SL	0.58 + 0.010*SL
	t_R	0.25	0.15 + 0.050*SL	0.17 + 0.041*SL	0.12 + 0.044*SL
	t_F	0.21	0.16 + 0.024*SL	0.19 + 0.017*SL	0.21 + 0.016*SL
SN to Q2	t_{PLH}	0.81	0.76 + 0.025*SL	0.78 + 0.020*SL	0.80 + 0.019*SL
	t_R	0.23	0.15 + 0.042*SL	0.15 + 0.043*SL	0.12 + 0.044*SL
CK to Q3	t_{PLH}	0.74	0.69 + 0.025*SL	0.71 + 0.020*SL	0.74 + 0.019*SL
	t_{PHL}	0.54	0.49 + 0.025*SL	0.53 + 0.013*SL	0.59 + 0.010*SL
	t_R	0.23	0.14 + 0.045*SL	0.14 + 0.043*SL	0.13 + 0.043*SL
	t_F	0.18	0.14 + 0.021*SL	0.15 + 0.017*SL	0.19 + 0.016*SL
RN to Q3	t_{PLH}	0.38	0.34 + 0.023*SL	0.34 + 0.020*SL	0.37 + 0.019*SL
	t_{PHL}	0.53	0.48 + 0.022*SL	0.51 + 0.014*SL	0.59 + 0.010*SL
	t_R	0.24	0.15 + 0.049*SL	0.17 + 0.041*SL	0.12 + 0.043*SL
	t_F	0.21	0.16 + 0.024*SL	0.18 + 0.017*SL	0.21 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD4D2X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q3	t_{PLH}	0.82	0.76 + 0.026*SL	0.78 + 0.020*SL	0.81 + 0.019*SL
	t_R	0.25	0.18 + 0.034*SL	0.16 + 0.041*SL	0.12 + 0.043*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD4D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D0 to CK)	t_{HD}	0.397
Input Hold Time (D1 to CK)	t_{HD}	0.397
Input Hold Time (D2 to CK)	t_{HD}	0.397
Input Hold Time (D3 to CK)	t_{HD}	0.397
Input Setup Time (D0 to CK)	t_{SU}	0.233
Input Setup Time (D1 to CK)	t_{SU}	0.233
Input Setup Time (D2 to CK)	t_{SU}	0.233
Input Setup Time (D3 to CK)	t_{SU}	0.233
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139

FD4D4X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

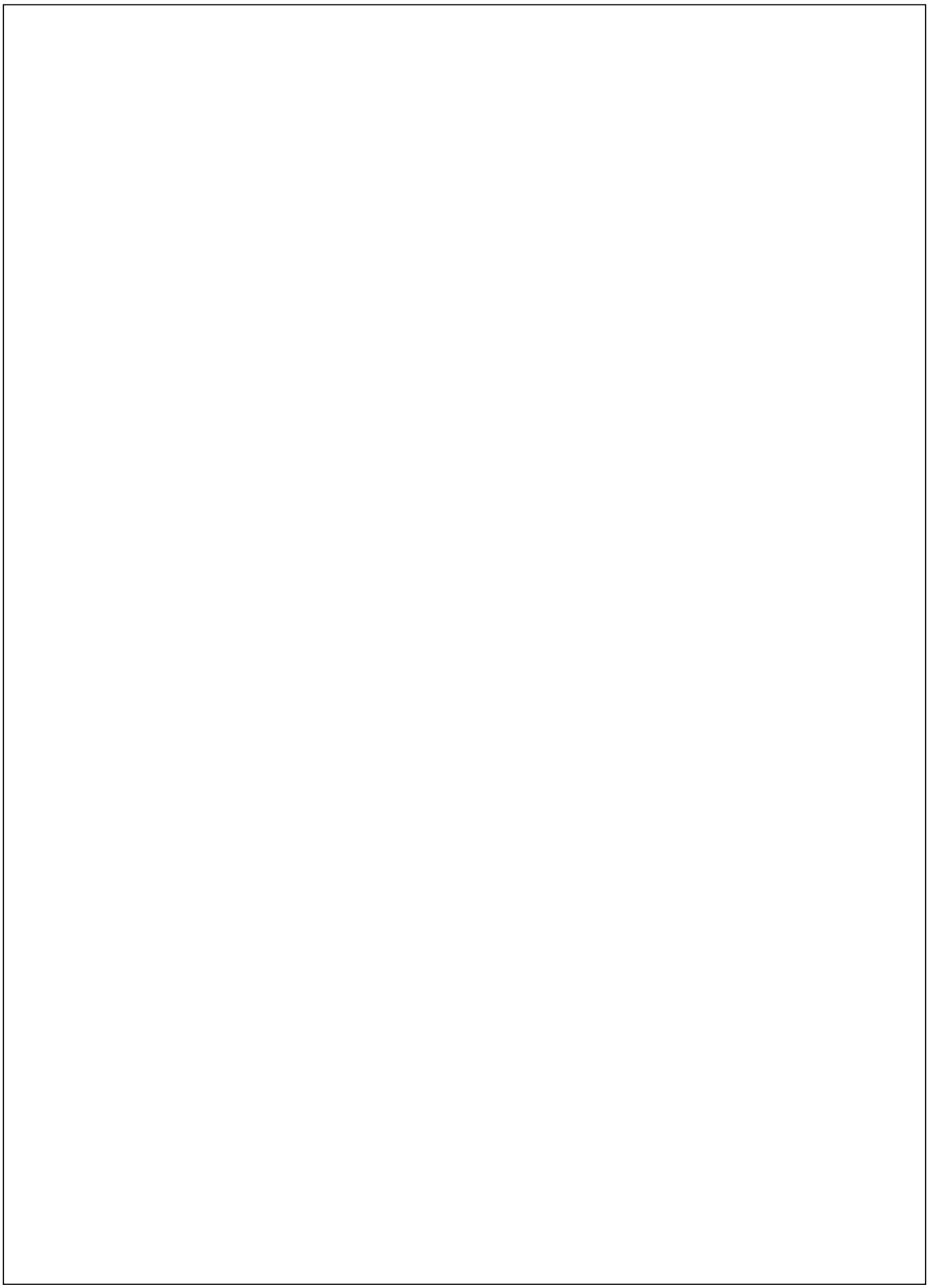
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	tPLH	0.80	0.77 + 0.014*SL	0.78 + 0.011*SL	0.81 + 0.010*SL
	tPHL	0.63	0.60 + 0.016*SL	0.62 + 0.009*SL	0.67 + 0.006*SL
	tR	0.22	0.18 + 0.018*SL	0.18 + 0.020*SL	0.17 + 0.021*SL
	tF	0.23	0.20 + 0.014*SL	0.21 + 0.010*SL	0.25 + 0.008*SL
RN to Q0	tPLH	0.44	0.42 + 0.013*SL	0.42 + 0.011*SL	0.45 + 0.010*SL
	tPHL	0.57	0.55 + 0.014*SL	0.56 + 0.009*SL	0.61 + 0.006*SL
	tR	0.23	0.19 + 0.020*SL	0.19 + 0.020*SL	0.17 + 0.021*SL
	tF	0.22	0.19 + 0.015*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
SN to Q0	tPLH	0.87	0.84 + 0.016*SL	0.85 + 0.011*SL	0.87 + 0.010*SL
	tR	0.23	0.20 + 0.015*SL	0.18 + 0.020*SL	0.19 + 0.020*SL
CK to Q1	tPLH	0.80	0.77 + 0.014*SL	0.78 + 0.011*SL	0.81 + 0.010*SL
	tPHL	0.63	0.60 + 0.015*SL	0.62 + 0.009*SL	0.67 + 0.006*SL
	tR	0.22	0.18 + 0.019*SL	0.18 + 0.021*SL	0.17 + 0.021*SL
	tF	0.23	0.20 + 0.014*SL	0.21 + 0.010*SL	0.24 + 0.009*SL
RN to Q1	tPLH	0.44	0.41 + 0.014*SL	0.42 + 0.011*SL	0.45 + 0.010*SL
	tPHL	0.57	0.54 + 0.014*SL	0.56 + 0.009*SL	0.61 + 0.006*SL
	tR	0.23	0.19 + 0.019*SL	0.19 + 0.020*SL	0.17 + 0.021*SL
	tF	0.23	0.20 + 0.015*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
SN to Q1	tPLH	0.87	0.84 + 0.015*SL	0.85 + 0.011*SL	0.87 + 0.010*SL
	tR	0.23	0.20 + 0.016*SL	0.18 + 0.021*SL	0.19 + 0.021*SL
CK to Q2	tPLH	0.80	0.77 + 0.014*SL	0.78 + 0.011*SL	0.81 + 0.010*SL
	tPHL	0.63	0.60 + 0.015*SL	0.62 + 0.009*SL	0.67 + 0.006*SL
	tR	0.22	0.18 + 0.019*SL	0.18 + 0.021*SL	0.17 + 0.021*SL
	tF	0.23	0.20 + 0.012*SL	0.21 + 0.010*SL	0.25 + 0.008*SL
RN to Q2	tPLH	0.44	0.41 + 0.014*SL	0.42 + 0.011*SL	0.45 + 0.010*SL
	tPHL	0.57	0.55 + 0.013*SL	0.56 + 0.009*SL	0.61 + 0.006*SL
	tR	0.23	0.19 + 0.020*SL	0.19 + 0.020*SL	0.17 + 0.021*SL
	tF	0.23	0.20 + 0.014*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
SN to Q2	tPLH	0.87	0.84 + 0.015*SL	0.85 + 0.011*SL	0.88 + 0.010*SL
	tR	0.23	0.20 + 0.013*SL	0.18 + 0.021*SL	0.19 + 0.021*SL
CK to Q3	tPLH	0.81	0.78 + 0.015*SL	0.79 + 0.011*SL	0.81 + 0.010*SL
	tPHL	0.63	0.60 + 0.015*SL	0.62 + 0.009*SL	0.67 + 0.006*SL
	tR	0.22	0.18 + 0.019*SL	0.18 + 0.021*SL	0.17 + 0.021*SL
	tF	0.23	0.20 + 0.012*SL	0.21 + 0.010*SL	0.25 + 0.008*SL
RN to Q3	tPLH	0.45	0.42 + 0.013*SL	0.43 + 0.011*SL	0.45 + 0.010*SL
	tPHL	0.57	0.55 + 0.013*SL	0.56 + 0.009*SL	0.61 + 0.006*SL
	tR	0.23	0.19 + 0.021*SL	0.19 + 0.020*SL	0.17 + 0.021*SL
	tF	0.23	0.20 + 0.014*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
SN to Q3	tPLH	0.87	0.84 + 0.015*SL	0.85 + 0.011*SL	0.88 + 0.010*SL
	tR	0.22	0.20 + 0.013*SL	0.17 + 0.021*SL	0.19 + 0.021*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD4D4X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

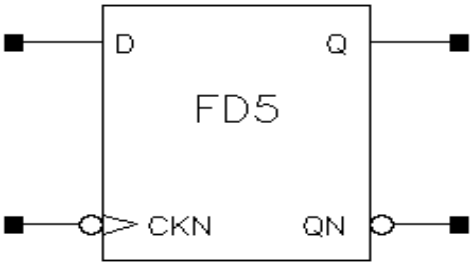
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.959
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (D0 to CK)	t_{HD}	0.397
Input Hold Time (D1 to CK)	t_{HD}	0.397
Input Hold Time (D2 to CK)	t_{HD}	0.397
Input Hold Time (D3 to CK)	t_{HD}	0.397
Input Setup Time (D0 to CK)	t_{SU}	0.233
Input Setup Time (D1 to CK)	t_{SU}	0.233
Input Setup Time (D2 to CK)	t_{SU}	0.233
Input Setup Time (D3 to CK)	t_{SU}	0.233
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139



Inputs: D, CKN
Outputs: Q, QN
Input Loading (SL):
- FD5: All: 1
- FD5D2: All: 1

Maximum Fanout (Rec. SL):
- FD5: All: 28
- FD5D2: All: 56

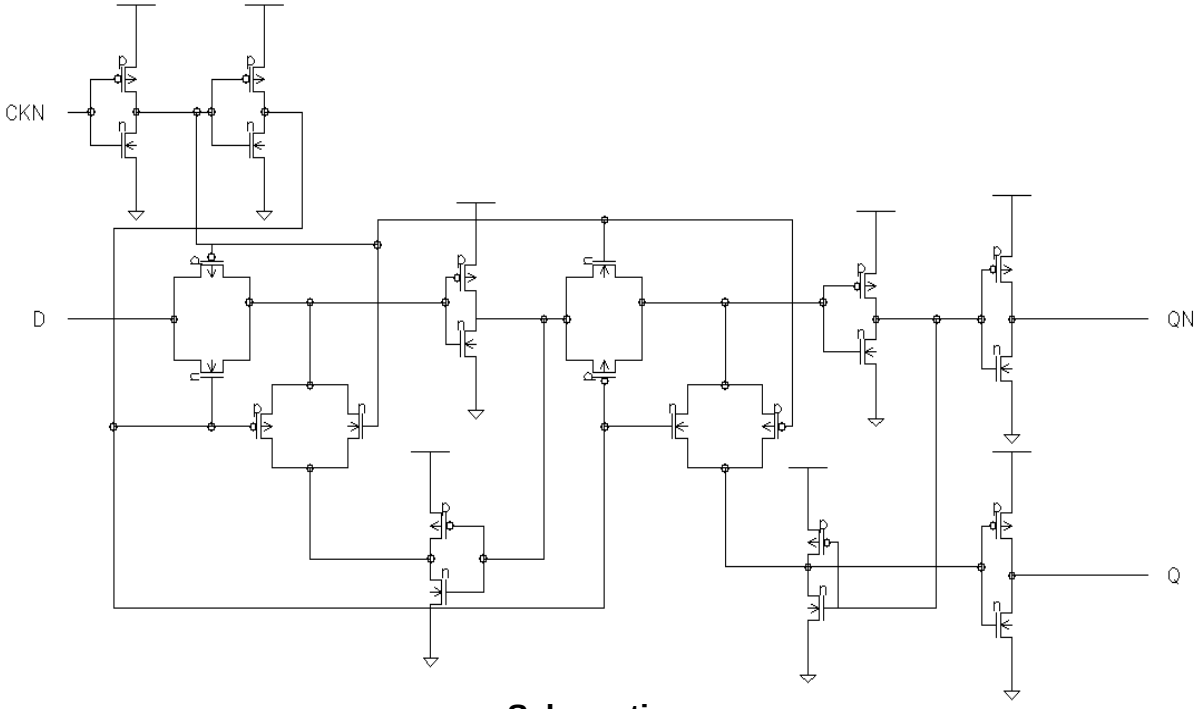
Gate Count
- FD5: 6
- FD5D2: 7



Symbol

D	CK	Qn+1	QNn+1
0	↓	0	1
1	↓	1	0
x	↑	Qn	QNn

Truth Table



Schematic

FD5 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	t_{PLH}	0.69	0.62 + 0.039*SL	0.62 + 0.037*SL	0.62 + 0.037*SL
	t_{PHL}	0.67	0.63 + 0.020*SL	0.64 + 0.017*SL	0.66 + 0.016*SL
	t_R	0.24	0.08 + 0.080*SL	0.06 + 0.086*SL	0.05 + 0.087*SL
	t_F	0.14	0.06 + 0.037*SL	0.08 + 0.031*SL	0.05 + 0.033*SL
CKN to QN	t_{PLH}	0.64	0.56 + 0.039*SL	0.56 + 0.038*SL	0.57 + 0.038*SL
	t_{PHL}	0.58	0.54 + 0.024*SL	0.56 + 0.017*SL	0.58 + 0.016*SL
	t_R	0.24	0.07 + 0.086*SL	0.07 + 0.088*SL	0.06 + 0.088*SL
	t_F	0.14	0.07 + 0.034*SL	0.08 + 0.032*SL	0.05 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD5 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D to CKN)	t_{HD}	0.342
Input Setup Time (D to CKN)	t_{SU}	0.123

FD5D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

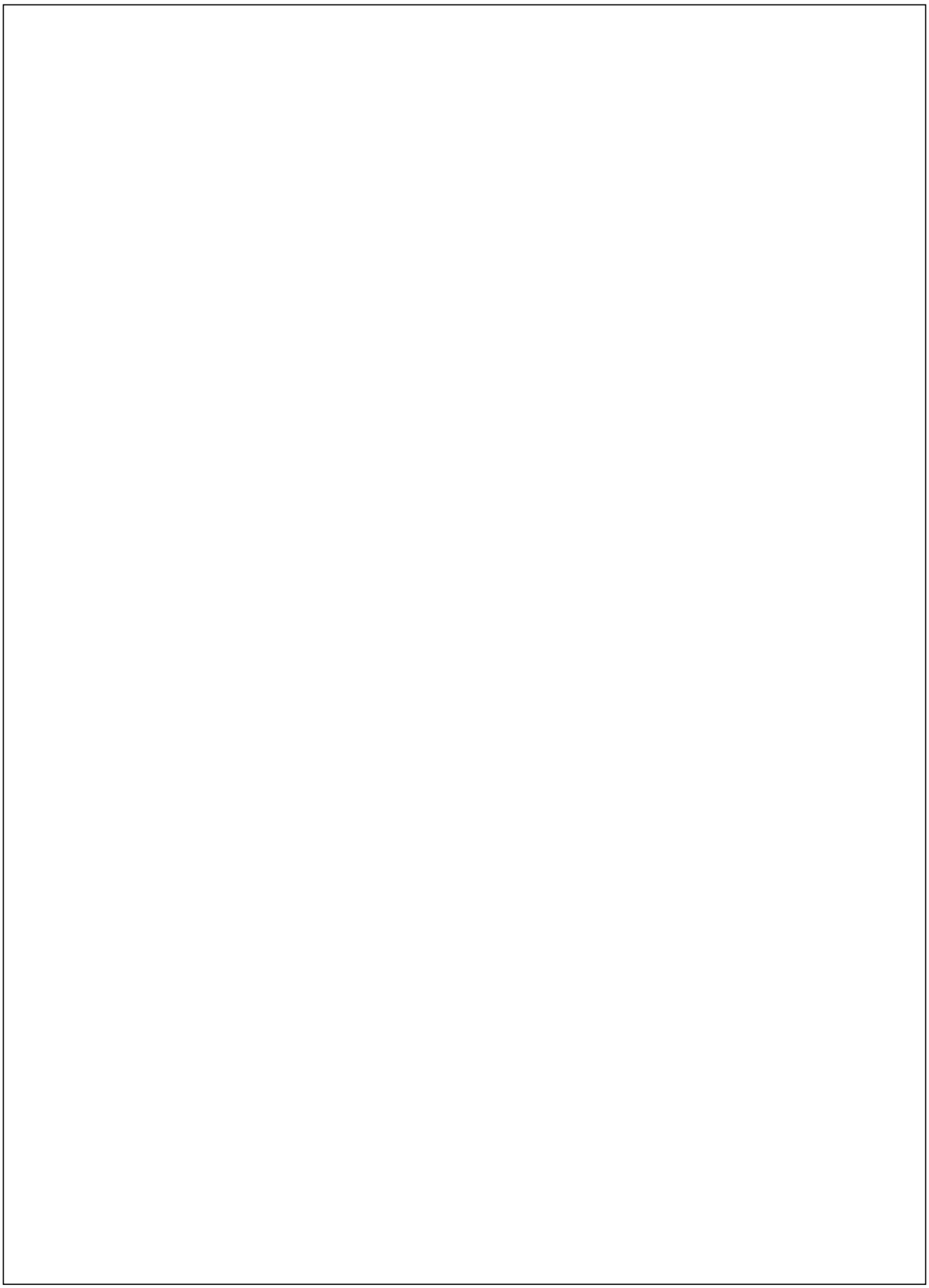
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.72	0.69 + 0.017*SL	0.69 + 0.018*SL	0.68 + 0.018*SL
	tPHL	0.72	0.69 + 0.013*SL	0.70 + 0.010*SL	0.73 + 0.008*SL
	tR	0.16	0.09 + 0.035*SL	0.08 + 0.041*SL	0.05 + 0.042*SL
	tF	0.12	0.08 + 0.015*SL	0.08 + 0.015*SL	0.07 + 0.016*SL
CKN to QN	tPLH	0.63	0.59 + 0.021*SL	0.59 + 0.019*SL	0.60 + 0.019*SL
	tPHL	0.59	0.56 + 0.015*SL	0.58 + 0.010*SL	0.61 + 0.008*SL
	tR	0.17	0.09 + 0.043*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	tF	0.12	0.09 + 0.019*SL	0.09 + 0.016*SL	0.09 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD5D2 Timing Requirements

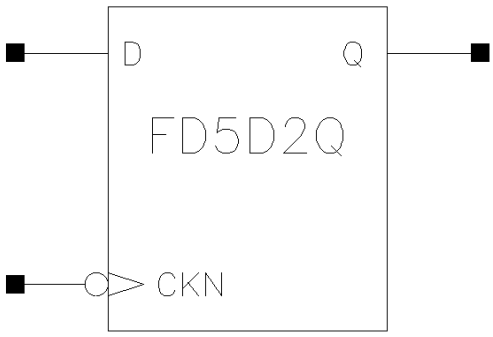
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.342
Input Setup Time (D to CKN)	tSU	0.123



Inputs: D, CK
Output: Q
Input Loading (SL): All: D: 3, CKN: 1
Maximum Fanout (Rec. SL):
- FD5D2Q: 56
- FD5D4Q: 112

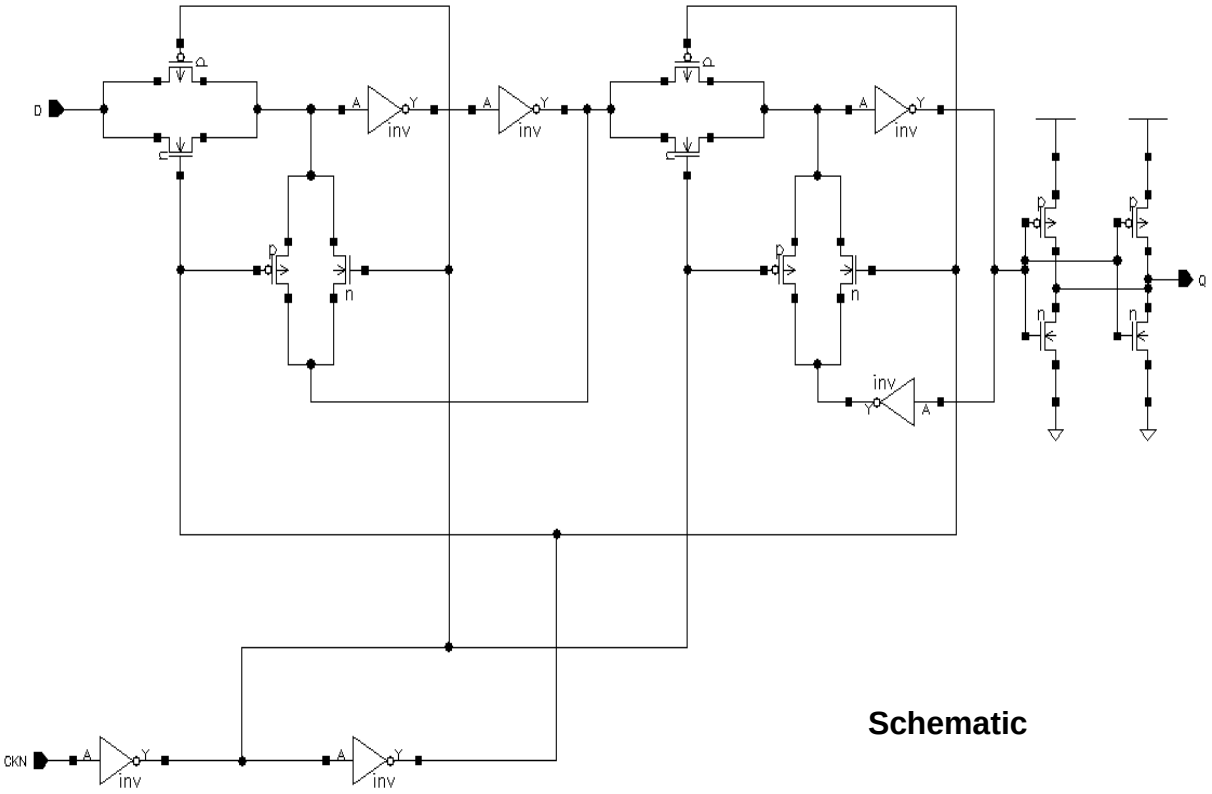
Gate Count:
- FD5D2Q: 6
- FD5D4Q: 7



Symbol

D	CK	Qn+1
0	↓	0
1	↓	1
x	↑	Qn

Truth Table



Schematic

FD5D2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	t_{PLH}	0.56	0.51 + 0.024*SL	0.52 + 0.020*SL	0.54 + 0.019*SL
	t_{PHL}	0.53	0.49 + 0.020*SL	0.51 + 0.013*SL	0.58 + 0.010*SL
	t_R	0.19	0.10 + 0.049*SL	0.11 + 0.044*SL	0.09 + 0.045*SL
	t_F	0.16	0.11 + 0.025*SL	0.13 + 0.019*SL	0.17 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD5D2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D to CKN)	t_{HD}	0.342
Input Setup Time (D to CKN)	t_{SU}	0.178

FD5D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	t_{PLH}	0.60	0.57 + 0.013*SL	0.58 + 0.011*SL	0.60 + 0.010*SL
	t_{PHL}	0.56	0.53 + 0.015*SL	0.55 + 0.009*SL	0.60 + 0.006*SL
	t_R	0.18	0.14 + 0.021*SL	0.14 + 0.022*SL	0.13 + 0.022*SL
	t_F	0.18	0.15 + 0.013*SL	0.16 + 0.011*SL	0.20 + 0.009*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD5D4Q Timing Requirements

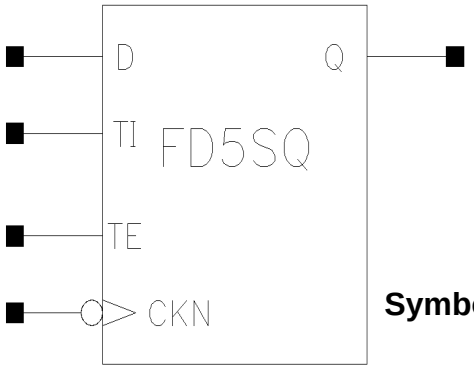
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D to CKN)	t_{HD}	0.397
Input Setup Time (D to CKN)	t_{SU}	0.178

Inputs: D, TI, TE, CKN
Output: Q
Input Loading (SL):
- FD5SD2Q: D, CKN, TI : 1
  TE : 2
- FD5SD4Q: D, CKN, TI : 1
  TE : 2

Maximum Fanout (Rec. SL):
- FD5SD2Q: 56
- FD5SD4Q: 112

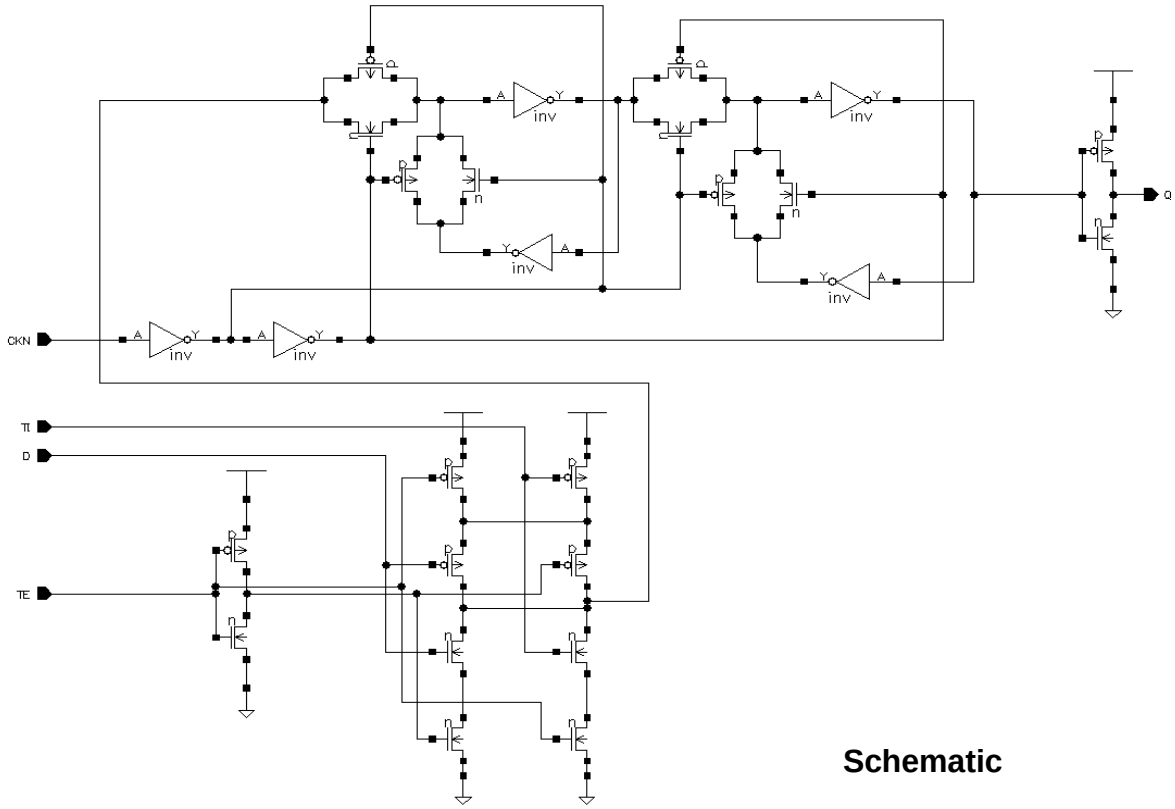
Gate Count:
- FD5SD2Q: 9
- FD5SD4Q: 10



Symbol

D	TI	TE	CKN	Qn+1
0	x	0	↓	0
1	x	o	↓	1
x	0	1	↓	0
x	1	1	↓	1
x	x	x	↑	QN

Truth Table



Schematic

FD5SD2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	t_{PLH}	0.63	0.58 + 0.021*SL	0.59 + 0.019*SL	0.60 + 0.019*SL
	t_{PHL}	0.60	0.56 + 0.016*SL	0.58 + 0.010*SL	0.62 + 0.009*SL
	t_R	0.17	0.08 + 0.046*SL	0.09 + 0.044*SL	0.06 + 0.045*SL
	t_F	0.12	0.09 + 0.017*SL	0.09 + 0.017*SL	0.09 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD5SD2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D to CKN)	t_{HD}	0.233
Input Hold Time (TE to CKN)	t_{HD}	0.233
Input Hold Time (TI to CKN)	t_{HD}	0.178
Input Setup Time (D to CKN)	t_{SU}	0.342
Input Setup Time (TE to CKN)	t_{SU}	0.452
Input Setup Time (TI to CKN)	t_{SU}	0.342

FD5SD4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

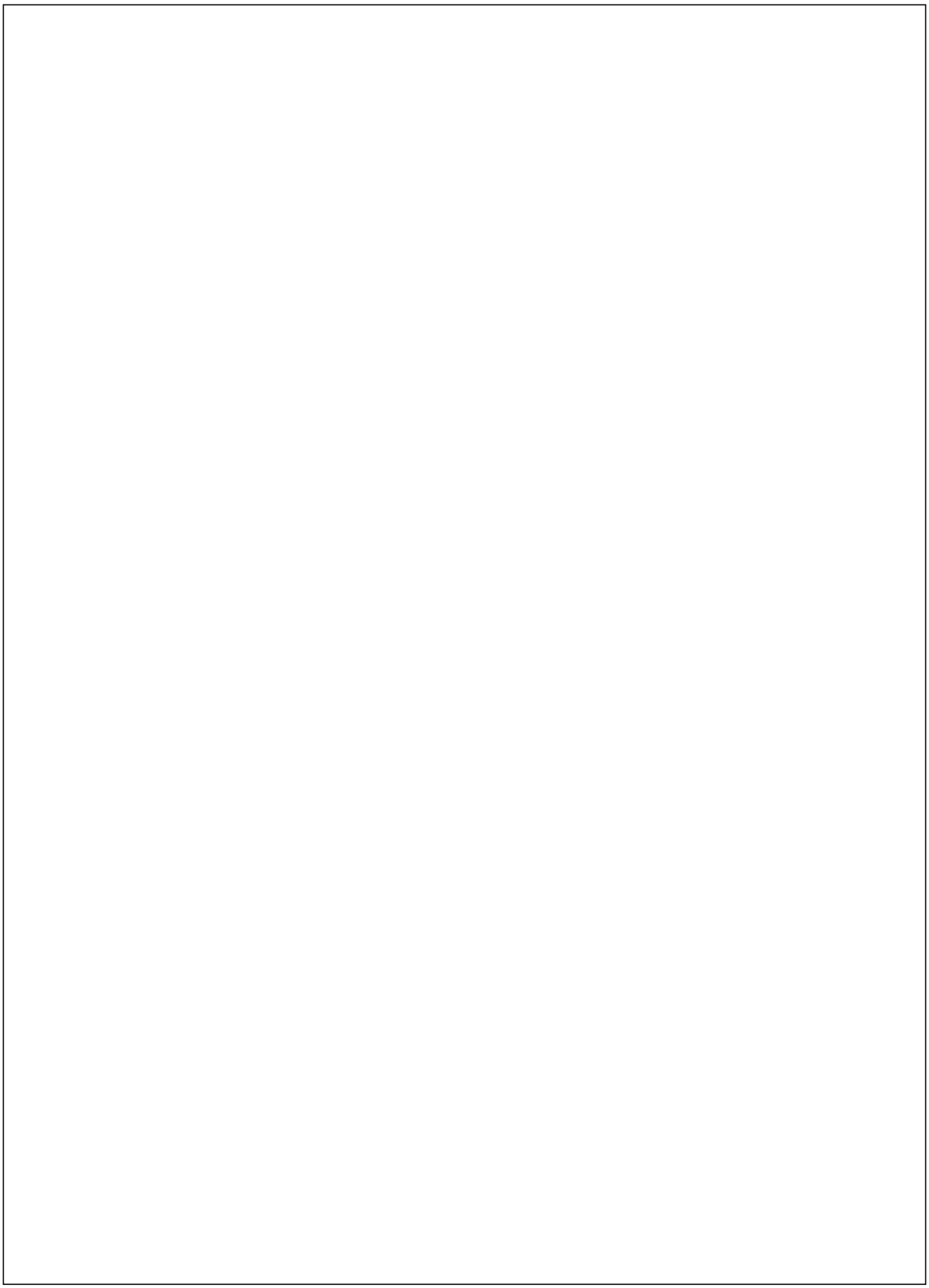
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.66	0.64 + 0.011*SL	0.64 + 0.010*SL	0.65 + 0.009*SL
	tPHL	0.64	0.62 + 0.011*SL	0.63 + 0.007*SL	0.67 + 0.005*SL
	tR	0.15	0.09 + 0.030*SL	0.12 + 0.021*SL	0.08 + 0.022*SL
	tF	0.14	0.12 + 0.011*SL	0.13 + 0.009*SL	0.15 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD5SD4Q Timing Requirements

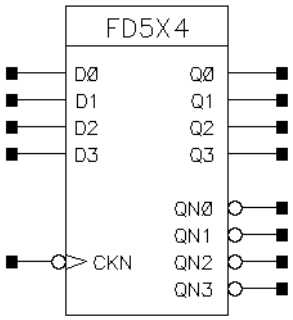
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.233
Input Hold Time (TE to CKN)	tHD	0.233
Input Hold Time (TI to CKN)	tHD	0.123
Input Setup Time (D to CKN)	tSU	0.342
Input Setup Time (TE to CKN)	tSU	0.452
Input Setup Time (TI to CKN)	tSU	0.342



Inputs: D0, D1, D2, D3, CKN
Outputs: Q0, Q1, Q2, Q3,
QN0, QN1, QN2, QN3
Input Loading (SL):
- D0, D1, D2, D3: 3
- CKN: 1

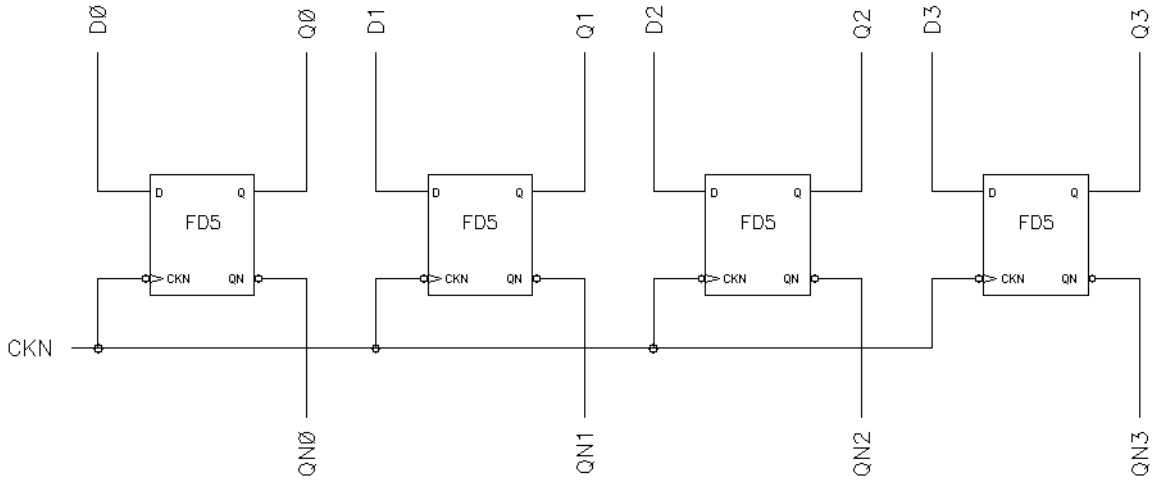
Maximum Fanout (Rec. SL): 28
Gate Count: 21



Symbol

D	CK	Qn+1	QNn+1
0	↓	0	1
1	↓	1	0
x	↑	Qn	QNn

Truth Table



Schematic

FD5X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	0.86	0.78 + 0.037*SL	0.78 + 0.037*SL	0.78 + 0.037*SL
	tPHL	0.97	0.93 + 0.021*SL	0.94 + 0.017*SL	0.96 + 0.016*SL
	tR	0.24	0.08 + 0.082*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	tF	0.13	0.07 + 0.033*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
CKN to Q1	tPLH	0.86	0.78 + 0.036*SL	0.78 + 0.036*SL	0.78 + 0.036*SL
	tPHL	0.97	0.93 + 0.020*SL	0.94 + 0.017*SL	0.95 + 0.017*SL
	tR	0.24	0.08 + 0.082*SL	0.07 + 0.084*SL	0.05 + 0.085*SL
	tF	0.13	0.07 + 0.029*SL	0.06 + 0.033*SL	0.05 + 0.034*SL
CKN to Q2	tPLH	0.86	0.78 + 0.036*SL	0.78 + 0.037*SL	0.78 + 0.036*SL
	tPHL	0.97	0.93 + 0.021*SL	0.94 + 0.017*SL	0.95 + 0.017*SL
	tR	0.24	0.08 + 0.077*SL	0.06 + 0.084*SL	0.05 + 0.085*SL
	tF	0.13	0.07 + 0.032*SL	0.06 + 0.033*SL	0.05 + 0.034*SL
CKN to Q3	tPLH	0.86	0.78 + 0.037*SL	0.78 + 0.037*SL	0.78 + 0.037*SL
	tPHL	0.97	0.93 + 0.021*SL	0.94 + 0.017*SL	0.96 + 0.016*SL
	tR	0.24	0.08 + 0.082*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	tF	0.13	0.07 + 0.033*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
CKN to QN0	tPLH	0.94	0.86 + 0.039*SL	0.86 + 0.038*SL	0.87 + 0.038*SL
	tPHL	0.76	0.71 + 0.024*SL	0.73 + 0.018*SL	0.75 + 0.016*SL
	tR	0.24	0.08 + 0.083*SL	0.06 + 0.088*SL	0.06 + 0.088*SL
	tF	0.14	0.07 + 0.038*SL	0.08 + 0.032*SL	0.05 + 0.034*SL
CKN to QN1	tPLH	0.94	0.86 + 0.038*SL	0.86 + 0.037*SL	0.87 + 0.037*SL
	tPHL	0.75	0.71 + 0.023*SL	0.73 + 0.018*SL	0.75 + 0.017*SL
	tR	0.25	0.07 + 0.086*SL	0.08 + 0.085*SL	0.06 + 0.086*SL
	tF	0.14	0.07 + 0.035*SL	0.08 + 0.033*SL	0.05 + 0.034*SL
CKN to QN2	tPLH	0.94	0.86 + 0.038*SL	0.86 + 0.037*SL	0.87 + 0.037*SL
	tPHL	0.76	0.71 + 0.024*SL	0.73 + 0.018*SL	0.75 + 0.016*SL
	tR	0.24	0.08 + 0.083*SL	0.07 + 0.085*SL	0.06 + 0.086*SL
	tF	0.14	0.07 + 0.035*SL	0.08 + 0.033*SL	0.05 + 0.034*SL
CKN to QN3	tPLH	0.94	0.86 + 0.039*SL	0.86 + 0.038*SL	0.87 + 0.038*SL
	tPHL	0.76	0.71 + 0.024*SL	0.73 + 0.018*SL	0.75 + 0.016*SL
	tR	0.24	0.08 + 0.083*SL	0.06 + 0.088*SL	0.06 + 0.088*SL
	tF	0.15	0.08 + 0.035*SL	0.08 + 0.032*SL	0.05 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD5X4 Timing Requirements

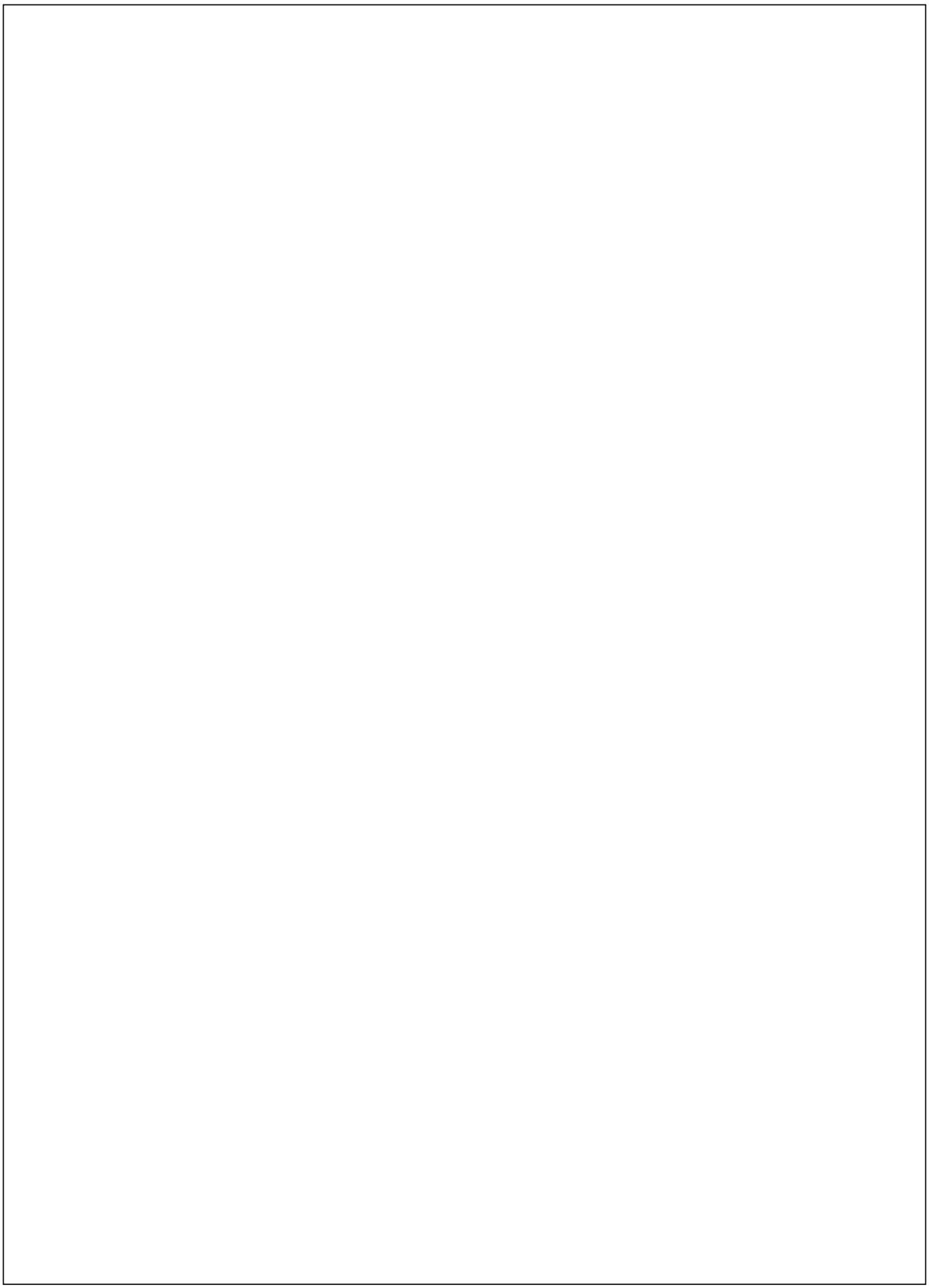
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920

FD5X4 Timing Requirements

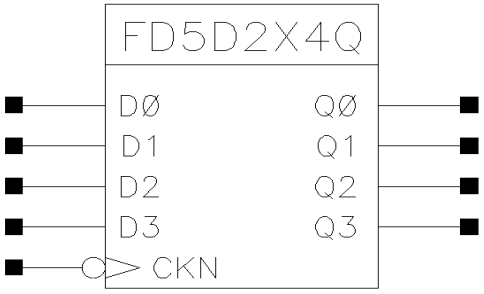
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D0 to CKN)	t_{HD}	0.561
Input Hold Time (D1 to CKN)	t_{HD}	0.561
Input Hold Time (D2 to CKN)	t_{HD}	0.561
Input Hold Time (D3 to CKN)	t_{HD}	0.561
Input Setup Time (D0 to CKN)	t_{SU}	0.000
Input Setup Time (D1 to CKN)	t_{SU}	0.000
Input Setup Time (D2 to CKN)	t_{SU}	0.000
Input Setup Time (D3 to CKN)	t_{SU}	0.000



Inputs: D0, D1, D2, D3, CKN
Output: Q0, Q1, Q2,Q3
Input Loading (SL): All : DO,D1,D2,D3: 3
CKN: 1
Maximum Fanout (Rec. SL):
- FD5D2x4Q: 112
- FD5D4X4Q: 112

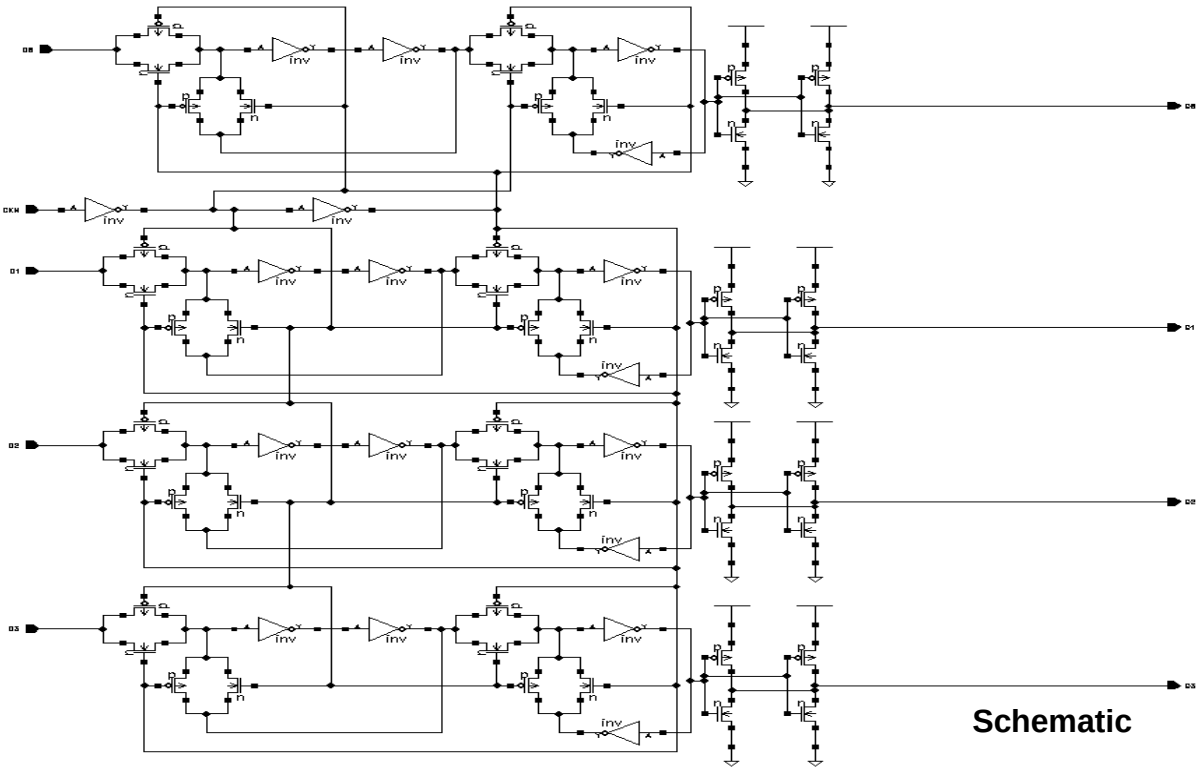
Gate Count:
- FD5D2X4Q: 21
- FD5D4X4Q: 25



Symbol

D	CK	Qn+1
0	↓	0
1	↓	1
x	↑	Qn

Truth Table



Schematic

FD5D2X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	0.74	0.70 + 0.022*SL	0.70 + 0.020*SL	0.72 + 0.019*SL
	tPHL	0.82	0.78 + 0.021*SL	0.81 + 0.013*SL	0.88 + 0.010*SL
	tR	0.20	0.10 + 0.046*SL	0.11 + 0.044*SL	0.09 + 0.045*SL
	tF	0.19	0.14 + 0.025*SL	0.16 + 0.018*SL	0.19 + 0.017*SL
CKN to Q1	tPLH	0.74	0.70 + 0.022*SL	0.70 + 0.019*SL	0.72 + 0.018*SL
	tPHL	0.82	0.78 + 0.021*SL	0.81 + 0.013*SL	0.88 + 0.010*SL
	tR	0.19	0.10 + 0.046*SL	0.11 + 0.042*SL	0.09 + 0.044*SL
	tF	0.19	0.14 + 0.024*SL	0.16 + 0.018*SL	0.19 + 0.016*SL
CKN to Q2	tPLH	0.74	0.70 + 0.022*SL	0.70 + 0.019*SL	0.72 + 0.018*SL
	tPHL	0.82	0.78 + 0.021*SL	0.80 + 0.013*SL	0.88 + 0.010*SL
	tR	0.19	0.10 + 0.046*SL	0.11 + 0.042*SL	0.08 + 0.044*SL
	tF	0.19	0.14 + 0.025*SL	0.16 + 0.018*SL	0.19 + 0.016*SL
CKN to Q3	tPLH	0.74	0.70 + 0.022*SL	0.70 + 0.020*SL	0.72 + 0.019*SL
	tPHL	0.82	0.78 + 0.021*SL	0.80 + 0.013*SL	0.88 + 0.010*SL
	tR	0.20	0.11 + 0.046*SL	0.11 + 0.044*SL	0.09 + 0.045*SL
	tF	0.19	0.14 + 0.025*SL	0.16 + 0.018*SL	0.19 + 0.017*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD5D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D0 to CKN)	tHD	0.561
Input Hold Time (D1 to CKN)	tHD	0.561
Input Hold Time (D2 to CKN)	tHD	0.561
Input Hold Time (D3 to CKN)	tHD	0.561
Input Setup Time (D0 to CKN)	tSU	0.000
Input Setup Time (D1 to CKN)	tSU	0.000
Input Setup Time (D2 to CKN)	tSU	0.000
Input Setup Time (D3 to CKN)	tSU	0.000

FD5D4X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

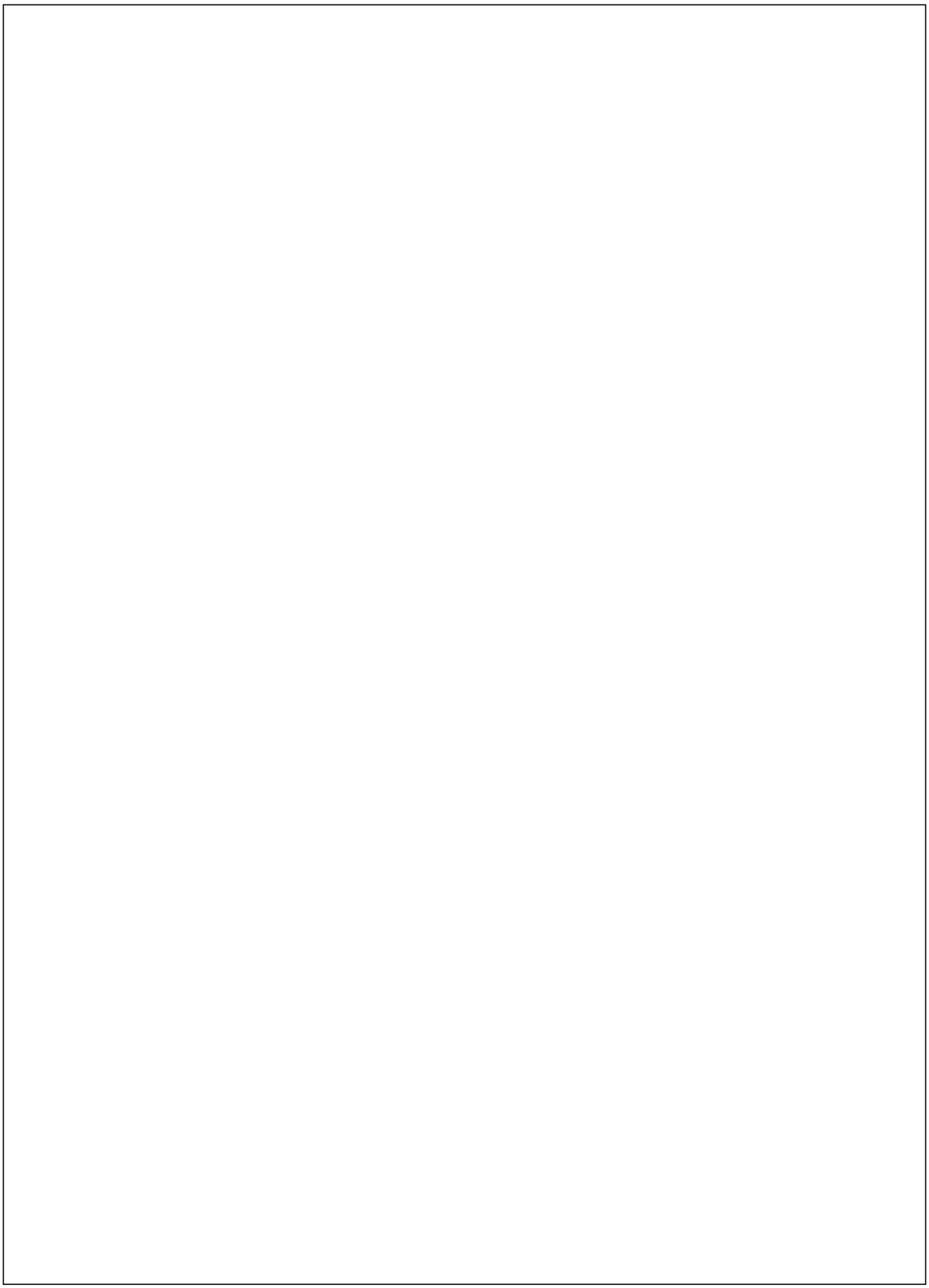
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	0.80	0.78 + 0.013*SL	0.79 + 0.011*SL	0.80 + 0.010*SL
	tPHL	0.85	0.83 + 0.012*SL	0.84 + 0.009*SL	0.89 + 0.006*SL
	tR	0.18	0.14 + 0.019*SL	0.13 + 0.022*SL	0.13 + 0.022*SL
	tF	0.20	0.17 + 0.016*SL	0.18 + 0.011*SL	0.23 + 0.009*SL
CKN to Q1	tPLH	0.80	0.78 + 0.013*SL	0.78 + 0.011*SL	0.80 + 0.009*SL
	tPHL	0.85	0.83 + 0.013*SL	0.84 + 0.009*SL	0.89 + 0.006*SL
	tR	0.17	0.13 + 0.019*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
	tF	0.20	0.17 + 0.015*SL	0.18 + 0.010*SL	0.21 + 0.009*SL
CKN to Q2	tPLH	0.80	0.78 + 0.013*SL	0.78 + 0.011*SL	0.80 + 0.009*SL
	tPHL	0.85	0.83 + 0.013*SL	0.84 + 0.009*SL	0.89 + 0.006*SL
	tR	0.17	0.13 + 0.019*SL	0.13 + 0.021*SL	0.13 + 0.021*SL
	tF	0.20	0.17 + 0.014*SL	0.18 + 0.010*SL	0.21 + 0.009*SL
CKN to Q3	tPLH	0.80	0.78 + 0.013*SL	0.78 + 0.011*SL	0.80 + 0.010*SL
	tPHL	0.85	0.83 + 0.013*SL	0.84 + 0.009*SL	0.89 + 0.006*SL
	tR	0.18	0.14 + 0.019*SL	0.13 + 0.022*SL	0.13 + 0.022*SL
	tF	0.20	0.17 + 0.015*SL	0.18 + 0.011*SL	0.23 + 0.009*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD5D4X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

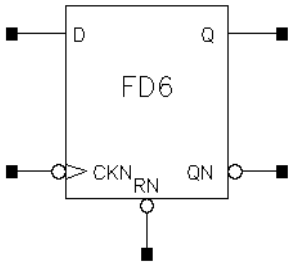
Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D0 to CKN)	tHD	0.561
Input Hold Time (D1 to CKN)	tHD	0.561
Input Hold Time (D2 to CKN)	tHD	0.561
Input Hold Time (D3 to CKN)	tHD	0.561
Input Setup Time (D0 to CKN)	tSU	0.000
Input Setup Time (D1 to CKN)	tSU	0.000
Input Setup Time (D2 to CKN)	tSU	0.000
Input Setup Time (D3 to CKN)	tSU	0.000



Inputs: D, CKN, RN
Outputs: Q, QN
Input Loading (SL):
- D: 3
- CKN: 1
- RN: 2

Maximum Fanout (Rec. SL):
- FD6: All : 28
- FD6D2: All : 56

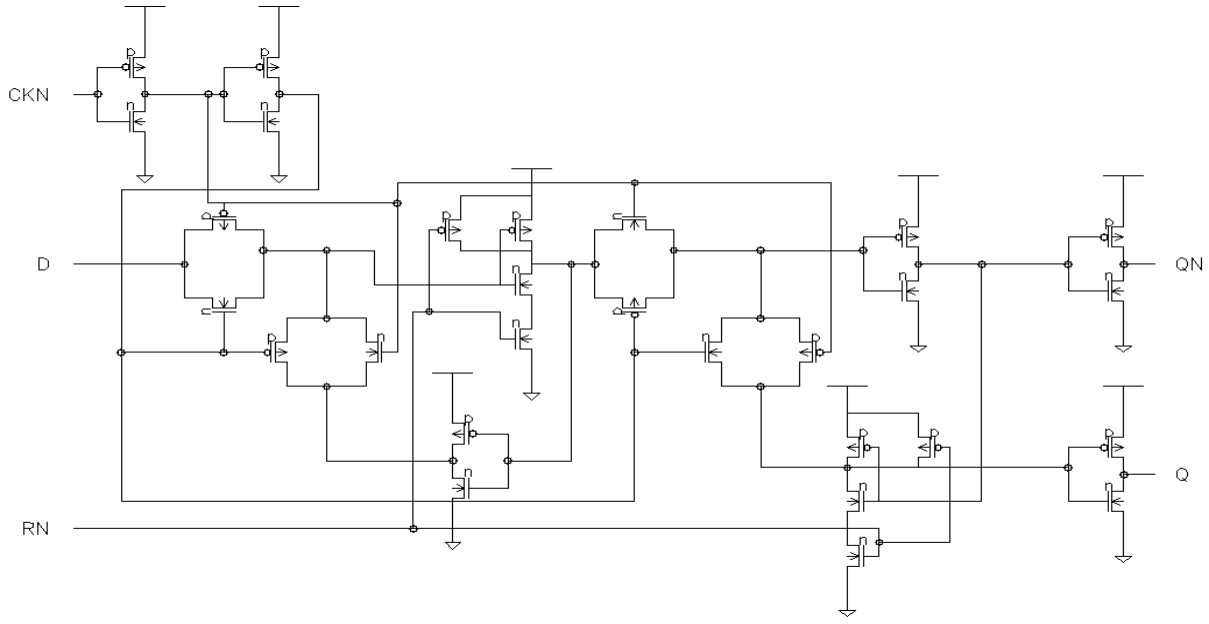
Gate Count:
- FD6: 7
- FD6D2: 8



Symbol

D	RN	CK	Qn+1	QNn+1
0	1	↓	0	1
1	1	↓	1	0
x	0	x	0	1
x	1	↑	Qn	QNn

Truth Table



Schematic

FD6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	t_{PLH}	0.78	0.71 + 0.035*SL	0.71 + 0.036*SL	0.70 + 0.036*SL
	t_{PHL}	0.69	0.65 + 0.022*SL	0.66 + 0.017*SL	0.68 + 0.016*SL
	t_R	0.25	0.09 + 0.079*SL	0.08 + 0.082*SL	0.06 + 0.084*SL
	t_F	0.13	0.06 + 0.034*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
RN to Q	t_{PHL}	0.37	0.32 + 0.027*SL	0.35 + 0.017*SL	0.37 + 0.016*SL
	t_F	0.17	0.10 + 0.034*SL	0.11 + 0.030*SL	0.06 + 0.033*SL
CKN to QN	t_{PLH}	0.64	0.57 + 0.037*SL	0.57 + 0.036*SL	0.57 + 0.036*SL
	t_{PHL}	0.62	0.57 + 0.024*SL	0.59 + 0.018*SL	0.62 + 0.016*SL
	t_R	0.24	0.07 + 0.082*SL	0.07 + 0.082*SL	0.05 + 0.083*SL
	t_F	0.14	0.07 + 0.035*SL	0.08 + 0.032*SL	0.07 + 0.032*SL
RN to QN	t_{PLH}	0.63	0.55 + 0.036*SL	0.55 + 0.036*SL	0.55 + 0.036*SL
	t_R	0.24	0.09 + 0.076*SL	0.07 + 0.082*SL	0.05 + 0.083*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD6 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D to CKN)	t_{HD}	0.287
Input Setup Time (D to CKN)	t_{SU}	0.123
Recovery Time (RN)	t_{RC}	0.139

FD6D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

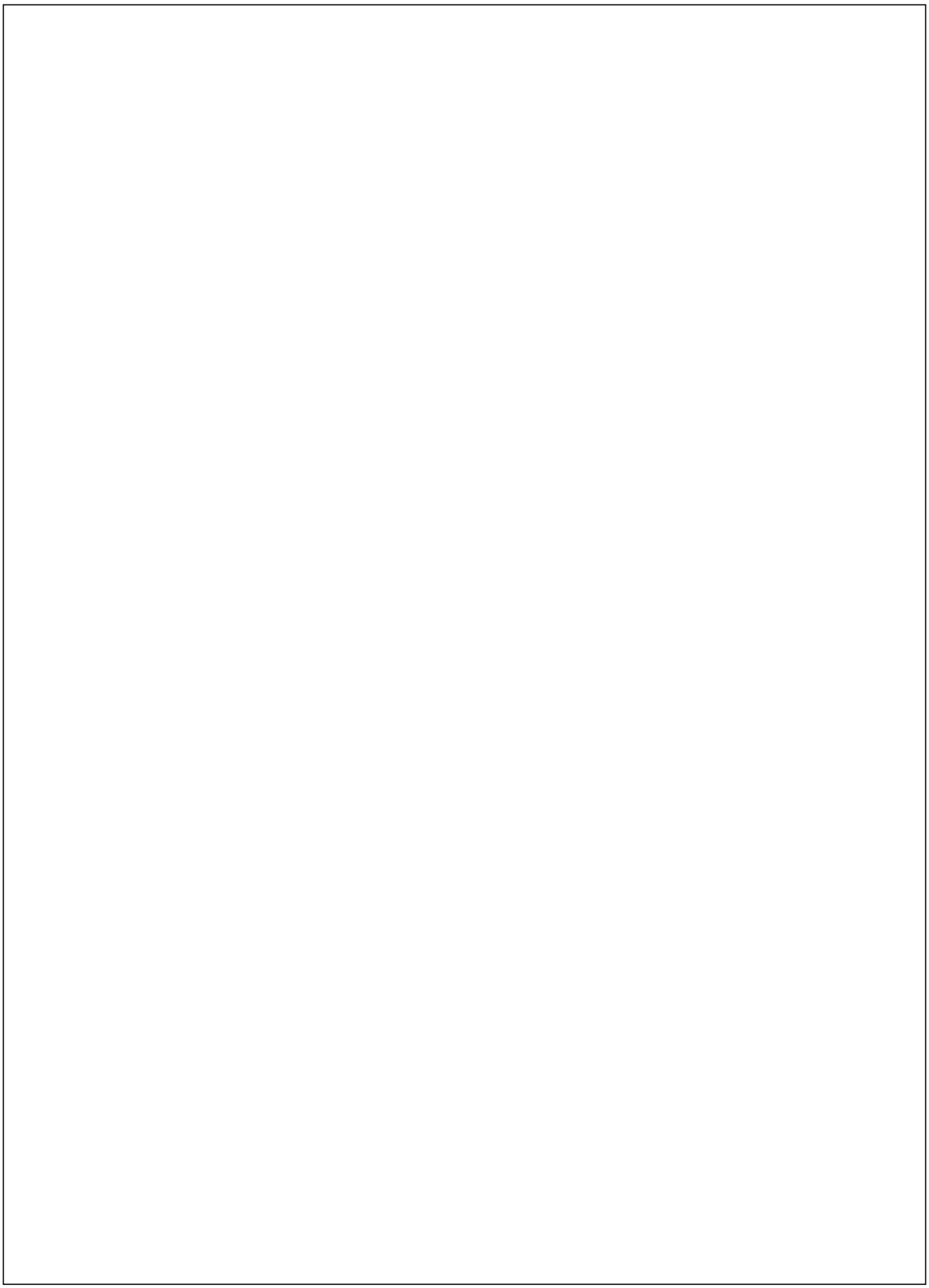
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	t_{PLH}	0.82	0.78 + 0.021*SL	0.79 + 0.018*SL	0.79 + 0.018*SL
	t_{PHL}	0.73	0.70 + 0.014*SL	0.71 + 0.010*SL	0.75 + 0.008*SL
	t_R	0.18	0.10 + 0.042*SL	0.10 + 0.040*SL	0.07 + 0.042*SL
	t_F	0.12	0.08 + 0.019*SL	0.09 + 0.017*SL	0.09 + 0.017*SL
RN to Q	t_{PHL}	0.38	0.35 + 0.016*SL	0.36 + 0.010*SL	0.40 + 0.008*SL
	t_F	0.16	0.12 + 0.015*SL	0.12 + 0.016*SL	0.12 + 0.016*SL
CKN to QN	t_{PLH}	0.63	0.59 + 0.021*SL	0.60 + 0.018*SL	0.60 + 0.018*SL
	t_{PHL}	0.63	0.61 + 0.014*SL	0.62 + 0.010*SL	0.65 + 0.008*SL
	t_R	0.17	0.08 + 0.041*SL	0.08 + 0.041*SL	0.06 + 0.042*SL
	t_F	0.14	0.11 + 0.016*SL	0.11 + 0.015*SL	0.10 + 0.016*SL
RN to QN	t_{PLH}	0.62	0.58 + 0.020*SL	0.59 + 0.018*SL	0.59 + 0.018*SL
	t_R	0.17	0.10 + 0.036*SL	0.08 + 0.041*SL	0.06 + 0.042*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD6D2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

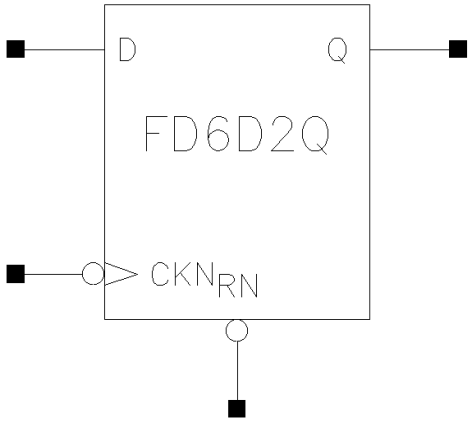
Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D to CKN)	t_{HD}	0.287
Input Setup Time (D to CKN)	t_{SU}	0.123
Recovery Time (RN)	t_{RC}	0.139



Inputs: D, CKN, RN
Output: Q
Input Loading (SL):
- FD6D2Q: D: 3, CKN : 1
  RN : 2
- FD6D4Q: D: 3, CKN : 1
  RN : 2

Maximum Fanout (Rec. SL): All :
- FD6D2Q: 56
- FD6D4Q: 112

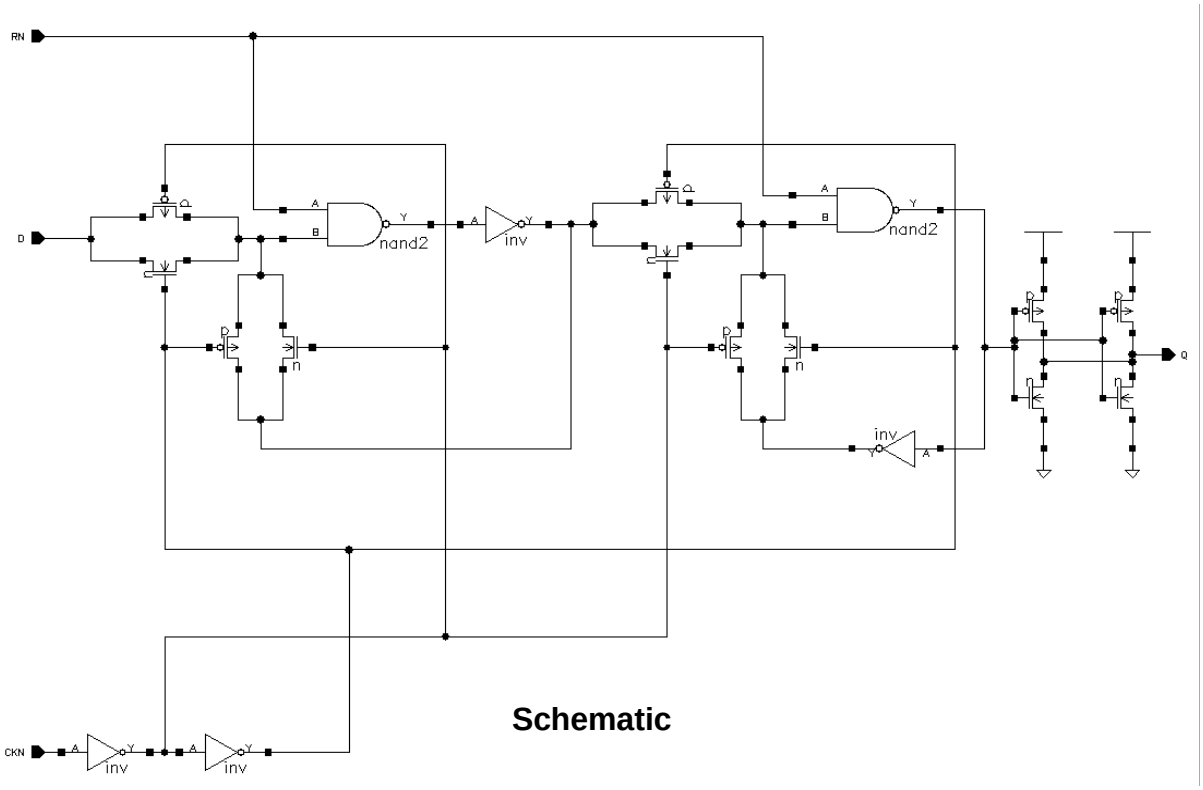
Gate Count:
- FD6D2Q: 7
- FD6D4Q: 8



Symbol

D	RN	CK	Qn+1
0	1	↓	0
1	1	↓	1
x	0	x	0
x	1	↑	Qn

Truth Table



Schematic

FD6D2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.61	0.55 + 0.026*SL	0.57 + 0.020*SL	0.61 + 0.019*SL
	tPHL	0.53	0.49 + 0.021*SL	0.51 + 0.013*SL	0.58 + 0.010*SL
	tR	0.22	0.13 + 0.042*SL	0.13 + 0.042*SL	0.12 + 0.042*SL
	tF	0.16	0.11 + 0.023*SL	0.13 + 0.019*SL	0.18 + 0.016*SL
RN to Q	tPHL	0.54	0.49 + 0.023*SL	0.52 + 0.013*SL	0.60 + 0.009*SL
	tF	0.23	0.19 + 0.017*SL	0.20 + 0.016*SL	0.20 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD6D2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.342
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (RN)	tRC	0.139

FD6D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

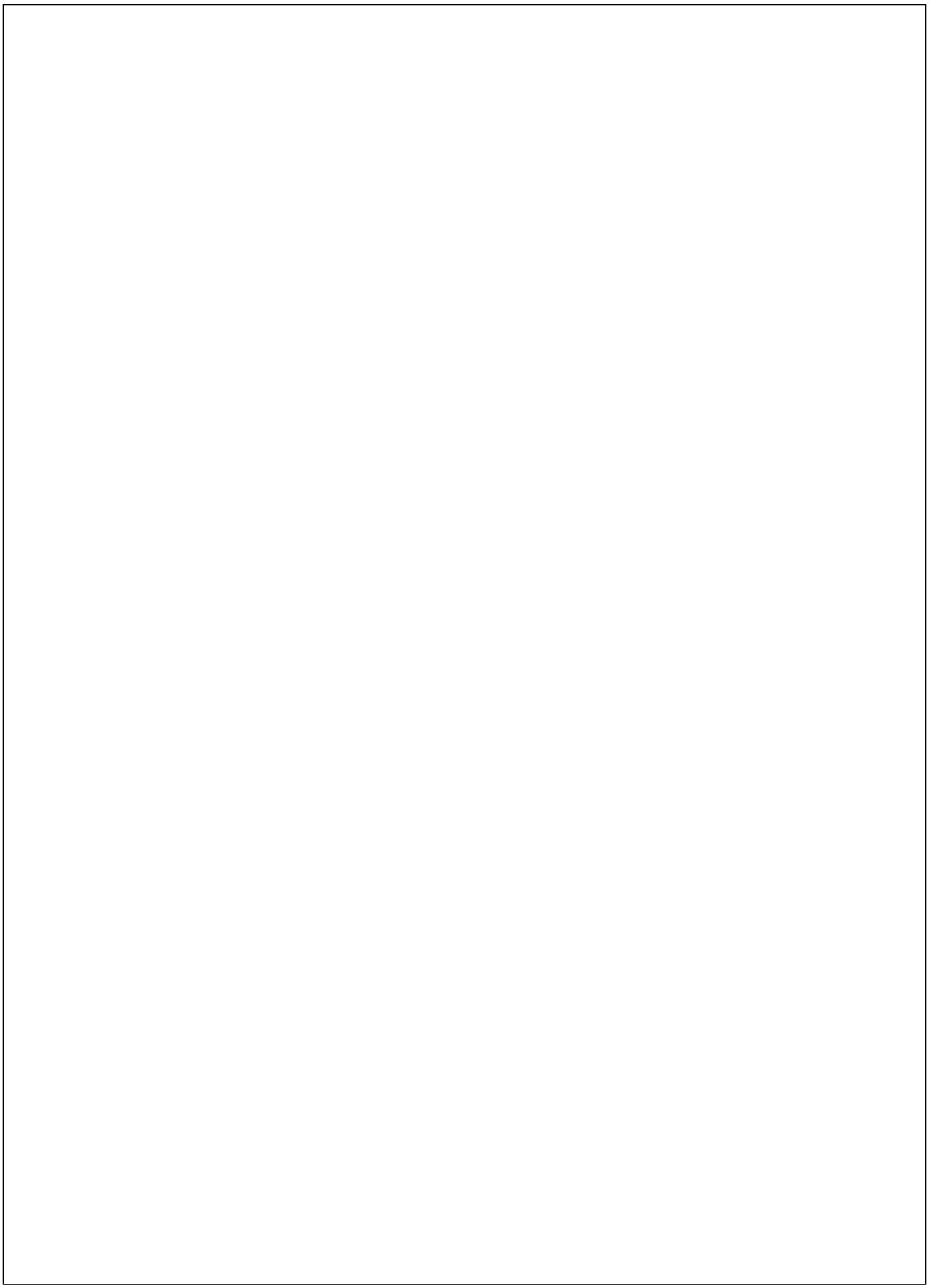
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.66	0.63 + 0.015*SL	0.64 + 0.011*SL	0.67 + 0.010*SL
	tPHL	0.56	0.53 + 0.015*SL	0.55 + 0.009*SL	0.60 + 0.006*SL
	tR	0.23	0.19 + 0.019*SL	0.19 + 0.020*SL	0.17 + 0.021*SL
	tF	0.18	0.15 + 0.013*SL	0.16 + 0.011*SL	0.21 + 0.009*SL
RN to Q	tPHL	0.59	0.56 + 0.012*SL	0.57 + 0.009*SL	0.63 + 0.006*SL
	tF	0.23	0.21 + 0.013*SL	0.22 + 0.009*SL	0.24 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD6D4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

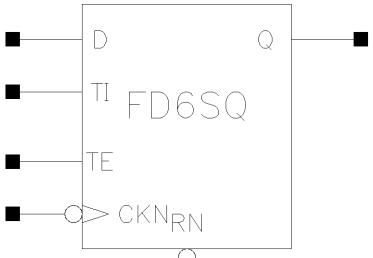
Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.342
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (RN)	tRC	0.139



Inputs: D, TI, TE, CK
Output: Q
Input Loading (SL):
- FD6SD2Q: D, CK, TI : 1
  RN, TE : 2
- FD6SD4Q: D, CK, TI : 1
  RN, TE : 2

Maximum Fanout (Rec. SL):
- FD6SD2Q: 56
- FD6SD4Q: 112

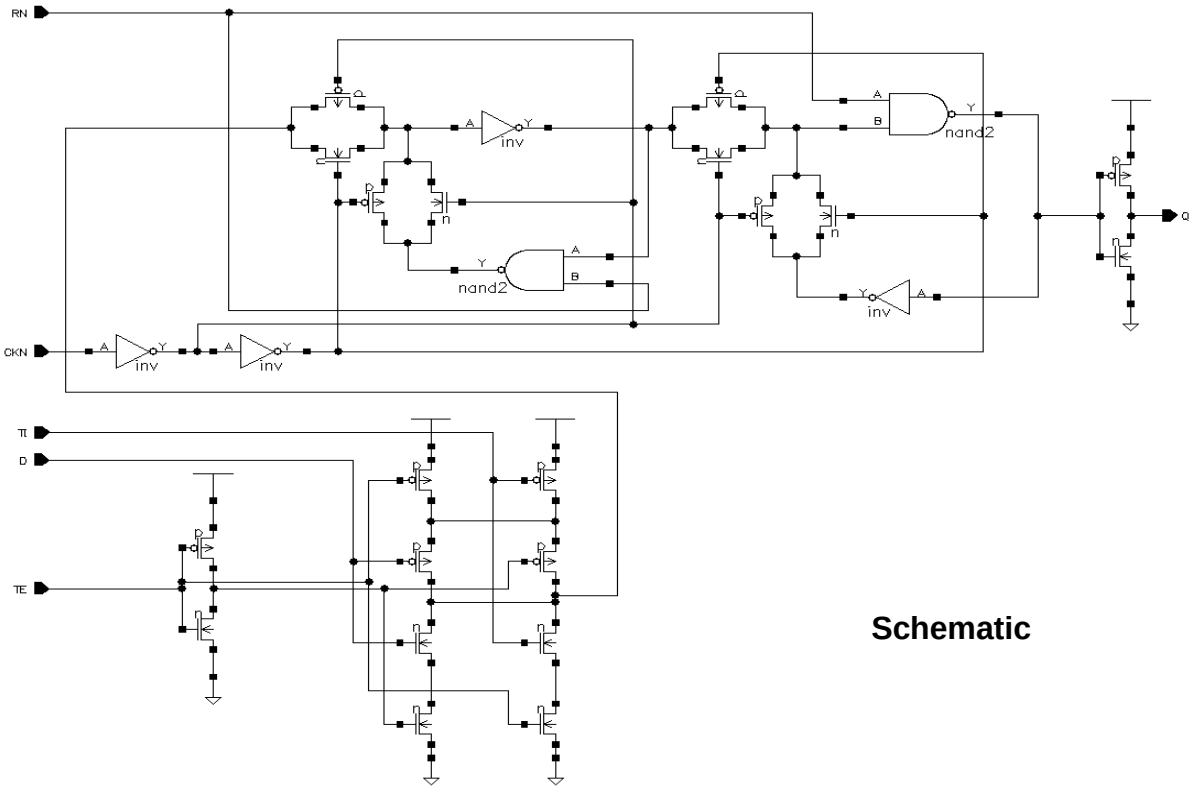
Gate Count:
- FD6SD2Q: 10
- FD6SD4Q: 11



Symbol

D	RN	TI	TE	CK	Qn+1
0	1	x	0	↓	0
1	1	x	0	↓	1
x	1	0	1	↓	0
x	1	1	1	↓	1
x	0	x	x	x	0
x	1	x	x	↑	Qn

Truth Table



Schematic

FD6SD2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.69	0.65 + 0.023*SL	0.66 + 0.019*SL	0.67 + 0.018*SL
	tPHL	0.60	0.57 + 0.015*SL	0.59 + 0.011*SL	0.63 + 0.008*SL
	tR	0.18	0.10 + 0.044*SL	0.10 + 0.042*SL	0.08 + 0.043*SL
	tF	0.13	0.09 + 0.018*SL	0.10 + 0.016*SL	0.10 + 0.016*SL
RN to Q	tPHL	0.40	0.36 + 0.019*SL	0.39 + 0.011*SL	0.44 + 0.008*SL
	tF	0.17	0.13 + 0.021*SL	0.14 + 0.014*SL	0.13 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD6SD2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.233
Input Hold Time (TE to CKN)	tHD	0.233
Input Hold Time (TI to CKN)	tHD	0.123
Input Setup Time (D to CKN)	tSU	0.342
Input Setup Time (TE to CKN)	tSU	0.452
Input Setup Time (TI to CKN)	tSU	0.397
Recovery Time (RN)	tRC	0.139

FD6SD4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

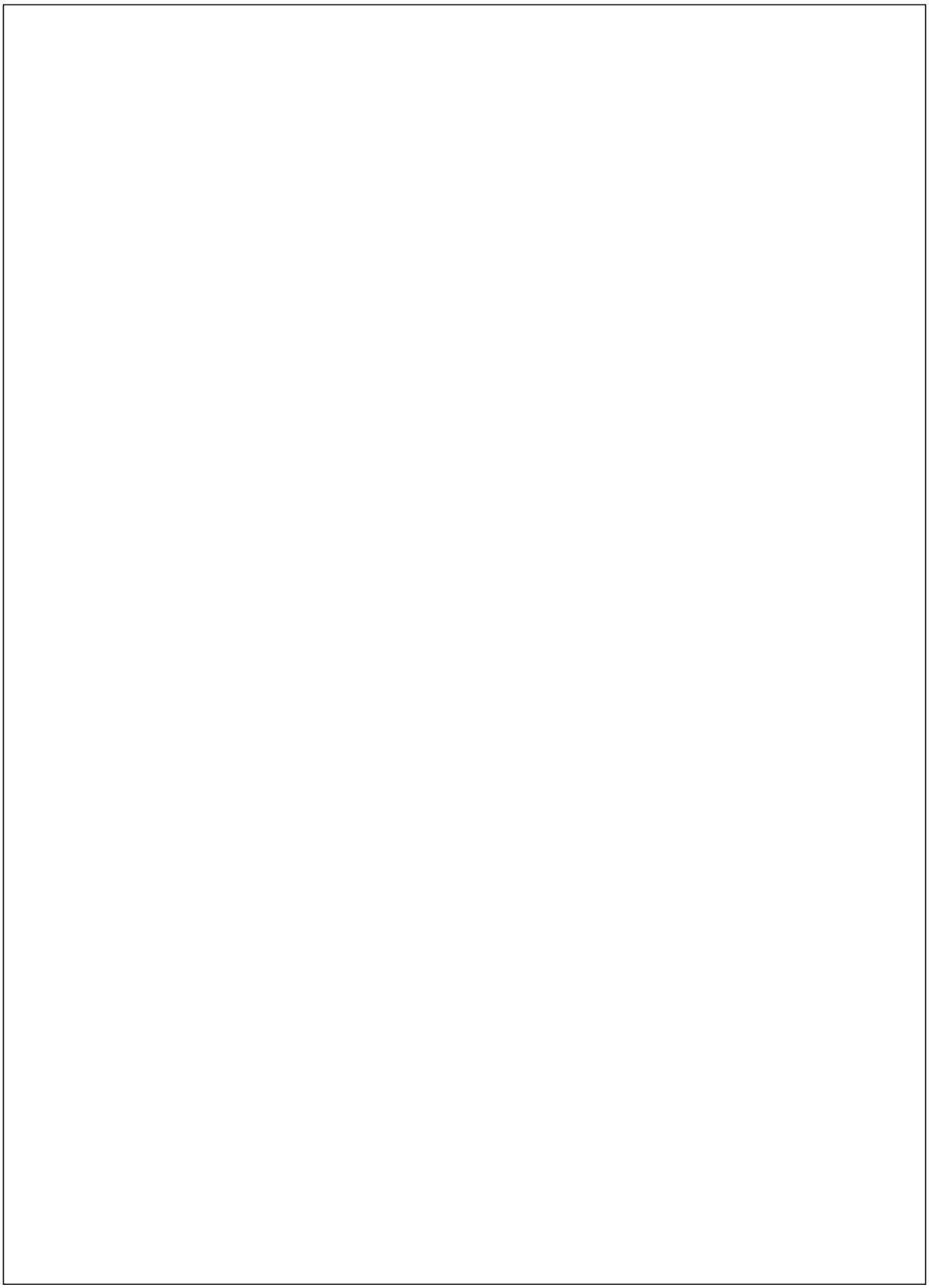
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.74	0.72 + 0.010*SL	0.72 + 0.010*SL	0.74 + 0.009*SL
	tPHL	0.65	0.63 + 0.007*SL	0.63 + 0.007*SL	0.68 + 0.005*SL
	tR	0.17	0.13 + 0.020*SL	0.13 + 0.020*SL	0.12 + 0.021*SL
	tF	0.15	0.13 + 0.008*SL	0.13 + 0.008*SL	0.13 + 0.008*SL
RN to Q	tPHL	0.46	0.43 + 0.011*SL	0.45 + 0.007*SL	0.49 + 0.005*SL
	tF	0.18	0.16 + 0.010*SL	0.17 + 0.007*SL	0.17 + 0.007*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD6SD4Q Timing Requirements

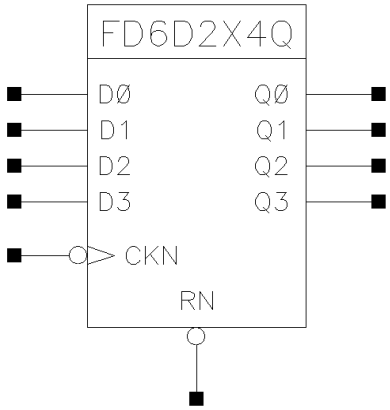
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.233
Input Hold Time (TE to CKN)	tHD	0.233
Input Hold Time (TI to CKN)	tHD	0.178
Input Setup Time (D to CKN)	tSU	0.342
Input Setup Time (TE to CKN)	tSU	0.452
Input Setup Time (TI to CKN)	tSU	0.397
Recovery Time (RN)	tRC	0.139



Inputs: D0, D1, D2, D3, CKN, RN
Output: Q0, Q1, Q2, Q3
Input Loading (SL): All: DO,D1,D2,D3: 3
CKN: 1, RN: 8
Maximum Fanout (Rec. SL):
- FD6D2X4Q: 56
- FD6D4X4Q: 112

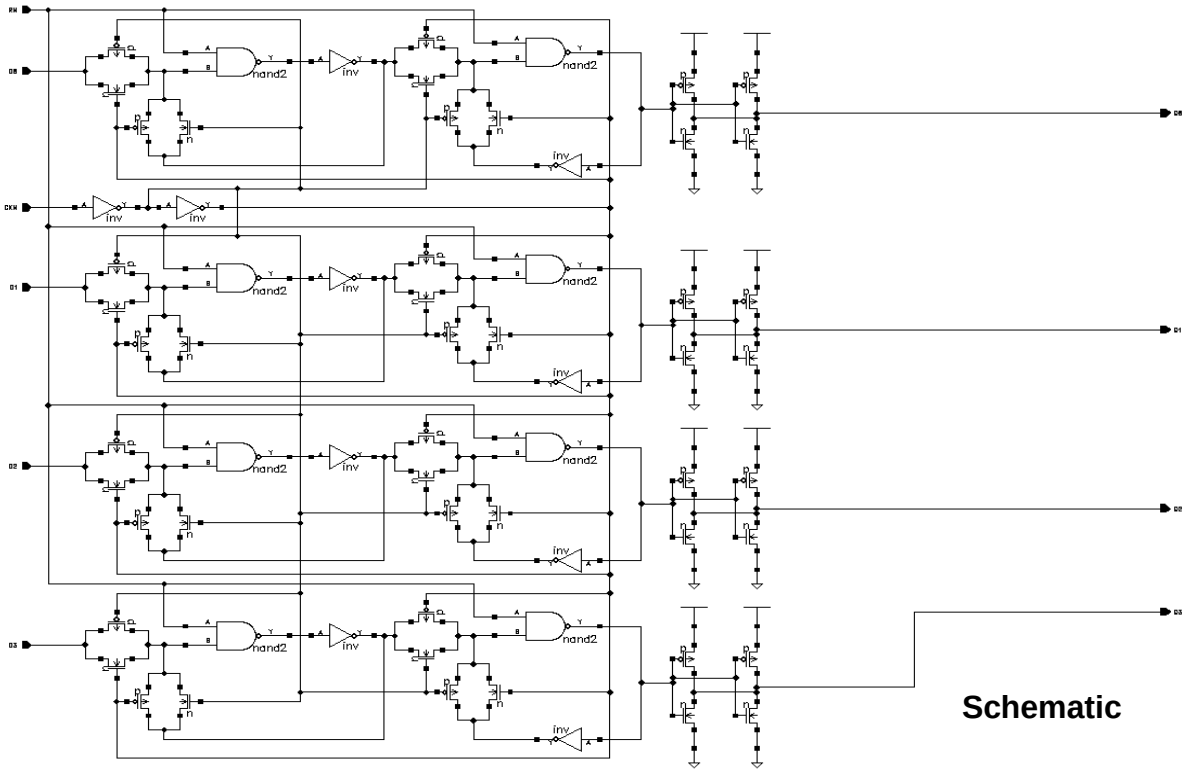
Gate Count:
- FD6D2X4Q: 25
- FD6D4X4Q: 29



Symbol

D	RN	CK	Qn+1
0	1	↓	0
1	1	↓	1
x	0	x	0
x	1	↑	Qn

Truth Table



Schematic

FD6D2X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	t_{PLH}	0.81	0.76 + 0.024*SL	0.77 + 0.021*SL	0.81 + 0.019*SL
	t_{PHL}	0.83	0.79 + 0.021*SL	0.81 + 0.014*SL	0.89 + 0.010*SL
	t_R	0.21	0.12 + 0.045*SL	0.13 + 0.042*SL	0.12 + 0.043*SL
	t_F	0.19	0.14 + 0.025*SL	0.16 + 0.018*SL	0.20 + 0.016*SL
RN to Q0	t_{PHL}	0.54	0.49 + 0.022*SL	0.52 + 0.013*SL	0.60 + 0.009*SL
	t_F	0.22	0.19 + 0.014*SL	0.19 + 0.016*SL	0.21 + 0.015*SL
CKN to Q1	t_{PLH}	0.80	0.76 + 0.024*SL	0.76 + 0.021*SL	0.80 + 0.019*SL
	t_{PHL}	0.83	0.78 + 0.021*SL	0.81 + 0.014*SL	0.88 + 0.010*SL
	t_R	0.21	0.12 + 0.047*SL	0.13 + 0.044*SL	0.12 + 0.044*SL
	t_F	0.19	0.14 + 0.025*SL	0.16 + 0.018*SL	0.20 + 0.016*SL
RN to Q1	t_{PHL}	0.53	0.49 + 0.022*SL	0.52 + 0.013*SL	0.60 + 0.009*SL
	t_F	0.22	0.20 + 0.014*SL	0.19 + 0.017*SL	0.20 + 0.016*SL
CKN to Q2	t_{PLH}	0.80	0.75 + 0.024*SL	0.76 + 0.021*SL	0.80 + 0.019*SL
	t_{PHL}	0.83	0.78 + 0.021*SL	0.81 + 0.014*SL	0.88 + 0.010*SL
	t_R	0.21	0.12 + 0.047*SL	0.13 + 0.044*SL	0.12 + 0.044*SL
	t_F	0.19	0.14 + 0.025*SL	0.16 + 0.018*SL	0.20 + 0.017*SL
RN to Q2	t_{PHL}	0.53	0.49 + 0.022*SL	0.52 + 0.013*SL	0.60 + 0.009*SL
	t_F	0.22	0.20 + 0.014*SL	0.19 + 0.017*SL	0.20 + 0.016*SL
CKN to Q3	t_{PLH}	0.81	0.76 + 0.024*SL	0.77 + 0.021*SL	0.81 + 0.019*SL
	t_{PHL}	0.83	0.79 + 0.021*SL	0.81 + 0.014*SL	0.89 + 0.010*SL
	t_R	0.21	0.12 + 0.045*SL	0.13 + 0.042*SL	0.12 + 0.043*SL
	t_F	0.19	0.14 + 0.025*SL	0.16 + 0.018*SL	0.20 + 0.016*SL
RN to Q3	t_{PHL}	0.54	0.49 + 0.022*SL	0.52 + 0.013*SL	0.60 + 0.009*SL
	t_F	0.22	0.19 + 0.014*SL	0.19 + 0.016*SL	0.21 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD6D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D0 to CKN)	t_{HD}	0.506
Input Hold Time (D1 to CKN)	t_{HD}	0.506
Input Hold Time (D2 to CKN)	t_{HD}	0.506

FD6D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Input Hold Time (D3 to CKN)	t_{HD}	0.506
Input Setup Time (D0 to CKN)	t_{SU}	0.000
Input Setup Time (D1 to CKN)	t_{SU}	0.000
Input Setup Time (D2 to CKN)	t_{SU}	0.000
Input Setup Time (D3 to CKN)	t_{SU}	0.000
Recovery Time (RN)	t_{RC}	0.139

FD6D4X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	t_{PLH}	0.89	0.86 + 0.015*SL	0.87 + 0.011*SL	0.90 + 0.010*SL
	t_{PHL}	0.86	0.83 + 0.013*SL	0.84 + 0.009*SL	0.90 + 0.006*SL
	t_R	0.23	0.19 + 0.020*SL	0.18 + 0.020*SL	0.17 + 0.021*SL
	t_F	0.20	0.18 + 0.012*SL	0.18 + 0.011*SL	0.23 + 0.008*SL
RN to Q0	t_{PHL}	0.59	0.56 + 0.013*SL	0.57 + 0.009*SL	0.63 + 0.006*SL
	t_F	0.23	0.21 + 0.012*SL	0.22 + 0.009*SL	0.25 + 0.008*SL
CKN to Q1	t_{PLH}	0.88	0.85 + 0.015*SL	0.86 + 0.011*SL	0.89 + 0.010*SL
	t_{PHL}	0.85	0.83 + 0.013*SL	0.84 + 0.009*SL	0.89 + 0.007*SL
	t_R	0.23	0.19 + 0.017*SL	0.18 + 0.021*SL	0.17 + 0.021*SL
	t_F	0.21	0.18 + 0.010*SL	0.18 + 0.011*SL	0.22 + 0.009*SL
RN to Q1	t_{PHL}	0.58	0.56 + 0.013*SL	0.57 + 0.009*SL	0.63 + 0.006*SL
	t_F	0.24	0.21 + 0.012*SL	0.22 + 0.009*SL	0.25 + 0.008*SL
CKN to Q2	t_{PLH}	0.88	0.85 + 0.015*SL	0.86 + 0.011*SL	0.89 + 0.010*SL
	t_{PHL}	0.85	0.83 + 0.013*SL	0.84 + 0.009*SL	0.89 + 0.007*SL
	t_R	0.23	0.20 + 0.016*SL	0.18 + 0.021*SL	0.17 + 0.022*SL
	t_F	0.21	0.18 + 0.011*SL	0.19 + 0.011*SL	0.23 + 0.009*SL
RN to Q2	t_{PHL}	0.58	0.56 + 0.013*SL	0.57 + 0.009*SL	0.62 + 0.006*SL
	t_F	0.24	0.21 + 0.012*SL	0.22 + 0.009*SL	0.25 + 0.008*SL
CKN to Q3	t_{PLH}	0.89	0.86 + 0.015*SL	0.87 + 0.011*SL	0.90 + 0.010*SL
	t_{PHL}	0.86	0.83 + 0.013*SL	0.84 + 0.009*SL	0.89 + 0.007*SL
	t_R	0.23	0.20 + 0.016*SL	0.18 + 0.020*SL	0.18 + 0.021*SL
	t_F	0.20	0.18 + 0.011*SL	0.18 + 0.011*SL	0.23 + 0.009*SL
RN to Q3	t_{PHL}	0.59	0.56 + 0.013*SL	0.57 + 0.009*SL	0.63 + 0.006*SL
	t_F	0.23	0.21 + 0.012*SL	0.22 + 0.009*SL	0.25 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD6D4X4Q Timing Requirements

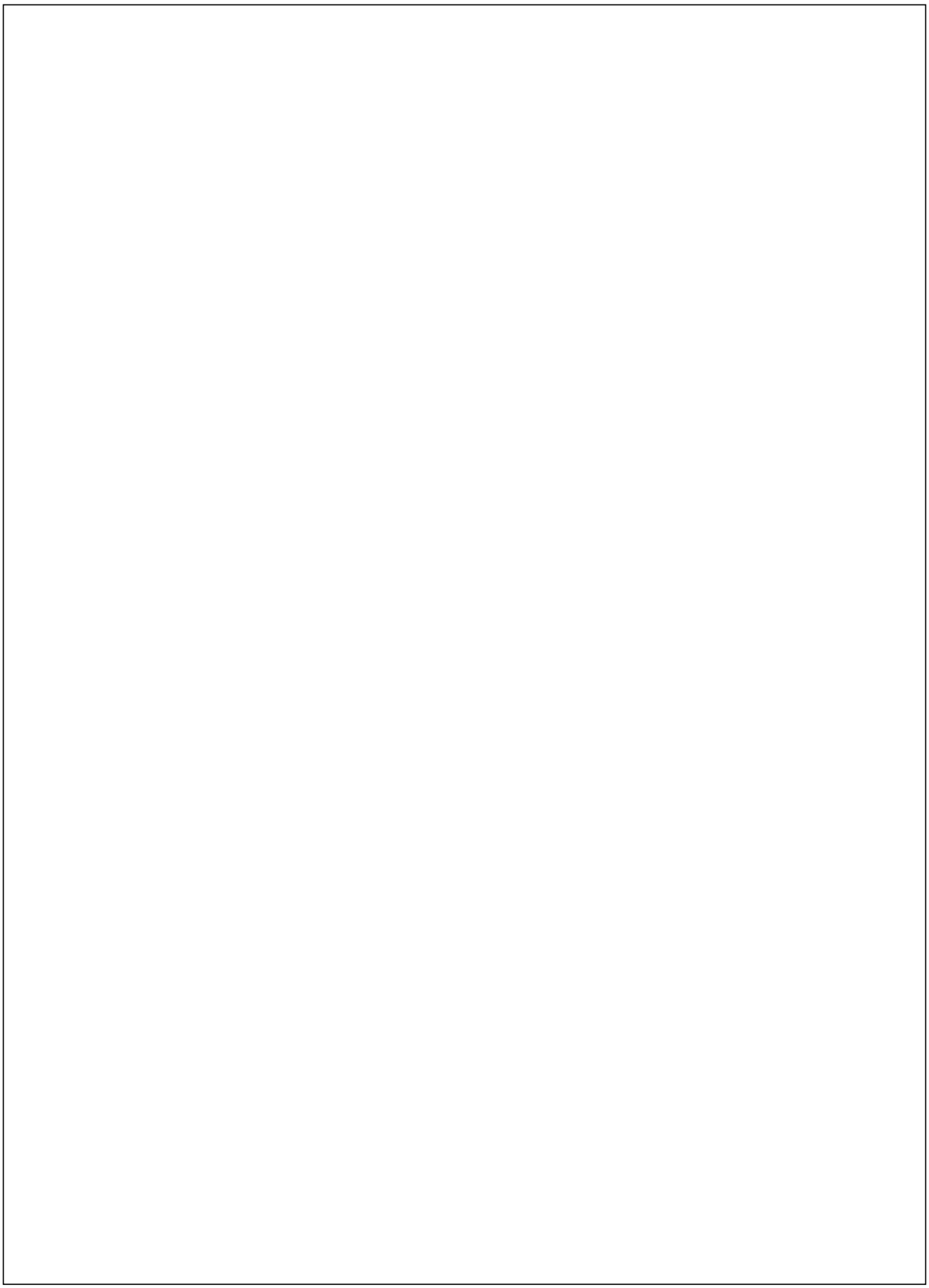
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D0 to CKN)	t_{HD}	0.506
Input Hold Time (D1 to CKN)	t_{HD}	0.506
Input Hold Time (D2 to CKN)	t_{HD}	0.506
Input Hold Time (D3 to CKN)	t_{HD}	0.506
Input Setup Time (D0 to CKN)	t_{SU}	0.000

FD6D4X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

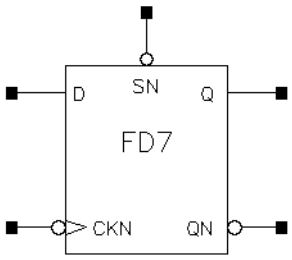
Parameter	Symbol	Value [ns]
Input Setup Time (D1 to CKN)	t_{SU}	0.000
Input Setup Time (D2 to CKN)	t_{SU}	0.000
Input Setup Time (D3 to CKN)	t_{SU}	0.000
Recovery Time (RN)	t_{RC}	0.139



Inputs: D, CK, SN
Outputs: Q, QN
Input Loading (SL):
- D: 3
- CKN: 1
- SN: 2

Maximum Fanout (Rec. SL):
- FD7: All : 28
- FD7D2: All : 56

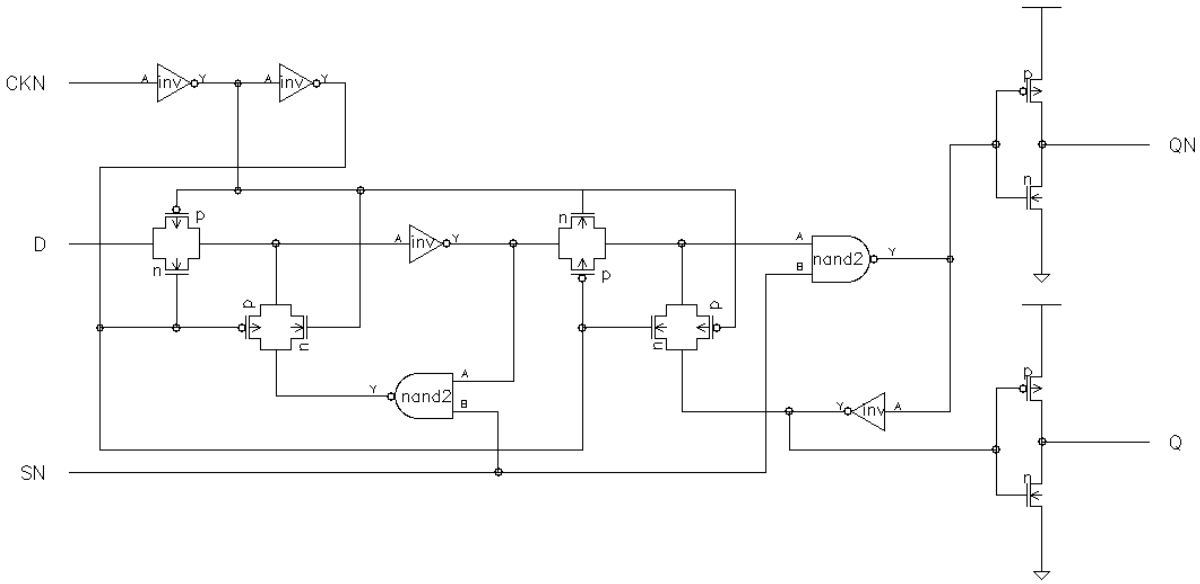
Gate Count:
- FD7: 7
- FD7D2: 8



Symbol

D	SN	CK	Qn+1	QNn+1
0	1	↓	0	1
1	1	↓	1	0
x	0	x	1	0
x	1	↑	Qn	QNn

Truth Table



Schematic

FD7 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	t_{PLH}	0.50	0.43 + 0.035*SL	0.43 + 0.036*SL	0.43 + 0.036*SL
	t_R	0.24	0.07 + 0.082*SL	0.07 + 0.082*SL	0.05 + 0.083*SL
CKN to Q	t_{PLH}	0.70	0.63 + 0.036*SL	0.63 + 0.036*SL	0.64 + 0.036*SL
	t_{PHL}	0.75	0.70 + 0.022*SL	0.72 + 0.017*SL	0.73 + 0.016*SL
	t_R	0.23	0.07 + 0.081*SL	0.06 + 0.083*SL	0.05 + 0.083*SL
	t_F	0.13	0.06 + 0.035*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
SN to QN	t_{PHL}	0.40	0.34 + 0.029*SL	0.37 + 0.018*SL	0.40 + 0.016*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.030*SL	0.08 + 0.032*SL
CKN to QN	t_{PLH}	0.71	0.63 + 0.040*SL	0.64 + 0.036*SL	0.64 + 0.036*SL
	t_{PHL}	0.60	0.55 + 0.025*SL	0.57 + 0.018*SL	0.60 + 0.016*SL
	t_R	0.25	0.09 + 0.085*SL	0.09 + 0.081*SL	0.06 + 0.083*SL
	t_F	0.14	0.07 + 0.037*SL	0.09 + 0.031*SL	0.06 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD7 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D to CKN)	t_{HD}	0.342
Input Setup Time (D to CKN)	t_{SU}	0.178
Recovery Time (SN)	t_{RC}	0.139

FD7D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

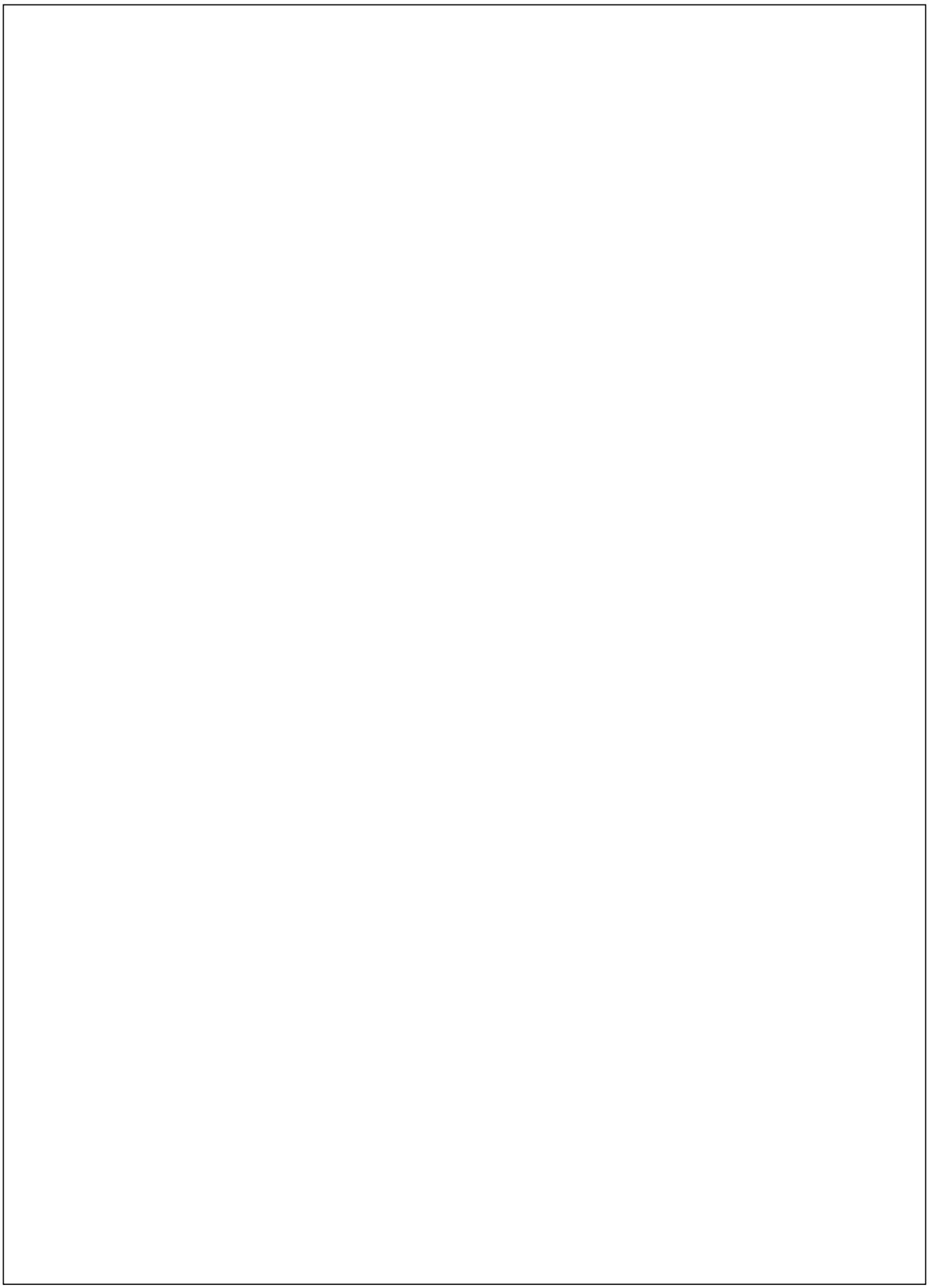
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	t_{PLH}	0.54	0.50 + 0.016*SL	0.50 + 0.018*SL	0.49 + 0.018*SL
	t_R	0.16	0.08 + 0.043*SL	0.08 + 0.040*SL	0.05 + 0.042*SL
CKN to Q	t_{PLH}	0.74	0.70 + 0.016*SL	0.70 + 0.018*SL	0.69 + 0.018*SL
	t_{PHL}	0.80	0.78 + 0.013*SL	0.79 + 0.009*SL	0.81 + 0.008*SL
	t_R	0.16	0.10 + 0.032*SL	0.07 + 0.041*SL	0.05 + 0.042*SL
	t_F	0.13	0.09 + 0.019*SL	0.10 + 0.015*SL	0.09 + 0.016*SL
SN to QN	t_{PHL}	0.40	0.36 + 0.018*SL	0.38 + 0.011*SL	0.43 + 0.008*SL
	t_F	0.16	0.13 + 0.018*SL	0.14 + 0.015*SL	0.13 + 0.015*SL
CKN to QN	t_{PLH}	0.70	0.66 + 0.022*SL	0.67 + 0.019*SL	0.68 + 0.018*SL
	t_{PHL}	0.61	0.58 + 0.016*SL	0.59 + 0.010*SL	0.63 + 0.008*SL
	t_R	0.18	0.10 + 0.044*SL	0.11 + 0.040*SL	0.08 + 0.042*SL
	t_F	0.13	0.09 + 0.018*SL	0.10 + 0.016*SL	0.10 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD7D2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

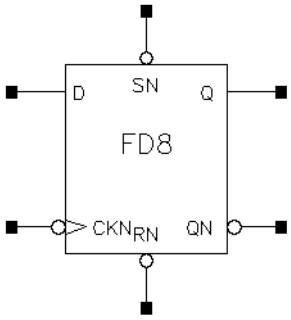
Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D to CKN)	t_{HD}	0.342
Input Setup Time (D to CKN)	t_{SU}	0.178
Recovery Time (SN)	t_{RC}	0.139



Inputs: D, CKN, SN, RN
Outputs: Q, QN
Input Loading (SL):
- D: 3
- CKN: 1
- SN, RN: 2

Maximum Fanout (Rec. SL):
- FD8: All : 28
- FD8D2: All : 56

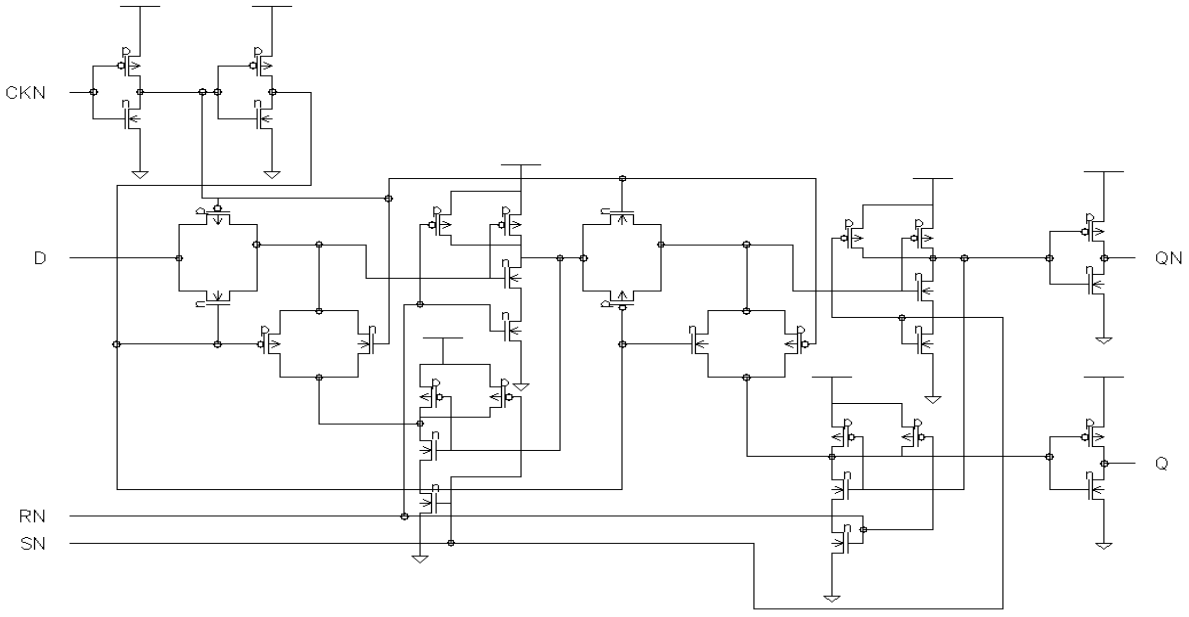
Gate Count:
- FD8: 8
- FD8D2: 9



Symbol

D	SN	RN	CK	Qn+1	QNn+1
0	1	1	↓	0	1
1	1	1	↓	1	0
x	0	1	x	1	0
x	1	0	x	0	1
x	0	0	x	0	0
x	1	1	↑	Qn	QNn

Truth Table



Schematic

FD8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.79	0.71 + 0.039*SL	0.72 + 0.037*SL	0.71 + 0.037*SL
	tPHL	0.74	0.70 + 0.023*SL	0.72 + 0.017*SL	0.73 + 0.016*SL
	tR	0.26	0.09 + 0.082*SL	0.08 + 0.085*SL	0.06 + 0.087*SL
	tF	0.14	0.07 + 0.035*SL	0.08 + 0.031*SL	0.05 + 0.032*SL
RN to Q	tPLH	0.22	0.13 + 0.042*SL	0.15 + 0.037*SL	0.15 + 0.037*SL
	tPHL	0.37	0.32 + 0.027*SL	0.35 + 0.017*SL	0.37 + 0.016*SL
	tR	0.27	0.11 + 0.082*SL	0.10 + 0.084*SL	0.06 + 0.086*SL
	tF	0.16	0.10 + 0.034*SL	0.11 + 0.030*SL	0.07 + 0.032*SL
SN to Q	tPLH	0.56	0.48 + 0.039*SL	0.49 + 0.037*SL	0.49 + 0.037*SL
	tR	0.26	0.09 + 0.082*SL	0.09 + 0.085*SL	0.06 + 0.087*SL
CKN to QN	tPLH	0.70	0.62 + 0.041*SL	0.63 + 0.038*SL	0.63 + 0.038*SL
	tPHL	0.62	0.58 + 0.024*SL	0.59 + 0.018*SL	0.62 + 0.016*SL
	tR	0.27	0.09 + 0.088*SL	0.10 + 0.087*SL	0.06 + 0.088*SL
	tF	0.14	0.08 + 0.030*SL	0.08 + 0.032*SL	0.07 + 0.032*SL
RN to QN	tPLH	0.68	0.60 + 0.040*SL	0.61 + 0.037*SL	0.61 + 0.038*SL
	tR	0.27	0.12 + 0.078*SL	0.09 + 0.087*SL	0.06 + 0.088*SL
SN to QN	tPLH	0.22	0.14 + 0.042*SL	0.15 + 0.037*SL	0.14 + 0.038*SL
	tPHL	0.39	0.33 + 0.028*SL	0.36 + 0.018*SL	0.40 + 0.016*SL
	tR	0.28	0.12 + 0.083*SL	0.11 + 0.086*SL	0.06 + 0.088*SL
	tF	0.17	0.11 + 0.032*SL	0.11 + 0.030*SL	0.08 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD8 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.287
Input Setup Time (D to CKN)	tSU	0.123
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

FD8D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

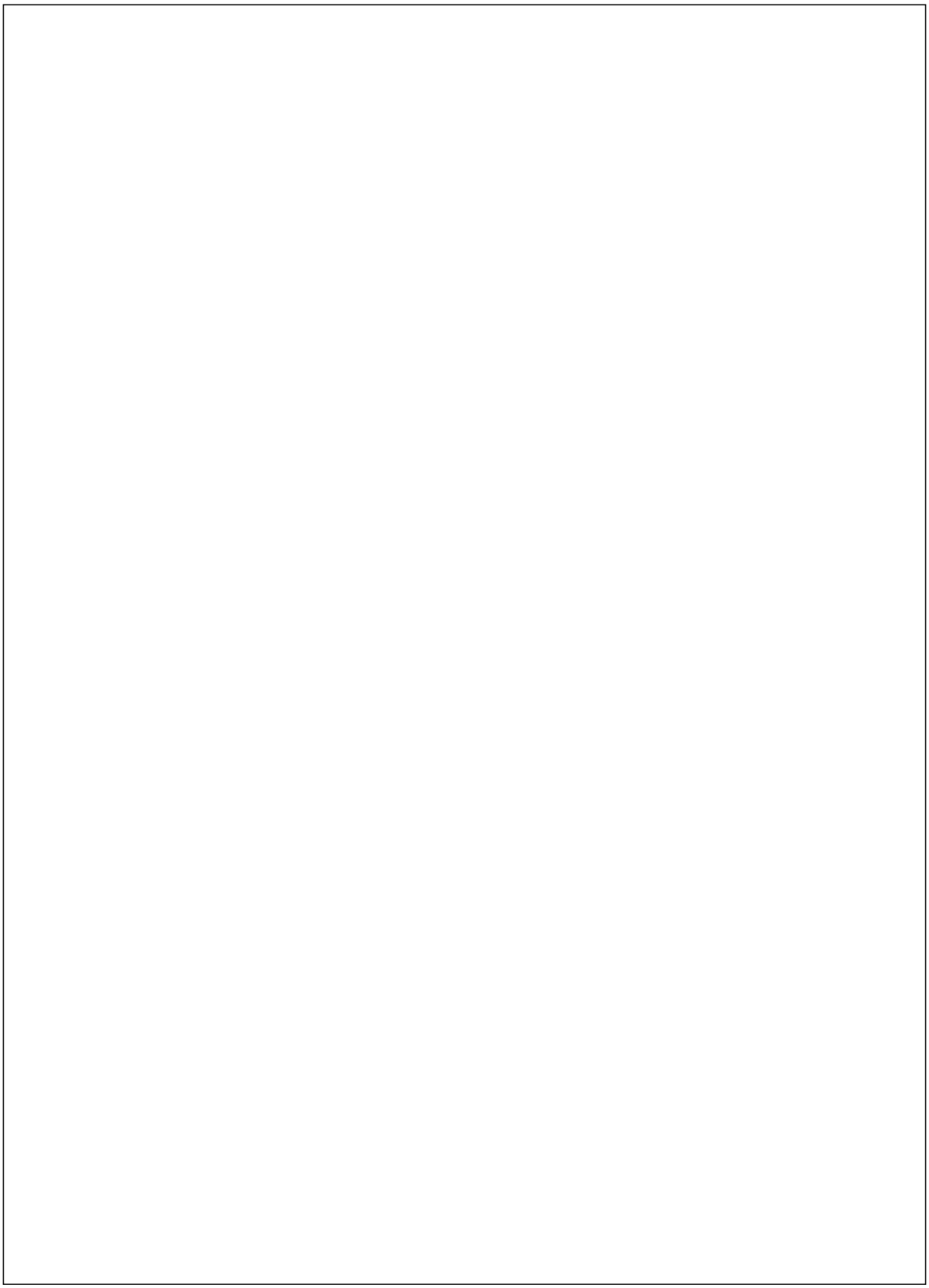
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.83	0.79 + 0.020*SL	0.80 + 0.018*SL	0.80 + 0.018*SL
	tPHL	0.80	0.77 + 0.014*SL	0.78 + 0.010*SL	0.81 + 0.008*SL
	tR	0.18	0.09 + 0.042*SL	0.10 + 0.040*SL	0.07 + 0.042*SL
	tF	0.13	0.09 + 0.020*SL	0.11 + 0.015*SL	0.09 + 0.016*SL
RN to Q	tPLH	0.21	0.17 + 0.022*SL	0.18 + 0.019*SL	0.19 + 0.018*SL
	tPHL	0.38	0.35 + 0.015*SL	0.37 + 0.010*SL	0.41 + 0.008*SL
	tR	0.20	0.13 + 0.034*SL	0.11 + 0.041*SL	0.09 + 0.042*SL
	tF	0.16	0.12 + 0.016*SL	0.13 + 0.015*SL	0.12 + 0.015*SL
SN to Q	tPLH	0.61	0.57 + 0.017*SL	0.57 + 0.018*SL	0.57 + 0.018*SL
	tR	0.18	0.10 + 0.040*SL	0.10 + 0.041*SL	0.07 + 0.042*SL
CKN to QN	tPLH	0.69	0.65 + 0.022*SL	0.66 + 0.019*SL	0.67 + 0.019*SL
	tPHL	0.64	0.61 + 0.014*SL	0.62 + 0.010*SL	0.65 + 0.008*SL
	tR	0.18	0.10 + 0.043*SL	0.10 + 0.044*SL	0.08 + 0.044*SL
	tF	0.14	0.11 + 0.015*SL	0.11 + 0.015*SL	0.09 + 0.016*SL
RN to QN	tPLH	0.68	0.64 + 0.021*SL	0.65 + 0.019*SL	0.66 + 0.019*SL
	tR	0.19	0.12 + 0.035*SL	0.09 + 0.044*SL	0.08 + 0.044*SL
SN to QN	tPLH	0.22	0.18 + 0.020*SL	0.18 + 0.019*SL	0.19 + 0.019*SL
	tPHL	0.39	0.36 + 0.017*SL	0.38 + 0.011*SL	0.42 + 0.008*SL
	tR	0.21	0.13 + 0.039*SL	0.12 + 0.043*SL	0.08 + 0.044*SL
	tF	0.16	0.13 + 0.015*SL	0.13 + 0.015*SL	0.13 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD8D2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

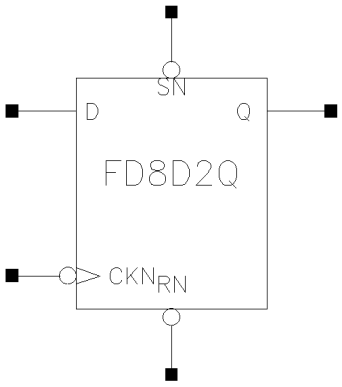
Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.287
Input Setup Time (D to CKN)	tSU	0.123
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



Inputs: D, CKN, RN, SN
Output: Q
Input Loading (SL):
- FD8D2Q: D: 3, CKN : 1
  RN, SN : 2
- FD8D4Q: D: 3, CKN: 1
  RN, SN : 2

Maximum Fanout (Rec. SL):
- FD8D2Q: 56
- FD8D4Q: 112

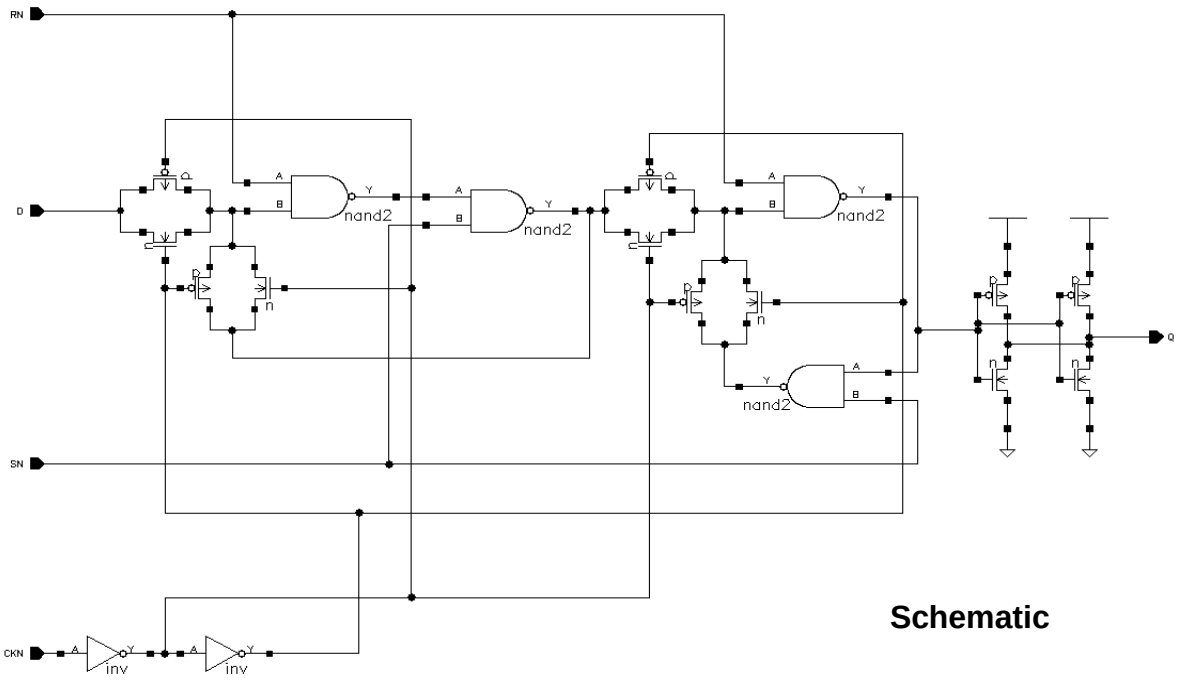
Gate Count:
- FD8D2Q: 8
- FD8D4Q: 9



Symbol

D	SN	RN	CK	Qn+1
0	1	1	↓	0
1	1	1	↓	1
x	0	1	x	1
x	1	0	x	0
x	0	0	x	0
x	1	1	↑	Qn

Truth Table



Schematic

FD8D2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	t_{PLH}	0.61	0.56 + 0.025*SL	0.58 + 0.020*SL	0.61 + 0.019*SL
	t_{PHL}	0.54	0.50 + 0.020*SL	0.52 + 0.013*SL	0.58 + 0.010*SL
	t_R	0.22	0.13 + 0.045*SL	0.14 + 0.042*SL	0.12 + 0.043*SL
	t_F	0.16	0.11 + 0.022*SL	0.12 + 0.019*SL	0.17 + 0.016*SL
RN to Q	t_{PLH}	0.38	0.33 + 0.024*SL	0.34 + 0.020*SL	0.37 + 0.019*SL
	t_{PHL}	0.53	0.48 + 0.021*SL	0.51 + 0.014*SL	0.59 + 0.010*SL
	t_R	0.25	0.18 + 0.037*SL	0.17 + 0.040*SL	0.12 + 0.043*SL
	t_F	0.21	0.17 + 0.022*SL	0.19 + 0.017*SL	0.22 + 0.015*SL
SN to Q	t_{PLH}	0.81	0.76 + 0.025*SL	0.78 + 0.020*SL	0.80 + 0.019*SL
	t_R	0.23	0.14 + 0.042*SL	0.15 + 0.041*SL	0.12 + 0.042*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD8D2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D to CKN)	t_{HD}	0.342
Input Setup Time (D to CKN)	t_{SU}	0.178
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139

FD8D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

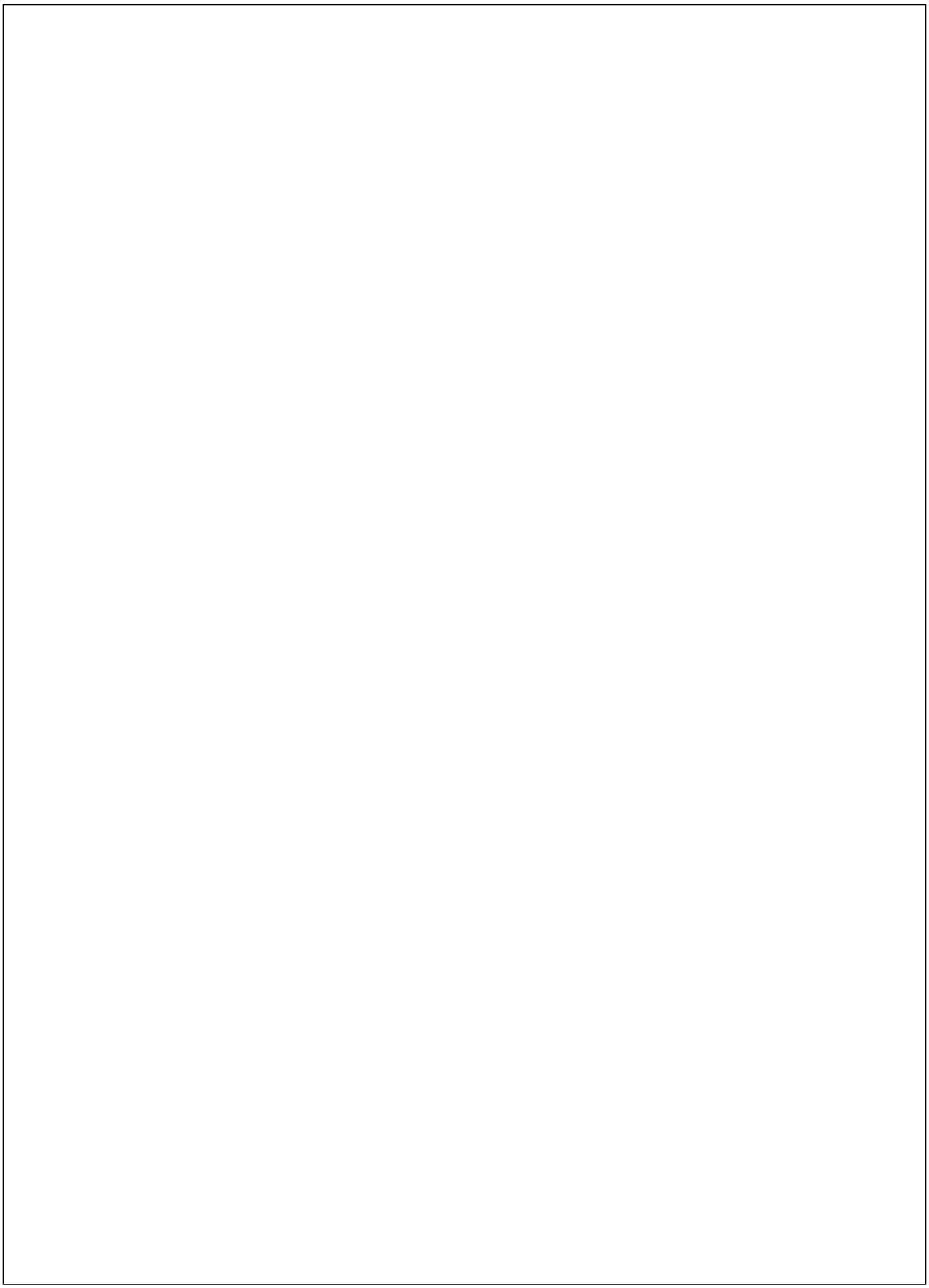
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.67	0.64 + 0.014*SL	0.65 + 0.011*SL	0.68 + 0.010*SL
	tPHL	0.56	0.53 + 0.015*SL	0.55 + 0.009*SL	0.59 + 0.006*SL
	tR	0.22	0.19 + 0.016*SL	0.17 + 0.020*SL	0.17 + 0.021*SL
	tF	0.17	0.14 + 0.013*SL	0.15 + 0.011*SL	0.20 + 0.009*SL
RN to Q	tPLH	0.44	0.41 + 0.014*SL	0.42 + 0.011*SL	0.45 + 0.010*SL
	tPHL	0.58	0.55 + 0.014*SL	0.56 + 0.009*SL	0.61 + 0.006*SL
	tR	0.23	0.18 + 0.024*SL	0.19 + 0.019*SL	0.17 + 0.020*SL
	tF	0.23	0.20 + 0.014*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
SN to Q	tPLH	0.87	0.84 + 0.015*SL	0.85 + 0.011*SL	0.87 + 0.010*SL
	tR	0.23	0.20 + 0.016*SL	0.18 + 0.020*SL	0.19 + 0.020*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD8D4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

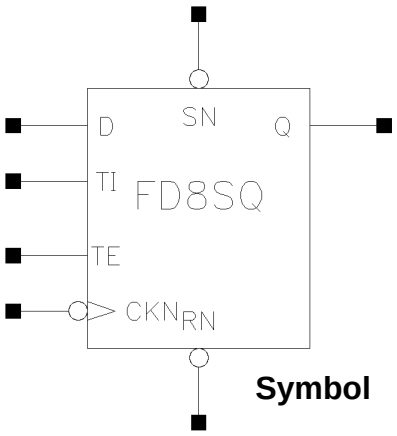
Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.342
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



Inputs: D, TI, TE, CKN, RN, SN
Output: Q
Input Loading (SL):
- FD8SD2Q: D, CKN, TI : 1
  RN, SN, TE : 2
- FD8SD4Q: D, CKN, TI : 1
  RN, SN, TE : 2

Maximum Fanout (Rec. SL):
- FD8SD2Q: 56
- FD8SD4Q: 112

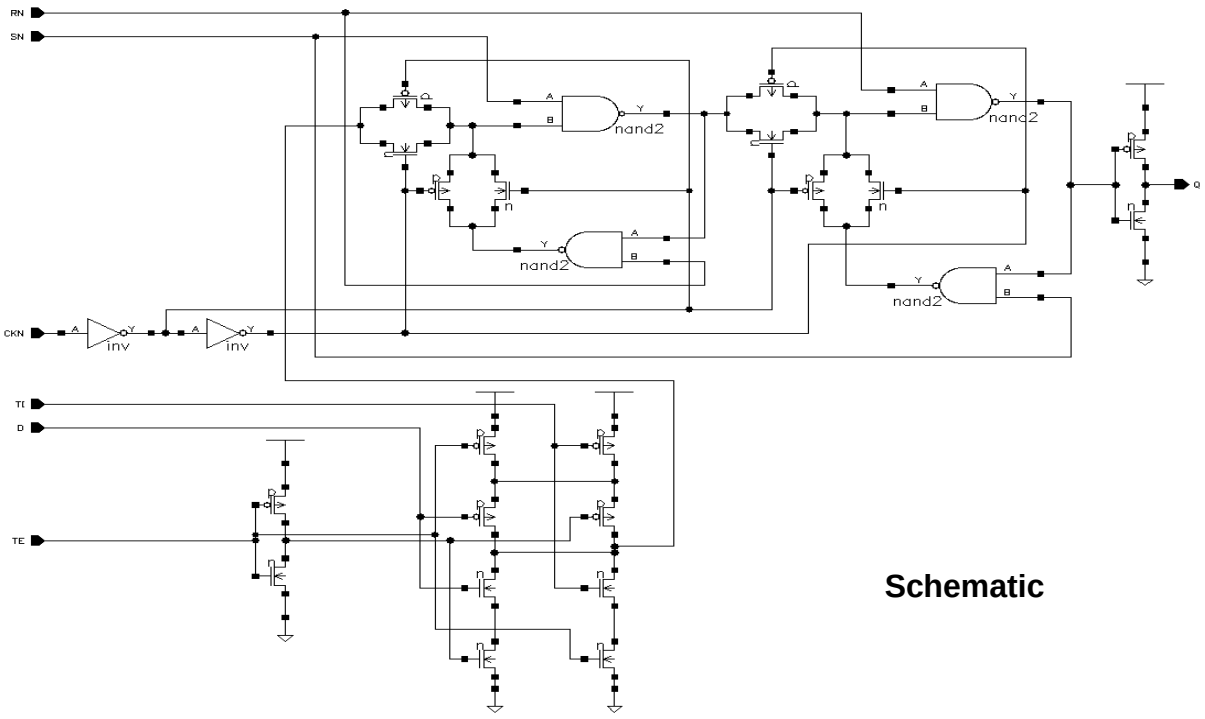
Gate Count:
- FD8SD2Q: 11
- FD8SD4Q: 12



Symbol

Truth Table

D	SN	RN	TI	TE	CKN	Qn+1
0	1	1	X	0	↓	0
1	1	1	X	0	↓	1
x	1	1	0	1	↓	0
x	1	1	1	1	↓	1
x	0	1	x	x	x	1
x	1	0	x	x	x	0
x	0	0	x	x	x	0
x	1	1	x	x	↑	Qn



Schematic

FD8SD2Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.68	0.64 + 0.020*SL	0.64 + 0.019*SL	0.65 + 0.018*SL
	tR	0.19	0.12 + 0.035*SL	0.10 + 0.042*SL	0.08 + 0.043*SL
RN to Q	tPLH	0.22	0.18 + 0.021*SL	0.18 + 0.019*SL	0.19 + 0.018*SL
	tPHL	0.39	0.36 + 0.018*SL	0.38 + 0.011*SL	0.42 + 0.008*SL
	tR	0.20	0.13 + 0.035*SL	0.11 + 0.042*SL	0.08 + 0.043*SL
	tF	0.16	0.12 + 0.022*SL	0.14 + 0.014*SL	0.12 + 0.016*SL
CKN to Q	tPLH	0.69	0.65 + 0.023*SL	0.66 + 0.019*SL	0.67 + 0.018*SL
	tPHL	0.63	0.60 + 0.015*SL	0.61 + 0.011*SL	0.65 + 0.008*SL
	tR	0.19	0.10 + 0.043*SL	0.11 + 0.042*SL	0.08 + 0.043*SL
	tF	0.13	0.09 + 0.019*SL	0.10 + 0.016*SL	0.11 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD8SD2Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.233
Input Hold Time (TE to CKN)	tHD	0.233
Input Hold Time (TI to CKN)	tHD	0.178
Input Setup Time (D to CKN)	tSU	0.397
Input Setup Time (TE to CKN)	tSU	0.506
Input Setup Time (TI to CKN)	tSU	0.452
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

FD8SD4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

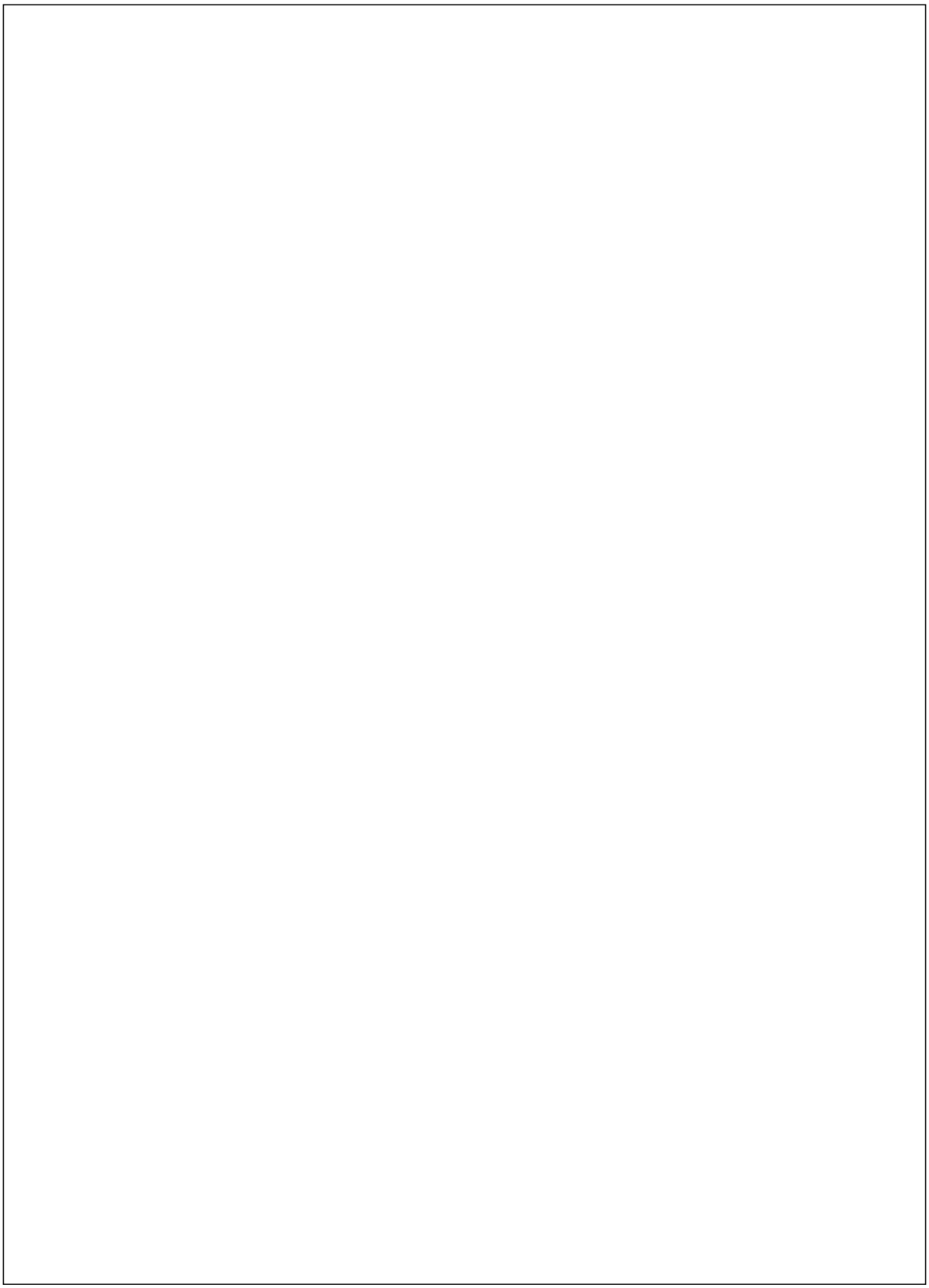
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.73	0.71 + 0.013*SL	0.72 + 0.010*SL	0.73 + 0.009*SL
	tR	0.16	0.13 + 0.019*SL	0.12 + 0.021*SL	0.13 + 0.020*SL
RN to Q	tPLH	0.27	0.25 + 0.012*SL	0.25 + 0.010*SL	0.27 + 0.009*SL
	tPHL	0.44	0.42 + 0.010*SL	0.43 + 0.007*SL	0.47 + 0.005*SL
	tR	0.18	0.15 + 0.015*SL	0.13 + 0.020*SL	0.13 + 0.020*SL
	tF	0.18	0.16 + 0.011*SL	0.17 + 0.007*SL	0.17 + 0.007*SL
CKN to Q	tPLH	0.74	0.72 + 0.013*SL	0.72 + 0.010*SL	0.74 + 0.009*SL
	tPHL	0.68	0.66 + 0.009*SL	0.67 + 0.007*SL	0.70 + 0.005*SL
	tR	0.17	0.12 + 0.023*SL	0.13 + 0.020*SL	0.12 + 0.021*SL
	tF	0.15	0.13 + 0.009*SL	0.14 + 0.008*SL	0.14 + 0.008*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FD8SD4Q Timing Requirements

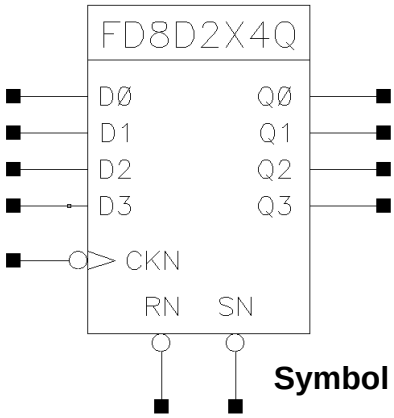
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.233
Input Hold Time (TE to CKN)	tHD	0.233
Input Hold Time (TI to CKN)	tHD	0.178
Input Setup Time (D to CKN)	tSU	0.397
Input Setup Time (TE to CKN)	tSU	0.506
Input Setup Time (TI to CKN)	tSU	0.452
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



Inputs: DO, D1, D2, D3, CKN, RN, SN
Output: Q0, Q1, Q2, Q3
Input Loading (SL): All: DO, D1, D2, D3: 3
CKN: 1, RN, SN: 8
Maximum Fanout (Rec. SL):
- FD8D2X4Q: 56
- FD8D4X4Q: 112

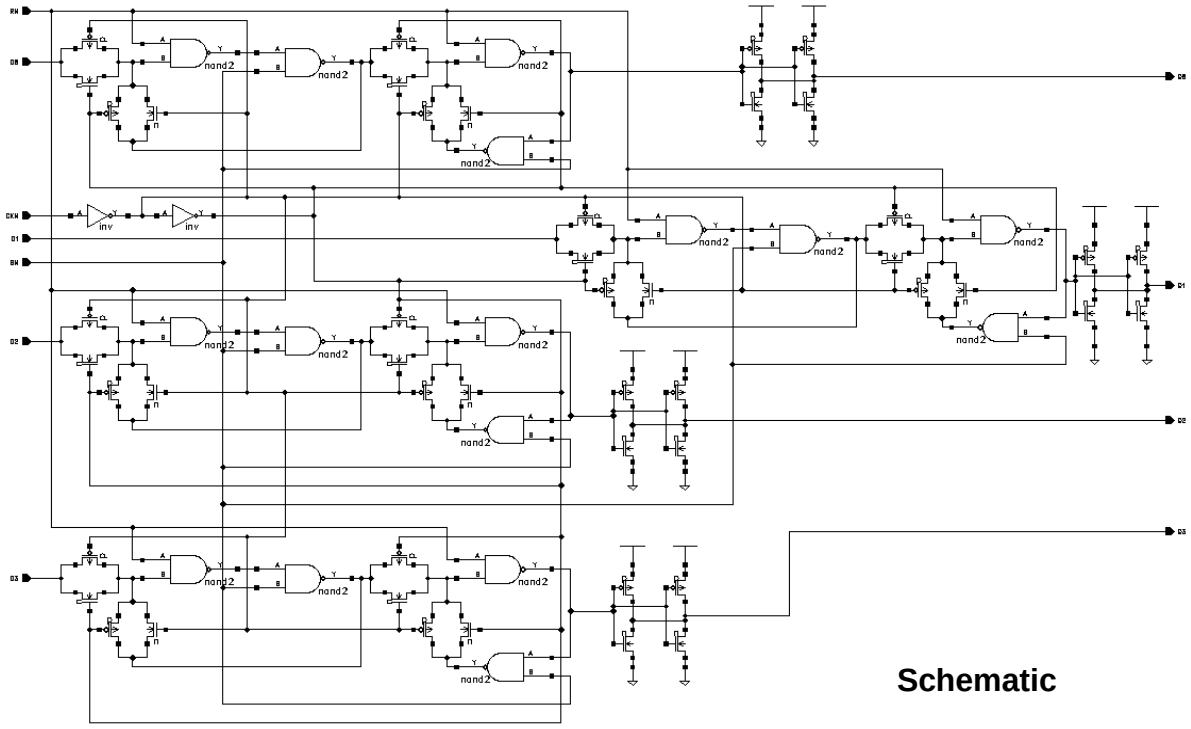
Gate Count:
- FD8D2X4Q: 29
- FD8D4X4Q: 33



Symbol

D	SN	RN	CK	Qn+1
0	1	1	↓	0
1	1	1	↓	1
x	0	1	x	1
x	1	0	x	0
x	0	0	x	0
x	1	1	↑	Qn

Truth Table



Schematic

FD8D2X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	0.82	0.77 + 0.023*SL	0.78 + 0.020*SL	0.82 + 0.019*SL
	tPHL	0.84	0.79 + 0.022*SL	0.82 + 0.014*SL	0.90 + 0.010*SL
	tR	0.22	0.12 + 0.050*SL	0.14 + 0.042*SL	0.12 + 0.043*SL
	tF	0.19	0.14 + 0.024*SL	0.16 + 0.017*SL	0.19 + 0.016*SL
RN to Q0	tPLH	0.38	0.33 + 0.023*SL	0.34 + 0.020*SL	0.37 + 0.019*SL
	tPHL	0.53	0.48 + 0.022*SL	0.51 + 0.014*SL	0.59 + 0.010*SL
	tR	0.24	0.15 + 0.049*SL	0.17 + 0.040*SL	0.12 + 0.043*SL
	tF	0.21	0.16 + 0.024*SL	0.18 + 0.017*SL	0.21 + 0.015*SL
SN to Q0	tPLH	0.81	0.76 + 0.025*SL	0.78 + 0.020*SL	0.80 + 0.019*SL
	tR	0.23	0.14 + 0.043*SL	0.15 + 0.041*SL	0.12 + 0.042*SL
CKN to Q1	tPLH	0.82	0.77 + 0.024*SL	0.78 + 0.021*SL	0.82 + 0.019*SL
	tPHL	0.84	0.79 + 0.022*SL	0.82 + 0.013*SL	0.89 + 0.010*SL
	tR	0.22	0.12 + 0.051*SL	0.14 + 0.044*SL	0.12 + 0.045*SL
	tF	0.19	0.15 + 0.024*SL	0.16 + 0.018*SL	0.19 + 0.016*SL
RN to Q1	tPLH	0.38	0.33 + 0.023*SL	0.34 + 0.021*SL	0.37 + 0.019*SL
	tPHL	0.52	0.48 + 0.022*SL	0.50 + 0.014*SL	0.58 + 0.010*SL
	tR	0.25	0.15 + 0.050*SL	0.17 + 0.042*SL	0.12 + 0.045*SL
	tF	0.21	0.16 + 0.024*SL	0.18 + 0.017*SL	0.21 + 0.016*SL
SN to Q1	tPLH	0.81	0.76 + 0.025*SL	0.78 + 0.020*SL	0.80 + 0.019*SL
	tR	0.23	0.15 + 0.043*SL	0.15 + 0.043*SL	0.12 + 0.045*SL
CKN to Q2	tPLH	0.82	0.77 + 0.024*SL	0.78 + 0.021*SL	0.82 + 0.019*SL
	tPHL	0.84	0.80 + 0.022*SL	0.82 + 0.014*SL	0.89 + 0.010*SL
	tR	0.23	0.14 + 0.046*SL	0.14 + 0.044*SL	0.12 + 0.045*SL
	tF	0.20	0.15 + 0.023*SL	0.16 + 0.018*SL	0.19 + 0.017*SL
RN to Q2	tPLH	0.38	0.33 + 0.023*SL	0.34 + 0.021*SL	0.37 + 0.019*SL
	tPHL	0.53	0.48 + 0.022*SL	0.51 + 0.014*SL	0.59 + 0.010*SL
	tR	0.25	0.15 + 0.050*SL	0.17 + 0.042*SL	0.12 + 0.045*SL
	tF	0.21	0.16 + 0.025*SL	0.19 + 0.017*SL	0.21 + 0.016*SL
SN to Q2	tPLH	0.82	0.76 + 0.026*SL	0.78 + 0.020*SL	0.80 + 0.019*SL
	tR	0.25	0.19 + 0.029*SL	0.14 + 0.043*SL	0.12 + 0.045*SL
CKN to Q3	tPLH	0.83	0.78 + 0.025*SL	0.79 + 0.020*SL	0.82 + 0.019*SL
	tPHL	0.84	0.80 + 0.022*SL	0.82 + 0.013*SL	0.89 + 0.010*SL
	tR	0.22	0.13 + 0.042*SL	0.13 + 0.043*SL	0.12 + 0.043*SL
	tF	0.19	0.14 + 0.024*SL	0.16 + 0.017*SL	0.20 + 0.016*SL
RN to Q3	tPLH	0.38	0.34 + 0.023*SL	0.34 + 0.020*SL	0.37 + 0.019*SL
	tPHL	0.53	0.48 + 0.022*SL	0.51 + 0.014*SL	0.59 + 0.010*SL
	tR	0.24	0.15 + 0.049*SL	0.17 + 0.040*SL	0.12 + 0.043*SL
	tF	0.21	0.16 + 0.024*SL	0.18 + 0.017*SL	0.21 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD8D2X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q3	tPLH	0.82	0.77 + 0.025*SL	0.78 + 0.020*SL	0.81 + 0.019*SL
	tR	0.24	0.18 + 0.028*SL	0.14 + 0.042*SL	0.12 + 0.043*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD8D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D0 to CKN)	tHD	0.506
Input Hold Time (D1 to CKN)	tHD	0.506
Input Hold Time (D2 to CKN)	tHD	0.506
Input Hold Time (D3 to CKN)	tHD	0.506
Input Setup Time (D0 to CKN)	tSU	0.000
Input Setup Time (D1 to CKN)	tSU	0.000
Input Setup Time (D2 to CKN)	tSU	0.000
Input Setup Time (D3 to CKN)	tSU	0.000
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

FD8D4X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

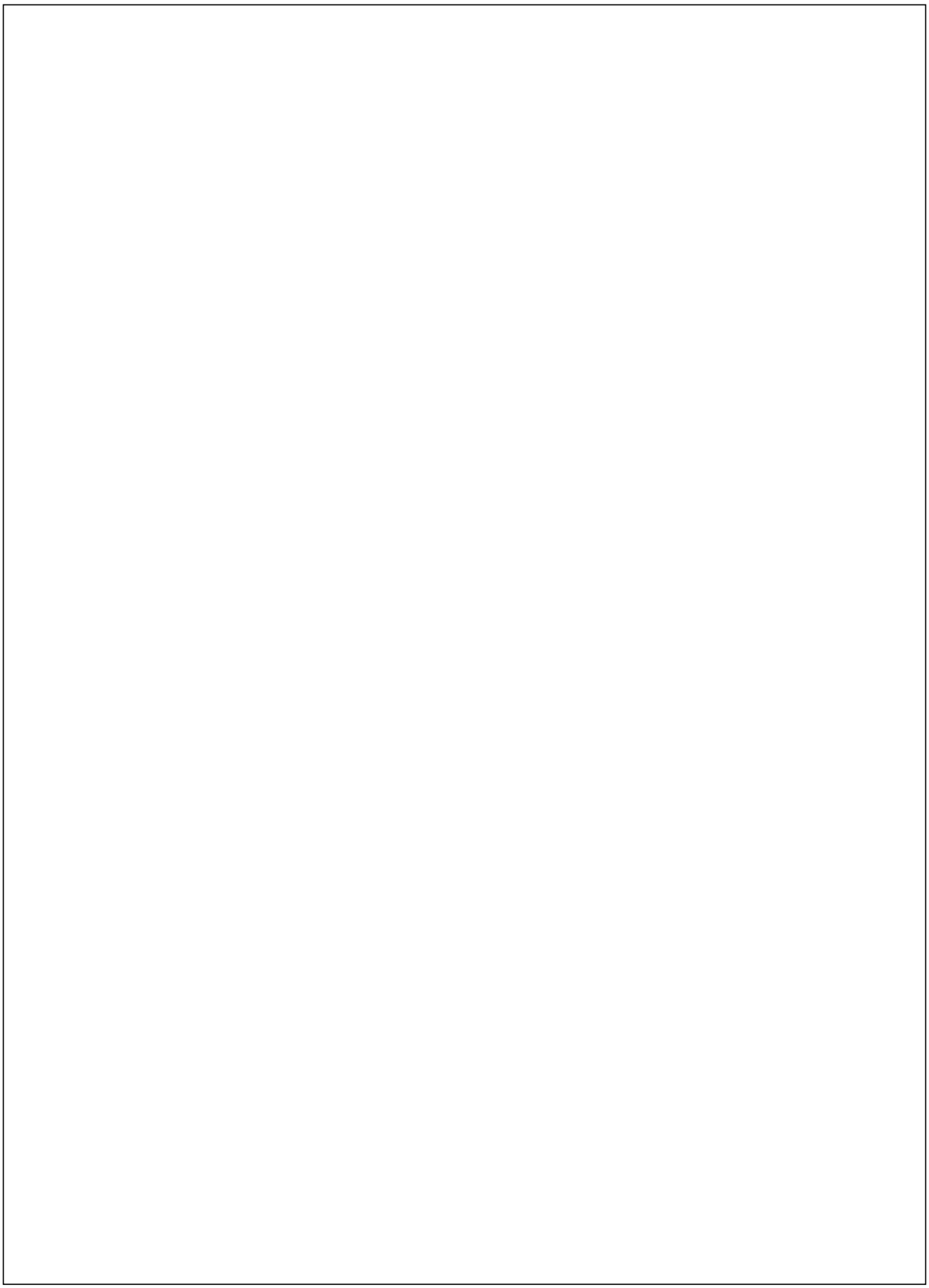
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	0.90	0.87 + 0.015*SL	0.88 + 0.011*SL	0.91 + 0.010*SL
	tPHL	0.87	0.84 + 0.014*SL	0.85 + 0.009*SL	0.90 + 0.007*SL
	tR	0.22	0.18 + 0.019*SL	0.17 + 0.021*SL	0.17 + 0.021*SL
	tF	0.20	0.18 + 0.012*SL	0.19 + 0.010*SL	0.22 + 0.009*SL
RN to Q0	tPLH	0.44	0.42 + 0.014*SL	0.42 + 0.011*SL	0.45 + 0.010*SL
	tPHL	0.57	0.55 + 0.013*SL	0.56 + 0.009*SL	0.61 + 0.006*SL
	tR	0.23	0.20 + 0.016*SL	0.19 + 0.020*SL	0.17 + 0.021*SL
	tF	0.22	0.20 + 0.014*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
SN to Q0	tPLH	0.87	0.84 + 0.015*SL	0.85 + 0.011*SL	0.87 + 0.010*SL
	tR	0.23	0.20 + 0.016*SL	0.18 + 0.020*SL	0.19 + 0.020*SL
CKN to Q1	tPLH	0.90	0.87 + 0.015*SL	0.88 + 0.011*SL	0.91 + 0.010*SL
	tPHL	0.87	0.84 + 0.013*SL	0.85 + 0.009*SL	0.90 + 0.007*SL
	tR	0.22	0.18 + 0.018*SL	0.18 + 0.021*SL	0.17 + 0.021*SL
	tF	0.21	0.18 + 0.015*SL	0.19 + 0.010*SL	0.22 + 0.009*SL
RN to Q1	tPLH	0.44	0.41 + 0.014*SL	0.42 + 0.011*SL	0.45 + 0.010*SL
	tPHL	0.57	0.55 + 0.013*SL	0.56 + 0.009*SL	0.61 + 0.006*SL
	tR	0.24	0.21 + 0.015*SL	0.19 + 0.020*SL	0.17 + 0.021*SL
	tF	0.23	0.20 + 0.014*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
SN to Q1	tPLH	0.87	0.84 + 0.015*SL	0.85 + 0.011*SL	0.87 + 0.010*SL
	tR	0.23	0.20 + 0.016*SL	0.18 + 0.021*SL	0.19 + 0.021*SL
CKN to Q2	tPLH	0.90	0.87 + 0.015*SL	0.88 + 0.011*SL	0.91 + 0.010*SL
	tPHL	0.87	0.84 + 0.014*SL	0.85 + 0.009*SL	0.90 + 0.007*SL
	tR	0.22	0.18 + 0.019*SL	0.18 + 0.021*SL	0.17 + 0.021*SL
	tF	0.21	0.18 + 0.015*SL	0.19 + 0.010*SL	0.22 + 0.009*SL
RN to Q2	tPLH	0.44	0.41 + 0.014*SL	0.42 + 0.011*SL	0.45 + 0.010*SL
	tPHL	0.57	0.55 + 0.013*SL	0.56 + 0.009*SL	0.61 + 0.006*SL
	tR	0.24	0.20 + 0.015*SL	0.19 + 0.020*SL	0.17 + 0.021*SL
	tF	0.23	0.20 + 0.014*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
SN to Q2	tPLH	0.87	0.84 + 0.015*SL	0.85 + 0.011*SL	0.88 + 0.010*SL
	tR	0.23	0.20 + 0.013*SL	0.18 + 0.021*SL	0.18 + 0.021*SL
CKN to Q3	tPLH	0.91	0.88 + 0.015*SL	0.89 + 0.011*SL	0.92 + 0.010*SL
	tPHL	0.87	0.84 + 0.014*SL	0.86 + 0.009*SL	0.90 + 0.007*SL
	tR	0.22	0.19 + 0.015*SL	0.17 + 0.021*SL	0.17 + 0.021*SL
	tF	0.21	0.18 + 0.014*SL	0.19 + 0.010*SL	0.23 + 0.009*SL
RN to Q3	tPLH	0.45	0.42 + 0.013*SL	0.42 + 0.011*SL	0.45 + 0.010*SL
	tPHL	0.57	0.55 + 0.013*SL	0.56 + 0.009*SL	0.61 + 0.006*SL
	tR	0.23	0.19 + 0.019*SL	0.19 + 0.020*SL	0.17 + 0.021*SL
	tF	0.22	0.20 + 0.014*SL	0.21 + 0.010*SL	0.24 + 0.008*SL
SN to Q3	tPLH	0.87	0.84 + 0.015*SL	0.85 + 0.011*SL	0.88 + 0.010*SL
	tR	0.23	0.19 + 0.017*SL	0.19 + 0.020*SL	0.18 + 0.020*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FD8D4X4Q Timing Requirements

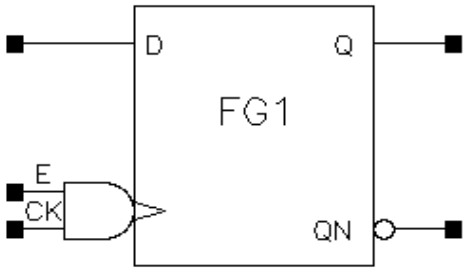
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CKN)	t_{PWH}	0.920
Input Hold Time (D0 to CKN)	t_{HD}	0.561
Input Hold Time (D1 to CKN)	t_{HD}	0.561
Input Hold Time (D2 to CKN)	t_{HD}	0.561
Input Hold Time (D3 to CKN)	t_{HD}	0.561
Input Setup Time (D0 to CKN)	t_{SU}	0.000
Input Setup Time (D1 to CKN)	t_{SU}	0.000
Input Setup Time (D2 to CKN)	t_{SU}	0.000
Input Setup Time (D3 to CKN)	t_{SU}	0.000
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139



Inputs: D, E, CK
Outputs: Q, QN
Input Loading (SL):
- D: 3
- E, CK: 1

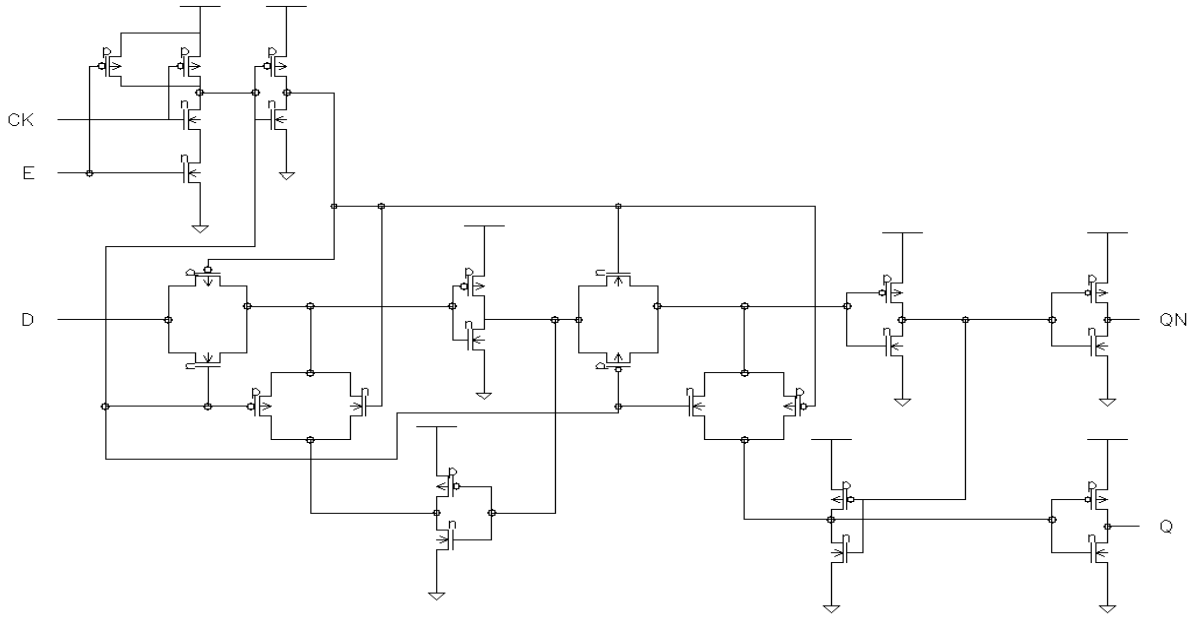
Maximum Fanout (Rec. SL): All : 28
Gate Count: 7



Symbol

D	E	CK	Qn+1	QNn+1
0	1	⎍	0	1
1	1	⎍	1	0
x	0	x	Qn	QNn
x	x	⎎	Qn	QNn

Truth Table



Schematic

FG1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.61	0.53 + 0.039*SL	0.54 + 0.037*SL	0.53 + 0.037*SL
	t_{PHL}	0.56	0.51 + 0.022*SL	0.53 + 0.017*SL	0.54 + 0.016*SL
	t_R	0.24	0.07 + 0.083*SL	0.06 + 0.086*SL	0.05 + 0.087*SL
	t_F	0.13	0.07 + 0.034*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
E to Q	t_{PLH}	0.57	0.50 + 0.037*SL	0.50 + 0.037*SL	0.50 + 0.037*SL
	t_{PHL}	0.51	0.47 + 0.020*SL	0.48 + 0.017*SL	0.50 + 0.016*SL
	t_R	0.24	0.07 + 0.084*SL	0.06 + 0.086*SL	0.05 + 0.087*SL
	t_F	0.13	0.07 + 0.030*SL	0.07 + 0.031*SL	0.04 + 0.033*SL
CK to QN	t_{PLH}	0.52	0.44 + 0.039*SL	0.45 + 0.038*SL	0.45 + 0.038*SL
	t_{PHL}	0.50	0.45 + 0.024*SL	0.47 + 0.017*SL	0.50 + 0.016*SL
	t_R	0.25	0.08 + 0.086*SL	0.07 + 0.087*SL	0.05 + 0.088*SL
	t_F	0.13	0.07 + 0.033*SL	0.07 + 0.032*SL	0.06 + 0.033*SL
E to QN	t_{PLH}	0.48	0.40 + 0.039*SL	0.40 + 0.038*SL	0.41 + 0.038*SL
	t_{PHL}	0.46	0.41 + 0.024*SL	0.43 + 0.017*SL	0.46 + 0.016*SL
	t_R	0.25	0.07 + 0.088*SL	0.07 + 0.088*SL	0.05 + 0.088*SL
	t_F	0.14	0.07 + 0.034*SL	0.07 + 0.032*SL	0.06 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

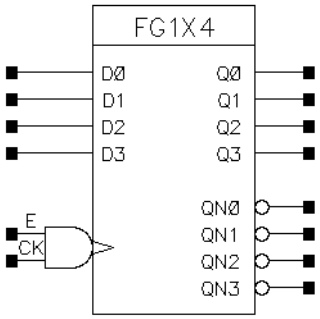
FG1 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (E)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Pulse Width High (E)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.233
Input Hold Time (D to E)	t_{HD}	0.233
Input Setup Time (D to CK)	t_{SU}	0.233
Input Setup Time (D to E)	t_{SU}	0.287

Inputs: D0, D1, D2, D3, E, CK
Outputs: Q0, Q1, Q2, Q3
QN0, QN1, QN2, QN3
Input Loading (SL):
- D0, D1, D2, D3: 3
- E, CK: 1

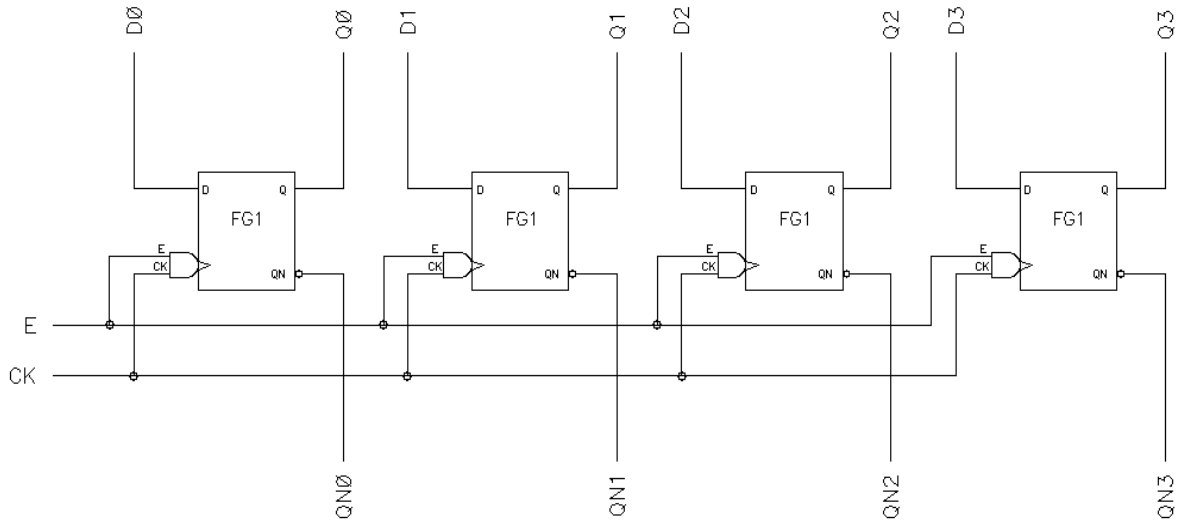
Maximum Fanout (Rec. SL): All : 28
Gate Count: 22



Symbol

D	E	CK	Qn+1	QNn+1
0	1	↑	0	1
1	1	↑	1	0
x	0	x	Qn	QNn
x	x	↓	Qn	QNn

Truth Table



Schematic

FG1X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	tPLH	0.96	0.88 + 0.037*SL	0.88 + 0.037*SL	0.88 + 0.037*SL
	tPHL	0.76	0.72 + 0.022*SL	0.73 + 0.017*SL	0.74 + 0.016*SL
	tR	0.24	0.06 + 0.087*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	tF	0.13	0.07 + 0.034*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
E to Q0	tPLH	0.90	0.82 + 0.039*SL	0.82 + 0.037*SL	0.82 + 0.037*SL
	tPHL	0.70	0.66 + 0.021*SL	0.67 + 0.017*SL	0.68 + 0.017*SL
	tR	0.24	0.07 + 0.085*SL	0.06 + 0.086*SL	0.05 + 0.087*SL
	tF	0.13	0.07 + 0.035*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
CK to Q1	tPLH	0.96	0.88 + 0.038*SL	0.88 + 0.037*SL	0.88 + 0.038*SL
	tPHL	0.76	0.72 + 0.021*SL	0.73 + 0.017*SL	0.74 + 0.016*SL
	tR	0.24	0.07 + 0.084*SL	0.06 + 0.088*SL	0.05 + 0.089*SL
	tF	0.13	0.07 + 0.032*SL	0.06 + 0.033*SL	0.04 + 0.034*SL
E to Q1	tPLH	0.90	0.82 + 0.038*SL	0.82 + 0.037*SL	0.82 + 0.038*SL
	tPHL	0.70	0.66 + 0.021*SL	0.67 + 0.017*SL	0.68 + 0.016*SL
	tR	0.24	0.07 + 0.084*SL	0.06 + 0.088*SL	0.05 + 0.089*SL
	tF	0.13	0.07 + 0.033*SL	0.07 + 0.033*SL	0.04 + 0.034*SL
CK to Q2	tPLH	0.96	0.88 + 0.038*SL	0.88 + 0.038*SL	0.88 + 0.038*SL
	tPHL	0.76	0.72 + 0.022*SL	0.73 + 0.017*SL	0.74 + 0.016*SL
	tR	0.24	0.06 + 0.090*SL	0.07 + 0.088*SL	0.05 + 0.089*SL
	tF	0.13	0.07 + 0.034*SL	0.07 + 0.033*SL	0.04 + 0.034*SL
E to Q2	tPLH	0.90	0.82 + 0.037*SL	0.82 + 0.038*SL	0.82 + 0.038*SL
	tPHL	0.70	0.66 + 0.022*SL	0.67 + 0.017*SL	0.68 + 0.017*SL
	tR	0.24	0.07 + 0.084*SL	0.06 + 0.088*SL	0.05 + 0.089*SL
	tF	0.13	0.06 + 0.035*SL	0.07 + 0.033*SL	0.04 + 0.034*SL
CK to Q3	tPLH	0.96	0.88 + 0.037*SL	0.88 + 0.037*SL	0.88 + 0.037*SL
	tPHL	0.76	0.71 + 0.022*SL	0.73 + 0.017*SL	0.74 + 0.016*SL
	tR	0.24	0.06 + 0.087*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	tF	0.13	0.06 + 0.034*SL	0.07 + 0.032*SL	0.05 + 0.033*SL
E to Q3	tPLH	0.90	0.82 + 0.039*SL	0.83 + 0.037*SL	0.82 + 0.037*SL
	tPHL	0.70	0.65 + 0.023*SL	0.67 + 0.017*SL	0.68 + 0.016*SL
	tR	0.25	0.09 + 0.079*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	tF	0.13	0.06 + 0.036*SL	0.07 + 0.032*SL	0.04 + 0.034*SL
CK to QN0	tPLH	0.72	0.64 + 0.039*SL	0.65 + 0.038*SL	0.65 + 0.038*SL
	tPHL	0.85	0.80 + 0.024*SL	0.82 + 0.018*SL	0.84 + 0.016*SL
	tR	0.25	0.08 + 0.084*SL	0.07 + 0.088*SL	0.06 + 0.088*SL
	tF	0.14	0.07 + 0.037*SL	0.08 + 0.033*SL	0.05 + 0.034*SL
E to QN0	tPLH	0.66	0.58 + 0.039*SL	0.59 + 0.038*SL	0.59 + 0.038*SL
	tPHL	0.79	0.74 + 0.024*SL	0.76 + 0.018*SL	0.78 + 0.016*SL
	tR	0.25	0.07 + 0.087*SL	0.07 + 0.088*SL	0.06 + 0.088*SL
	tF	0.14	0.07 + 0.036*SL	0.08 + 0.033*SL	0.06 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FG1X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

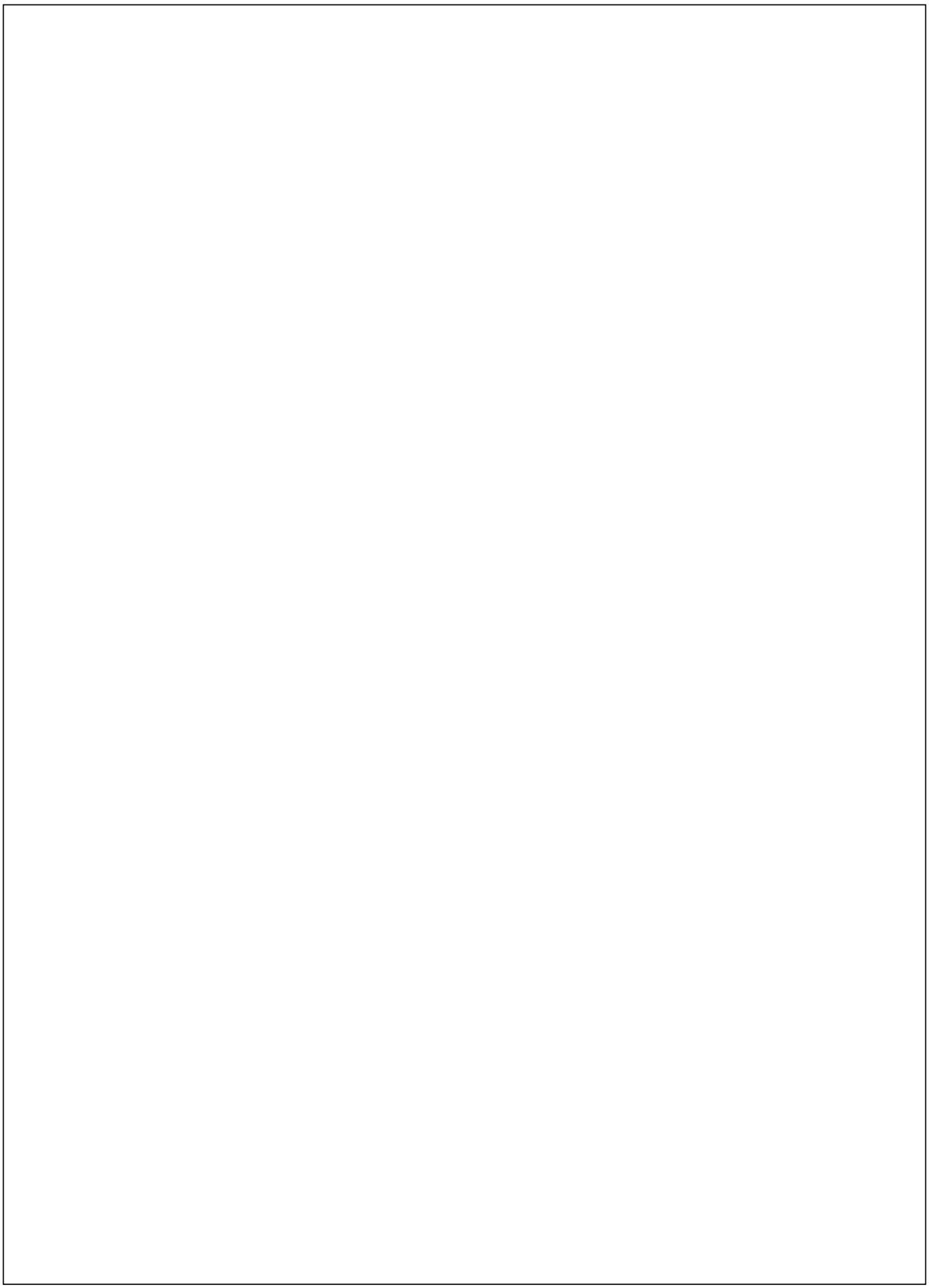
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to QN1	t_{PLH}	0.72	0.65 + 0.039*SL	0.65 + 0.038*SL	0.65 + 0.038*SL
	t_{PHL}	0.85	0.80 + 0.024*SL	0.82 + 0.018*SL	0.84 + 0.016*SL
	t_R	0.25	0.08 + 0.086*SL	0.07 + 0.088*SL	0.06 + 0.088*SL
	t_F	0.14	0.07 + 0.036*SL	0.08 + 0.033*SL	0.05 + 0.034*SL
E to QN1	t_{PLH}	0.66	0.58 + 0.040*SL	0.59 + 0.038*SL	0.59 + 0.038*SL
	t_{PHL}	0.79	0.74 + 0.024*SL	0.76 + 0.018*SL	0.78 + 0.016*SL
	t_R	0.25	0.08 + 0.085*SL	0.07 + 0.088*SL	0.06 + 0.088*SL
	t_F	0.14	0.07 + 0.036*SL	0.08 + 0.033*SL	0.06 + 0.034*SL
CK to QN2	t_{PLH}	0.72	0.64 + 0.039*SL	0.65 + 0.038*SL	0.65 + 0.038*SL
	t_{PHL}	0.85	0.80 + 0.024*SL	0.82 + 0.018*SL	0.84 + 0.016*SL
	t_R	0.25	0.08 + 0.084*SL	0.07 + 0.088*SL	0.06 + 0.088*SL
	t_F	0.14	0.07 + 0.038*SL	0.08 + 0.033*SL	0.06 + 0.034*SL
E to QN2	t_{PLH}	0.66	0.58 + 0.039*SL	0.59 + 0.038*SL	0.59 + 0.038*SL
	t_{PHL}	0.79	0.74 + 0.025*SL	0.76 + 0.018*SL	0.78 + 0.016*SL
	t_R	0.25	0.07 + 0.087*SL	0.07 + 0.088*SL	0.06 + 0.088*SL
	t_F	0.14	0.07 + 0.036*SL	0.08 + 0.033*SL	0.06 + 0.034*SL
CK to QN3	t_{PLH}	0.72	0.64 + 0.039*SL	0.65 + 0.038*SL	0.65 + 0.038*SL
	t_{PHL}	0.85	0.80 + 0.024*SL	0.82 + 0.018*SL	0.85 + 0.016*SL
	t_R	0.25	0.08 + 0.084*SL	0.07 + 0.088*SL	0.06 + 0.088*SL
	t_F	0.14	0.07 + 0.037*SL	0.08 + 0.033*SL	0.05 + 0.034*SL
E to QN3	t_{PLH}	0.66	0.58 + 0.039*SL	0.59 + 0.038*SL	0.59 + 0.038*SL
	t_{PHL}	0.79	0.74 + 0.025*SL	0.76 + 0.018*SL	0.78 + 0.016*SL
	t_R	0.25	0.08 + 0.085*SL	0.07 + 0.088*SL	0.06 + 0.088*SL
	t_F	0.14	0.07 + 0.034*SL	0.08 + 0.033*SL	0.05 + 0.034*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FG1X4 Timing Requirements

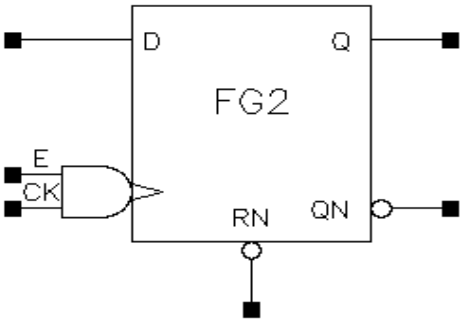
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (E)	t_{PWL}	0.998
Pulse Width High (CK)	t_{PWH}	0.920
Pulse Width High (E)	t_{PWH}	0.920
Input Hold Time (D0 to CK)	t_{HD}	0.506
Input Hold Time (D0 to E)	t_{HD}	0.452
Input Hold Time (D1 to CK)	t_{HD}	0.506
Input Hold Time (D1 to E)	t_{HD}	0.452



Inputs: D, E, CK, RN
Outputs: Q, QN
Input Loading (SL):
- D: 3
- E, CK: 1
- RN: 2

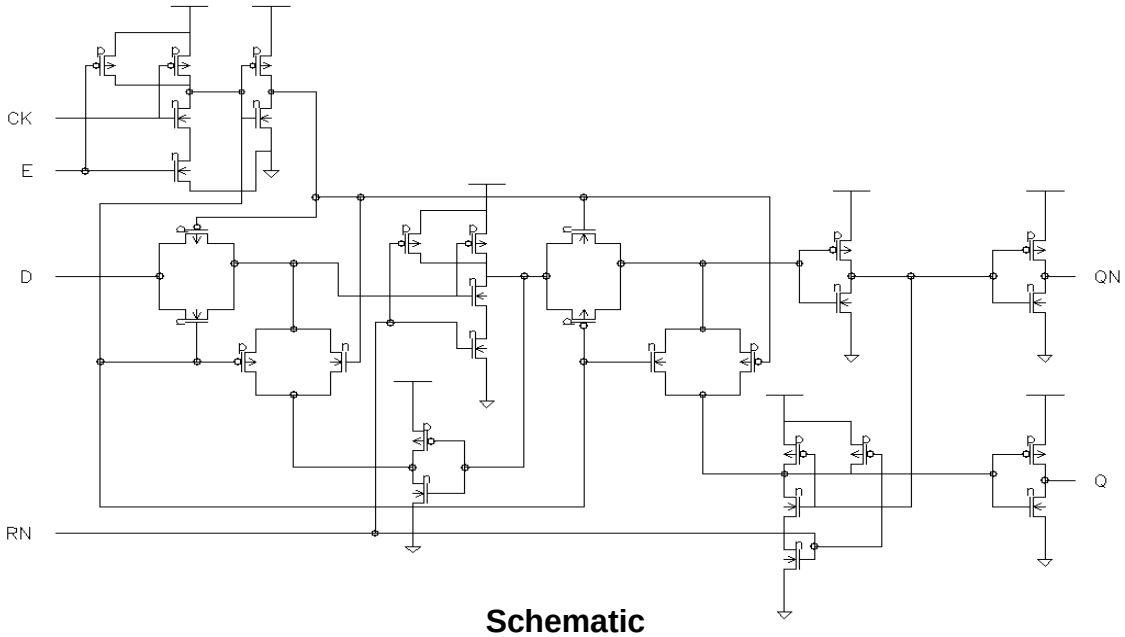
Maximum Fanout (Rec. SL): All : 28
Gate Count: 8



Symbol

D	RN	E	CK	Qn+1	QNn+1
0	1	1	↑	0	1
1	1	1	↑	1	0
x	1	0	x	Qn	QNn
x	0	x	x	0	1
x	1	x	↓	Qn	QNn

Truth Table



Schematic

FG2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	t_{PHL}	0.37	0.32 + 0.027*SL	0.35 + 0.017*SL	0.37 + 0.016*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.030*SL	0.06 + 0.032*SL
CK to Q	t_{PLH}	0.70	0.62 + 0.036*SL	0.62 + 0.036*SL	0.62 + 0.036*SL
	t_{PHL}	0.57	0.52 + 0.022*SL	0.54 + 0.017*SL	0.55 + 0.016*SL
	t_R	0.25	0.09 + 0.079*SL	0.08 + 0.083*SL	0.05 + 0.085*SL
	t_F	0.14	0.06 + 0.036*SL	0.08 + 0.031*SL	0.05 + 0.032*SL
E to Q	t_{PLH}	0.66	0.58 + 0.037*SL	0.58 + 0.036*SL	0.58 + 0.036*SL
	t_{PHL}	0.53	0.48 + 0.022*SL	0.50 + 0.017*SL	0.52 + 0.016*SL
	t_R	0.25	0.08 + 0.085*SL	0.08 + 0.083*SL	0.05 + 0.085*SL
	t_F	0.13	0.07 + 0.033*SL	0.07 + 0.031*SL	0.05 + 0.032*SL
RN to QN	t_{PLH}	0.63	0.55 + 0.037*SL	0.56 + 0.036*SL	0.55 + 0.036*SL
	t_R	0.25	0.09 + 0.076*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
CK to QN	t_{PLH}	0.52	0.44 + 0.038*SL	0.45 + 0.037*SL	0.45 + 0.036*SL
	t_{PHL}	0.54	0.49 + 0.023*SL	0.51 + 0.017*SL	0.53 + 0.016*SL
	t_R	0.23	0.07 + 0.080*SL	0.06 + 0.084*SL	0.05 + 0.084*SL
	t_F	0.14	0.09 + 0.028*SL	0.08 + 0.031*SL	0.06 + 0.032*SL
E to QN	t_{PLH}	0.48	0.40 + 0.038*SL	0.41 + 0.037*SL	0.41 + 0.036*SL
	t_{PHL}	0.50	0.45 + 0.023*SL	0.47 + 0.017*SL	0.49 + 0.016*SL
	t_R	0.24	0.07 + 0.085*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.14	0.08 + 0.029*SL	0.07 + 0.031*SL	0.06 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

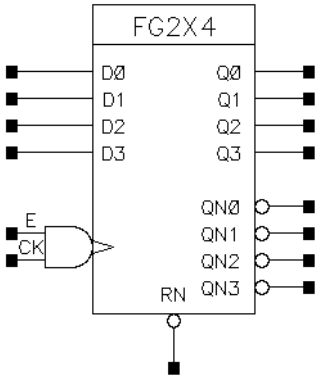
FG2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (E)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Pulse Width High (E)	t_{PWH}	0.920
Input Hold Time (D to CK)	t_{HD}	0.233
Input Hold Time (D to E)	t_{HD}	0.178
Input Setup Time (D to CK)	t_{SU}	0.233
Input Setup Time (D to E)	t_{SU}	0.287
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (RN)	t_{RC}	0.139

Inputs: D0, D1, D2, D3, E, CK, RN
Outputs: Q0, Q1, Q2, Q3,
QN0, QN1, QN2, QN3
Input Loading (SL):
- D0, D1, D2, D3: 3
- E, CK: 1
- RN: 8

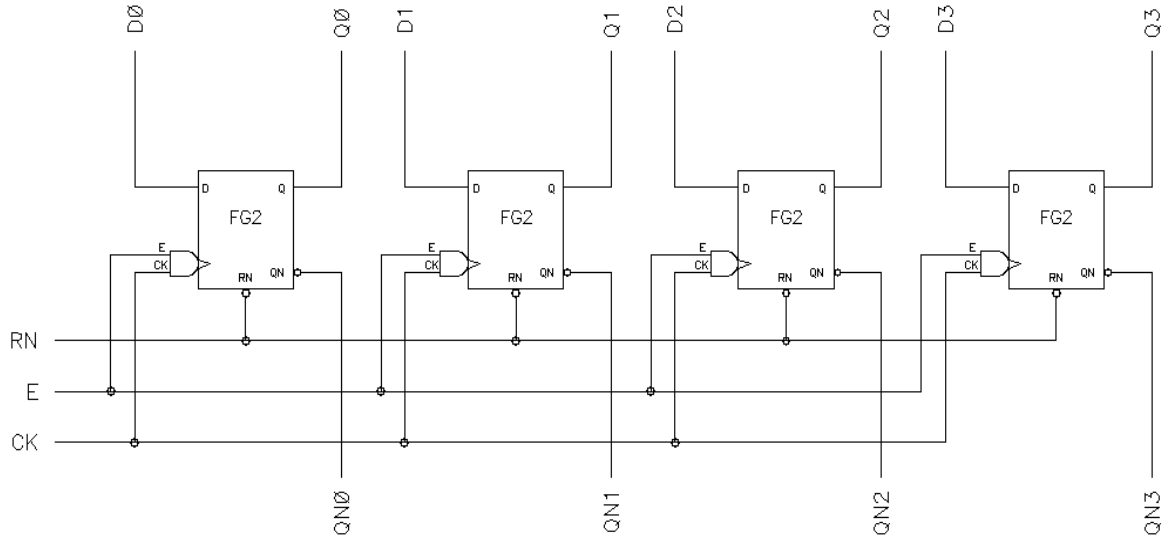
Maximum Fanout (Rec. SL): All : 28
Gate Count: 26



Symbol

D	RN	E	CK	Qn+1	QNn+1
0	1	1	↑	0	1
1	1	1	↑	1	0
x	1	0	x	Qn	QNn
x	0	x	x	0	1
x	1	x	↓	Qn	QNn

Truth Table



Schematic

FG2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q0	tPHL	0.37	0.32 + 0.026*SL	0.35 + 0.017*SL	0.37 + 0.016*SL
	tF	0.16	0.10 + 0.032*SL	0.11 + 0.030*SL	0.06 + 0.032*SL
CK to Q0	tPLH	1.06	0.99 + 0.037*SL	0.99 + 0.036*SL	0.99 + 0.036*SL
	tPHL	0.78	0.73 + 0.022*SL	0.75 + 0.017*SL	0.76 + 0.016*SL
	tR	0.25	0.09 + 0.083*SL	0.08 + 0.083*SL	0.05 + 0.085*SL
	tF	0.13	0.07 + 0.033*SL	0.07 + 0.031*SL	0.05 + 0.032*SL
E to Q0	tPLH	1.00	0.93 + 0.037*SL	0.93 + 0.036*SL	0.93 + 0.036*SL
	tPHL	0.71	0.67 + 0.022*SL	0.69 + 0.017*SL	0.70 + 0.016*SL
	tR	0.25	0.09 + 0.080*SL	0.08 + 0.083*SL	0.05 + 0.085*SL
	tF	0.13	0.06 + 0.035*SL	0.07 + 0.031*SL	0.05 + 0.032*SL
RN to Q1	tPHL	0.37	0.32 + 0.027*SL	0.35 + 0.018*SL	0.37 + 0.017*SL
	tF	0.17	0.10 + 0.034*SL	0.11 + 0.032*SL	0.06 + 0.034*SL
CK to Q1	tPLH	1.06	0.99 + 0.038*SL	0.99 + 0.037*SL	0.98 + 0.038*SL
	tPHL	0.77	0.73 + 0.023*SL	0.74 + 0.017*SL	0.76 + 0.017*SL
	tR	0.26	0.09 + 0.085*SL	0.09 + 0.087*SL	0.06 + 0.089*SL
	tF	0.14	0.07 + 0.034*SL	0.08 + 0.033*SL	0.05 + 0.034*SL
E to Q1	tPLH	1.00	0.93 + 0.037*SL	0.93 + 0.037*SL	0.92 + 0.038*SL
	tPHL	0.71	0.67 + 0.023*SL	0.68 + 0.017*SL	0.70 + 0.017*SL
	tR	0.26	0.10 + 0.082*SL	0.08 + 0.087*SL	0.06 + 0.089*SL
	tF	0.14	0.06 + 0.035*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
RN to Q2	tPHL	0.37	0.32 + 0.027*SL	0.35 + 0.018*SL	0.37 + 0.017*SL
	tF	0.17	0.10 + 0.034*SL	0.11 + 0.032*SL	0.06 + 0.034*SL
CK to Q2	tPLH	1.06	0.98 + 0.038*SL	0.99 + 0.037*SL	0.98 + 0.038*SL
	tPHL	0.77	0.72 + 0.023*SL	0.74 + 0.017*SL	0.76 + 0.017*SL
	tR	0.26	0.09 + 0.085*SL	0.09 + 0.087*SL	0.06 + 0.089*SL
	tF	0.14	0.07 + 0.035*SL	0.08 + 0.033*SL	0.05 + 0.034*SL
E to Q2	tPLH	1.00	0.93 + 0.036*SL	0.93 + 0.037*SL	0.92 + 0.038*SL
	tPHL	0.71	0.67 + 0.022*SL	0.68 + 0.017*SL	0.70 + 0.017*SL
	tR	0.26	0.09 + 0.084*SL	0.09 + 0.087*SL	0.05 + 0.089*SL
	tF	0.14	0.07 + 0.034*SL	0.07 + 0.033*SL	0.05 + 0.034*SL
RN to Q3	tPHL	0.37	0.32 + 0.026*SL	0.35 + 0.017*SL	0.37 + 0.016*SL
	tF	0.16	0.10 + 0.032*SL	0.11 + 0.030*SL	0.06 + 0.032*SL
CK to Q3	tPLH	1.06	0.98 + 0.037*SL	0.99 + 0.036*SL	0.98 + 0.036*SL
	tPHL	0.77	0.73 + 0.022*SL	0.75 + 0.017*SL	0.76 + 0.016*SL
	tR	0.25	0.09 + 0.082*SL	0.08 + 0.083*SL	0.06 + 0.085*SL
	tF	0.14	0.07 + 0.035*SL	0.08 + 0.031*SL	0.05 + 0.032*SL
E to Q3	tPLH	1.00	0.93 + 0.037*SL	0.93 + 0.036*SL	0.93 + 0.036*SL
	tPHL	0.71	0.67 + 0.022*SL	0.69 + 0.017*SL	0.70 + 0.016*SL
	tR	0.25	0.10 + 0.077*SL	0.08 + 0.083*SL	0.05 + 0.085*SL
	tF	0.13	0.06 + 0.034*SL	0.07 + 0.031*SL	0.05 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FG2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to QN0	tPLH	0.63	0.55 + 0.037*SL	0.55 + 0.036*SL	0.56 + 0.036*SL
	tR	0.24	0.08 + 0.084*SL	0.08 + 0.083*SL	0.05 + 0.084*SL
CK to QN0	tPLH	0.73	0.65 + 0.037*SL	0.65 + 0.036*SL	0.66 + 0.036*SL
	tPHL	0.90	0.86 + 0.023*SL	0.87 + 0.017*SL	0.90 + 0.016*SL
	tR	0.24	0.08 + 0.079*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.08 + 0.029*SL	0.07 + 0.031*SL	0.06 + 0.032*SL
E to QN0	tPLH	0.66	0.59 + 0.037*SL	0.59 + 0.036*SL	0.59 + 0.036*SL
	tPHL	0.84	0.79 + 0.024*SL	0.81 + 0.017*SL	0.84 + 0.016*SL
	tR	0.24	0.07 + 0.082*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.07 + 0.035*SL	0.08 + 0.031*SL	0.06 + 0.032*SL
RN to QN1	tPLH	0.63	0.55 + 0.037*SL	0.55 + 0.037*SL	0.55 + 0.037*SL
	tR	0.25	0.07 + 0.089*SL	0.08 + 0.087*SL	0.05 + 0.089*SL
CK to QN1	tPLH	0.73	0.65 + 0.039*SL	0.65 + 0.038*SL	0.65 + 0.038*SL
	tPHL	0.90	0.85 + 0.023*SL	0.87 + 0.018*SL	0.90 + 0.016*SL
	tR	0.25	0.08 + 0.085*SL	0.07 + 0.088*SL	0.05 + 0.089*SL
	tF	0.14	0.08 + 0.031*SL	0.07 + 0.033*SL	0.06 + 0.034*SL
E to QN1	tPLH	0.66	0.59 + 0.039*SL	0.59 + 0.038*SL	0.59 + 0.038*SL
	tPHL	0.84	0.80 + 0.024*SL	0.81 + 0.018*SL	0.84 + 0.016*SL
	tR	0.25	0.07 + 0.087*SL	0.07 + 0.088*SL	0.05 + 0.088*SL
	tF	0.15	0.09 + 0.030*SL	0.08 + 0.033*SL	0.06 + 0.034*SL
RN to QN2	tPLH	0.62	0.55 + 0.037*SL	0.55 + 0.037*SL	0.54 + 0.037*SL
	tR	0.25	0.07 + 0.089*SL	0.08 + 0.087*SL	0.05 + 0.089*SL
CK to QN2	tPLH	0.72	0.65 + 0.040*SL	0.65 + 0.038*SL	0.65 + 0.038*SL
	tPHL	0.90	0.85 + 0.023*SL	0.87 + 0.018*SL	0.90 + 0.016*SL
	tR	0.25	0.08 + 0.086*SL	0.07 + 0.088*SL	0.05 + 0.089*SL
	tF	0.14	0.08 + 0.031*SL	0.07 + 0.033*SL	0.06 + 0.034*SL
E to QN2	tPLH	0.66	0.58 + 0.040*SL	0.59 + 0.038*SL	0.60 + 0.038*SL
	tPHL	0.84	0.80 + 0.022*SL	0.81 + 0.018*SL	0.84 + 0.016*SL
	tR	0.25	0.07 + 0.088*SL	0.07 + 0.088*SL	0.05 + 0.088*SL
	tF	0.15	0.09 + 0.029*SL	0.08 + 0.033*SL	0.07 + 0.033*SL
RN to QN3	tPLH	0.62	0.55 + 0.037*SL	0.55 + 0.036*SL	0.55 + 0.036*SL
	tR	0.24	0.08 + 0.084*SL	0.08 + 0.083*SL	0.05 + 0.084*SL
CK to QN3	tPLH	0.72	0.65 + 0.037*SL	0.65 + 0.037*SL	0.66 + 0.036*SL
	tPHL	0.90	0.85 + 0.023*SL	0.87 + 0.017*SL	0.90 + 0.016*SL
	tR	0.24	0.08 + 0.079*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.08 + 0.029*SL	0.07 + 0.032*SL	0.07 + 0.032*SL
E to QN3	tPLH	0.66	0.59 + 0.038*SL	0.59 + 0.036*SL	0.59 + 0.036*SL
	tPHL	0.84	0.80 + 0.023*SL	0.81 + 0.017*SL	0.84 + 0.016*SL
	tR	0.24	0.07 + 0.082*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	tF	0.14	0.08 + 0.030*SL	0.08 + 0.031*SL	0.06 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

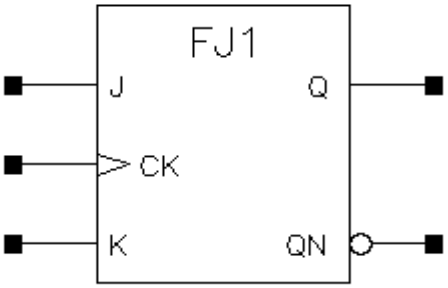
FG2X4 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (E)	t_{PWL}	0.998
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Pulse Width High (E)	t_{PWH}	0.920
Input Hold Time (D0 to CK)	t_{HD}	0.506
Input Hold Time (D0 to E)	t_{HD}	0.397
Input Hold Time (D1 to CK)	t_{HD}	0.506
Input Hold Time (D1 to E)	t_{HD}	0.397
Input Hold Time (D2 to CK)	t_{HD}	0.452
Input Hold Time (D2 to E)	t_{HD}	0.397
Input Hold Time (D3 to CK)	t_{HD}	0.506
Input Hold Time (D3 to E)	t_{HD}	0.397
Input Setup Time (D0 to CK)	t_{SU}	0.123
Input Setup Time (D0 to E)	t_{SU}	0.178
Input Setup Time (D1 to CK)	t_{SU}	0.123
Input Setup Time (D1 to E)	t_{SU}	0.178
Input Setup Time (D2 to CK)	t_{SU}	0.123
Input Setup Time (D2 to E)	t_{SU}	0.178
Input Setup Time (D3 to CK)	t_{SU}	0.123
Input Setup Time (D3 to E)	t_{SU}	0.178
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (RN)	t_{RC}	0.139

Inputs: J, K, CK
Outputs: Q, QN
Input Loading (SL): All : 1
Maximum Fanout (Rec. SL): All :
- FJ1: 28
- FJ1D2:56

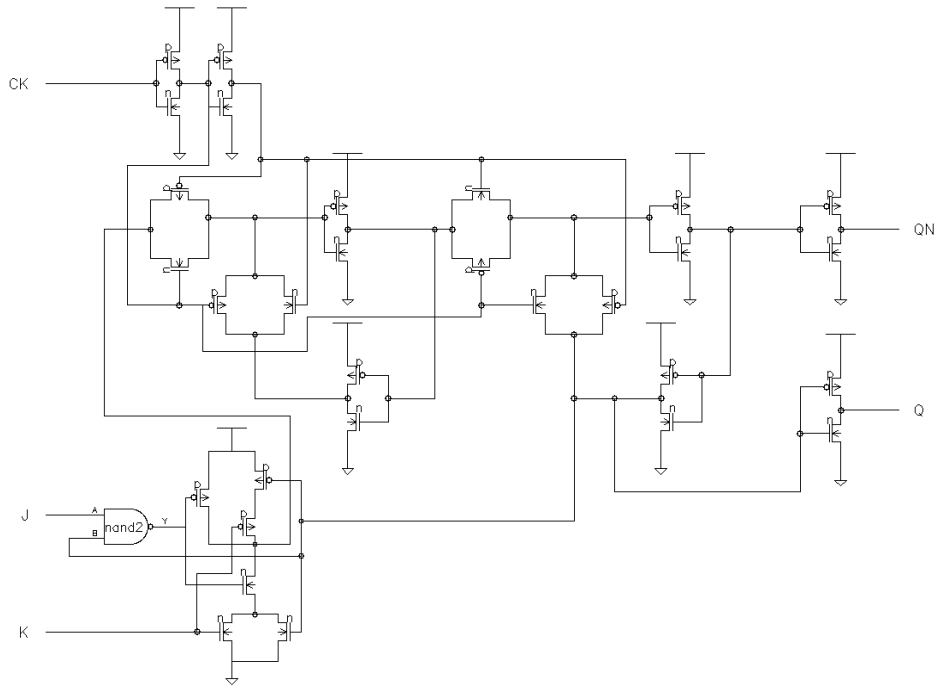
Gate Count:
- FJ1: 9
- FJ1D2:10



Symbol

J	K	CK	Qn+1	QNn+1
0	1	⎍	0	1
1	0	⎍	1	0
0	0	⎍	Qn	QNn
1	1	⎍	QNn	Qn
x	x	⎎	Qn	QNn

Truth Table



Schematic

FJ1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.57	0.50 + 0.037*SL	0.50 + 0.036*SL	0.50 + 0.036*SL
	t_{PHL}	0.52	0.47 + 0.027*SL	0.50 + 0.018*SL	0.54 + 0.016*SL
	t_R	0.24	0.08 + 0.080*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.17	0.10 + 0.037*SL	0.12 + 0.030*SL	0.08 + 0.032*SL
CK to QN	t_{PLH}	0.41	0.33 + 0.038*SL	0.34 + 0.037*SL	0.34 + 0.036*SL
	t_{PHL}	0.41	0.36 + 0.023*SL	0.38 + 0.017*SL	0.40 + 0.016*SL
	t_R	0.24	0.07 + 0.084*SL	0.07 + 0.084*SL	0.05 + 0.085*SL
	t_F	0.14	0.07 + 0.031*SL	0.07 + 0.031*SL	0.05 + 0.032*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FJ1 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (J to CK)	t_{HD}	0.000
Input Hold Time (K to CK)	t_{HD}	0.000
Input Setup Time (J to CK)	t_{SU}	0.397
Input Setup Time (K to CK)	t_{SU}	0.342

FJ1D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

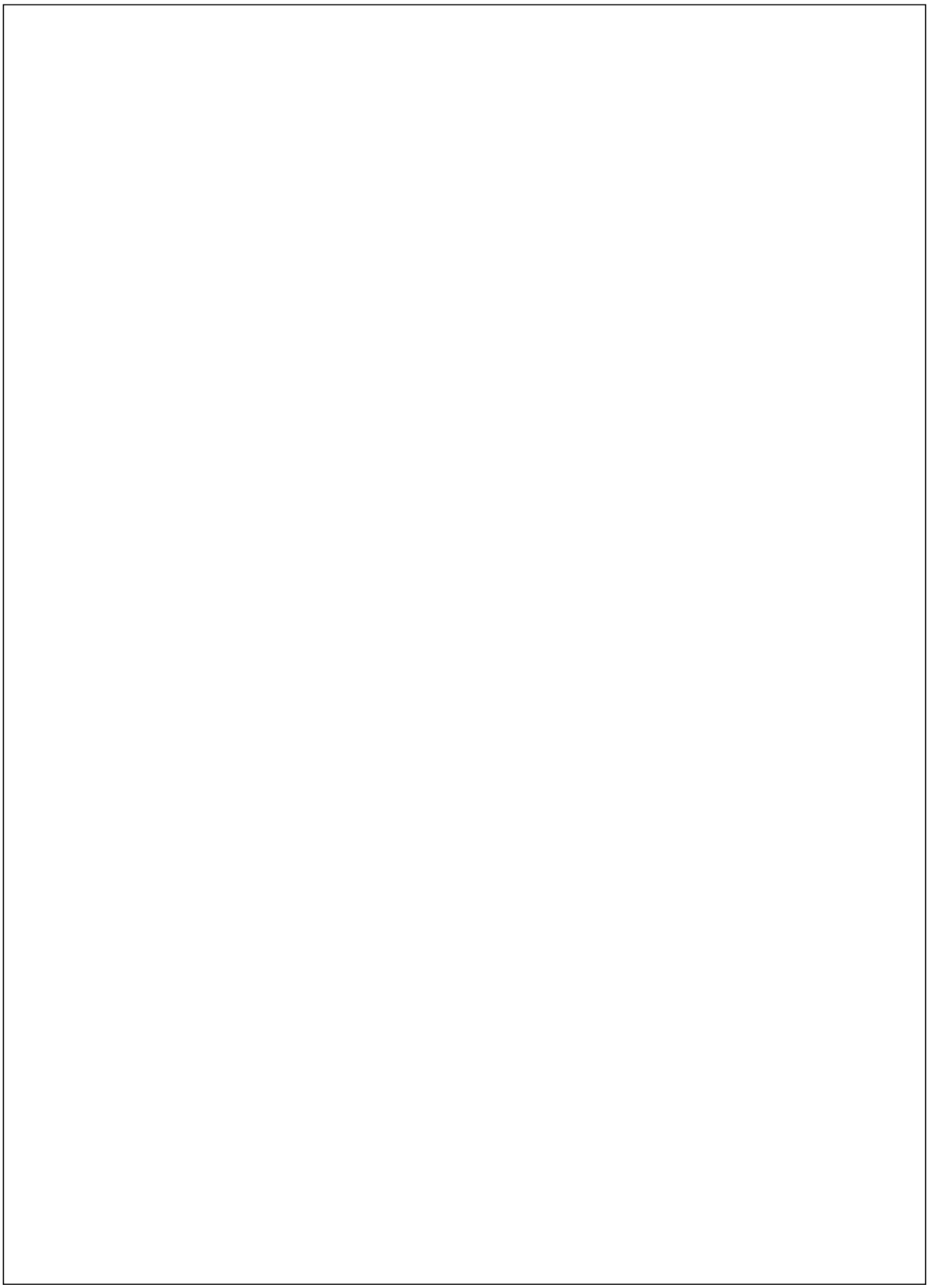
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.60	0.56 + 0.018*SL	0.56 + 0.018*SL	0.56 + 0.018*SL
	t_{PHL}	0.56	0.52 + 0.017*SL	0.54 + 0.011*SL	0.59 + 0.009*SL
	t_R	0.17	0.09 + 0.039*SL	0.09 + 0.041*SL	0.07 + 0.042*SL
	t_F	0.15	0.11 + 0.021*SL	0.13 + 0.015*SL	0.12 + 0.016*SL
CK to QN	t_{PLH}	0.40	0.36 + 0.021*SL	0.36 + 0.019*SL	0.37 + 0.018*SL
	t_{PHL}	0.42	0.39 + 0.015*SL	0.40 + 0.010*SL	0.43 + 0.008*SL
	t_R	0.16	0.07 + 0.046*SL	0.08 + 0.042*SL	0.06 + 0.043*SL
	t_F	0.12	0.09 + 0.018*SL	0.09 + 0.016*SL	0.10 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FJ1D2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

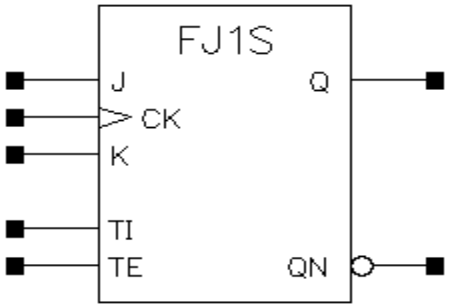
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (J to CK)	t_{HD}	0.000
Input Hold Time (K to CK)	t_{HD}	0.000
Input Setup Time (J to CK)	t_{SU}	0.397
Input Setup Time (K to CK)	t_{SU}	0.342



Inputs: J, K, CK, TI, TE
Outputs: Q, QN
Input Loading (SL):
- J, K, CK, TI: 1
- TE: 2

Maximum Fanout (Rec. SL): All :
- FJ1S: 28
- FJ1SD2:56

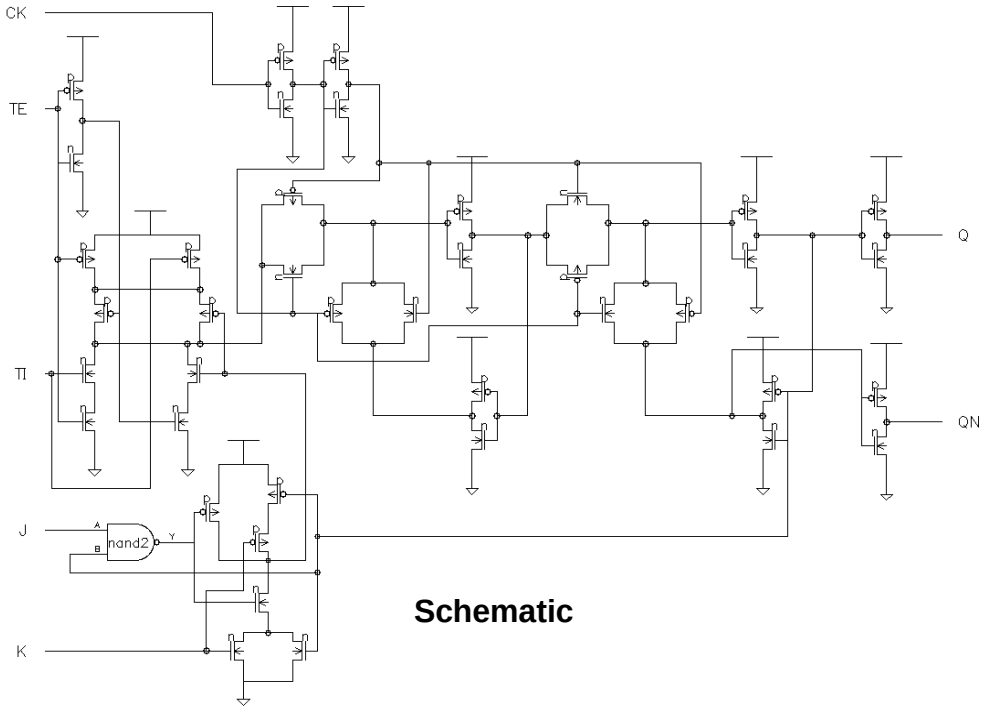
Gate Count:
- FJ1S: 11
- FJ1SD2:12



Symbol

J	K	TI	TE	CK	Qn+1	QNn+1
0	1	x	0	↑	0	1
1	0	x	0	↑	1	0
0	0	x	0	↑	Qn	QNn
1	1	x	0	↑	QNn	Qn
x	x	x	x	↓	Qn	QNn
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0

Truth Table



Schematic

FJ1S Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.47	0.39 + 0.039*SL	0.40 + 0.037*SL	0.40 + 0.036*SL
	t_{PHL}	0.48	0.42 + 0.029*SL	0.46 + 0.019*SL	0.51 + 0.016*SL
	t_R	0.25	0.09 + 0.081*SL	0.08 + 0.083*SL	0.06 + 0.084*SL
	t_F	0.17	0.10 + 0.037*SL	0.12 + 0.031*SL	0.10 + 0.032*SL
CK to QN	t_{PLH}	0.59	0.52 + 0.036*SL	0.52 + 0.036*SL	0.52 + 0.036*SL
	t_{PHL}	0.51	0.47 + 0.021*SL	0.48 + 0.017*SL	0.49 + 0.016*SL
	t_R	0.24	0.07 + 0.084*SL	0.07 + 0.083*SL	0.05 + 0.084*SL
	t_F	0.13	0.07 + 0.031*SL	0.07 + 0.031*SL	0.04 + 0.033*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FJ1S Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (J to CK)	t_{HD}	0.000
Input Hold Time (K to CK)	t_{HD}	0.000
Input Hold Time (TE to CK)	t_{HD}	0.000
Input Hold Time (TI to CK)	t_{HD}	0.000
Input Setup Time (J to CK)	t_{SU}	0.506
Input Setup Time (K to CK)	t_{SU}	0.452
Input Setup Time (TE to CK)	t_{SU}	0.670
Input Setup Time (TI to CK)	t_{SU}	0.670

FJ1SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

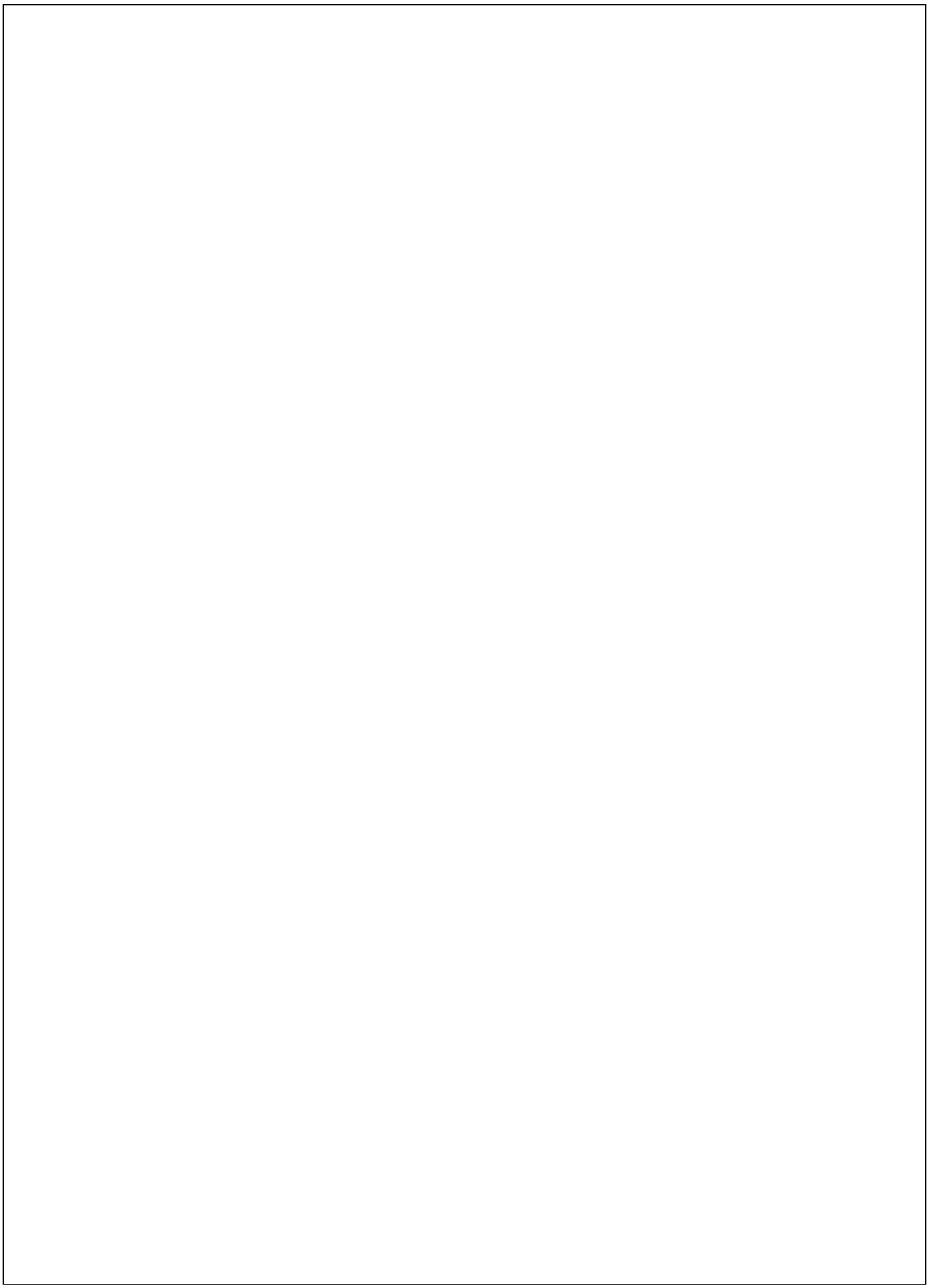
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.46	0.42 + 0.021*SL	0.42 + 0.019*SL	0.43 + 0.018*SL
	t_{PHL}	0.48	0.45 + 0.018*SL	0.47 + 0.012*SL	0.53 + 0.009*SL
	t_R	0.17	0.09 + 0.039*SL	0.09 + 0.042*SL	0.07 + 0.043*SL
	t_F	0.16	0.11 + 0.021*SL	0.13 + 0.016*SL	0.14 + 0.015*SL
CK to QN	t_{PLH}	0.63	0.59 + 0.017*SL	0.59 + 0.018*SL	0.58 + 0.018*SL
	t_{PHL}	0.55	0.53 + 0.012*SL	0.54 + 0.009*SL	0.56 + 0.008*SL
	t_R	0.16	0.10 + 0.031*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
	t_F	0.12	0.09 + 0.013*SL	0.08 + 0.016*SL	0.09 + 0.016*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FJ1SD2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

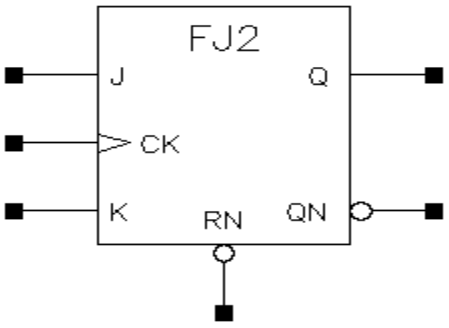
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (J to CK)	t_{HD}	0.000
Input Hold Time (K to CK)	t_{HD}	0.000
Input Hold Time (TE to CK)	t_{HD}	0.000
Input Hold Time (TI to CK)	t_{HD}	0.000
Input Setup Time (J to CK)	t_{SU}	0.506
Input Setup Time (K to CK)	t_{SU}	0.452
Input Setup Time (TE to CK)	t_{SU}	0.670
Input Setup Time (TI to CK)	t_{SU}	0.670



Inputs: J, K, CK, RN
Outputs: Q, QN
Input Loading (SL):
- J, K, CK: 1
- RN: 2

Maximum Fanout (Rec. SL): All :
- FJ2: 28
- FJ2D2:56

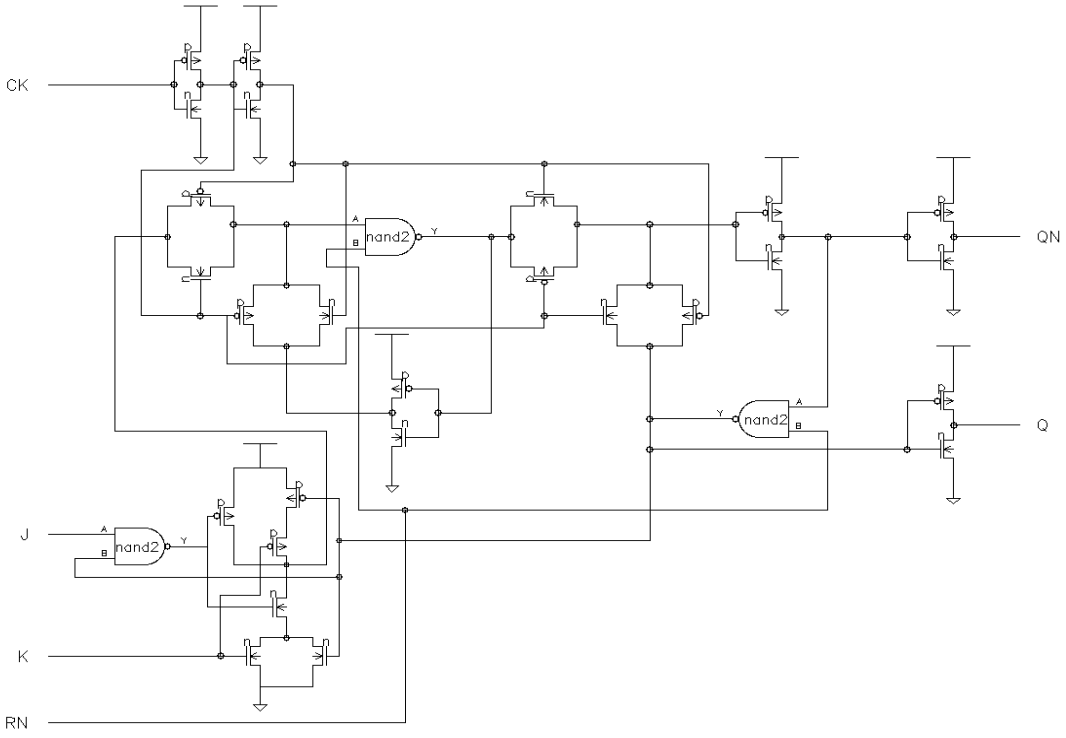
Gate Count:
- FJ2: 10
- FJ2D2: 11



Symbol

J	K	RN	CK	Qn+1	QNn+1
0	1	1	↑	0	1
1	0	1	↑	1	0
0	0	1	↑	Qn	QNn
1	1	1	↑	QNn	Qn
x	x	1	↓	Qn	QNn
x	x	0	x	0	1

Truth Table



Schematic

FJ2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.68	0.60 + 0.041*SL	0.62 + 0.036*SL	0.62 + 0.036*SL
	t_{PHL}	0.54	0.48 + 0.027*SL	0.51 + 0.018*SL	0.55 + 0.016*SL
	t_R	0.27	0.12 + 0.078*SL	0.11 + 0.082*SL	0.07 + 0.084*SL
	t_F	0.17	0.09 + 0.040*SL	0.12 + 0.030*SL	0.09 + 0.032*SL
RN to Q	t_{PHL}	0.45	0.39 + 0.030*SL	0.43 + 0.018*SL	0.46 + 0.016*SL
	t_F	0.20	0.13 + 0.035*SL	0.15 + 0.028*SL	0.08 + 0.032*SL
CK to QN	t_{PLH}	0.42	0.34 + 0.038*SL	0.34 + 0.036*SL	0.35 + 0.036*SL
	t_{PHL}	0.44	0.40 + 0.023*SL	0.41 + 0.017*SL	0.43 + 0.016*SL
	t_R	0.24	0.08 + 0.082*SL	0.07 + 0.084*SL	0.06 + 0.085*SL
	t_F	0.14	0.08 + 0.029*SL	0.07 + 0.032*SL	0.06 + 0.033*SL
RN to QN	t_{PLH}	0.63	0.55 + 0.039*SL	0.56 + 0.036*SL	0.56 + 0.036*SL
	t_R	0.25	0.09 + 0.079*SL	0.08 + 0.083*SL	0.05 + 0.085*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FJ2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (J to CK)	t_{HD}	0.000
Input Hold Time (K to CK)	t_{HD}	0.000
Input Setup Time (J to CK)	t_{SU}	0.397
Input Setup Time (K to CK)	t_{SU}	0.342
Recovery Time (RN)	t_{RC}	0.139

FJ2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

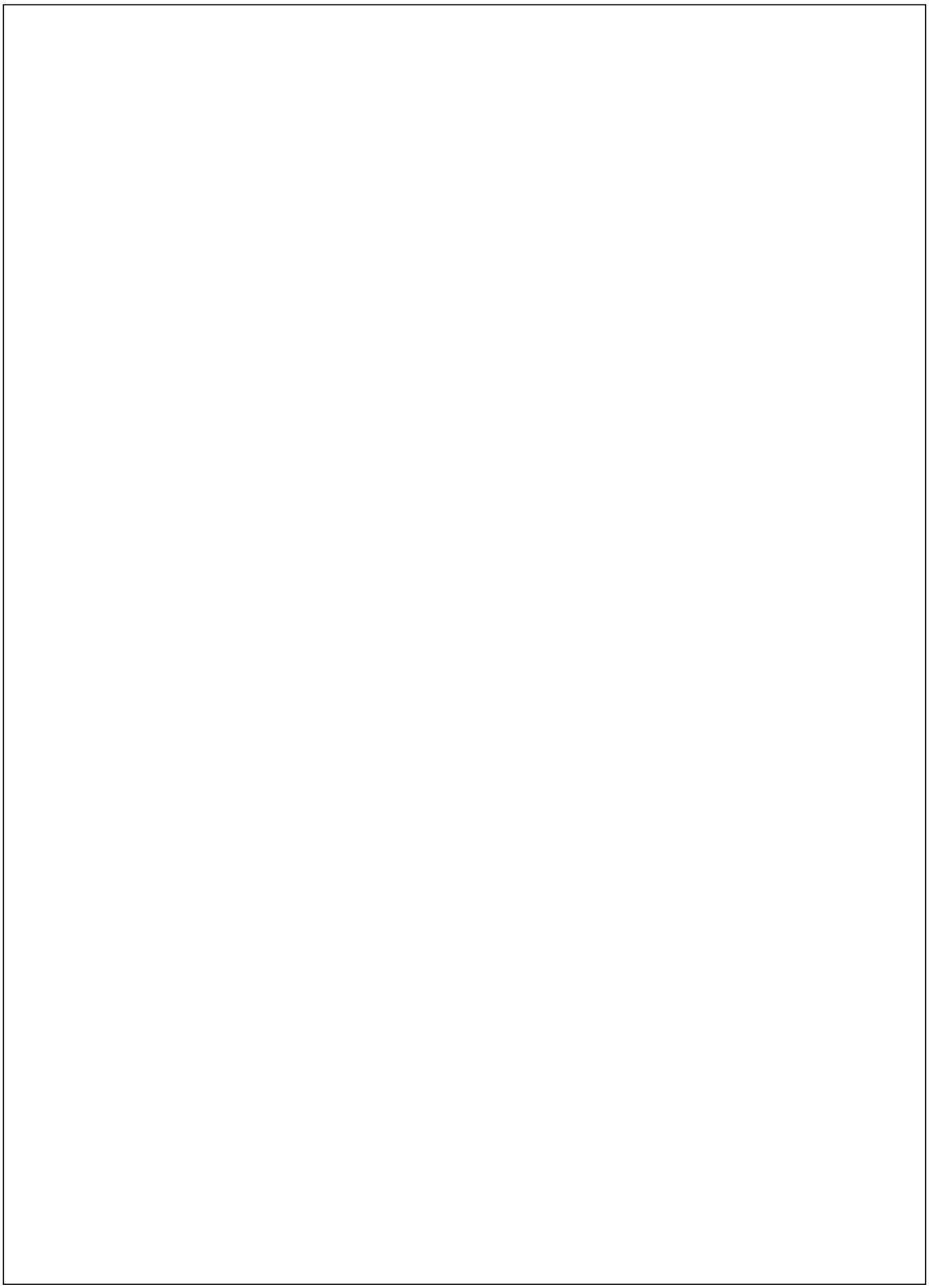
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.73	0.68 + 0.021*SL	0.69 + 0.019*SL	0.70 + 0.018*SL
	t_{PHL}	0.57	0.54 + 0.018*SL	0.56 + 0.011*SL	0.60 + 0.009*SL
	t_R	0.19	0.11 + 0.041*SL	0.11 + 0.041*SL	0.10 + 0.042*SL
	t_F	0.15	0.11 + 0.021*SL	0.12 + 0.016*SL	0.13 + 0.015*SL
RN to Q	t_{PHL}	0.45	0.41 + 0.020*SL	0.44 + 0.011*SL	0.49 + 0.008*SL
	t_F	0.18	0.15 + 0.019*SL	0.16 + 0.014*SL	0.14 + 0.015*SL
CK to QN	t_{PLH}	0.41	0.37 + 0.020*SL	0.37 + 0.019*SL	0.38 + 0.018*SL
	t_{PHL}	0.45	0.42 + 0.016*SL	0.44 + 0.010*SL	0.47 + 0.009*SL
	t_R	0.16	0.08 + 0.044*SL	0.08 + 0.041*SL	0.06 + 0.043*SL
	t_F	0.13	0.09 + 0.019*SL	0.10 + 0.016*SL	0.09 + 0.016*SL
RN to QN	t_{PLH}	0.62	0.58 + 0.020*SL	0.59 + 0.018*SL	0.59 + 0.018*SL
	t_R	0.17	0.10 + 0.036*SL	0.08 + 0.042*SL	0.06 + 0.043*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FJ2D2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

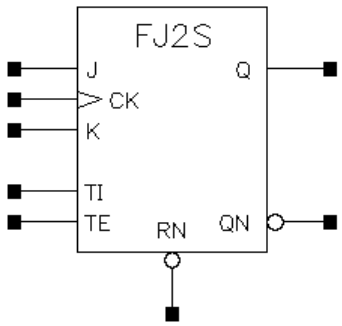
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (J to CK)	t_{HD}	0.000
Input Hold Time (K to CK)	t_{HD}	0.000
Input Setup Time (J to CK)	t_{SU}	0.397
Input Setup Time (K to CK)	t_{SU}	0.342
Recovery Time (RN)	t_{RC}	0.139



Inputs: J, K, CK, TI, TE, RN
Outputs: Q, QN
Input Loading (SL):
- J, K, CK, TI: 1
- TE, RN: 2

Maximum Fanout (Rec. SL): All :
- FJ2S: 28
- FJ2SD2: 56

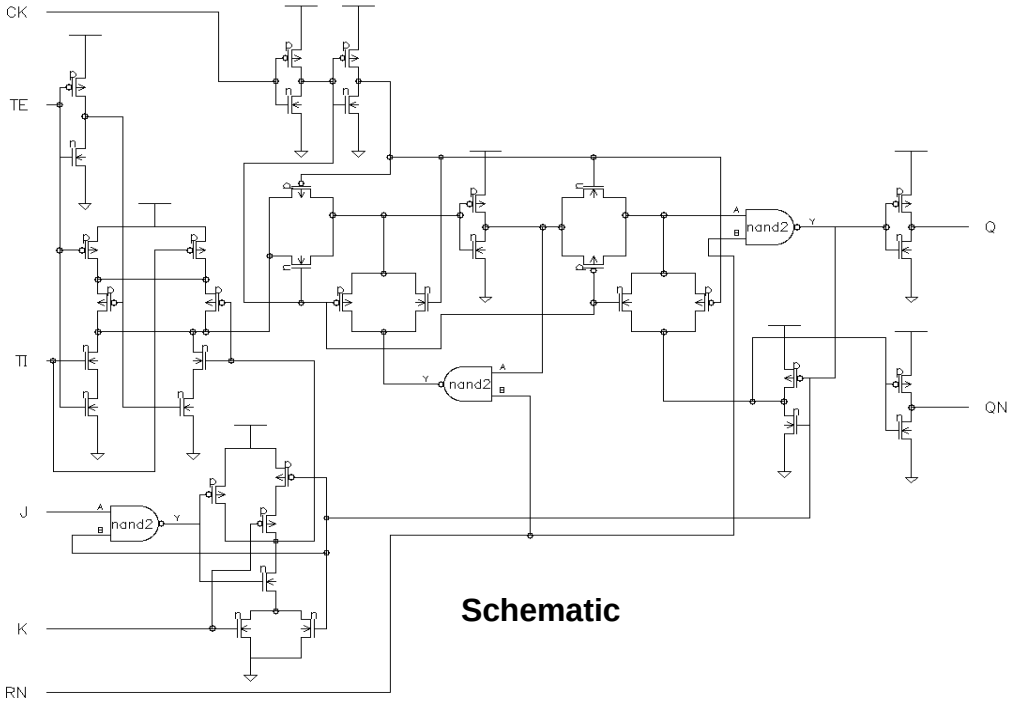
Gate Count:
- FJ2S: 12
- FJ2SD2: 13



Symbol

J	K	RN	TI	TE	CK	Qn+1	QNn+1
0	1	1	x	0	↑	0	1
1	0	1	x	0	↑	1	0
0	0	1	x	0	↑	Qn	QNn
1	1	1	x	0	↑	QNn	Qn
x	x	1	x	0	↓	Qn	QNn
x	x	0	x	x	x	0	1
x	x	1	0	1	↑	0	1
x	x	1	1	1	↑	1	0

Truth Table



Schematic

FJ2S Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.56	0.48 + 0.043*SL	0.49 + 0.038*SL	0.51 + 0.038*SL
	tPHL	0.50	0.44 + 0.031*SL	0.47 + 0.019*SL	0.53 + 0.016*SL
	tR	0.28	0.10 + 0.091*SL	0.12 + 0.086*SL	0.08 + 0.088*SL
	tF	0.18	0.11 + 0.038*SL	0.13 + 0.031*SL	0.11 + 0.032*SL
RN to Q	tPHL	0.47	0.41 + 0.032*SL	0.45 + 0.018*SL	0.50 + 0.016*SL
	tF	0.21	0.15 + 0.032*SL	0.15 + 0.029*SL	0.10 + 0.032*SL
CK to QN	tPLH	0.62	0.55 + 0.037*SL	0.55 + 0.037*SL	0.55 + 0.037*SL
	tPHL	0.61	0.57 + 0.020*SL	0.58 + 0.017*SL	0.59 + 0.016*SL
	tR	0.24	0.07 + 0.086*SL	0.07 + 0.086*SL	0.05 + 0.087*SL
	tF	0.14	0.07 + 0.034*SL	0.08 + 0.031*SL	0.06 + 0.032*SL
RN to QN	tPLH	0.60	0.53 + 0.038*SL	0.53 + 0.037*SL	0.52 + 0.037*SL
	tR	0.25	0.08 + 0.085*SL	0.08 + 0.085*SL	0.05 + 0.086*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FJ2S Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.506
Input Setup Time (K to CK)	tSU	0.452
Input Setup Time (TE to CK)	tSU	0.670
Input Setup Time (TI to CK)	tSU	0.670
Recovery Time (RN)	tRC	0.139

FJ2SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

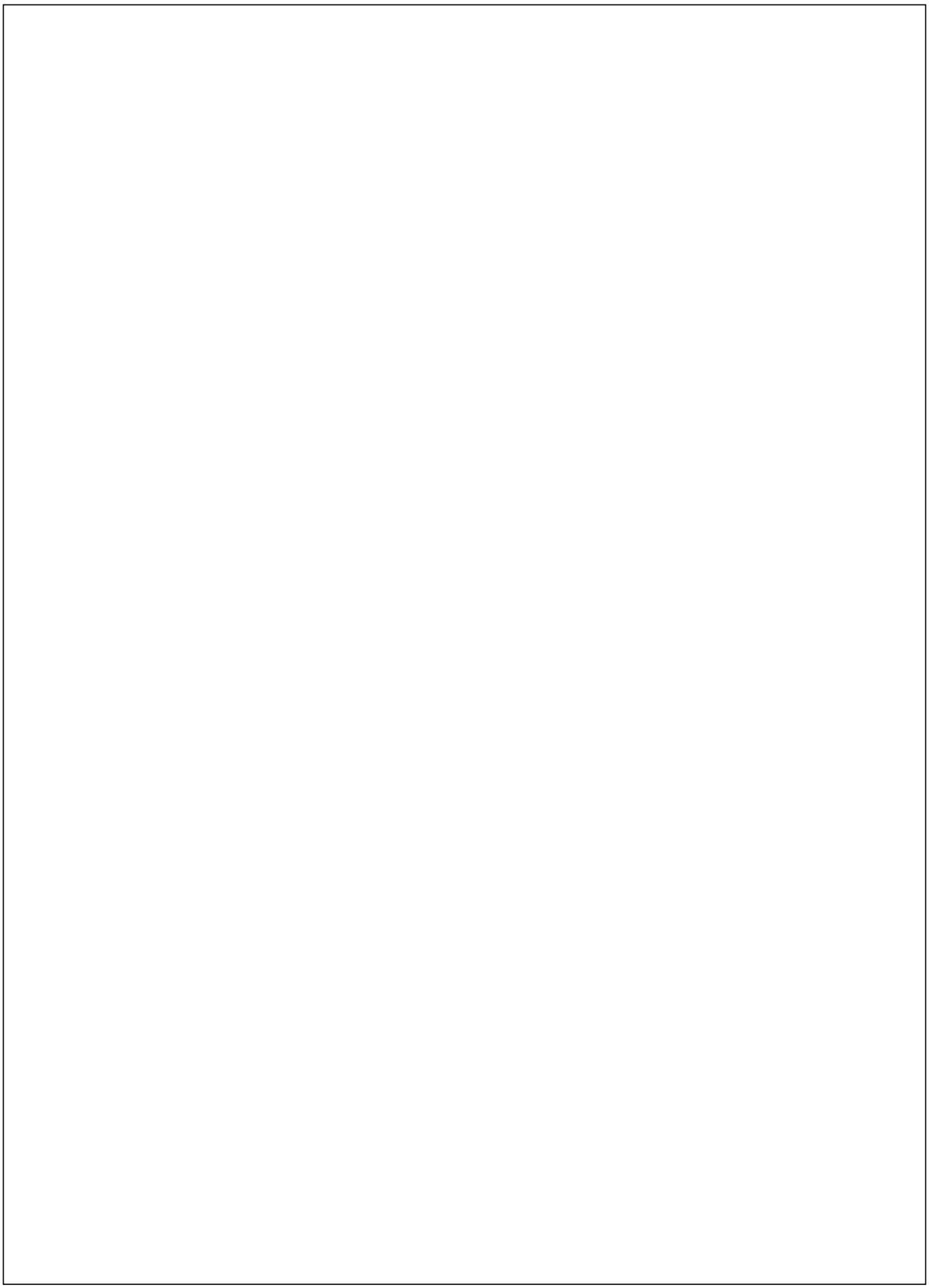
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.55	0.50 + 0.024*SL	0.52 + 0.020*SL	0.54 + 0.019*SL
	tPHL	0.50	0.47 + 0.018*SL	0.48 + 0.012*SL	0.54 + 0.009*SL
	tR	0.20	0.12 + 0.043*SL	0.12 + 0.044*SL	0.10 + 0.044*SL
	tF	0.16	0.13 + 0.016*SL	0.13 + 0.017*SL	0.15 + 0.016*SL
RN to Q	tPHL	0.47	0.43 + 0.020*SL	0.46 + 0.011*SL	0.51 + 0.009*SL
	tF	0.19	0.16 + 0.018*SL	0.17 + 0.015*SL	0.15 + 0.016*SL
CK to QN	tPLH	0.65	0.62 + 0.017*SL	0.62 + 0.018*SL	0.61 + 0.018*SL
	tPHL	0.66	0.64 + 0.012*SL	0.64 + 0.010*SL	0.67 + 0.008*SL
	tR	0.16	0.10 + 0.032*SL	0.07 + 0.041*SL	0.06 + 0.042*SL
	tF	0.13	0.10 + 0.016*SL	0.10 + 0.015*SL	0.09 + 0.016*SL
RN to QN	tPLH	0.63	0.60 + 0.016*SL	0.59 + 0.018*SL	0.59 + 0.018*SL
	tR	0.17	0.09 + 0.037*SL	0.08 + 0.041*SL	0.06 + 0.042*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FJ2SD2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

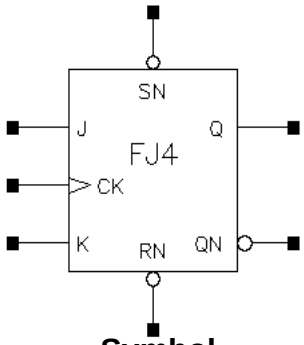
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.506
Input Setup Time (K to CK)	tSU	0.452
Input Setup Time (TE to CK)	tSU	0.670
Input Setup Time (TI to CK)	tSU	0.670
Recovery Time (RN)	tRC	0.139



Inputs: J, K, CK, SN, RN
Outputs: Q, QN
Input Loading (SL):
- J, K, CK: 1
- SN, RN: 2

Maximum Fanout (Rec. SL): All :
- FJ4: 28
- FJ4D2:56

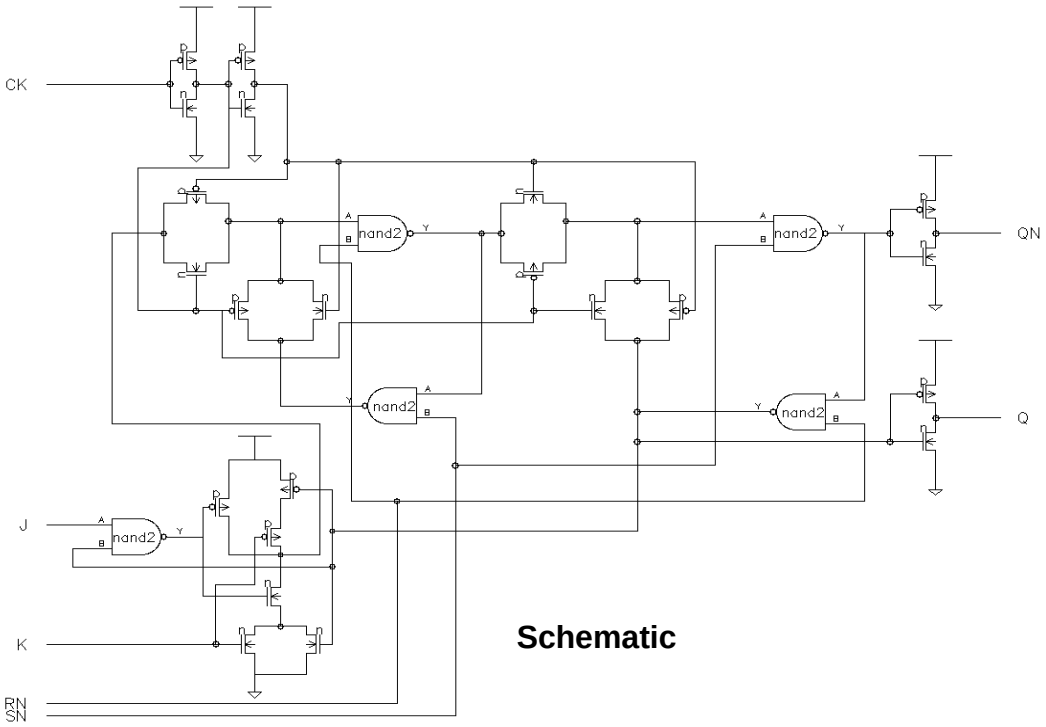
Gate Count:
- FJ4: 11
- FJ4D2:12



Symbol

J	K	RN	SN	CK	Qn+1	QNn+1
0	1	1	1	↑	0	1
1	0	1	1	↑	1	0
0	0	1	1	↑	Qn	QNn
1	1	1	1	↑	QNn	Qn
x	x	1	1	↓	Qn	QNn
x	x	0	1	x	0	1
x	x	1	0	x	1	0
x	x	0	0	x	0	0

Truth Table



Schematic

FJ4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.64	0.56 + 0.039*SL	0.58 + 0.036*SL	0.57 + 0.036*SL
	tR	0.27	0.11 + 0.080*SL	0.10 + 0.082*SL	0.07 + 0.084*SL
CK to Q	tPLH	0.69	0.61 + 0.041*SL	0.62 + 0.036*SL	0.62 + 0.036*SL
	tPHL	0.60	0.54 + 0.027*SL	0.57 + 0.018*SL	0.61 + 0.016*SL
	tR	0.28	0.11 + 0.081*SL	0.11 + 0.082*SL	0.07 + 0.084*SL
	tF	0.17	0.11 + 0.034*SL	0.12 + 0.031*SL	0.09 + 0.032*SL
RN to Q	tPLH	0.31	0.23 + 0.042*SL	0.24 + 0.036*SL	0.25 + 0.036*SL
	tPHL	0.46	0.40 + 0.031*SL	0.44 + 0.018*SL	0.48 + 0.016*SL
	tR	0.28	0.13 + 0.078*SL	0.12 + 0.081*SL	0.07 + 0.084*SL
	tF	0.20	0.14 + 0.032*SL	0.15 + 0.029*SL	0.09 + 0.032*SL
SN to QN	tPLH	0.22	0.13 + 0.043*SL	0.15 + 0.036*SL	0.14 + 0.037*SL
	tPHL	0.38	0.33 + 0.026*SL	0.36 + 0.018*SL	0.39 + 0.016*SL
	tR	0.27	0.12 + 0.078*SL	0.11 + 0.082*SL	0.06 + 0.084*SL
	tF	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.08 + 0.033*SL
CK to QN	tPLH	0.47	0.39 + 0.040*SL	0.40 + 0.037*SL	0.41 + 0.036*SL
	tPHL	0.45	0.40 + 0.024*SL	0.42 + 0.017*SL	0.44 + 0.016*SL
	tR	0.25	0.09 + 0.082*SL	0.08 + 0.083*SL	0.06 + 0.084*SL
	tF	0.15	0.08 + 0.034*SL	0.08 + 0.032*SL	0.07 + 0.033*SL
RN to QN	tPLH	0.68	0.60 + 0.039*SL	0.61 + 0.036*SL	0.61 + 0.036*SL
	tR	0.26	0.10 + 0.077*SL	0.09 + 0.083*SL	0.06 + 0.084*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FJ4 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.397
Input Setup Time (K to CK)	tSU	0.342
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

FJ4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

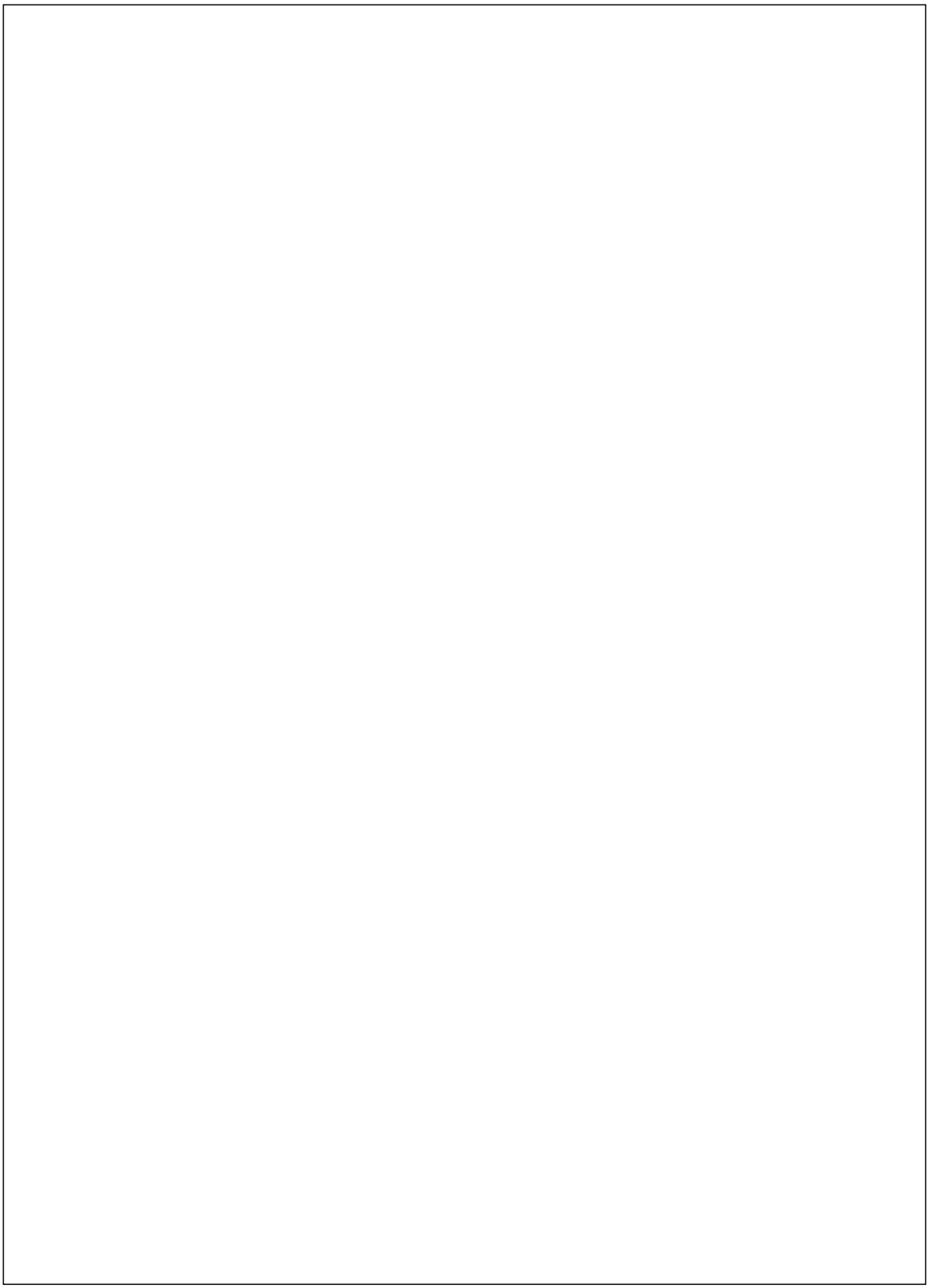
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	t_{PLH}	0.69	0.65 + 0.020*SL	0.66 + 0.018*SL	0.66 + 0.018*SL
	t_R	0.21	0.13 + 0.040*SL	0.13 + 0.040*SL	0.09 + 0.042*SL
CK to Q	t_{PLH}	0.73	0.69 + 0.020*SL	0.70 + 0.019*SL	0.71 + 0.018*SL
	t_{PHL}	0.64	0.61 + 0.016*SL	0.62 + 0.011*SL	0.67 + 0.009*SL
	t_R	0.20	0.12 + 0.041*SL	0.12 + 0.041*SL	0.10 + 0.042*SL
	t_F	0.16	0.12 + 0.020*SL	0.13 + 0.015*SL	0.13 + 0.016*SL
RN to Q	t_{PLH}	0.30	0.26 + 0.022*SL	0.27 + 0.019*SL	0.29 + 0.018*SL
	t_{PHL}	0.46	0.42 + 0.020*SL	0.44 + 0.011*SL	0.50 + 0.008*SL
	t_R	0.21	0.12 + 0.044*SL	0.13 + 0.040*SL	0.11 + 0.041*SL
	t_F	0.18	0.14 + 0.020*SL	0.16 + 0.014*SL	0.16 + 0.014*SL
SN to QN	t_{PLH}	0.22	0.18 + 0.021*SL	0.18 + 0.019*SL	0.20 + 0.018*SL
	t_{PHL}	0.39	0.36 + 0.016*SL	0.38 + 0.011*SL	0.42 + 0.009*SL
	t_R	0.20	0.13 + 0.035*SL	0.11 + 0.041*SL	0.09 + 0.042*SL
	t_F	0.16	0.13 + 0.014*SL	0.13 + 0.015*SL	0.12 + 0.016*SL
CK to QN	t_{PLH}	0.47	0.43 + 0.022*SL	0.43 + 0.019*SL	0.44 + 0.018*SL
	t_{PHL}	0.45	0.42 + 0.017*SL	0.44 + 0.010*SL	0.47 + 0.009*SL
	t_R	0.18	0.10 + 0.041*SL	0.09 + 0.042*SL	0.07 + 0.043*SL
	t_F	0.13	0.09 + 0.018*SL	0.10 + 0.016*SL	0.09 + 0.016*SL
RN to QN	t_{PLH}	0.68	0.63 + 0.023*SL	0.65 + 0.019*SL	0.66 + 0.018*SL
	t_R	0.19	0.11 + 0.041*SL	0.11 + 0.041*SL	0.08 + 0.043*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FJ4D2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

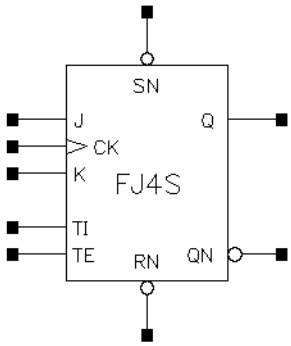
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (J to CK)	t_{HD}	0.000
Input Hold Time (K to CK)	t_{HD}	0.000
Input Setup Time (J to CK)	t_{SU}	0.397
Input Setup Time (K to CK)	t_{SU}	0.342
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139



Inputs: J, K, CK, TI, TE, SN, RN
Outputs: Q, QN
Input Loading (SL):
- J, K, CK, TI: 1
- TE, SN, RN: 2

Maximum Fanout (Rec. SL): All :
- FJ4S: 28
- FJ4SD2: 56

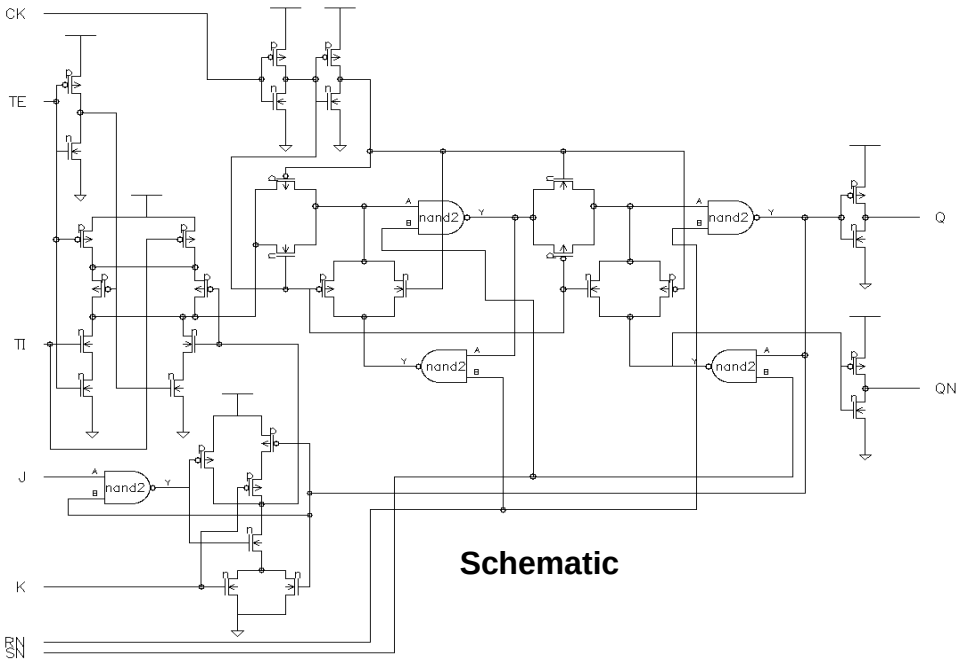
Gate Count:
- FJ4S: 13
- FJ4SD2: 14



Symbol

J	K	RN	SN	TI	TE	CK	Qn+1	QNn+1
0	1	1	1	x	0	↑	0	1
1	0	1	1	x	0	↑	1	0
0	0	1	1	x	0	↑	Qn	QNn
1	1	1	1	x	0	↑	QNn	Qn
x	x	1	1	x	0	↓	Qn	QNn
x	x	0	1	x	x	x	0	1
x	x	1	0	x	x	x	1	0
x	x	0	0	x	x	x	0	0
x	x	1	1	0	1	↑	0	1
x	x	1	1	1	1	↑	1	0

Truth Table



Schematic

FJ4S Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.78	0.70 + 0.040*SL	0.71 + 0.036*SL	0.71 + 0.036*SL
	tR	0.28	0.13 + 0.079*SL	0.12 + 0.082*SL	0.07 + 0.084*SL
CK to Q	tPLH	0.56	0.47 + 0.043*SL	0.49 + 0.037*SL	0.51 + 0.036*SL
	tPHL	0.53	0.47 + 0.031*SL	0.50 + 0.019*SL	0.56 + 0.016*SL
	tR	0.28	0.10 + 0.087*SL	0.12 + 0.082*SL	0.08 + 0.084*SL
	tF	0.18	0.11 + 0.036*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
RN to Q	tPLH	0.32	0.24 + 0.039*SL	0.25 + 0.037*SL	0.26 + 0.036*SL
	tPHL	0.46	0.40 + 0.031*SL	0.44 + 0.019*SL	0.49 + 0.016*SL
	tR	0.29	0.13 + 0.080*SL	0.13 + 0.082*SL	0.07 + 0.084*SL
	tF	0.20	0.14 + 0.033*SL	0.15 + 0.030*SL	0.11 + 0.032*SL
SN to QN	tPLH	0.22	0.13 + 0.042*SL	0.15 + 0.036*SL	0.15 + 0.036*SL
	tPHL	0.37	0.32 + 0.026*SL	0.34 + 0.017*SL	0.36 + 0.016*SL
	tR	0.27	0.10 + 0.082*SL	0.10 + 0.082*SL	0.06 + 0.084*SL
	tF	0.17	0.10 + 0.034*SL	0.11 + 0.030*SL	0.07 + 0.032*SL
CK to QN	tPLH	0.71	0.63 + 0.038*SL	0.64 + 0.036*SL	0.64 + 0.036*SL
	tPHL	0.61	0.56 + 0.024*SL	0.58 + 0.017*SL	0.60 + 0.016*SL
	tR	0.25	0.09 + 0.080*SL	0.09 + 0.083*SL	0.06 + 0.084*SL
	tF	0.14	0.08 + 0.031*SL	0.08 + 0.031*SL	0.06 + 0.032*SL
RN to QN	tPLH	0.64	0.57 + 0.036*SL	0.57 + 0.036*SL	0.57 + 0.036*SL
	tR	0.26	0.10 + 0.080*SL	0.09 + 0.082*SL	0.06 + 0.084*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FJ4S Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.506
Input Setup Time (K to CK)	tSU	0.506
Input Setup Time (TE to CK)	tSU	0.725
Input Setup Time (TI to CK)	tSU	0.725

FJ4S Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139

FJ4SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	t_{PLH}	0.77	0.73 + 0.023*SL	0.74 + 0.019*SL	0.75 + 0.018*SL
	t_R	0.22	0.15 + 0.037*SL	0.13 + 0.041*SL	0.10 + 0.042*SL
CK to Q	t_{PLH}	0.55	0.51 + 0.023*SL	0.52 + 0.020*SL	0.55 + 0.018*SL
	t_{PHL}	0.53	0.49 + 0.018*SL	0.51 + 0.012*SL	0.57 + 0.009*SL
	t_R	0.21	0.11 + 0.048*SL	0.13 + 0.041*SL	0.11 + 0.042*SL
	t_F	0.17	0.14 + 0.016*SL	0.13 + 0.017*SL	0.16 + 0.015*SL
RN to Q	t_{PLH}	0.31	0.26 + 0.024*SL	0.27 + 0.019*SL	0.29 + 0.018*SL
	t_{PHL}	0.46	0.41 + 0.022*SL	0.44 + 0.012*SL	0.50 + 0.009*SL
	t_R	0.22	0.14 + 0.040*SL	0.14 + 0.041*SL	0.12 + 0.042*SL
	t_F	0.19	0.15 + 0.020*SL	0.17 + 0.015*SL	0.15 + 0.015*SL
SN to QN	t_{PLH}	0.22	0.17 + 0.022*SL	0.18 + 0.019*SL	0.19 + 0.018*SL
	t_{PHL}	0.38	0.34 + 0.016*SL	0.36 + 0.010*SL	0.39 + 0.009*SL
	t_R	0.19	0.12 + 0.035*SL	0.11 + 0.041*SL	0.09 + 0.042*SL
	t_F	0.16	0.12 + 0.018*SL	0.13 + 0.015*SL	0.13 + 0.015*SL
CK to QN	t_{PLH}	0.75	0.72 + 0.018*SL	0.72 + 0.018*SL	0.72 + 0.018*SL
	t_{PHL}	0.66	0.63 + 0.013*SL	0.64 + 0.010*SL	0.67 + 0.008*SL
	t_R	0.19	0.10 + 0.041*SL	0.11 + 0.040*SL	0.07 + 0.042*SL
	t_F	0.13	0.09 + 0.017*SL	0.10 + 0.016*SL	0.09 + 0.016*SL
RN to QN	t_{PLH}	0.69	0.65 + 0.017*SL	0.65 + 0.018*SL	0.65 + 0.018*SL
	t_R	0.19	0.11 + 0.036*SL	0.10 + 0.041*SL	0.07 + 0.042*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

FJ4SD2 Timing Requirements

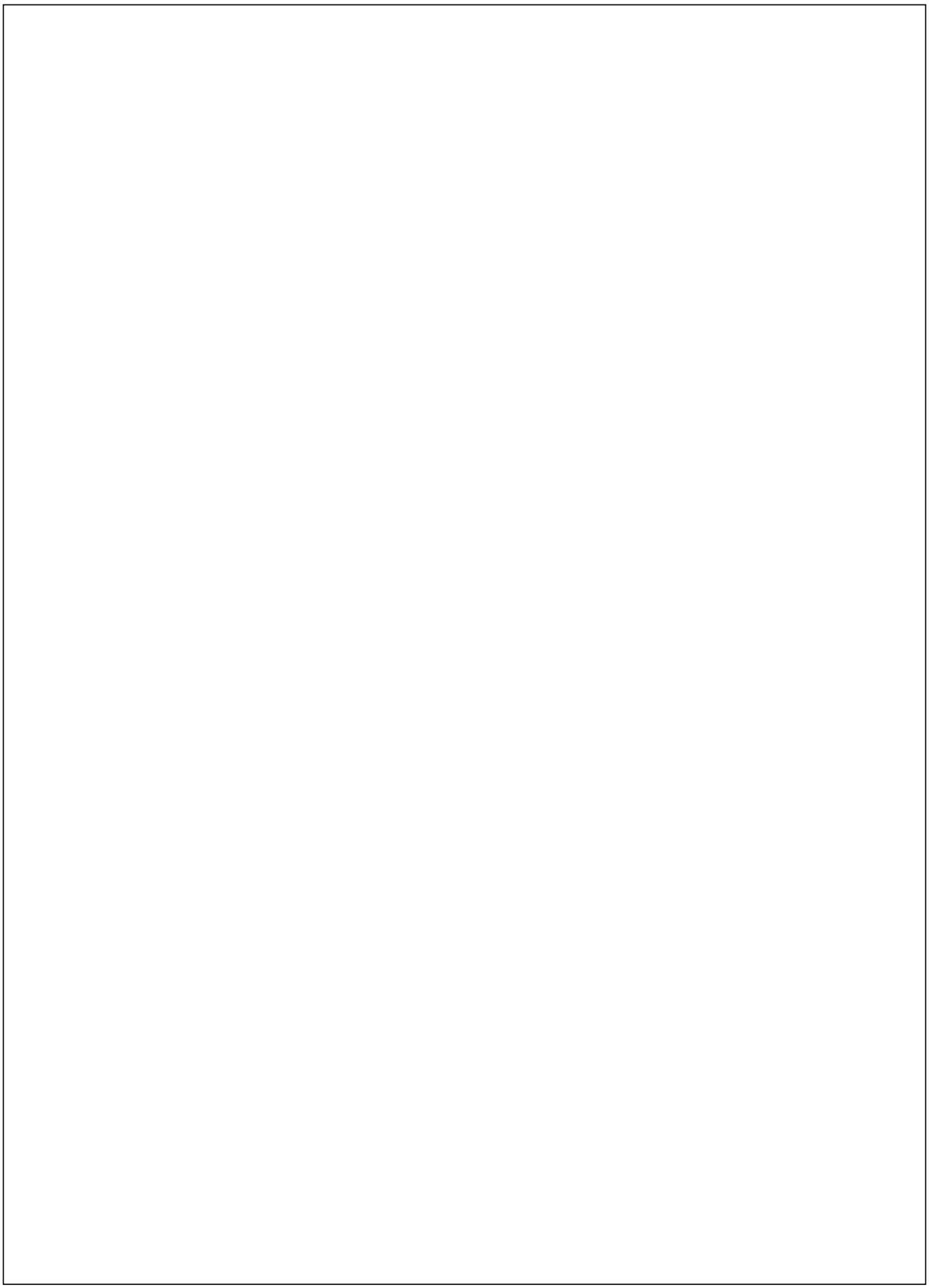
[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.920
Pulse Width Low (RN)	t_{PWL}	0.920
Pulse Width Low (SN)	t_{PWL}	0.920
Pulse Width High (CK)	t_{PWH}	0.920
Input Hold Time (J to CK)	t_{HD}	0.000
Input Hold Time (K to CK)	t_{HD}	0.000
Input Hold Time (TE to CK)	t_{HD}	0.000
Input Hold Time (TI to CK)	t_{HD}	0.000
Input Setup Time (J to CK)	t_{SU}	0.506
Input Setup Time (K to CK)	t_{SU}	0.506

FJ4SD2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

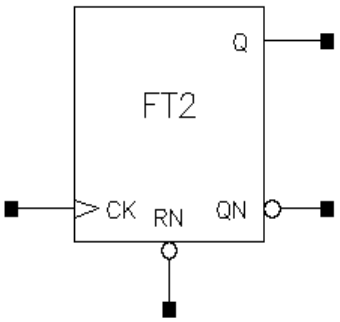
Parameter	Symbol	Value [ns]
Input Setup Time (TE to CK)	t_{SU}	0.725
Input Setup Time (TI to CK)	t_{SU}	0.725
Recovery Time (RN)	t_{RC}	0.139
Recovery Time (SN)	t_{RC}	0.139



Inputs: CK, RN
Outputs: Q, QN
Input Loading (SL):
- CK: 1
- RN: 2

Maximum Fanout (Rec. SL): All :
- FT2: 28
- FT2D2:56

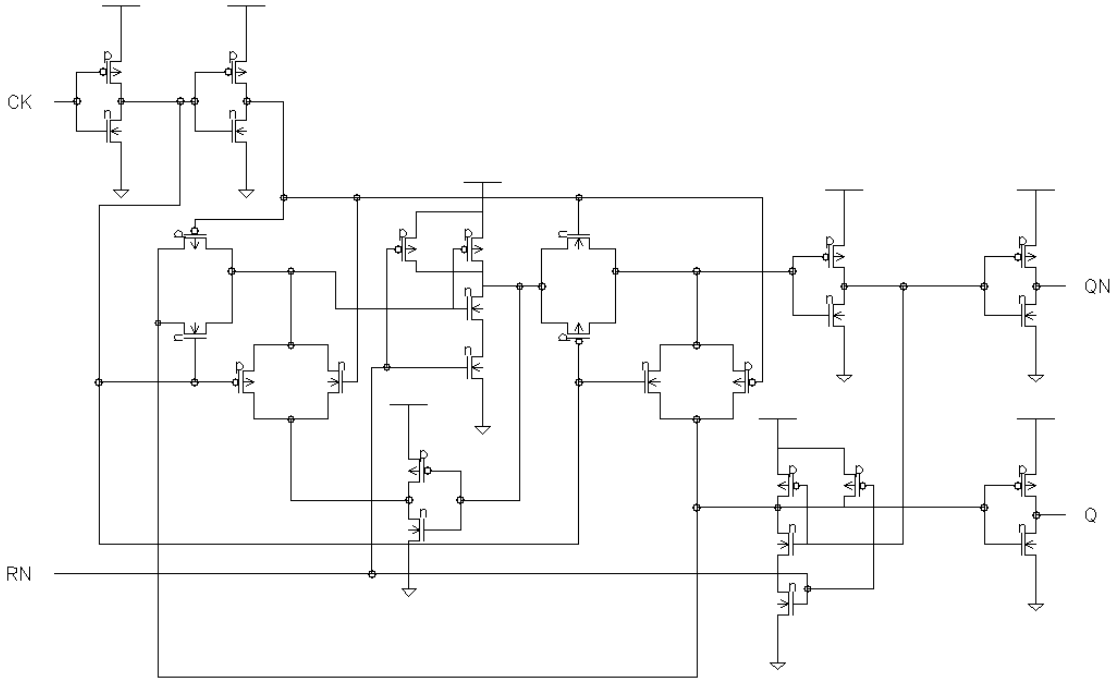
Gate Count:
- FT2: 7
- FT2D2:8



Symbol

RN	CK	Qn+1	QNn+1
1	⎍	QNn	Qn
0	x	0	1

Truth Table



Schematic

FT2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t_{PLH}	0.63	0.56 + 0.038*SL	0.56 + 0.036*SL	0.56 + 0.036*SL
	t_{PHL}	0.49	0.44 + 0.023*SL	0.46 + 0.017*SL	0.48 + 0.016*SL
	t_R	0.25	0.09 + 0.083*SL	0.09 + 0.082*SL	0.05 + 0.084*SL
	t_F	0.14	0.07 + 0.036*SL	0.09 + 0.030*SL	0.06 + 0.032*SL
RN to Q	t_{PHL}	0.39	0.34 + 0.026*SL	0.36 + 0.017*SL	0.39 + 0.016*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.029*SL	0.07 + 0.032*SL
CK to QN	t_{PLH}	0.42	0.34 + 0.038*SL	0.35 + 0.037*SL	0.35 + 0.036*SL
	t_{PHL}	0.44	0.40 + 0.023*SL	0.41 + 0.017*SL	0.44 + 0.016*SL
	t_R	0.24	0.08 + 0.080*SL	0.07 + 0.084*SL	0.05 + 0.085*SL
	t_F	0.14	0.08 + 0.029*SL	0.07 + 0.032*SL	0.06 + 0.033*SL
RN to QN	t_{PLH}	0.62	0.55 + 0.039*SL	0.55 + 0.036*SL	0.56 + 0.036*SL
	t_R	0.24	0.09 + 0.077*SL	0.07 + 0.084*SL	0.05 + 0.085*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FT2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t_{PWL}	0.000
Pulse Width Low (RN)	t_{PWL}	0.000
Pulse Width High (CK)	t_{PWH}	0.000
Recovery Time (RN)	t_{RC}	0.000

FT2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

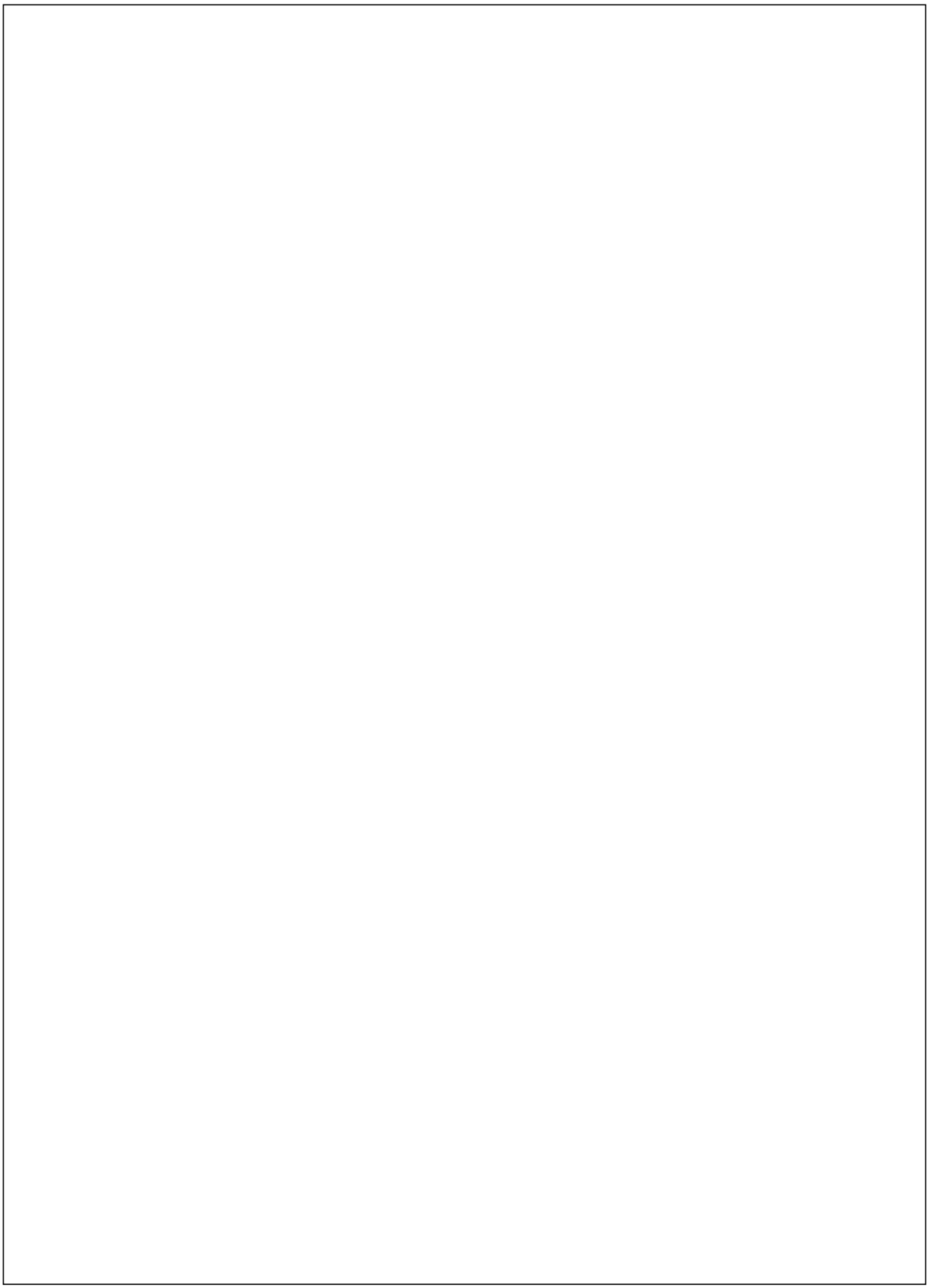
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.68	0.64 + 0.021*SL	0.65 + 0.018*SL	0.64 + 0.018*SL
	tPHL	0.53	0.50 + 0.017*SL	0.52 + 0.010*SL	0.55 + 0.008*SL
	tR	0.19	0.11 + 0.039*SL	0.11 + 0.040*SL	0.08 + 0.042*SL
	tF	0.13	0.08 + 0.023*SL	0.10 + 0.015*SL	0.09 + 0.016*SL
RN to Q	tPHL	0.40	0.36 + 0.017*SL	0.38 + 0.011*SL	0.43 + 0.008*SL
	tF	0.16	0.13 + 0.018*SL	0.14 + 0.014*SL	0.12 + 0.015*SL
CK to QN	tPLH	0.41	0.37 + 0.021*SL	0.38 + 0.018*SL	0.38 + 0.018*SL
	tPHL	0.45	0.43 + 0.014*SL	0.44 + 0.010*SL	0.47 + 0.009*SL
	tR	0.17	0.08 + 0.042*SL	0.08 + 0.042*SL	0.06 + 0.043*SL
	tF	0.14	0.10 + 0.016*SL	0.10 + 0.016*SL	0.11 + 0.016*SL
RN to QN	tPLH	0.62	0.59 + 0.017*SL	0.58 + 0.019*SL	0.60 + 0.018*SL
	tR	0.17	0.10 + 0.034*SL	0.08 + 0.042*SL	0.06 + 0.043*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 20.00, *Range3 : 20.00 < SL

FT2D2 Timing Requirements

[Values for typical process, 25.00°C, 3.30V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.000
Pulse Width Low (RN)	tPWL	0.000
Pulse Width High (CK)	tPWH	0.000
Recovery Time (RN)	tRC	0.000

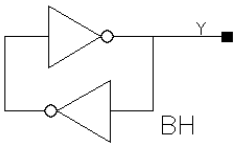


Busholder

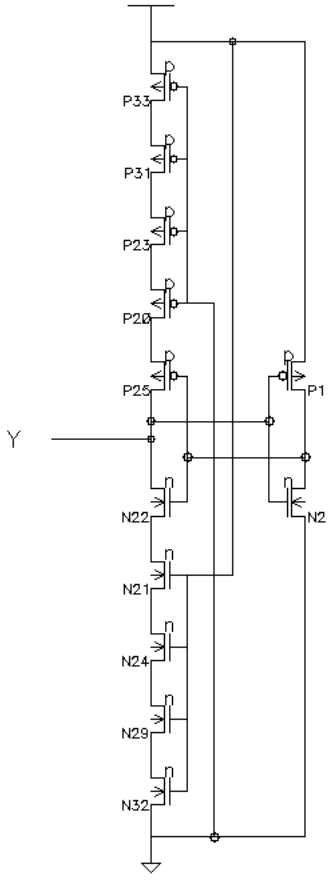
Inputs: Y
Outputs: Y

Input Loading (SL): 2

Gate Count: 2



Symbol



Schematic