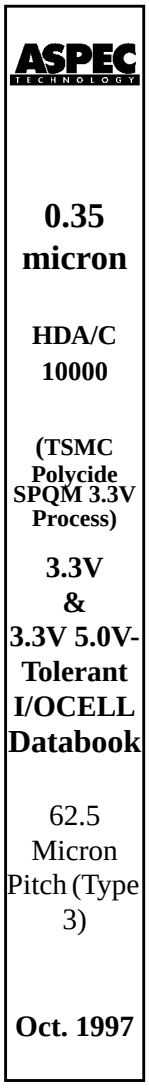
ASPEC Technology, Inc.

0.35 Micron

HDA/C 10000
(TSMC Polycide SPQM 3.3V Process)

3.3V
&
3.3V 5.0V-Tolerant
I/OCELL Databook
62.5 Micron Pitch (Type 3)

October 1997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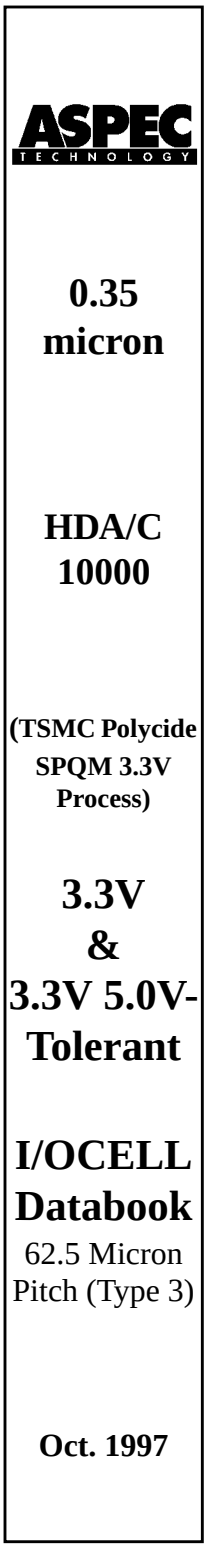
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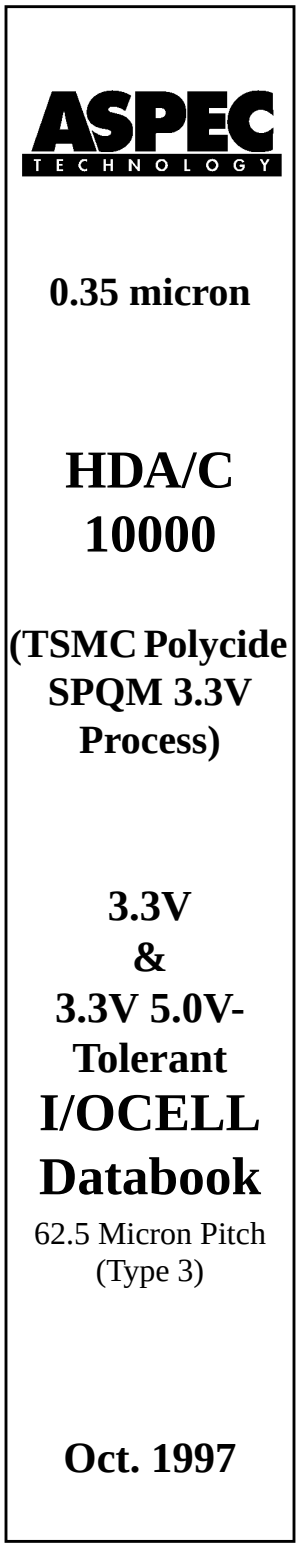
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Table of Contents

Chapter 1: Introduction to the 0.35μm Products

This databook provides basic technical information on the HDA/C10000 product line, including input and output DC characteristics, cell name conventions and Application Notes on Power and Ground rules and Clock Skew Management.

1.1 Product Description

HDA/C10000, based on a patented architecture, supports a triple layer metal HCMOS process. The high gate-density of this architecture results in lower on-chip noise, higher chip level performance, and lower component cost. HDA/C10000 is well-suited for cost-sensitive applications that also demand high circuit performance.

HDA/C10000 libraries support over 300 different combinations of I/O buffers, including Input Buffers with CMOS, TTL and Schmitt Trigger threshold voltages, and Output Buffers with varied slew-rate control for VSS/VDD bus noise management. Buffers that provide an interface between a 3.3V environment in the chip core and a 5.0V environment external to the the chip are also available.

1.2 CAE Support

HDA/C10000 supports popular design platforms and environments such as Verilog, Viewlogic, Mentor, and Synopsys for front-end logic design capture and simulation, and Cadence Cell3, Avant! Arc-CellXO, and SVR Sonic for back-end place-and-route. For higher simulation accuracy, HDA/C10000 uses the ADVER™ delay calculator. Signal interconnect delay is based on RC Tree analysis.

1.3 I/O (Input/Output) Buffers

There are more than 300 I/O buffers. Each I/O cell is implemented solely on the basic I/O cell architecture which forms the periphery of the masterslice. Test logic is provided to enable efficient parametric (threshold voltage) testing on input buffers, including CMOS and TTL level converters, Schmitt Trigger Input buffers, Clock drivers and Oscillator buffers. Pull-up and pull-down resistors are optional features. The I/O structure has been fully characterized for ESD protection and latch-up resistance.

Three basic types of single voltage output buffers, non-inverting, 3-state and open drain, are available in a range of driving capabilities from 1 mA to 24 mA. Slew-rate control buffers are provided for each output buffer type (except 1mA and 2mA buffers) to reduce power/ground bus noise and signal ringing, especially for simultaneous switching outputs.

Also available are two basic types of 5.0V Tolerant output buffers, 3-state and open-drain, in a range of driving capabilities from 1mA to 6mA.

Bidirectional buffers are combinations of input buffers and output 3-state buffers (or open drain buffers) in a single unit.

1.4 Special Pad Descriptions

VDD5 - 5V Power Cell

VDDO, VSSO - Output driver VDD/VSS cells

VDDI, VSSI - Core VDD/VSS cells

VDDP, VSSP - Input and pre-driver VDD/VSS cells

VDDOI, VSSOI - Core and output VDD/VSS cells

VDDOP, VSSOP - Output driver, input and pre-driver VDD/VSS cells

VDDPI. VSSPI - Input, pre-driver and core VDD/VSS cells

VDDOPI, VSSOPI - Output, input, pre-driver and core VDD/VSS cells

CORNER - Corner cell

IO_SPACER - Spacer cell

PADCON - PAD connect for 3V I/O

PWRCON - Pad connect for power cell

PADCON5V -Pad connect for 5V tolerant I/O

1.5 VDD and VSS Rules and Guidelines

There are three types of VDD and VSS in this product family, each with its related bus and pad cells.

1. Core Logic

   VSSI, VDDI

2. Input Buffers

   VSSP, VDDP

3. Output Buffers

   VSSO, VDDO

The number of VSS and VDD pads required for a specific design depends on the following factors:

Number of input and output buffers

Number of simultaneous switching inputs

Number of simultaneous switching outputs

Number of used gates and number of simultaneous switching gates

Operating frequency of the design

1.5.1 Output Buffer VDDO Bus and VSSO Guidelines

For SSO:

Notation: n = package inductance in nH

i = sum of sso current in mA that 1 VSSO/VDDO pad supports

I = Total sso current for the design

# of VSSO pad = I / i (Round up to the next highest integer)

For n <= 15nH i = -2.4n + 84

For n >= 15nH i = -1.2n + 66

ie n=12nH and Total SSO current for the design (I) is 250mA

i = -2.4(12) + 84

= 55.2ma

# of VSSO pad = 250mA / 55.2 mA

= 4.5

Round up to the next highest integer

VSSO for SSO in the design is 5

of VDDO pad is the same as # VSSO pad

For non SSO:

Notation: n = package inductance in nH

i = sum of sso current in mA that 1 VSSO/VDDO pad supports

I = Total sso current for the design

# of VSSO pad = I / i (Round up to the next highest integer)

For n <= 15nH i = -3.6n + 126

For n >= 15nH i = -1.8n + 99

ie n=12nH and Total SSO current for the design (I) is 350mA

i = -3.6(12) + 126

= 82.8ma

# of VSSO pad = 350mA / 82.8 mA

= 4.2

Round up to the next highest integer

VSSO for SSO in the design is 5

of VDDO pad is the same as # VSSO pad

1.5.2 Core Logic VSS Bus and VSSI Pad Allocation Guidelines

The purpose of these guidelines is to ensure that VDD/VSS bounce due to simultaneous gate switching is kept to a minimum. Voltage bounce on the power bus could have a negative impact on gate switching speed, and in an extreme case could even affect the functionality of the macrocells, e.g., flip-flops and latches. Because of variations in package inductance, the number of VDD/VSS pads required for a specific design is a function of the operating frequency of the chip, i.e., designs operating at high frequency should use more VDD/VSS pads.

- VDD Bus width and pad requirement is the same as VSS.
- VDD/VSS Bus and Pads should be distributed evenly in the core and on all sides of the chip.
- At least one (1) VSSI pad should be used on each side of the chip.
- The total number of VDDI pads required is the same as VSSI.

The number of VSSI pads required for a design can be calculated from the following expression:

Notation: G = Total number of used gates in thousands
S = % of simultaneous switch gates
F = Switching frequence in MHz

# of VSSI pad = I / i (Round up to the next highest integer)
# of VSSI PAD = G * S * F * 1.8e-5
ie G = 100K S = 30% F = 50MHz

# of VSSI PAD = 100 * 30 * 50 * 1.8e-5
= 2.7
Round up to the next highest integer
VSSI in the design is 3

of VDDI pad is the same as # VSSI pad

1.6 Propagation Delays

Interconnect wire-length, temperature and supply voltage are the chief factors affecting propagation delay.

1.6.1 Length Loading Estimation

Loading due to interconnect wire-length can be estimated with the following expression. The result is given in terms of number of equivalent standard loads.

$$C_{WL} = C_{fo} \times (0.049 \times \sqrt{A} + 0.48) + 0.079 \times \sqrt{A} + 0.33$$

where C_{fo} = number of fan-outs in standard load
A = area of block size in mm^2
C_{WL} = number of equivalent standard loads due to interconnect

e.g., C_{fo} = 7 (standard loads)
A = 25 mm^2
C_{WL} = 5.8 (standard load)

1.6.2 Temperature and Supply Voltage

Fig. 1.1 describes propagation delay correction factor (K_T) as a function of on-chip junction temperature (T_j), and voltage delay correction factor (K_V) as a function of supply voltage (V_{DD}). As a result of increasing CMOS power dissipation, ambient and junction temperature are generally not the same. The temperature of the die inside the package (junction temperature, T_j), is calculated using chip power dissipation and the Thermal Resistance to Ambient (θ_{ja}) temperature of the package. Information on package thermal performance can be obtained from ASPEC Application Engineers.

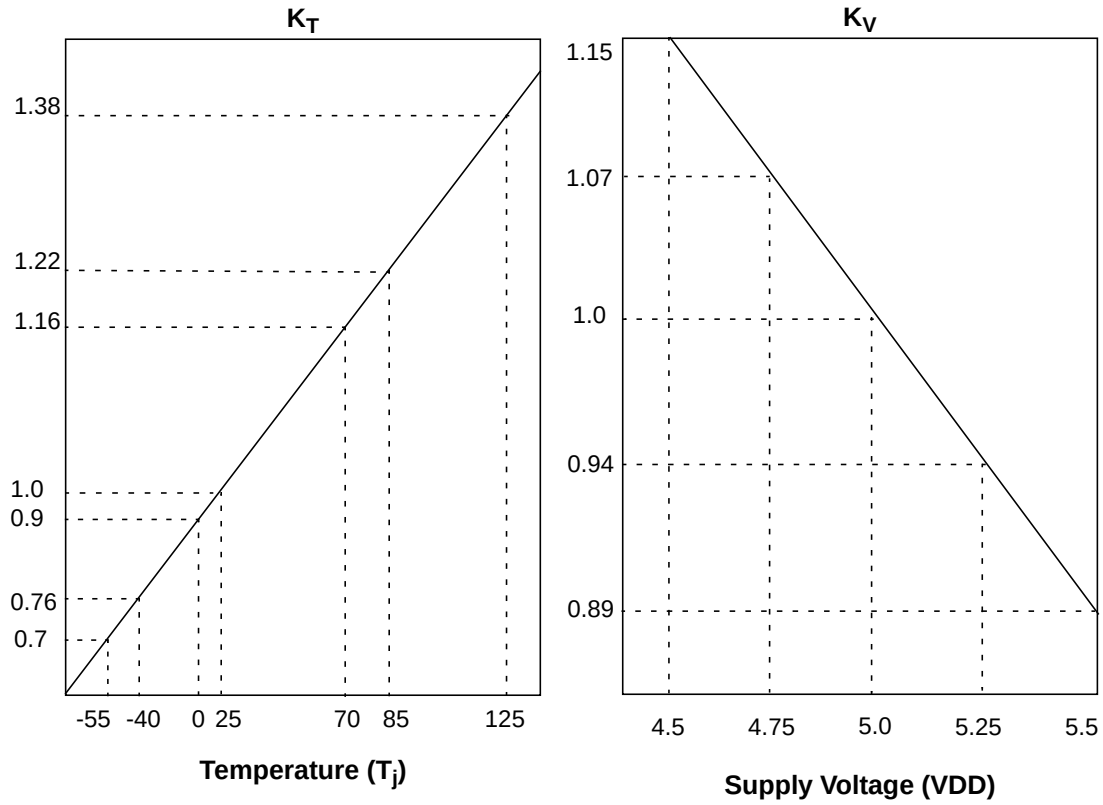


Figure 1.1: Effect of Temperature and Supply Voltage on Propagation Delay

1.6.3 Propagation Delay

A circuit should be designed to operate properly within a given specification level, either commercial, industrial or military. It is recommended that circuits be simulated for Best Case, Nominal Case and Worst Case conditions at each specification level. The following expressions also allow for the effect of process variation on circuit performance.

Worst Case:

$$_{WC} = K_{PWC} \times K_T \times K_V \times t_{nom} = K_{WC} \times t_{nom}$$

Best Case:

$$T_{BC} = K_{PBC} \times K_T \times K_V \times t_{nom} = K_{BC} \times t_{nom}$$

T_{WC} = Worst case propagation delay
T_{BC} = Best case propagation delay
t_{nom} = nominal propagation delay (T_j = 25^{o}C, V_{DD} =3.3V and typical process parameters)
K_{PWC} = Worst case process correction factor
K_{PBC} = Best case process correction factor

Chapter 2.0 DC Characteristics

2.1 VDD = 3.3V (range: 3.0V - 3.6V), junction temperature range -55 to +125^{o}C.

Table 2.1: DC CHARACTERISTICS AT VDD = 3.3v

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage					
	CMOS				$0.3V_{DD}$	V
	CMOS Schmitt Trigger				$0.3V_{DD}$	V
	TTL				0.8	V
	TTL Schmitt Trigger				0.8	V
V_{IH}	Input High Voltage					
	CMOS		$0.7V_{DD}$			V
	CMOS Schmitt Trigger		$0.7V_{DD}$			V
	TTL		2.0			V
	TTL Schmitt Trigger		2.0			V
I_{IH}	Input High Current	$V_{IN}=V_{DD}$	-10		10	µA
	Input with pull-down	$V_{IN}=V_{DD}$	4		100	µA
I_{IL}	Input Low Current	$V_{IN}=V_{SS}$	-10		10	µA
	Input with pull-up	$V_{IN}=V_{SS}$	-100		-4	µA
V_{OH}	Output High Voltage					
	Type B1	I_{OH}= -1mA	2.4			V
	Type B2	I_{OH}= -2mA	2.4			V
	Type B4	I_{OH}= -4mA	2.4			V
	Type B6	I_{OH}= -6mA	2.4			V
	Type B8	I_{OH}= -8mA	2.4			V
	Type B10	I_{OH}= -10mA	2.4			V
	Type B12	I_{OH}= -12mA	2.4			V
V_{OL}	Output Low Voltage					
	Type B1	I_{OH}= 1mA			0.4	V
	Type B2	I_{OH}= 2mA			0.4	V
	Type B4	I_{OH}= 4mA			0.4	V
	Type B6	I_{OH}= 6mA			0.4	V
	Type B8	I_{OH}= 8mA			0.4	V
	Type B10	I_{OH}= 10mA			0.4	V
	Type B12	I_{OH}= 12mA			0.4	V
I_{OZ}	3-State Output Leakage Current	$V_{OH}=V_{SS}$ or V_{DD}	-10		10	µA
I_{DD}	Quiescent Supply Current	$V_{IN}=V_{SS}$ or V_{DD}			80[1]	µA

1. Depends on customer design

2.4 Absolute Maximum Ratings

Table 2.2: Maximum Ratings

	Symbol	Parameter	Rating	Unit
Absolute Maximum Ratings	V_{DD}	DC Supply Voltage	-0.3 to 7.0	V
	V_{IN}	DC Input Voltage	-0.3 to VDD +0.3	V
	I_{IN}	DC Input Current	$\pm$ 10	mA
	T_{STG}	Storage Temperature	-40 to +125	^{o}C
Recommended Operating Conditions	V_{DD}	DC Supply Voltage	3.0 - 3.6V	V
	T_A	Commercial Temperature	0 to 70	^{o}C
	T_A	Industrial Temperature	-40 to 85	^{o}C
	T_A	Military Temperature	-55 to 125	^{o}C

Next Chapter

Chapter 3.0 I/O Buffers, Clock Drivers and Oscillators

3.1 Overview

This chapter describes the AC characteristics of Input and Output Buffers, Clock Drivers and Oscillators. The AC characteristics of Bidirectional Buffers can be derived from different combinations of Input and Output Buffers.

As there are over 300 possible combinations of I/O Buffers in the library, naming conventions have been adopted to help designers to memorize and use the cell library more efficiently. Naming conventions are described at the beginning of each sub-section.

3.2 Summary Tables

Table 3.1Input Buffers

Cell Name	Description	Page
PIC/PICU/PICD	CMOS Level Non-Inverting Input Buffers	3-8
PIS/PISU/PISD	CMOS Schmitt Trigger Level Non-Inverting Input Buffers	3-10

Table 3.2 Output Buffers

Cell Name	Description	Page
POB1/2/4/8/12/16/20/24 and POB(4/8/12/16/20/24)SM	Non-Inverting Output Buffers with no slew-rate control and medium slew-rate control.	3-14
POT1/2/4/8/12/16/20/24 and POT(4/8/12/16/20/24)SM	Tristate Non-Inverting Output Buffers with no slew-rate control and medium slew-rate control.	3-18
POD1/2/4/8/12/16/20/24 and POD(4/8/12/16/20/24)SM	Open Drain Output Buffers with no slew-rate control and medium slew-rate control.	3-26

Table 3.3 Bidirectional Buffers

Cell Name	Description	Page
PBCD (1/2/4/8/12/16/20/24)	CMOS Non-inverted, no pull, open drain	3-34
PBCD (4/8/12/16/20/24) SM	CMOS Non-inverted, no pull, open drain with medium slew-rate control	3-34
PBCUD (1/2/4/8/12/16/20/24)	CMOS Non-inverted, pull up, open drain	3-34
PBCUD (4/8/12/16/20/24) SM	CMOS Non-inverted, pull up, open drain with medium slew-rate control	3-34
PBCT (1/2/4/8/12/16/20/24)	CMOS Non-inverted, no pull, tri-state	3-33
PBCT (4/8/12/16/20/24) SM	CMOS Non-inverted, no pull, tri-state with medium slew-rate contro	3-33
PBCDT (1/2/4/8/12/16/20/24)	CMOS Non-inverted, pull down, tri-state	3-33
PBCDT (4/8/12/16/20/24) SM	CMOS Non-inverted, pull down, tri-state with medium slew-rate control	3-33
PBCUT (1/2/4/8/12/16/20/24)	CMOS Non-inverted, pull up, tri-state	3-33
PBCUT (4/8/12/16/20/24) SM	CMOS Non-inverted, pull up, tri-state with medium slew-rate control	3-33
PBSD (1/2/4/8/12/16/20/24)	CMOS Schmitt Trigger Non-inverted, no pull, open drain	3-34
PBSD (4/8/12/16/20/24) SM	CMOS Schmitt Trigger Non-inverted, no pull, open drain with medium slew-rate control	3-34
PBSUD (1/2/4/8/12/16/20/24)	CMOS Schmitt Trigger Non-inverted, pull up, open drain	3-34
PBSUD (4/8/12/16/20/24) SM	CMOS Schmitt Trigger Non-inverted, pull up, open drain with medium slew-rate control	3-34
PBST (1/2/4/8/12/16/20/24)	CMOS Schmitt Trigger Non-inverted, no pull, tri-state	3-33
PBST (4/8/12/16/20/24) SM	CMOS Schmitt Trigger Non-inverted, no pull, tri-state with medium slew-rate control	3-33
PBSDT (1/2/4/8/12/16/20/24)	CMOS Schmitt Trigger Non-inverted, pull down, tri-state	3-33
PBSDT (4/8/12/16/20/24) SM	CMOS Schmitt Trigger Non-inverted, pull down, tri-state with medium slew-rate control	3-33
PBSUT (1/2/4/8/12/16/20/24)	CMOS Schmitt Trigger Non-inverted, pull up, tri-state	3-33
PBSUT (4/8/12/16/20/24) SM	CMOS Schmitt Trigger Non-inverted, pull up, tri-state with medium slew-rate control	3-33

Table 3.4: Input Clock Drivers

Cell Name	Description	Page
CK2/4/6/8/12/16/20	Internal Clock Driver CMOS Level	3-36
PSCKDC2/4/6/8/12 PSCKDCD2/4/6/8/12 PSCKDCU2/4/6/8/12	CMOS Level Clock Drivers with no Pull, Pull-Up and Pull-Down	3-40
PSCKDS2/4/6/8/12 PSCKDSD2/4/6/8/12 PSCKDSU2/4/6/8/12	CMOS Schmitt Trigger Level Clock Drivers with no Pull, Pull-Up and Pull-Down	3-44

Table 3.5:Oscillators

Cell Name	Description	Page
PSOSCA	Oscillator Buffer	3-48
PSOSCB	Oscillator Buffer	3-50

Next Chapter

3.3 Input Buffers

Input Buffer Naming Conventions:

PI x z

where x = C -- CMOS levels
S -- CMOS Schmitt Trigger levels

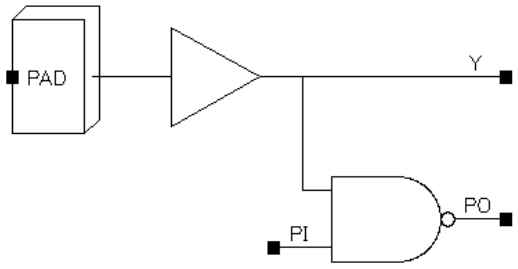
z = (optional)
U -- pull-up resistor
D -- pull-down resistor

e.g. PISD - CMOS Schmitt Trigger input buffer with pull-down

Input: PAD, PI
Output Y, PO

Input Loading (SL):
PI: 3.3556

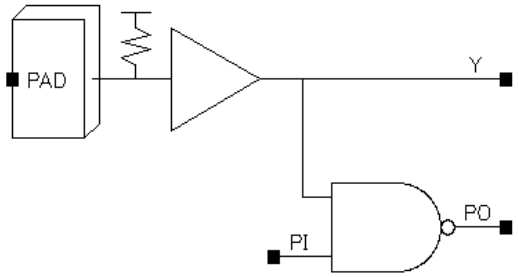
I/O Slots: 1



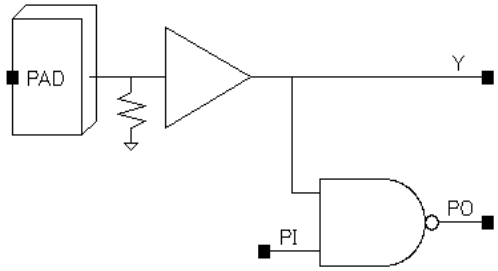
PIC Symbol

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Truth Table



PICU Symbol



PICD Symbol

PIC Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.13	0.09 + 0.018*SL	0.11 + 0.011*SL	0.18 + 0.008*SL
	tPHL	0.14	0.10 + 0.018*SL	0.12 + 0.013*SL	0.17 + 0.010*SL
	tR	0.30	0.26 + 0.018*SL	0.28 + 0.014*SL	0.28 + 0.013*SL
	tF	0.29	0.23 + 0.027*SL	0.26 + 0.018*SL	0.25 + 0.018*SL
PI to PO	tPLH	0.17	0.14 + 0.012*SL	0.15 + 0.010*SL	0.20 + 0.008*SL
	tPHL	0.10	0.07 + 0.017*SL	0.08 + 0.012*SL	0.12 + 0.010*SL
	tR	0.33	0.31 + 0.009*SL	0.30 + 0.013*SL	0.30 + 0.013*SL
	tF	0.29	0.26 + 0.018*SL	0.26 + 0.017*SL	0.22 + 0.019*SL
PAD to Y	tPLH	0.20	0.19 + 0.004*SL	0.20 + 0.003*SL	0.21 + 0.002*SL
	tPHL	0.34	0.32 + 0.008*SL	0.32 + 0.007*SL	0.33 + 0.007*SL
	tR	0.11	0.09 + 0.006*SL	0.10 + 0.005*SL	0.09 + 0.005*SL
	tF	0.14	0.12 + 0.012*SL	0.12 + 0.012*SL	0.12 + 0.012*SL

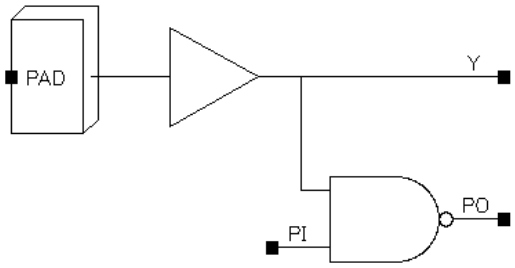
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Note: The timing tables for PICU and PICD are the same as for PIC.

Input: PAD, PI
Output Y, PO

Input Loading (SL):
PI: 3.3556

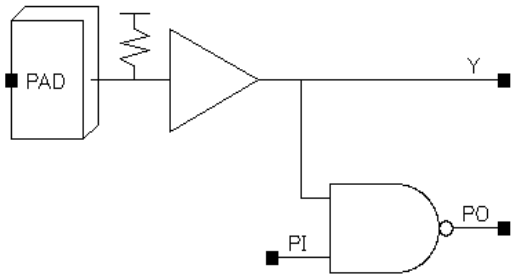
I/O Slots: 1



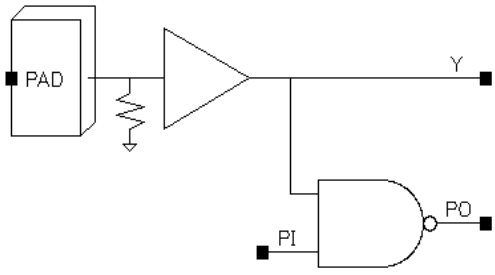
PIS Symbol

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Truth Table



PISU Symbol



PISD Symbol

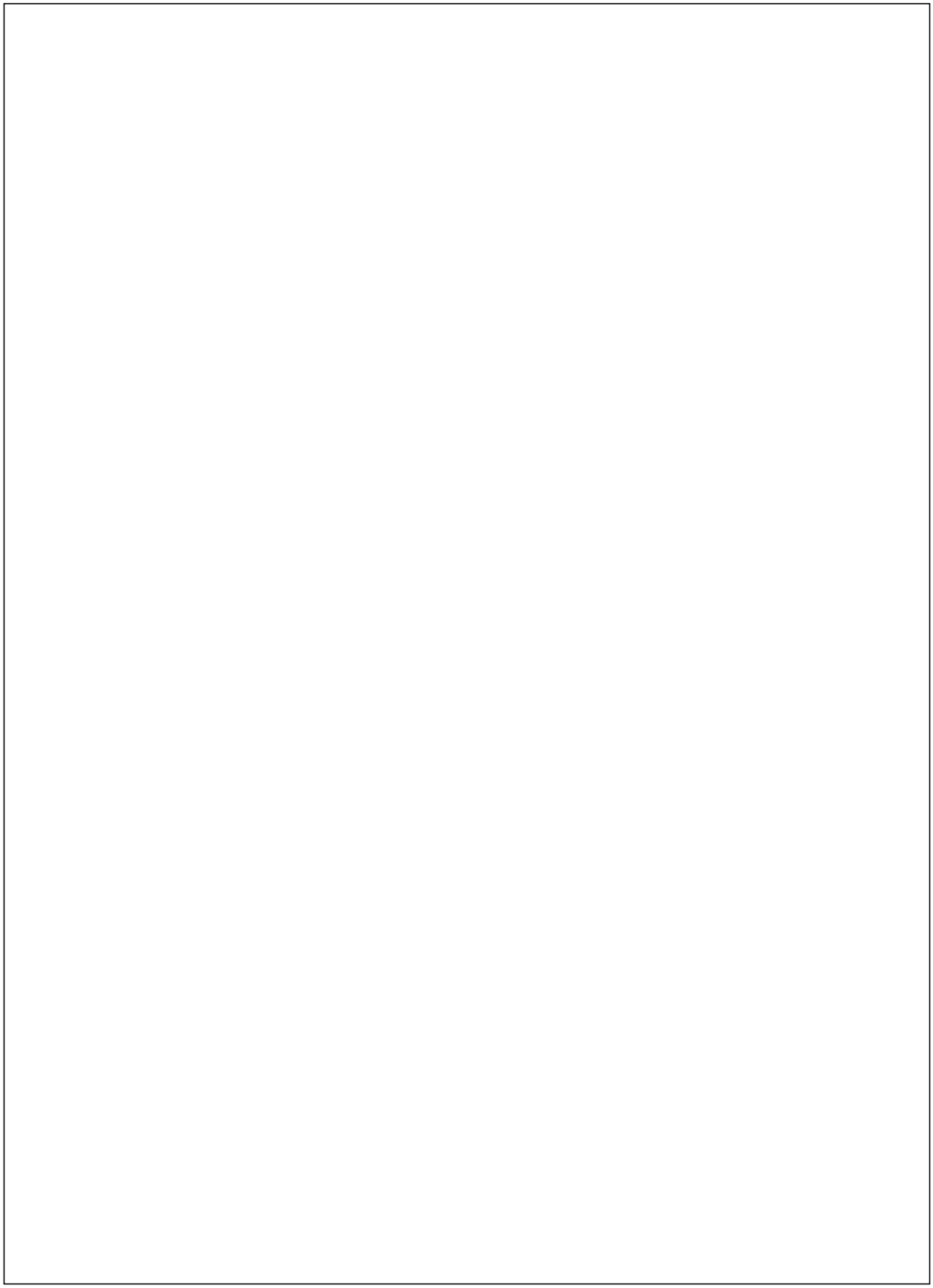
PIS Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.13	0.09 + 0.018*SL	0.11 + 0.011*SL	0.18 + 0.008*SL
	tPHL	0.14	0.10 + 0.018*SL	0.12 + 0.013*SL	0.17 + 0.010*SL
	tR	0.30	0.26 + 0.018*SL	0.28 + 0.014*SL	0.28 + 0.013*SL
	tF	0.29	0.23 + 0.027*SL	0.26 + 0.018*SL	0.25 + 0.018*SL
PI to PO	tPLH	0.17	0.14 + 0.012*SL	0.15 + 0.010*SL	0.20 + 0.008*SL
	tPHL	0.10	0.07 + 0.017*SL	0.08 + 0.012*SL	0.12 + 0.010*SL
	tR	0.33	0.31 + 0.009*SL	0.30 + 0.013*SL	0.30 + 0.013*SL
	tF	0.29	0.26 + 0.018*SL	0.26 + 0.017*SL	0.22 + 0.019*SL
PAD to Y	tPLH	0.46	0.45 + 0.003*SL	0.45 + 0.002*SL	0.46 + 0.002*SL
	tPHL	0.75	0.74 + 0.004*SL	0.74 + 0.004*SL	0.75 + 0.004*SL
	tR	0.14	0.14 + 0.002*SL	0.13 + 0.003*SL	0.14 + 0.003*SL
	tF	0.16	0.15 + 0.006*SL	0.14 + 0.007*SL	0.16 + 0.006*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Note: The timing tables for PISU and PISD are the same as for PIS.



3.4 Output Buffers

Output Buffer Naming Conventions:

PO u v w

where u = B -- Normal non-inverting buffer
T -- Tristate non-inverting buffer
D -- Open-drain output

v = 1 -- 1mA drive
2 -- 2mA drive
4 -- 4mA drive
8 -- 8mA drive
12 -- 12mA drive
16 -- 16mA drive
20 -- 20mA drive
24 -- 24mA drive

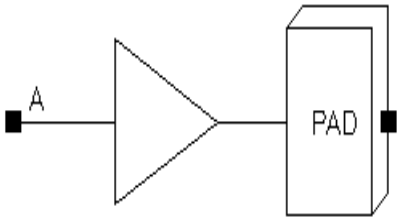
w = (optional)
none -- no slew-rate control
SM -- medium slew-rate control

e.g., POT12SM - 3-state output buffer with 12mA drive and medium slew-rate control

Input: A
Output: PAD

Input Loading (SL): A:
- POB1/2/20/24: 13.5556
- POB4/8/12: 9.0000
- POB16: 11.2778
- POB(12/16/20/24)SM:27.0000

I/O Slots: 1



Symbol

A	PAD
0	0
1	1

Truth Table

POB1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	13.25	2.27 + 0.220*CL	2.31 + 0.219*CL	2.35 + 0.218*CL
	tPHL	8.44	1.41 + 0.141*CL	1.50 + 0.139*CL	1.59 + 0.138*CL
	tR	30.64	5.15 + 0.510*CL	5.04 + 0.512*CL	4.93 + 0.513*CL
	tF	19.22	4.92 + 0.286*CL	4.29 + 0.299*CL	4.48 + 0.296*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	9.13	1.64 + 0.150*CL	1.65 + 0.150*CL	1.68 + 0.149*CL
	tPHL	8.45	1.42 + 0.141*CL	1.51 + 0.139*CL	1.60 + 0.138*CL
	tR	20.98	3.54 + 0.349*CL	3.53 + 0.349*CL	3.47 + 0.350*CL
	tF	19.21	4.90 + 0.286*CL	4.29 + 0.299*CL	4.48 + 0.296*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	5.51	1.07 + 0.089*CL	1.07 + 0.089*CL	1.08 + 0.089*CL
	tPHL	4.51	0.87 + 0.073*CL	0.94 + 0.071*CL	1.02 + 0.070*CL
	tR	12.52	2.13 + 0.208*CL	2.12 + 0.208*CL	2.13 + 0.208*CL
	tF	10.52	4.08 + 0.129*CL	3.41 + 0.142*CL	2.91 + 0.149*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB4SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	5.61	1.18 + 0.089*CL	1.18 + 0.089*CL	1.18 + 0.089*CL
	tPHL	4.54	0.90 + 0.073*CL	0.97 + 0.071*CL	1.05 + 0.070*CL
	tR	12.52	2.13 + 0.208*CL	2.12 + 0.208*CL	2.13 + 0.208*CL
	tF	10.53	4.08 + 0.129*CL	3.41 + 0.142*CL	2.91 + 0.149*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.29	0.87 + 0.048*CL	0.86 + 0.049*CL	0.86 + 0.049*CL
	tPHL	2.25	0.63 + 0.032*CL	0.68 + 0.031*CL	0.74 + 0.031*CL
	tR	6.95	1.22 + 0.115*CL	1.20 + 0.115*CL	1.20 + 0.115*CL
	tF	4.91	1.79 + 0.063*CL	1.87 + 0.061*CL	1.96 + 0.060*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB8SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.60	1.15 + 0.049*CL	1.16 + 0.049*CL	1.16 + 0.049*CL
	tPHL	2.48	0.85 + 0.033*CL	0.91 + 0.031*CL	0.98 + 0.031*CL
	tR	7.00	1.31 + 0.114*CL	1.27 + 0.115*CL	1.24 + 0.115*CL
	tF	4.95	1.85 + 0.062*CL	1.93 + 0.060*CL	2.00 + 0.059*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	t_{PLH}	2.39	0.86 + 0.031*CL	0.85 + 0.031*CL	0.84 + 0.031*CL
	t_{PHL}	1.92	0.68 + 0.025*CL	0.73 + 0.024*CL	0.79 + 0.023*CL
	t_R	4.48	0.85 + 0.072*CL	0.82 + 0.073*CL	0.80 + 0.073*CL
	t_F	3.63	1.10 + 0.050*CL	1.25 + 0.047*CL	1.40 + 0.046*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB12SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	t_{PLH}	2.65	1.06 + 0.032*CL	1.07 + 0.032*CL	1.08 + 0.032*CL
	t_{PHL}	2.09	0.80 + 0.026*CL	0.88 + 0.024*CL	0.96 + 0.023*CL
	t_R	4.61	1.00 + 0.072*CL	0.96 + 0.073*CL	0.92 + 0.074*CL
	t_F	3.68	1.17 + 0.050*CL	1.33 + 0.047*CL	1.47 + 0.045*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB16 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	t_{PLH}	2.08	0.96 + 0.022*CL	0.95 + 0.023*CL	0.94 + 0.023*CL
	t_{PHL}	1.75	0.66 + 0.022*CL	0.72 + 0.021*CL	0.81 + 0.019*CL
	t_R	3.36	0.73 + 0.053*CL	0.69 + 0.054*CL	0.65 + 0.054*CL
	t_F	2.91	0.77 + 0.043*CL	0.93 + 0.040*CL	1.11 + 0.037*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB16SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	t_{PLH}	2.24	1.04 + 0.024*CL	1.07 + 0.023*CL	1.09 + 0.023*CL
	t_{PHL}	1.87	0.75 + 0.023*CL	0.83 + 0.021*CL	0.94 + 0.020*CL
	t_R	3.51	0.88 + 0.052*CL	0.87 + 0.053*CL	0.83 + 0.053*CL
	t_F	2.99	0.93 + 0.041*CL	1.05 + 0.039*CL	1.20 + 0.037*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB20 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.02	1.14 + 0.018*CL	1.11 + 0.018*CL	1.09 + 0.018*CL
	tPHL	1.66	0.70 + 0.019*CL	0.77 + 0.018*CL	0.86 + 0.017*CL
	tR	2.86	0.76 + 0.042*CL	0.71 + 0.043*CL	0.65 + 0.044*CL
	tF	2.37	0.62 + 0.035*CL	0.77 + 0.032*CL	0.92 + 0.030*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB20SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.06	1.06 + 0.020*CL	1.09 + 0.019*CL	1.11 + 0.019*CL
	tPHL	1.77	0.78 + 0.020*CL	0.87 + 0.018*CL	0.97 + 0.017*CL
	tR	2.99	0.82 + 0.043*CL	0.81 + 0.043*CL	0.79 + 0.044*CL
	tF	2.48	0.85 + 0.033*CL	0.95 + 0.031*CL	1.05 + 0.029*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB24 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	1.97	1.27 + 0.014*CL	1.24 + 0.015*CL	1.22 + 0.015*CL
	tPHL	1.70	0.76 + 0.019*CL	0.86 + 0.017*CL	0.96 + 0.016*CL
	tR	2.46	0.78 + 0.033*CL	0.72 + 0.035*CL	0.67 + 0.035*CL
	tF	2.19	0.61 + 0.031*CL	0.77 + 0.028*CL	0.92 + 0.026*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB24SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

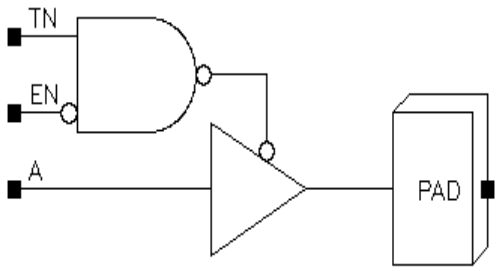
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	1.95	1.08 + 0.017*CL	1.13 + 0.016*CL	1.16 + 0.016*CL
	tPHL	1.77	0.79 + 0.020*CL	0.91 + 0.017*CL	1.02 + 0.016*CL
	tR	2.58	0.80 + 0.036*CL	0.80 + 0.036*CL	0.79 + 0.036*CL
	tF	2.30	0.82 + 0.030*CL	0.94 + 0.027*CL	1.06 + 0.026*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

Input: TN, EN, A
Output: PAD

Input Loading (SL):
- TN: All : 3.3556
- EN: All : 3.3556
- A: All : 5.6111

I/O Slots: 1



Symbol

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

Truth Table

POT1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	13.49	2.51 + 0.220*CL	2.55 + 0.219*CL	2.59 + 0.218*CL
	tPHL	8.69	1.66 + 0.141*CL	1.75 + 0.139*CL	1.84 + 0.138*CL
	tR	30.64	5.15 + 0.510*CL	5.04 + 0.512*CL	4.94 + 0.513*CL
	tF	19.21	4.92 + 0.286*CL	4.29 + 0.299*CL	4.49 + 0.296*CL
EN to PAD	tPLH	13.39	2.77 + 0.212*CL	4.60 + 0.176*CL	9.84 + 0.110*CL
	tPHL	8.85	1.82 + 0.141*CL	1.91 + 0.139*CL	2.00 + 0.138*CL
	tR	30.63	5.15 + 0.510*CL	5.07 + 0.511*CL	5.02 + 0.512*CL
	tF	19.22	4.93 + 0.286*CL	4.29 + 0.299*CL	4.49 + 0.296*CL
	tPLZ	0.58	0.58 + -0.000*CL	0.58 + -0.000*CL	0.57 + 0.000*CL
	tPHZ	0.49	0.49 + -0.000*CL	0.49 + -0.000*CL	0.49 + -0.000*CL
TN to PAD	tPLH	13.28	2.66 + 0.212*CL	4.45 + 0.177*CL	9.65 + 0.112*CL
	tPHL	8.74	1.70 + 0.141*CL	1.79 + 0.139*CL	1.88 + 0.138*CL
	tR	30.63	5.15 + 0.510*CL	5.07 + 0.511*CL	5.02 + 0.512*CL
	tF	19.22	4.93 + 0.286*CL	4.29 + 0.299*CL	4.48 + 0.296*CL
	tPLZ	0.64	0.64 + -0.000*CL	0.65 + -0.000*CL	0.64 + -0.000*CL
	tPHZ	0.57	0.57 + -0.000*CL	0.57 + -0.000*CL	0.57 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	9.38	1.88 + 0.150*CL	1.90 + 0.149*CL	1.92 + 0.149*CL
	tPHL	8.70	1.66 + 0.141*CL	1.75 + 0.139*CL	1.84 + 0.138*CL
	tR	20.98	3.54 + 0.349*CL	3.53 + 0.349*CL	3.47 + 0.350*CL
	tF	19.21	4.90 + 0.286*CL	4.29 + 0.299*CL	4.48 + 0.296*CL
EN to PAD	tPLH	9.34	2.09 + 0.145*CL	3.32 + 0.120*CL	6.90 + 0.075*CL
	tPHL	8.85	1.82 + 0.141*CL	1.91 + 0.139*CL	1.99 + 0.138*CL
	tR	20.98	3.55 + 0.349*CL	3.55 + 0.348*CL	3.53 + 0.349*CL
	tF	19.21	4.90 + 0.286*CL	4.29 + 0.299*CL	4.48 + 0.296*CL
	tPLZ	0.58	0.58 + -0.000*CL	0.58 + -0.000*CL	0.57 + 0.000*CL
	tPHZ	0.51	0.51 + -0.000*CL	0.51 + -0.000*CL	0.51 + -0.000*CL
TN to PAD	tPLH	9.23	1.98 + 0.145*CL	3.19 + 0.121*CL	6.74 + 0.076*CL
	tPHL	8.74	1.70 + 0.141*CL	1.79 + 0.139*CL	1.88 + 0.138*CL
	tR	20.98	3.55 + 0.349*CL	3.55 + 0.348*CL	3.54 + 0.349*CL
	tF	19.21	4.90 + 0.286*CL	4.29 + 0.299*CL	4.49 + 0.296*CL
	tPLZ	0.64	0.64 + -0.000*CL	0.65 + -0.000*CL	0.64 + -0.000*CL
	tPHZ	0.59	0.59 + -0.000*CL	0.59 + -0.000*CL	0.59 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	5.75	1.31 + 0.089*CL	1.31 + 0.089*CL	1.32 + 0.089*CL
	tPHL	4.74	1.10 + 0.073*CL	1.17 + 0.071*CL	1.25 + 0.070*CL
	tR	12.52	2.13 + 0.208*CL	2.12 + 0.208*CL	2.13 + 0.208*CL
	tF	10.53	4.08 + 0.129*CL	3.41 + 0.142*CL	2.91 + 0.148*CL
EN to PAD	tPLH	5.82	1.39 + 0.089*CL	1.41 + 0.088*CL	1.55 + 0.086*CL
	tPHL	4.89	1.25 + 0.073*CL	1.33 + 0.071*CL	1.40 + 0.070*CL
	tR	12.52	2.13 + 0.208*CL	2.12 + 0.208*CL	2.13 + 0.208*CL
	tF	10.53	4.08 + 0.129*CL	3.42 + 0.142*CL	2.91 + 0.149*CL
	tPLZ	0.69	0.69 + 0.000*CL	0.69 + -0.000*CL	0.69 + -0.000*CL
	tPHZ	0.69	0.70 + -0.000*CL	0.69 + -0.000*CL	0.69 + -0.000*CL
TN to PAD	tPLH	5.71	1.28 + 0.089*CL	1.30 + 0.088*CL	1.44 + 0.086*CL
	tPHL	4.78	1.14 + 0.073*CL	1.21 + 0.071*CL	1.29 + 0.070*CL
	tR	12.52	2.13 + 0.208*CL	2.12 + 0.208*CL	2.13 + 0.208*CL
	tF	10.53	4.08 + 0.129*CL	3.41 + 0.142*CL	2.92 + 0.148*CL
	tPLZ	0.75	0.75 + -0.000*CL	0.75 + -0.000*CL	0.75 + -0.000*CL
	tPHZ	0.77	0.77 + -0.000*CL	0.77 + -0.000*CL	0.78 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT4SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	t_{PLH}	5.88	1.44 + 0.089*CL	1.44 + 0.089*CL	1.45 + 0.089*CL
	t_{PHL}	4.84	1.20 + 0.073*CL	1.28 + 0.071*CL	1.35 + 0.070*CL
	t_R	12.52	2.13 + 0.208*CL	2.12 + 0.208*CL	2.14 + 0.208*CL
	t_F	10.53	4.08 + 0.129*CL	3.41 + 0.142*CL	2.91 + 0.149*CL
EN to PAD	t_{PLH}	5.96	1.53 + 0.089*CL	1.55 + 0.088*CL	1.70 + 0.086*CL
	t_{PHL}	5.00	1.36 + 0.073*CL	1.43 + 0.071*CL	1.51 + 0.070*CL
	t_R	12.52	2.13 + 0.208*CL	2.13 + 0.208*CL	2.13 + 0.208*CL
	t_F	10.53	4.09 + 0.129*CL	3.42 + 0.142*CL	2.91 + 0.149*CL
	t_{PLZ}	0.69	0.69 + 0.000*CL	0.70 + -0.000*CL	0.68 + -0.000*CL
	t_{PHZ}	0.56	0.56 + -0.000*CL	0.56 + -0.000*CL	0.56 + -0.000*CL
TN to PAD	t_{PLH}	5.85	1.42 + 0.089*CL	1.44 + 0.088*CL	1.58 + 0.086*CL
	t_{PHL}	4.88	1.24 + 0.073*CL	1.31 + 0.071*CL	1.39 + 0.070*CL
	t_R	12.52	2.13 + 0.208*CL	2.13 + 0.208*CL	2.13 + 0.208*CL
	t_F	10.53	4.09 + 0.129*CL	3.41 + 0.142*CL	2.92 + 0.148*CL
	t_{PLZ}	0.74	0.74 + 0.000*CL	0.74 + -0.000*CL	0.74 + -0.000*CL
	t_{PHZ}	0.64	0.64 + -0.000*CL	0.64 + -0.000*CL	0.64 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	t_{PLH}	3.51	1.08 + 0.049*CL	1.08 + 0.049*CL	1.08 + 0.049*CL
	t_{PHL}	2.45	0.84 + 0.032*CL	0.89 + 0.031*CL	0.95 + 0.031*CL
	t_R	6.95	1.22 + 0.115*CL	1.20 + 0.115*CL	1.20 + 0.115*CL
	t_F	4.92	1.79 + 0.063*CL	1.88 + 0.061*CL	1.96 + 0.060*CL
EN to PAD	t_{PLH}	3.58	1.13 + 0.049*CL	1.13 + 0.049*CL	1.14 + 0.049*CL
	t_{PHL}	2.60	0.98 + 0.032*CL	1.04 + 0.031*CL	1.10 + 0.031*CL
	t_R	6.95	1.22 + 0.115*CL	1.21 + 0.115*CL	1.20 + 0.115*CL
	t_F	4.92	1.79 + 0.063*CL	1.88 + 0.061*CL	1.96 + 0.060*CL
	t_{PLZ}	1.00	1.00 + 0.000*CL	1.00 + 0.000*CL	1.00 + -0.000*CL
	t_{PHZ}	0.90	0.90 + -0.000*CL	0.90 + -0.000*CL	0.90 + -0.000*CL
TN to PAD	t_{PLH}	3.46	1.01 + 0.049*CL	1.02 + 0.049*CL	1.02 + 0.049*CL
	t_{PHL}	2.49	0.86 + 0.032*CL	0.92 + 0.031*CL	0.98 + 0.031*CL
	t_R	6.95	1.22 + 0.115*CL	1.21 + 0.115*CL	1.20 + 0.115*CL
	t_F	4.92	1.79 + 0.063*CL	1.88 + 0.061*CL	1.97 + 0.060*CL
	t_{PLZ}	1.06	1.06 + -0.000*CL	1.06 + -0.000*CL	1.06 + -0.000*CL
	t_{PHZ}	0.97	0.97 + -0.000*CL	0.97 + -0.000*CL	0.97 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT8SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.87	1.42 + 0.049*CL	1.42 + 0.049*CL	1.43 + 0.049*CL
	tPHL	2.72	1.09 + 0.033*CL	1.15 + 0.031*CL	1.22 + 0.031*CL
	tR	7.00	1.31 + 0.114*CL	1.27 + 0.115*CL	1.24 + 0.115*CL
	tF	4.95	1.84 + 0.062*CL	1.93 + 0.060*CL	2.00 + 0.060*CL
EN to PAD	tPLH	3.95	1.50 + 0.049*CL	1.51 + 0.049*CL	1.51 + 0.049*CL
	tPHL	2.88	1.25 + 0.033*CL	1.31 + 0.031*CL	1.37 + 0.031*CL
	tR	7.00	1.31 + 0.114*CL	1.27 + 0.115*CL	1.24 + 0.115*CL
	tF	4.95	1.85 + 0.062*CL	1.93 + 0.060*CL	2.00 + 0.060*CL
	tPLZ	0.63	0.63 + 0.000*CL	0.63 + -0.000*CL	0.63 + -0.000*CL
	tPHZ	0.53	0.53 + -0.000*CL	0.53 + -0.000*CL	0.53 + -0.000*CL
TN to PAD	tPLH	3.84	1.39 + 0.049*CL	1.40 + 0.049*CL	1.40 + 0.049*CL
	tPHL	2.76	1.13 + 0.033*CL	1.19 + 0.031*CL	1.26 + 0.031*CL
	tR	7.00	1.31 + 0.114*CL	1.27 + 0.115*CL	1.24 + 0.115*CL
	tF	4.95	1.85 + 0.062*CL	1.93 + 0.060*CL	2.00 + 0.059*CL
	tPLZ	0.70	0.70 + -0.000*CL	0.70 + -0.000*CL	0.70 + -0.000*CL
	tPHZ	0.61	0.58 + 0.001*CL	0.61 + -0.000*CL	0.61 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.60	1.07 + 0.031*CL	1.06 + 0.031*CL	1.05 + 0.031*CL
	tPHL	2.11	0.87 + 0.025*CL	0.92 + 0.024*CL	0.98 + 0.023*CL
	tR	4.48	0.84 + 0.073*CL	0.82 + 0.073*CL	0.80 + 0.073*CL
	tF	3.63	1.10 + 0.051*CL	1.26 + 0.047*CL	1.40 + 0.046*CL
EN to PAD	tPLH	2.65	1.08 + 0.031*CL	1.09 + 0.031*CL	1.09 + 0.031*CL
	tPHL	2.25	0.98 + 0.025*CL	1.05 + 0.024*CL	1.12 + 0.023*CL
	tR	4.48	0.83 + 0.073*CL	0.82 + 0.073*CL	0.80 + 0.073*CL
	tF	3.63	1.07 + 0.051*CL	1.25 + 0.048*CL	1.41 + 0.046*CL
	tPLZ	1.20	1.20 + -0.000*CL	1.20 + -0.000*CL	1.20 + -0.000*CL
	tPHZ	1.14	1.14 + -0.000*CL	1.14 + -0.000*CL	1.14 + -0.000*CL
TN to PAD	tPLH	2.53	0.97 + 0.031*CL	0.97 + 0.031*CL	0.98 + 0.031*CL
	tPHL	2.13	0.86 + 0.025*CL	0.93 + 0.024*CL	1.00 + 0.023*CL
	tR	4.48	0.83 + 0.073*CL	0.82 + 0.073*CL	0.80 + 0.073*CL
	tF	3.63	1.07 + 0.051*CL	1.25 + 0.048*CL	1.41 + 0.046*CL
	tPLZ	1.27	1.27 + -0.000*CL	1.27 + 0.000*CL	1.27 + -0.000*CL
	tPHZ	1.22	1.22 + -0.000*CL	1.22 + -0.000*CL	1.22 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT12SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.92	1.33 + 0.032*CL	1.34 + 0.032*CL	1.35 + 0.032*CL
	tPHL	2.33	1.05 + 0.026*CL	1.12 + 0.024*CL	1.20 + 0.023*CL
	tR	4.61	1.00 + 0.072*CL	0.96 + 0.073*CL	0.92 + 0.074*CL
	tF	3.67	1.16 + 0.050*CL	1.32 + 0.047*CL	1.46 + 0.045*CL
EN to PAD	tPLH	3.00	1.40 + 0.032*CL	1.42 + 0.032*CL	1.43 + 0.032*CL
	tPHL	2.49	1.20 + 0.026*CL	1.28 + 0.024*CL	1.36 + 0.023*CL
	tR	4.61	1.00 + 0.072*CL	0.96 + 0.073*CL	0.92 + 0.074*CL
	tF	3.68	1.17 + 0.050*CL	1.33 + 0.047*CL	1.47 + 0.045*CL
	tPLZ	0.74	0.74 + 0.000*CL	0.74 + -0.000*CL	0.74 + 0.000*CL
	tPHZ	0.58	0.58 + 0.000*CL	0.58 + 0.000*CL	0.58 + 0.000*CL
TN to PAD	tPLH	2.89	1.29 + 0.032*CL	1.31 + 0.032*CL	1.32 + 0.032*CL
	tPHL	2.37	1.08 + 0.026*CL	1.16 + 0.024*CL	1.24 + 0.023*CL
	tR	4.61	1.00 + 0.072*CL	0.96 + 0.073*CL	0.92 + 0.074*CL
	tF	3.68	1.18 + 0.050*CL	1.33 + 0.047*CL	1.47 + 0.045*CL
	tPLZ	0.81	0.81 + 0.000*CL	0.81 + 0.000*CL	0.81 + -0.000*CL
	tPHZ	0.64	0.64 + -0.000*CL	0.64 + -0.000*CL	0.64 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT16 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.29	1.17 + 0.022*CL	1.16 + 0.023*CL	1.15 + 0.023*CL
	tPHL	1.95	0.86 + 0.022*CL	0.92 + 0.021*CL	1.01 + 0.019*CL
	tR	3.36	0.71 + 0.053*CL	0.68 + 0.054*CL	0.65 + 0.054*CL
	tF	2.92	0.77 + 0.043*CL	0.93 + 0.040*CL	1.11 + 0.037*CL
EN to PAD	tPLH	2.32	1.16 + 0.023*CL	1.17 + 0.023*CL	1.17 + 0.023*CL
	tPHL	2.09	0.99 + 0.022*CL	1.05 + 0.021*CL	1.15 + 0.020*CL
	tR	3.36	0.68 + 0.054*CL	0.67 + 0.054*CL	0.65 + 0.054*CL
	tF	2.92	0.77 + 0.043*CL	0.94 + 0.040*CL	1.12 + 0.037*CL
	tPLZ	1.41	1.41 + -0.000*CL	1.42 + -0.000*CL	1.41 + -0.000*CL
	tPHZ	0.93	0.93 + -0.000*CL	0.93 + -0.000*CL	0.93 + -0.000*CL
TN to PAD	tPLH	2.21	1.04 + 0.023*CL	1.05 + 0.023*CL	1.06 + 0.023*CL
	tPHL	1.98	0.87 + 0.022*CL	0.94 + 0.021*CL	1.03 + 0.020*CL
	tR	3.36	0.69 + 0.053*CL	0.67 + 0.054*CL	0.65 + 0.054*CL
	tF	2.92	0.77 + 0.043*CL	0.94 + 0.040*CL	1.12 + 0.037*CL
	tPLZ	1.47	1.47 + -0.000*CL	1.47 + -0.000*CL	1.47 + -0.000*CL
	tPHZ	1.01	1.01 + -0.000*CL	1.01 + -0.000*CL	1.01 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT16SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.50	1.30 + 0.024*CL	1.33 + 0.023*CL	1.35 + 0.023*CL
	tPHL	2.16	1.04 + 0.022*CL	1.12 + 0.021*CL	1.23 + 0.020*CL
	tR	3.51	0.88 + 0.053*CL	0.87 + 0.053*CL	0.83 + 0.053*CL
	tF	2.98	0.89 + 0.042*CL	1.03 + 0.039*CL	1.19 + 0.037*CL
EN to PAD	tPLH	2.57	1.36 + 0.024*CL	1.40 + 0.023*CL	1.42 + 0.023*CL
	tPHL	2.31	1.18 + 0.023*CL	1.27 + 0.021*CL	1.38 + 0.020*CL
	tR	3.51	0.91 + 0.052*CL	0.88 + 0.053*CL	0.84 + 0.053*CL
	tF	3.00	0.93 + 0.041*CL	1.05 + 0.039*CL	1.21 + 0.037*CL
	tPLZ	0.89	0.91 + -0.000*CL	0.87 + 0.000*CL	0.90 + 0.000*CL
	tPHZ	0.64	0.64 + -0.000*CL	0.64 + -0.000*CL	0.64 + -0.000*CL
TN to PAD	tPLH	2.46	1.24 + 0.024*CL	1.28 + 0.023*CL	1.30 + 0.023*CL
	tPHL	2.20	1.07 + 0.023*CL	1.15 + 0.021*CL	1.26 + 0.020*CL
	tR	3.51	0.90 + 0.052*CL	0.88 + 0.053*CL	0.84 + 0.053*CL
	tF	3.00	0.93 + 0.041*CL	1.05 + 0.039*CL	1.21 + 0.037*CL
	tPLZ	0.96	0.96 + -0.000*CL	0.96 + 0.000*CL	0.96 + 0.000*CL
	tPHZ	0.71	0.71 + -0.000*CL	0.71 + -0.000*CL	0.71 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT20 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.24	1.35 + 0.018*CL	1.32 + 0.018*CL	1.30 + 0.019*CL
	tPHL	1.85	0.89 + 0.019*CL	0.96 + 0.018*CL	1.05 + 0.017*CL
	tR	2.85	0.73 + 0.042*CL	0.69 + 0.043*CL	0.63 + 0.044*CL
	tF	2.37	0.62 + 0.035*CL	0.77 + 0.032*CL	0.92 + 0.030*CL
EN to PAD	tPLH	2.21	1.24 + 0.020*CL	1.25 + 0.019*CL	1.26 + 0.019*CL
	tPHL	2.00	1.03 + 0.019*CL	1.11 + 0.018*CL	1.20 + 0.017*CL
	tR	2.83	0.64 + 0.044*CL	0.62 + 0.044*CL	0.60 + 0.044*CL
	tF	2.38	0.63 + 0.035*CL	0.78 + 0.032*CL	0.93 + 0.030*CL
	tPLZ	1.72	1.72 + -0.000*CL	1.72 + 0.000*CL	1.72 + -0.000*CL
	tPHZ	0.86	0.86 + -0.000*CL	0.85 + 0.000*CL	0.86 + -0.000*CL
TN to PAD	tPLH	2.10	1.13 + 0.019*CL	1.14 + 0.019*CL	1.15 + 0.019*CL
	tPHL	1.88	0.91 + 0.019*CL	0.99 + 0.018*CL	1.08 + 0.017*CL
	tR	2.83	0.64 + 0.044*CL	0.62 + 0.044*CL	0.60 + 0.044*CL
	tF	2.38	0.63 + 0.035*CL	0.78 + 0.032*CL	0.93 + 0.030*CL
	tPLZ	1.78	1.78 + -0.000*CL	1.78 + 0.000*CL	1.78 + -0.000*CL
	tPHZ	0.93	0.93 + -0.000*CL	0.93 + -0.000*CL	0.93 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT20SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.32	1.31 + 0.020*CL	1.35 + 0.019*CL	1.37 + 0.019*CL
	tPHL	2.06	1.06 + 0.020*CL	1.16 + 0.018*CL	1.26 + 0.017*CL
	tR	2.99	0.82 + 0.043*CL	0.81 + 0.043*CL	0.79 + 0.044*CL
	tF	2.47	0.81 + 0.033*CL	0.91 + 0.031*CL	1.04 + 0.029*CL
EN to PAD	tPLH	2.37	1.33 + 0.021*CL	1.38 + 0.020*CL	1.42 + 0.019*CL
	tPHL	2.21	1.20 + 0.020*CL	1.30 + 0.018*CL	1.40 + 0.017*CL
	tR	3.00	0.86 + 0.043*CL	0.85 + 0.043*CL	0.82 + 0.044*CL
	tF	2.49	0.86 + 0.033*CL	0.95 + 0.031*CL	1.06 + 0.029*CL
	tPLZ	1.00	1.00 + -0.000*CL	1.00 + -0.000*CL	1.00 + 0.000*CL
	tPHZ	0.69	0.69 + -0.000*CL	0.69 + -0.000*CL	0.69 + -0.000*CL
TN to PAD	tPLH	2.26	1.22 + 0.021*CL	1.27 + 0.020*CL	1.30 + 0.019*CL
	tPHL	2.09	1.08 + 0.020*CL	1.18 + 0.018*CL	1.29 + 0.017*CL
	tR	3.00	0.86 + 0.043*CL	0.85 + 0.043*CL	0.82 + 0.044*CL
	tF	2.49	0.86 + 0.033*CL	0.96 + 0.031*CL	1.06 + 0.029*CL
	tPLZ	1.06	1.06 + 0.000*CL	1.06 + -0.000*CL	1.06 + -0.000*CL
	tPHZ	0.77	0.77 + -0.000*CL	0.77 + -0.000*CL	0.77 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT24 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.19	1.47 + 0.014*CL	1.45 + 0.015*CL	1.43 + 0.015*CL
	tPHL	1.89	0.96 + 0.019*CL	1.05 + 0.017*CL	1.15 + 0.016*CL
	tR	2.44	0.75 + 0.034*CL	0.70 + 0.035*CL	0.65 + 0.035*CL
	tF	2.19	0.61 + 0.031*CL	0.77 + 0.028*CL	0.92 + 0.027*CL
EN to PAD	tPLH	2.12	1.30 + 0.016*CL	1.32 + 0.016*CL	1.34 + 0.016*CL
	tPHL	2.04	1.09 + 0.019*CL	1.19 + 0.017*CL	1.30 + 0.016*CL
	tR	2.39	0.62 + 0.035*CL	0.60 + 0.036*CL	0.58 + 0.036*CL
	tF	2.20	0.63 + 0.032*CL	0.78 + 0.028*CL	0.94 + 0.026*CL
	tPLZ	1.92	1.92 + -0.000*CL	1.92 + -0.000*CL	1.92 + 0.000*CL
	tPHZ	0.94	0.94 + -0.000*CL	0.94 + -0.000*CL	0.94 + -0.000*CL
TN to PAD	tPLH	2.01	1.19 + 0.016*CL	1.21 + 0.016*CL	1.22 + 0.016*CL
	tPHL	1.92	0.98 + 0.019*CL	1.07 + 0.017*CL	1.18 + 0.016*CL
	tR	2.39	0.62 + 0.035*CL	0.60 + 0.036*CL	0.58 + 0.036*CL
	tF	2.20	0.63 + 0.032*CL	0.78 + 0.028*CL	0.94 + 0.026*CL
	tPLZ	1.99	1.99 + -0.000*CL	1.99 + -0.000*CL	1.99 + -0.000*CL
	tPHZ	1.01	1.01 + -0.000*CL	1.01 + -0.000*CL	1.01 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT24SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

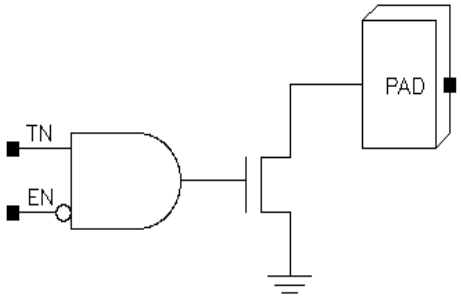
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	t_{PLH}	2.20	1.34 + 0.017*CL	1.38 + 0.016*CL	1.41 + 0.016*CL
	t_{PHL}	2.06	1.09 + 0.019*CL	1.19 + 0.017*CL	1.31 + 0.016*CL
	t_R	2.58	0.80 + 0.036*CL	0.80 + 0.036*CL	0.79 + 0.036*CL
	t_F	2.29	0.79 + 0.030*CL	0.91 + 0.028*CL	1.04 + 0.026*CL
EN to PAD	t_{PLH}	2.24	1.32 + 0.018*CL	1.40 + 0.017*CL	1.45 + 0.016*CL
	t_{PHL}	2.20	1.20 + 0.020*CL	1.33 + 0.017*CL	1.45 + 0.016*CL
	t_R	2.61	0.84 + 0.035*CL	0.85 + 0.035*CL	0.83 + 0.035*CL
	t_F	2.32	0.84 + 0.030*CL	0.96 + 0.027*CL	1.08 + 0.026*CL
	t_{PLZ}	1.10	1.10 + -0.000*CL	1.10 + -0.000*CL	1.10 + -0.000*CL
	t_{PHZ}	0.75	0.75 + -0.000*CL	0.75 + -0.000*CL	0.75 + -0.000*CL
TN to PAD	t_{PLH}	2.13	1.21 + 0.018*CL	1.28 + 0.017*CL	1.33 + 0.016*CL
	t_{PHL}	2.08	1.09 + 0.020*CL	1.21 + 0.017*CL	1.33 + 0.016*CL
	t_R	2.61	0.84 + 0.035*CL	0.85 + 0.035*CL	0.83 + 0.035*CL
	t_F	2.32	0.84 + 0.030*CL	0.96 + 0.027*CL	1.08 + 0.026*CL
	t_{PLZ}	1.17	1.17 + -0.000*CL	1.17 + -0.000*CL	1.17 + -0.000*CL
	t_{PHZ}	0.82	0.82 + -0.000*CL	0.82 + -0.000*CL	0.82 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

Input: TN, EN
Output: PAD

Input Loading (SL):
- TN: All : 3.3556
- EN: All : 3.3556

I/O Slots: 1



Symbol

EN	TN	PAD
0	1	0
x	0	Hi-Z
1	x	Hi-Z

Truth Table

POD1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	8.78	1.74 + 0.141*CL	1.83 + 0.139*CL	1.93 + 0.138*CL
	tF	19.22	4.97 + 0.285*CL	4.29 + 0.299*CL	4.48 + 0.296*CL
	tPLZ	0.50	0.50 + -0.000*CL	0.50 + -0.000*CL	0.50 + -0.000*CL
TN to PAD	tPHL	8.66	1.62 + 0.141*CL	1.71 + 0.139*CL	1.80 + 0.138*CL
	tF	19.22	4.97 + 0.285*CL	4.29 + 0.299*CL	4.48 + 0.296*CL
	tPLZ	0.56	0.56 + -0.000*CL	0.56 + 0.000*CL	0.56 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	8.78	1.74 + 0.141*CL	1.83 + 0.139*CL	1.93 + 0.138*CL
	tF	19.22	4.97 + 0.285*CL	4.29 + 0.299*CL	4.48 + 0.296*CL
	tPLZ	0.50	0.50 + -0.000*CL	0.50 + -0.000*CL	0.50 + -0.000*CL
TN to PAD	tPHL	8.66	1.62 + 0.141*CL	1.71 + 0.139*CL	1.80 + 0.138*CL
	tF	19.22	4.97 + 0.285*CL	4.29 + 0.299*CL	4.48 + 0.296*CL
	tPLZ	0.56	0.56 + -0.000*CL	0.56 + 0.000*CL	0.56 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	4.81	1.17 + 0.073*CL	1.24 + 0.071*CL	1.31 + 0.070*CL
	tF	10.58	4.23 + 0.127*CL	3.52 + 0.141*CL	2.96 + 0.148*CL
	tPLZ	0.62	0.62 + 0.000*CL	0.62 + 0.000*CL	0.62 + 0.000*CL
TN to PAD	tPHL	4.69	1.04 + 0.073*CL	1.11 + 0.071*CL	1.19 + 0.070*CL
	tF	10.58	4.23 + 0.127*CL	3.52 + 0.141*CL	2.96 + 0.148*CL
	tPLZ	0.66	0.66 + -0.000*CL	0.66 + -0.000*CL	0.66 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD4SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	4.91	1.27 + 0.073*CL	1.34 + 0.071*CL	1.41 + 0.070*CL
	tF	10.58	4.23 + 0.127*CL	3.52 + 0.141*CL	2.96 + 0.148*CL
	tPLZ	0.54	0.54 + 0.000*CL	0.54 + 0.000*CL	0.54 + -0.000*CL
TN to PAD	tPHL	4.79	1.15 + 0.073*CL	1.22 + 0.071*CL	1.29 + 0.070*CL
	tF	10.58	4.23 + 0.127*CL	3.52 + 0.141*CL	2.96 + 0.148*CL
	tPLZ	0.59	0.59 + -0.000*CL	0.59 + -0.000*CL	0.59 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.50	0.89 + 0.032*CL	0.93 + 0.031*CL	0.99 + 0.031*CL
	tF	5.02	2.04 + 0.059*CL	2.05 + 0.059*CL	2.07 + 0.059*CL
	tPLZ	0.92	0.92 + 0.000*CL	0.92 + 0.000*CL	0.92 + -0.000*CL
TN to PAD	tPHL	2.37	0.76 + 0.032*CL	0.81 + 0.031*CL	0.86 + 0.031*CL
	tF	5.02	2.05 + 0.059*CL	2.05 + 0.059*CL	2.08 + 0.059*CL
	tPLZ	0.98	0.98 + -0.000*CL	0.98 + -0.000*CL	0.98 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD8SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.78	1.16 + 0.032*CL	1.22 + 0.031*CL	1.27 + 0.031*CL
	tF	5.05	2.11 + 0.059*CL	2.10 + 0.059*CL	2.12 + 0.059*CL
	tPLZ	0.54	0.54 + -0.000*CL	0.54 + 0.000*CL	0.54 + -0.000*CL
TN to PAD	tPHL	2.66	1.04 + 0.032*CL	1.09 + 0.031*CL	1.15 + 0.031*CL
	tF	5.05	2.11 + 0.059*CL	2.10 + 0.059*CL	2.11 + 0.059*CL
	tPLZ	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.10	0.87 + 0.025*CL	0.91 + 0.024*CL	0.97 + 0.023*CL
	tF	3.72	1.28 + 0.049*CL	1.40 + 0.046*CL	1.53 + 0.045*CL
	tPLZ	1.13	1.13 + -0.000*CL	1.13 + -0.000*CL	1.13 + -0.000*CL
TN to PAD	tPHL	1.98	0.74 + 0.025*CL	0.79 + 0.024*CL	0.85 + 0.023*CL
	tF	3.72	1.28 + 0.049*CL	1.40 + 0.046*CL	1.52 + 0.045*CL
	tPLZ	1.19	1.19 + -0.000*CL	1.19 + -0.000*CL	1.19 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD12SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.36	1.10 + 0.025*CL	1.16 + 0.024*CL	1.23 + 0.023*CL
	tF	3.78	1.38 + 0.048*CL	1.48 + 0.046*CL	1.59 + 0.045*CL
	tPLZ	0.65	0.65 + 0.000*CL	0.65 + 0.000*CL	0.65 + -0.000*CL
TN to PAD	tPHL	2.24	0.98 + 0.025*CL	1.04 + 0.024*CL	1.10 + 0.023*CL
	tF	3.78	1.38 + 0.048*CL	1.48 + 0.046*CL	1.59 + 0.045*CL
	tPLZ	0.71	0.71 + 0.000*CL	0.71 + 0.000*CL	0.71 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD16 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	1.91	0.87 + 0.021*CL	0.92 + 0.020*CL	0.98 + 0.019*CL
	tF	2.98	0.88 + 0.042*CL	1.04 + 0.039*CL	1.19 + 0.037*CL
	tPLZ	1.34	1.34 + -0.000*CL	1.34 + -0.000*CL	1.34 + -0.000*CL
TN to PAD	tPHL	1.79	0.74 + 0.021*CL	0.80 + 0.020*CL	0.85 + 0.019*CL
	tF	2.98	0.88 + 0.042*CL	1.04 + 0.039*CL	1.18 + 0.037*CL
	tPLZ	1.39	1.39 + -0.000*CL	1.39 + -0.000*CL	1.39 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD16SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.14	1.07 + 0.022*CL	1.14 + 0.020*CL	1.21 + 0.019*CL
	tF	3.05	1.03 + 0.040*CL	1.14 + 0.038*CL	1.27 + 0.037*CL
	tPLZ	0.75	0.75 + -0.000*CL	0.75 + -0.000*CL	0.75 + -0.000*CL
TN to PAD	tPHL	2.02	0.94 + 0.022*CL	1.01 + 0.020*CL	1.08 + 0.019*CL
	tF	3.05	1.04 + 0.040*CL	1.14 + 0.038*CL	1.27 + 0.037*CL
	tPLZ	0.81	0.81 + -0.000*CL	0.81 + -0.000*CL	0.81 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD20 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	1.75	0.88 + 0.017*CL	0.92 + 0.017*CL	0.96 + 0.016*CL
	tF	2.33	0.62 + 0.034*CL	0.74 + 0.032*CL	0.88 + 0.030*CL
	tPLZ	1.65	1.65 + -0.000*CL	1.65 + -0.000*CL	1.65 + -0.000*CL
TN to PAD	tPHL	1.63	0.76 + 0.017*CL	0.80 + 0.017*CL	0.84 + 0.016*CL
	tF	2.33	0.62 + 0.034*CL	0.74 + 0.032*CL	0.88 + 0.030*CL
	tPLZ	1.70	1.70 + -0.000*CL	1.70 + -0.000*CL	1.70 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD20SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.00	1.07 + 0.018*CL	1.14 + 0.017*CL	1.20 + 0.016*CL
	tF	2.46	0.86 + 0.032*CL	0.94 + 0.031*CL	1.03 + 0.029*CL
	tPLZ	0.86	0.86 + -0.000*CL	0.86 + -0.000*CL	0.86 + 0.000*CL
TN to PAD	tPHL	1.87	0.95 + 0.018*CL	1.01 + 0.017*CL	1.08 + 0.016*CL
	tF	2.46	0.86 + 0.032*CL	0.93 + 0.031*CL	1.03 + 0.029*CL
	tPLZ	0.91	0.91 + -0.000*CL	0.91 + -0.000*CL	0.91 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD24 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	1.70	0.90 + 0.016*CL	0.94 + 0.015*CL	0.98 + 0.015*CL
	tF	2.06	0.53 + 0.031*CL	0.65 + 0.028*CL	0.77 + 0.027*CL
	tPLZ	1.85	1.85 + -0.000*CL	1.85 + -0.000*CL	1.85 + -0.000*CL
TN to PAD	tPHL	1.57	0.78 + 0.016*CL	0.82 + 0.015*CL	0.86 + 0.015*CL
	tF	2.06	0.53 + 0.031*CL	0.65 + 0.028*CL	0.77 + 0.027*CL
	tPLZ	1.90	1.90 + -0.000*CL	1.90 + -0.000*CL	1.90 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD24SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	t_{PHL}	1.92	1.06 + 0.017*CL	1.13 + 0.016*CL	1.20 + 0.015*CL
	t_F	2.22	0.79 + 0.029*CL	0.87 + 0.027*CL	0.95 + 0.026*CL
	t_{PLZ}	0.96	0.96 + -0.000*CL	0.96 + -0.000*CL	0.96 + -0.000*CL
TN to PAD	t_{PHL}	1.80	0.94 + 0.017*CL	1.01 + 0.016*CL	1.07 + 0.015*CL
	t_F	2.22	0.78 + 0.029*CL	0.87 + 0.027*CL	0.95 + 0.026*CL
	t_{PLZ}	1.02	1.02 + -0.000*CL	1.02 + -0.000*CL	1.02 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

3.5 Bidirectional I/O Buffers

Bidirectional Buffer Naming Conventions:

P B xz u v w

where x = C -- CMOS levels
S -- CMOS Schmitt Trigger levels

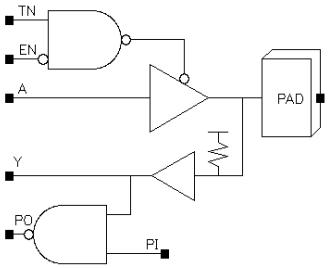
z = (optional)
U -- pull-up resistor
D -- pull-down resistor

u = B -- Normal non-inverting buffer
T -- Tristate non-inverting buffer
D -- Open-drain output

v = 1 -- 1mA drive
2 -- 2mA drive
4 -- 4mA drive
8 -- 8mA drive
12 -- 12mA drive
16 -- 16mA drive
20 -- 20mA drive
24 -- 24mA drive

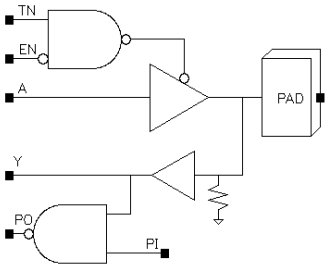
w = (optional)
none -- no slew-rate control
SM -- medium slew-rate control

e.g. PBSUT16SM - CMOS Schmitt Trigger input buffer, pull-up, tristate non-inverting with 16mA drive and medium slew-rate control



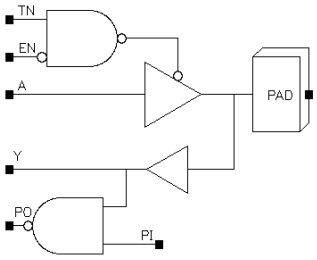
PBxUTvw

Bidirectional Tristate Buffer with Pull-Up, Non-Inverting Input



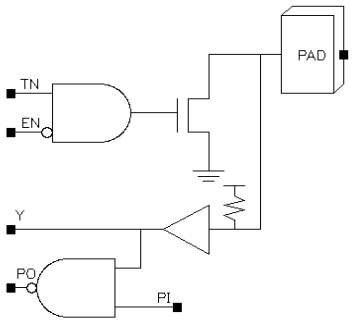
PBxDTvw

Bidirectional Tristate Buffer with Pull-Down, Non-Inverting Input



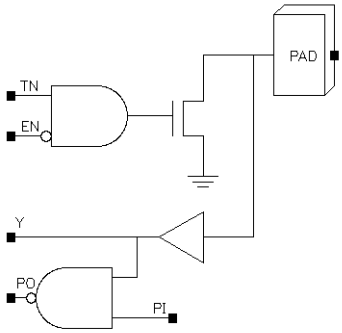
PBxTvw

Bidirectional Tristate Buffer with Non-Inverting Input



PBxUDvw

Bidirectional Open Drain Buffer with Pull-Up, Non-Inverting Input



PBxDvw

Bidirectional Open Drain Buffer with Non-Inverting Input

3.6 Clock Drivers

Clock Driver Naming Convention:

CK z

PSCKD x y z

where x = C -- CMOS level

S -- CMOS Schmitt Trigger level

y = (optional)

U -- pull-up resistor

D -- pull-down resistor

z = Maximum Load

2 -- 5pF

4 -- 10pF

6 -- 15pF

8 -- 20pF

12 -- 30pF

16 -- 40pF

20 -- 50pF

Cell Propagation Time:

T_{PHL} 1ns (typical)

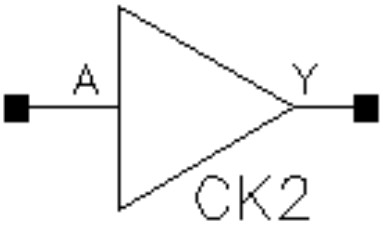
T_{PLH} 0.8ns (typical)

Inputs: A

Outputs: Y

Input Loading (SL): A:
- CK2: 3.3556
- CK4: 7.7778
- CK6: 10.0556
- CK8: 14.5000
- CK12: 13.4444
- CK16: 22.2778
- CK20: 32.3333

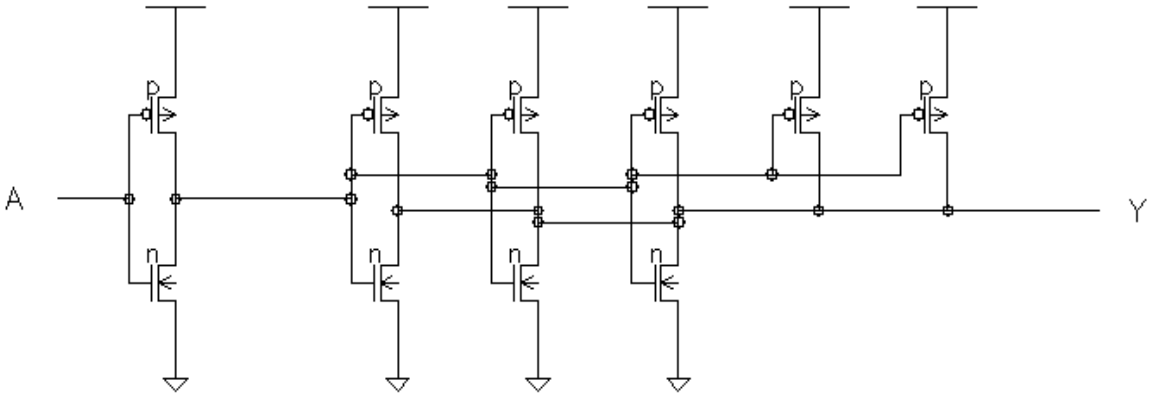
I/O Slots: All : 1



Symbol

A	Y
0	0
1	1

Truth Table



Schematic

CK2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=5.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.78	0.29 + 0.100*CL	0.30 + 0.097*CL	0.29 + 0.099*CL
	tPHL	1.13	0.52 + 0.123*CL	0.52 + 0.121*CL	0.52 + 0.121*CL
	tR	1.19	0.16 + 0.200*CL	0.13 + 0.212*CL	0.11 + 0.216*CL
	tF	1.22	0.14 + 0.209*CL	0.12 + 0.220*CL	0.08 + 0.227*CL

*Range1 : CL < 2.50, *Range2 : 2.50 ≦ CL ≦ 5.00, *Range3 : 5.00 < CL

CK4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=10.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.70	0.14 + 0.056*CL	0.14 + 0.056*CL	0.13 + 0.056*CL
	tPHL	1.18	0.57 + 0.061*CL	0.57 + 0.060*CL	0.57 + 0.061*CL
	tR	1.34	0.15 + 0.116*CL	0.11 + 0.123*CL	0.08 + 0.126*CL
	tF	1.21	0.12 + 0.109*CL	0.11 + 0.110*CL	0.08 + 0.113*CL

*Range1 : CL < 5.00, *Range2 : 5.00 ≦ CL ≦ 10.00, *Range3 : 10.00 < CL

CK6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=15.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.78	0.29 + 0.033*CL	0.30 + 0.032*CL	0.29 + 0.033*CL
	tPHL	1.13	0.52 + 0.041*CL	0.52 + 0.040*CL	0.52 + 0.040*CL
	tR	1.19	0.16 + 0.067*CL	0.13 + 0.071*CL	0.11 + 0.072*CL
	tF	1.22	0.14 + 0.070*CL	0.12 + 0.073*CL	0.08 + 0.076*CL

*Range1 : CL < 7.50, *Range2 : 7.50 ≦ CL ≦ 15.00, *Range3 : 15.00 < CL

CK8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=20.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.78	0.29 + 0.025*CL	0.30 + 0.024*CL	0.29 + 0.025*CL
	tPHL	1.13	0.52 + 0.031*CL	0.52 + 0.030*CL	0.52 + 0.030*CL
	tR	1.19	0.16 + 0.050*CL	0.13 + 0.053*CL	0.11 + 0.054*CL
	tF	1.22	0.14 + 0.052*CL	0.12 + 0.055*CL	0.08 + 0.057*CL

*Range1 : CL < 10.00, *Range2 : 10.00 ≦ CL ≦ 20.00, *Range3 : 20.00 < CL

CK12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=30.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.78	0.25 + 0.018*CL	0.25 + 0.018*CL	0.25 + 0.018*CL
	tPHL	1.18	0.57 + 0.020*CL	0.57 + 0.020*CL	0.57 + 0.020*CL
	tR	1.29	0.14 + 0.038*CL	0.13 + 0.039*CL	0.10 + 0.040*CL
	tF	1.21	0.14 + 0.035*CL	0.12 + 0.036*CL	0.09 + 0.038*CL

*Range1 : CL < 15.00, *Range2 : 15.00 ≦ CL ≦ 30.00, *Range3 : 30.00 < CL

CK16 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=40.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.77	0.23 + 0.014*CL	0.23 + 0.013*CL	0.23 + 0.014*CL
	tPHL	1.19	0.61 + 0.015*CL	0.61 + 0.015*CL	0.61 + 0.014*CL
	tR	1.31	0.16 + 0.028*CL	0.12 + 0.030*CL	0.09 + 0.030*CL
	tF	1.17	0.16 + 0.025*CL	0.13 + 0.026*CL	0.09 + 0.027*CL

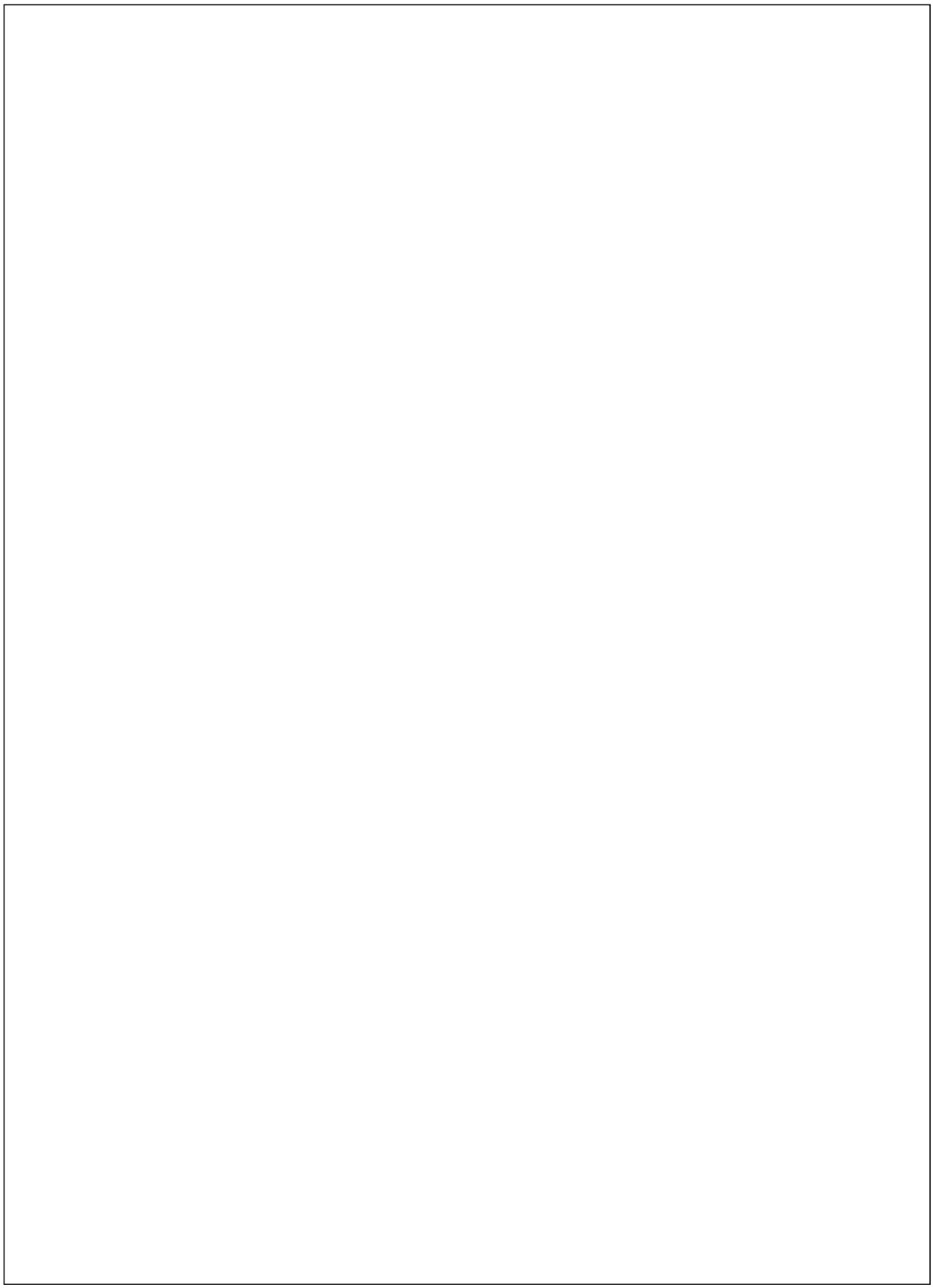
*Range1 : CL < 20.00, *Range2 : 20.00 ≦ CL ≦ 40.00, *Range3 : 40.00 < CL

CK20 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.78	0.22 + 0.011*CL	0.22 + 0.011*CL	0.22 + 0.011*CL
	tPHL	1.16	0.55 + 0.012*CL	0.55 + 0.012*CL	0.55 + 0.012*CL
	tR	1.35	0.16 + 0.023*CL	0.12 + 0.025*CL	0.08 + 0.025*CL
	tF	1.21	0.15 + 0.021*CL	0.11 + 0.022*CL	0.08 + 0.023*CL

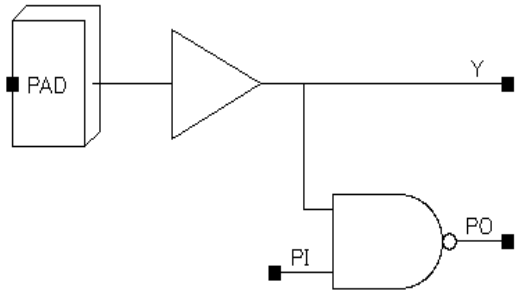
*Range1 : CL < 25.00, *Range2 : 25.00 ≦ CL ≦ 50.00, *Range3 : 50.00 < CL



Inputs: PAD, PI
Outputs: Y, PO

Input Loading (SL): All:
- PI: 3.3556

I/O Slots: 1



Symbol

Note: For timing information for PSCKDCD2/4/6/8/12 or PSCKDCU2/4/6/8/12, please refer to the timing tables for PSCKDC.

PSCKDC2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=5.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	3.26	0.14 + 0.646*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	tPHL	3.78	0.15 + 0.747*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	tR	4.44	0.52 + 0.798*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	tF	5.65	0.49 + 1.044*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	tPLH	3.12	0.24 + 0.591*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	tPHL	3.35	0.06 + 0.675*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	tR	4.33	0.59 + 0.758*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	tF	5.30	0.52 + 0.956*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	tPLH	1.09	0.60 + 0.101*CL	0.60 + 0.098*CL	0.59 + 0.100*CL
	tPHL	0.84	0.22 + 0.125*CL	0.22 + 0.124*CL	0.24 + 0.119*CL
	tR	1.20	0.16 + 0.203*CL	0.13 + 0.214*CL	0.11 + 0.218*CL
	tF	1.23	0.13 + 0.215*CL	0.11 + 0.224*CL	0.09 + 0.228*CL

*Range1 : CL < 2.50, *Range2 : 2.50 ≦ CL ≦ 5.00, *Range3 : 5.00 < CL

PSCKDC4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=10.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	t_{PLH}	6.26	0.14 + 0.623*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	t_{PHL}	7.31	0.15 + 0.726*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	t_R	8.31	0.52 + 0.785*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	t_F	10.74	0.49 + 1.032*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	t_{PLH}	5.91	0.24 + 0.575*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	t_{PHL}	6.56	0.06 + 0.658*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	t_R	8.03	0.59 + 0.749*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	t_F	10.07	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	t_{PLH}	1.26	0.69 + 0.058*CL	0.70 + 0.056*CL	0.70 + 0.056*CL
	t_{PHL}	0.91	0.29 + 0.062*CL	0.30 + 0.061*CL	0.30 + 0.061*CL
	t_R	1.37	0.16 + 0.118*CL	0.15 + 0.122*CL	0.12 + 0.125*CL
	t_F	1.22	0.16 + 0.102*CL	0.12 + 0.110*CL	0.09 + 0.113*CL

*Range1 : CL < 5.00, *Range2 : 5.00 ≦ CL ≦ 10.00, *Range3 : 10.00 < CL

PSCKDC6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=15.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	t_{PLH}	9.26	0.14 + 0.615*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	t_{PHL}	10.83	0.15 + 0.719*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	t_R	12.17	0.52 + 0.781*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	t_F	15.84	0.49 + 1.028*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	t_{PLH}	8.70	0.24 + 0.570*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	t_{PHL}	9.76	0.06 + 0.652*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	t_R	11.74	0.59 + 0.746*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	t_F	14.85	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	t_{PLH}	1.17	0.67 + 0.034*CL	0.68 + 0.033*CL	0.68 + 0.033*CL
	t_{PHL}	0.99	0.37 + 0.041*CL	0.38 + 0.041*CL	0.38 + 0.041*CL
	t_R	1.20	0.15 + 0.070*CL	0.14 + 0.071*CL	0.12 + 0.072*CL
	t_F	1.22	0.16 + 0.068*CL	0.11 + 0.074*CL	0.09 + 0.076*CL

*Range1 : CL < 7.50, *Range2 : 7.50 ≦ CL ≦ 15.00, *Range3 : 15.00 < CL

PSCKDC8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=20.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	t_{PLH}	12.26	0.14 + 0.611*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	t_{PHL}	14.36	0.15 + 0.716*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	t_R	16.03	0.52 + 0.779*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	t_F	20.94	0.49 + 1.026*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	t_{PLH}	11.50	0.24 + 0.567*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	t_{PHL}	12.97	0.06 + 0.650*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	t_R	15.44	0.59 + 0.745*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	t_F	19.62	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	t_{PLH}	1.22	0.71 + 0.027*CL	0.73 + 0.025*CL	0.74 + 0.024*CL
	t_{PHL}	1.04	0.42 + 0.031*CL	0.43 + 0.031*CL	0.43 + 0.030*CL
	t_R	1.21	0.20 + 0.049*CL	0.17 + 0.052*CL	0.11 + 0.055*CL
	t_F	1.23	0.16 + 0.051*CL	0.12 + 0.055*CL	0.10 + 0.056*CL

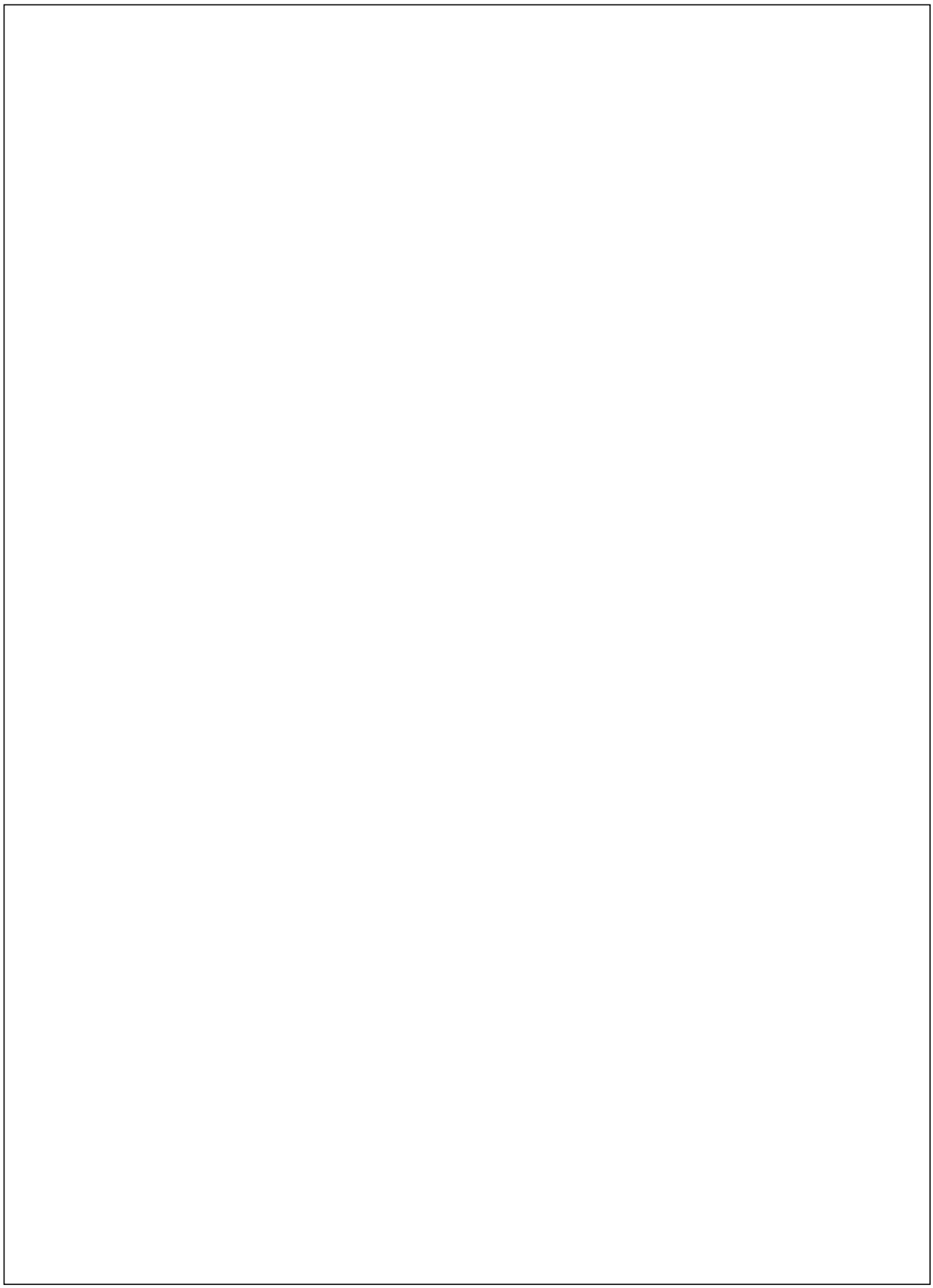
*Range1 : CL < 10.00, *Range2 : 10.00 ≦ CL ≦ 20.00, *Range3 : 20.00 < CL

PSCKDC12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=30.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	t_{PLH}	18.26	0.14 + 0.608*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	t_{PHL}	21.41	0.15 + 0.712*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	t_R	23.76	0.52 + 0.777*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	t_F	31.14	0.49 + 1.024*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	t_{PLH}	17.09	0.24 + 0.564*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	t_{PHL}	19.38	0.06 + 0.647*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	t_R	22.84	0.59 + 0.743*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	t_F	29.17	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	t_{PLH}	1.36	0.80 + 0.019*CL	0.82 + 0.018*CL	0.83 + 0.018*CL
	t_{PHL}	1.11	0.49 + 0.021*CL	0.50 + 0.020*CL	0.51 + 0.020*CL
	t_R	1.33	0.21 + 0.036*CL	0.17 + 0.039*CL	0.14 + 0.039*CL
	t_F	1.23	0.18 + 0.034*CL	0.14 + 0.036*CL	0.11 + 0.037*CL

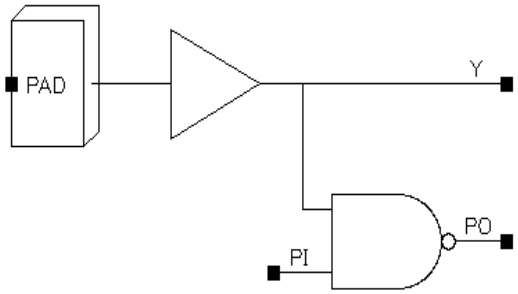
*Range1 : CL < 15.00, *Range2 : 15.00 ≦ CL ≦ 30.00, *Range3 : 30.00 < CL



Inputs: PAD, PI
Outputs: Y, PO

Input Loading (SL): All:
- PI: 3.3556

I/O Slots: 1



Symbol

Note: For timing information for PSCKDSD2/4/6/8/12 or PSCKDSU2/4/6/8/12, please refer to the timing tables for PSCKDS.

PSCKDS2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=5.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	t_{PLH}	3.26	0.14 + 0.646*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	t_{PHL}	3.78	0.15 + 0.747*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	t_R	4.44	0.52 + 0.798*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	t_F	5.65	0.49 + 1.044*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	t_{PLH}	3.12	0.24 + 0.591*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	t_{PHL}	3.35	0.06 + 0.675*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	t_R	4.33	0.59 + 0.758*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	t_F	5.30	0.52 + 0.956*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	t_{PLH}	1.07	0.57 + 0.102*CL	0.58 + 0.098*CL	0.58 + 0.098*CL
	t_{PHL}	2.02	1.38 + 0.132*CL	1.40 + 0.122*CL	1.41 + 0.122*CL
	t_R	1.20	0.18 + 0.197*CL	0.14 + 0.213*CL	0.10 + 0.219*CL
	t_F	1.25	0.19 + 0.205*CL	0.16 + 0.219*CL	0.14 + 0.223*CL

*Range1 : CL < 2.50, *Range2 : 2.50 ≦ CL ≦ 5.00, *Range3 : 5.00 < CL

PSCKDS4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=10.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	6.26	0.14 + 0.623*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	tPHL	7.31	0.15 + 0.726*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	tR	8.31	0.52 + 0.785*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	tF	10.74	0.49 + 1.032*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	tPLH	5.91	0.24 + 0.575*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	tPHL	6.56	0.06 + 0.658*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	tR	8.03	0.59 + 0.749*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	tF	10.07	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	tPLH	1.29	0.71 + 0.060*CL	0.73 + 0.056*CL	0.73 + 0.056*CL
	tPHL	2.25	1.59 + 0.069*CL	1.63 + 0.063*CL	1.64 + 0.061*CL
	tR	1.38	0.20 + 0.115*CL	0.17 + 0.121*CL	0.14 + 0.124*CL
	tF	1.30	0.25 + 0.104*CL	0.24 + 0.106*CL	0.21 + 0.109*CL

*Range1 : CL < 5.00, *Range2 : 5.00 ≦ CL ≦ 10.00, *Range3 : 10.00 < CL

PSCKDS6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=15.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	9.26	0.14 + 0.615*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	tPHL	10.83	0.15 + 0.719*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	tR	12.17	0.52 + 0.781*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	tF	15.84	0.49 + 1.028*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	tPLH	8.70	0.24 + 0.570*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	tPHL	9.76	0.06 + 0.652*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	tR	11.74	0.59 + 0.746*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	tF	14.85	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	tPLH	1.08	0.58 + 0.034*CL	0.59 + 0.033*CL	0.59 + 0.032*CL
	tPHL	2.24	1.59 + 0.045*CL	1.62 + 0.041*CL	1.63 + 0.041*CL
	tR	1.20	0.16 + 0.068*CL	0.13 + 0.071*CL	0.10 + 0.073*CL
	tF	1.28	0.23 + 0.068*CL	0.20 + 0.072*CL	0.18 + 0.073*CL

*Range1 : CL < 7.50, *Range2 : 7.50 ≦ CL ≦ 15.00, *Range3 : 15.00 < CL

PSCKDS8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=20.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	12.26	0.14 + 0.611*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	tPHL	14.36	0.15 + 0.716*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	tR	16.03	0.52 + 0.779*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	tF	20.94	0.49 + 1.026*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	tPLH	11.50	0.24 + 0.567*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	tPHL	12.97	0.06 + 0.650*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	tR	15.44	0.59 + 0.745*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	tF	19.62	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	tPLH	1.16	0.64 + 0.027*CL	0.66 + 0.025*CL	0.67 + 0.024*CL
	tPHL	2.39	1.73 + 0.035*CL	1.76 + 0.032*CL	1.78 + 0.031*CL
	tR	1.22	0.18 + 0.051*CL	0.16 + 0.053*CL	0.14 + 0.054*CL
	tF	1.31	0.28 + 0.050*CL	0.25 + 0.053*CL	0.22 + 0.055*CL

*Range1 : CL < 10.00, *Range2 : 10.00 ≦ CL ≦ 20.00, *Range3 : 20.00 < CL

PSCKDS12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=30.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	18.26	0.14 + 0.608*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	tPHL	21.41	0.15 + 0.712*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	tR	23.76	0.52 + 0.777*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	tF	31.14	0.49 + 1.024*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	tPLH	17.09	0.24 + 0.564*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	tPHL	19.38	0.06 + 0.647*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	tR	22.84	0.59 + 0.743*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	tF	29.17	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	tPLH	1.31	0.75 + 0.019*CL	0.77 + 0.018*CL	0.77 + 0.018*CL
	tPHL	2.62	1.93 + 0.024*CL	1.97 + 0.022*CL	2.00 + 0.021*CL
	tR	1.34	0.22 + 0.036*CL	0.18 + 0.038*CL	0.15 + 0.040*CL
	tF	1.38	0.35 + 0.034*CL	0.34 + 0.035*CL	0.31 + 0.036*CL

*Range1 : CL < 15.00, *Range2 : 15.00 ≦ CL ≦ 30.00, *Range3 : 30.00 < CL

3.7 Oscillators

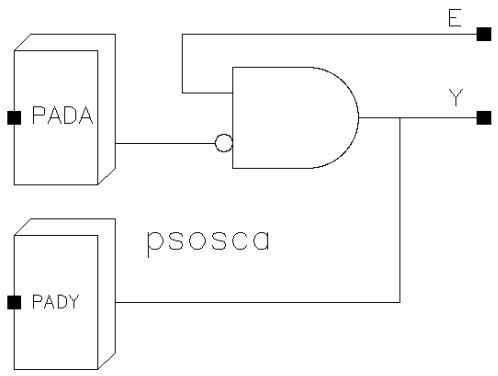
Oscillator Naming Conventions:

No naming conventions have been adopted for the two oscillators.

Inputs: PADA, E
Outputs: PADY, Y

Input Loading (SL):
- E : 8.6667

I/O Slots: 2



Symbol

PADA	E	PADY	Y
x	0	0	0
0	1	1	1
1	1	0	0

Truth Table

PSOSCA Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
PADA to PADY	t_{PLH}	5.45	1.01 + 0.089*CL	1.01 + 0.089*CL	1.01 + 0.089*CL
	t_{PHL}	5.51	1.86 + 0.073*CL	1.95 + 0.071*CL	2.10 + 0.069*CL
	t_R	12.52	2.13 + 0.208*CL	2.12 + 0.208*CL	2.13 + 0.208*CL
	t_F	10.55	4.15 + 0.128*CL	3.46 + 0.142*CL	2.96 + 0.148*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PSOSCA Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
E to PADY	t_{PLH}	5.37	0.94 + 0.089*CL	0.94 + 0.089*CL	0.94 + 0.089*CL
	t_{PHL}	5.19	1.56 + 0.073*CL	1.63 + 0.071*CL	1.79 + 0.069*CL
	t_R	12.52	2.13 + 0.208*CL	2.12 + 0.208*CL	2.13 + 0.208*CL
	t_F	10.55	4.15 + 0.128*CL	3.47 + 0.142*CL	2.95 + 0.148*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PSOSCA Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

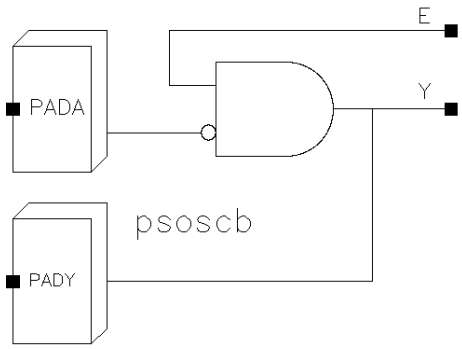
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
PADY to Y	t_{PLH}	0.12	0.11 + 0.004*SL	0.11 + 0.003*SL	0.12 + 0.002*SL
	t_{PHL}	0.37	0.35 + 0.006*SL	0.36 + 0.004*SL	0.37 + 0.004*SL
	t_R	0.12	0.10 + 0.010*SL	0.11 + 0.004*SL	0.12 + 0.004*SL
	t_F	0.10	0.09 + 0.008*SL	0.09 + 0.006*SL	0.11 + 0.006*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Inputs: PADA, E
Outputs: PADY, Y

Input Loading (SL):
- E : 3.3556

I/O Slots: 2



Symbol

PADA	E	PADY	Y
x	0	0	0
0	1	1	1
1	1	0	0

Truth Table

PSOSCB Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
PADA to PADY	tPLH	2.14	1.36 + 0.016*CL	1.36 + 0.016*CL	1.36 + 0.016*CL
	tPHL	1.85	0.90 + 0.019*CL	1.01 + 0.017*CL	1.10 + 0.016*CL
	tR	2.28	0.46 + 0.036*CL	0.45 + 0.037*CL	0.45 + 0.037*CL
	tF	2.23	0.64 + 0.032*CL	0.80 + 0.029*CL	0.97 + 0.027*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PSOSCB Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
E to PADY	tPLH	1.67	0.89 + 0.016*CL	0.89 + 0.016*CL	0.89 + 0.016*CL
	tPHL	1.90	0.95 + 0.019*CL	1.05 + 0.017*CL	1.16 + 0.016*CL
	tR	2.28	0.46 + 0.036*CL	0.45 + 0.037*CL	0.45 + 0.037*CL
	tF	2.23	0.64 + 0.032*CL	0.80 + 0.029*CL	0.97 + 0.027*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PSOSCB Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
PADY to Y	tPLH	0.54	0.54 + 0.000*SL	0.54 + 0.000*SL	0.54 + 0.000*SL
	tPHL	0.51	0.51 + 0.001*SL	0.51 + 0.001*SL	0.50 + 0.001*SL
	tR	0.11	0.11 + 0.000*SL	0.11 + 0.000*SL	0.11 + 0.001*SL
	tF	0.09	0.09 + 0.000*SL	0.09 + 0.000*SL	0.08 + 0.001*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Next chapter

Chapter 4.0 5.0V-Tolerant I/O Buffers and Clock Drivers

4.1 Overview

This chapter describes the AC characteristics of 5.0V-Tolerant Input and Output Buffers and Clock Drivers. The AC characteristics of Bidirectional Buffers can be derived from different combinations of Input and Output Buffers.

As there are over 300 possible combinations of I/O Buffers in the library, naming conventions have been adopted to help designers to memorize and use the cell library more efficiently. Naming conventions are described at the beginning of each sub-section.

4.2 Summary Tables

Table 4.1: 5.0V-Tolerant Input Buffers

Cell Name	Description	Page
PTIC/PTICU/PTICD	5.0V-Tolerant CMOS Level Non-Inverting Input Buffers	4-8
PTIS/PTISU/PTISD	5.0V-Tolerant CMOS Schmitt Trigger Level Non-Inverting input Buffers	4-10

Table 4.2 5.0V-Tolerant Output Buffers

Cell Name	Description	Page
PTOT1/2/4/6	5.0V-Tolerant Tristate Non-Inverting Output Buffers	4-14
PTOD1/2/4/6	5.0V-Tolerant Open Drain Output Buffers	4-17

Table 4.3 5.0V-Tolerant Bi-Directional Buffers

Cell Name	Description	Page
PTBCD 1/2/4/6	CMOS Non-inverted, no pull, open drain	4-21
PTBCUD 1/2/4/6	CMOS Non-inverted, pull up, open drain	4-21
PTBCT 1/2/4/6	CMOS Non-inverted, no pull, tri-state	4-20
PTBCDT 1/2/4/6	CMOS Non-inverted, pull down, tri-state	4-20
PTBCUT 1/2/4/6	CMOS Non-inverted, pull up, tri-state	4-20
PTBSD 1/2/4/6	CMOS Schmitt Trigger Non-inverted, no pull, open drain	4-21
PTBSUD 1/2/4/6	CMOS Schmitt Trigger Non-inverted, pull up, open drain	4-21
PTBST 1/2/4/6	CMOS Schmitt Trigger Non-inverted, no pull, tri-state	4-20
PTBSDT 1/2/4/6	CMOS Schmitt Trigger Non-inverted, pull down, tri-state	4-20
PTBSUT 1/2/4/6	CMOS Schmitt Trigger Non-inverted, pull up, tri-state	4-20

Table 4.4 5.0V-Tolerant Input Clock Drivers

Cell Name	Description	Page
PTSCKDC2/4/8/12	5.0V-Tolerant CMOS Level Clock Drivers with no Pull	4-24
PTSCKDCD2/4/8/12	5.0V-Tolerant CMOS Level Clock Drivers with Pull-Down	4-24
PTSCKDCU2/4/8/12	5.0V-Tolerant CMOS Level Clock Drivers with Pull-Up	4-24
PTSCKDS2/4/8/12	5.0V-Tolerant CMOS Schmitt Trigger Level Clock Drivers with no Pul	4-28
PTSCKDSD2/4/8/12	5.0V-Tolerant CMOS Schmitt Trigger Level Clock Drivers with Pull-Down	4-28
PTSCKDSU2/4/8/12	5.0V-Tolerant CMOS Schmitt Trigger Level Clock Drivers withPull-Up	4-28

Next Chapter

4.3 5.0V-Tolerant Input Buffers

5.0V-Tolerant Input Buffer Naming Conventions:

PTI x z

where x = C -- CMOS levels
S -- CMOS Schmitt Trigger levels

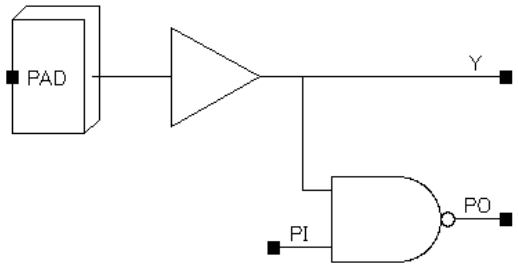
z = (optional)
U -- pull-up resistor
D -- pull-down resistor

e.g. PTISD - CMOS Schmitt Trigger input buffer with pull-down

Input: PAD, PI
Output Y, PO

Input Loading (SL): All
PI: 3.3556

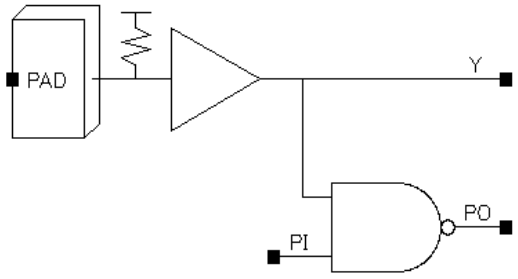
I/O Slots: 1



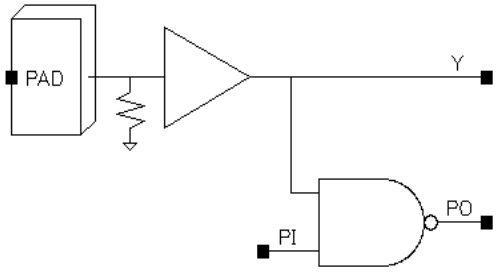
PTIC Symbol

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Truth Table



PTICU Symbol



PTICD Symbol

PTIC Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	t_{PLH}	0.13	0.09 + 0.018*SL	0.11 + 0.011*SL	0.18 + 0.008*SL
	t_{PHL}	0.14	0.10 + 0.018*SL	0.12 + 0.013*SL	0.17 + 0.010*SL
	t_R	0.30	0.26 + 0.018*SL	0.28 + 0.014*SL	0.28 + 0.013*SL
	t_F	0.29	0.23 + 0.027*SL	0.26 + 0.018*SL	0.25 + 0.018*SL
PI to PO	t_{PLH}	0.17	0.14 + 0.012*SL	0.15 + 0.010*SL	0.20 + 0.008*SL
	t_{PHL}	0.10	0.07 + 0.017*SL	0.08 + 0.012*SL	0.12 + 0.010*SL
	t_R	0.33	0.31 + 0.009*SL	0.30 + 0.013*SL	0.30 + 0.013*SL
	t_F	0.29	0.26 + 0.018*SL	0.26 + 0.017*SL	0.22 + 0.019*SL
PAD to Y	t_{PLH}	0.75	0.74 + 0.006*SL	0.74 + 0.004*SL	0.76 + 0.003*SL
	t_{PHL}	0.83	0.82 + 0.008*SL	0.82 + 0.007*SL	0.83 + 0.007*SL
	t_R	0.19	0.18 + 0.003*SL	0.18 + 0.005*SL	0.18 + 0.005*SL
	t_F	0.14	0.12 + 0.010*SL	0.11 + 0.013*SL	0.13 + 0.012*SL

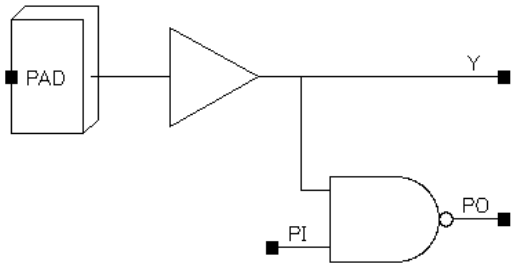
*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Note: The timing tables for PTICU and PTICD are the same as for PTIC.

Input: PAD, PI
Output Y, PO

Input Loading (SL): All
PI: 3.3556

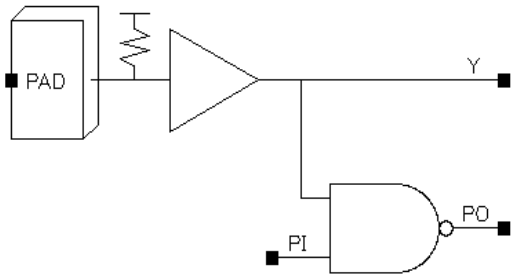
I/O Slots: 1



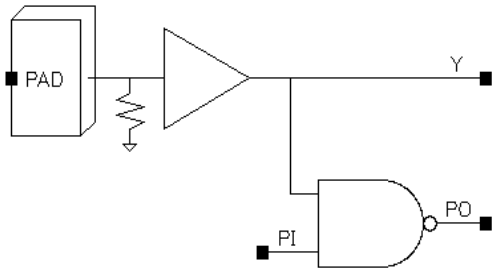
PTIS Symbol

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Truth Table



PTISU Symbol



PTISD Symbol

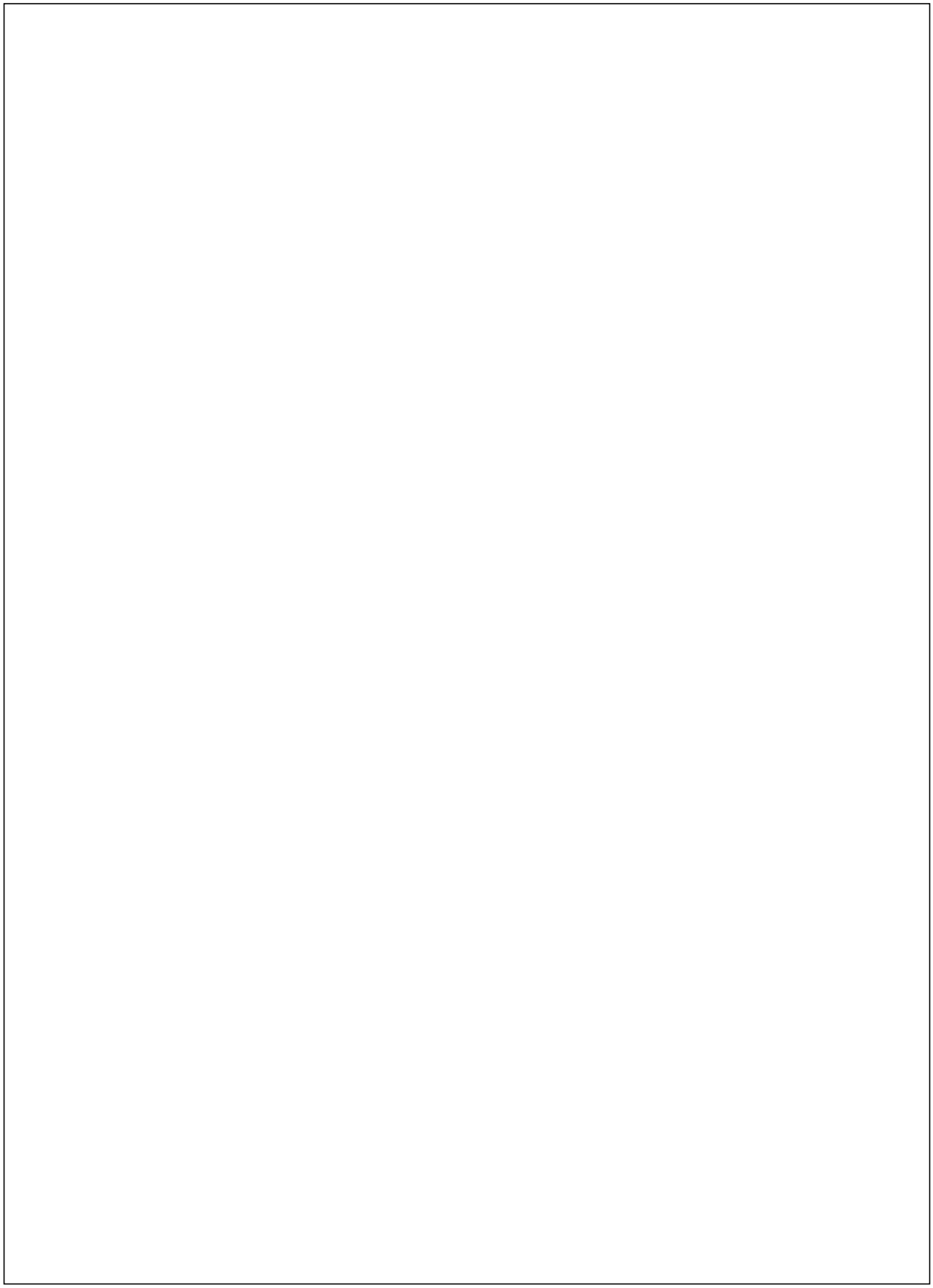
PTIS Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.13	0.09 + 0.018*SL	0.11 + 0.011*SL	0.18 + 0.008*SL
	tPHL	0.14	0.10 + 0.018*SL	0.12 + 0.013*SL	0.17 + 0.010*SL
	tR	0.30	0.26 + 0.018*SL	0.28 + 0.014*SL	0.28 + 0.013*SL
	tF	0.29	0.23 + 0.027*SL	0.26 + 0.018*SL	0.25 + 0.018*SL
PI to PO	tPLH	0.17	0.14 + 0.012*SL	0.15 + 0.010*SL	0.20 + 0.008*SL
	tPHL	0.10	0.07 + 0.017*SL	0.08 + 0.012*SL	0.12 + 0.010*SL
	tR	0.33	0.31 + 0.009*SL	0.30 + 0.013*SL	0.30 + 0.013*SL
	tF	0.29	0.26 + 0.018*SL	0.26 + 0.017*SL	0.22 + 0.019*SL
PAD to Y	tPLH	1.47	1.46 + 0.004*SL	1.46 + 0.003*SL	1.48 + 0.002*SL
	tPHL	1.38	1.37 + 0.005*SL	1.37 + 0.004*SL	1.38 + 0.004*SL
	tR	0.29	0.28 + 0.002*SL	0.28 + 0.003*SL	0.29 + 0.003*SL
	tF	0.17	0.15 + 0.006*SL	0.15 + 0.007*SL	0.18 + 0.005*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Note: The timing tables for PTISU and PTISD are the same as for PTIS.



4.4 5.0V-Tolerant Output Buffers

5.0V-Tolerant Output Buffer Naming Conventions:

PTO u v

where u = T -- Tristate non-inverting buffer
D -- Open-drain output

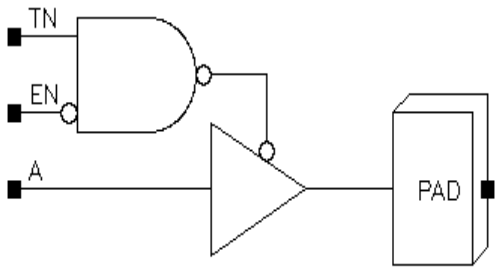
v = 1 -- 1mA drive
2 -- 2mA drive
4 -- 4mA drive
6 -- 6mA drive

e.g., PTOT12 - 3-state output buffer with 12mA drive

Input: TN, EN, A
Output: PAD

Input Loading (SL):
- TN: All: 3.3556
- EN: All : 3.3556
- A: All : 5.6111

I/O Slots: 1



Symbol

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

Truth Table

PTOT1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	11.61	2.27 + 0.187*CL	2.28 + 0.187*CL	2.33 + 0.186*CL
	tPHL	8.53	1.53 + 0.140*CL	1.62 + 0.138*CL	1.68 + 0.138*CL
	tR	24.00	3.84 + 0.403*CL	3.81 + 0.404*CL	3.60 + 0.407*CL
	tF	19.05	3.83 + 0.304*CL	4.17 + 0.298*CL	4.40 + 0.295*CL
EN to PAD	tPLH	11.58	2.55 + 0.181*CL	4.17 + 0.148*CL	8.86 + 0.090*CL
	tPHL	8.71	1.72 + 0.140*CL	1.79 + 0.138*CL	1.85 + 0.138*CL
	tR	24.00	3.84 + 0.403*CL	3.78 + 0.404*CL	3.80 + 0.404*CL
	tF	19.04	3.86 + 0.304*CL	4.15 + 0.298*CL	4.40 + 0.295*CL
	tPLZ	0.61	0.61 + -0.000*CL	0.61 + -0.000*CL	0.62 + -0.000*CL
	tPHZ	0.54	0.54 + 0.000*CL	0.54 + 0.000*CL	0.54 + 0.000*CL
TN to PAD	tPLH	11.47	2.43 + 0.181*CL	4.02 + 0.149*CL	8.68 + 0.091*CL
	tPHL	8.59	1.60 + 0.140*CL	1.67 + 0.138*CL	1.75 + 0.138*CL
	tR	24.00	3.84 + 0.403*CL	3.78 + 0.404*CL	3.77 + 0.405*CL
	tF	19.04	3.85 + 0.304*CL	4.15 + 0.298*CL	4.39 + 0.295*CL
	tPLZ	0.67	0.67 + -0.000*CL	0.67 + 0.000*CL	0.65 + 0.000*CL
	tPHZ	0.63	0.63 + 0.000*CL	0.63 + 0.000*CL	0.63 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PTOT2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	11.61	2.27 + 0.187*CL	2.28 + 0.187*CL	2.33 + 0.186*CL
	tPHL	8.53	1.53 + 0.140*CL	1.62 + 0.138*CL	1.68 + 0.138*CL
	tR	24.00	3.84 + 0.403*CL	3.81 + 0.404*CL	3.60 + 0.407*CL
	tF	19.05	3.83 + 0.304*CL	4.17 + 0.298*CL	4.40 + 0.295*CL
EN to PAD	tPLH	11.58	2.55 + 0.181*CL	4.17 + 0.148*CL	8.86 + 0.090*CL
	tPHL	8.71	1.72 + 0.140*CL	1.79 + 0.138*CL	1.85 + 0.138*CL
	tR	24.00	3.84 + 0.403*CL	3.78 + 0.404*CL	3.80 + 0.404*CL
	tF	19.04	3.86 + 0.304*CL	4.15 + 0.298*CL	4.40 + 0.295*CL
	tPLZ	0.61	0.61 + -0.000*CL	0.61 + -0.000*CL	0.62 + -0.000*CL
	tPHZ	0.54	0.54 + 0.000*CL	0.54 + 0.000*CL	0.54 + 0.000*CL
TN to PAD	tPLH	11.47	2.43 + 0.181*CL	4.02 + 0.149*CL	8.68 + 0.091*CL
	tPHL	8.59	1.60 + 0.140*CL	1.67 + 0.138*CL	1.75 + 0.138*CL
	tR	24.00	3.84 + 0.403*CL	3.78 + 0.404*CL	3.77 + 0.405*CL
	tF	19.04	3.85 + 0.304*CL	4.15 + 0.298*CL	4.39 + 0.295*CL
	tPLZ	0.67	0.67 + -0.000*CL	0.67 + 0.000*CL	0.65 + 0.000*CL
	tPHZ	0.63	0.63 + 0.000*CL	0.63 + 0.000*CL	0.63 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PTOT4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	7.20	1.68 + 0.110*CL	1.68 + 0.110*CL	1.66 + 0.111*CL
	tPHL	4.69	1.09 + 0.072*CL	1.17 + 0.071*CL	1.23 + 0.070*CL
	tR	14.37	2.32 + 0.241*CL	2.33 + 0.241*CL	2.33 + 0.241*CL
	tF	10.02	2.08 + 0.159*CL	2.34 + 0.154*CL	2.57 + 0.151*CL
EN to PAD	tPLH	7.31	1.79 + 0.110*CL	1.82 + 0.110*CL	1.99 + 0.108*CL
	tPHL	4.87	1.27 + 0.072*CL	1.35 + 0.071*CL	1.41 + 0.070*CL
	tR	14.37	2.32 + 0.241*CL	2.33 + 0.241*CL	2.31 + 0.241*CL
	tF	10.02	2.08 + 0.159*CL	2.34 + 0.154*CL	2.57 + 0.151*CL
	tPLZ	0.71	0.71 + -0.000*CL	0.71 + 0.000*CL	0.71 + -0.000*CL
	tPHZ	0.58	0.58 + 0.000*CL	0.58 + 0.000*CL	0.58 + 0.000*CL
TN to PAD	tPLH	7.20	1.68 + 0.110*CL	1.71 + 0.110*CL	1.87 + 0.108*CL
	tPHL	4.76	1.15 + 0.072*CL	1.23 + 0.071*CL	1.28 + 0.070*CL
	tR	14.37	2.32 + 0.241*CL	2.33 + 0.241*CL	2.31 + 0.241*CL
	tF	10.02	2.08 + 0.159*CL	2.35 + 0.153*CL	2.54 + 0.151*CL
	tPLZ	0.79	0.79 + 0.000*CL	0.78 + 0.000*CL	0.79 + -0.000*CL
	tPHZ	0.65	0.65 + 0.000*CL	0.65 + 0.000*CL	0.65 + 0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PTOT6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

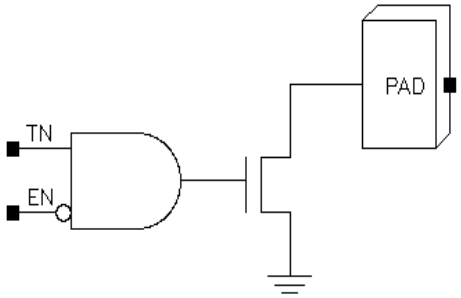
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	5.40	1.46 + 0.079*CL	1.48 + 0.078*CL	1.48 + 0.078*CL
	tPHL	2.87	0.91 + 0.039*CL	0.99 + 0.038*CL	1.08 + 0.036*CL
	tR	10.27	1.69 + 0.172*CL	1.68 + 0.172*CL	1.69 + 0.172*CL
	tF	5.40	1.18 + 0.085*CL	1.38 + 0.080*CL	1.57 + 0.078*CL
EN to PAD	tPLH	5.51	1.57 + 0.079*CL	1.59 + 0.078*CL	1.59 + 0.078*CL
	tPHL	3.04	1.08 + 0.039*CL	1.16 + 0.038*CL	1.26 + 0.036*CL
	tR	10.27	1.69 + 0.172*CL	1.68 + 0.172*CL	1.69 + 0.172*CL
	tF	5.40	1.17 + 0.085*CL	1.38 + 0.080*CL	1.57 + 0.078*CL
	tPLZ	0.92	0.92 + -0.000*CL	0.92 + 0.000*CL	0.92 + -0.000*CL
	tPHZ	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL
TN to PAD	tPLH	5.40	1.46 + 0.079*CL	1.47 + 0.078*CL	1.48 + 0.078*CL
	tPHL	2.93	0.97 + 0.039*CL	1.05 + 0.038*CL	1.14 + 0.036*CL
	tR	10.27	1.69 + 0.172*CL	1.68 + 0.172*CL	1.69 + 0.172*CL
	tF	5.40	1.17 + 0.085*CL	1.38 + 0.080*CL	1.56 + 0.078*CL
	tPLZ	0.98	1.00 + -0.000*CL	0.97 + 0.000*CL	0.98 + 0.000*CL
	tPHZ	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.68 + 0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

Input: TN, EN
Output: PAD

Input Loading (SL):
- TN: All: 3.3556
- EN: All : 3.3556

I/O Slots: 1



Symbol

EN	TN	PAD
0	1	0
x	0	Hi-Z
1	x	Hi-Z

Truth Table

PTOD1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	8.64	1.64 + 0.140*CL	1.72 + 0.138*CL	1.78 + 0.138*CL
	tF	19.03	3.83 + 0.304*CL	4.15 + 0.298*CL	4.39 + 0.295*CL
	tPLZ	0.53	0.53 + 0.000*CL	0.53 + -0.000*CL	0.53 + -0.000*CL
TN to PAD	tPHL	8.51	1.52 + 0.140*CL	1.60 + 0.138*CL	1.66 + 0.138*CL
	tF	19.04	3.83 + 0.304*CL	4.16 + 0.297*CL	4.36 + 0.295*CL
	tPLZ	0.60	0.60 + -0.000*CL	0.60 + 0.000*CL	0.60 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

PTOD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	8.64	1.64 + 0.140*CL	1.72 + 0.138*CL	1.78 + 0.138*CL
	tF	19.03	3.83 + 0.304*CL	4.15 + 0.298*CL	4.39 + 0.295*CL
	tPLZ	0.53	0.53 + 0.000*CL	0.53 + -0.000*CL	0.53 + -0.000*CL
TN to PAD	tPHL	8.51	1.52 + 0.140*CL	1.60 + 0.138*CL	1.66 + 0.138*CL
	tF	19.04	3.83 + 0.304*CL	4.16 + 0.297*CL	4.36 + 0.295*CL
	tPLZ	0.60	0.60 + -0.000*CL	0.60 + 0.000*CL	0.60 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PTOD4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	4.79	1.19 + 0.072*CL	1.26 + 0.071*CL	1.34 + 0.070*CL
	tF	10.02	2.07 + 0.159*CL	2.33 + 0.154*CL	2.62 + 0.150*CL
	tPLZ	0.65	0.65 + 0.000*CL	0.65 + 0.000*CL	0.65 + -0.000*CL
TN to PAD	tPHL	4.67	1.07 + 0.072*CL	1.15 + 0.071*CL	1.21 + 0.070*CL
	tF	10.02	2.07 + 0.159*CL	2.35 + 0.153*CL	2.57 + 0.151*CL
	tPLZ	0.70	0.70 + -0.000*CL	0.70 + 0.000*CL	0.70 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PTOD6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.97	1.00 + 0.039*CL	1.08 + 0.038*CL	1.18 + 0.036*CL
	tF	5.40	1.16 + 0.085*CL	1.37 + 0.080*CL	1.58 + 0.078*CL
	tPLZ	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + -0.000*CL
TN to PAD	tPHL	2.85	0.88 + 0.039*CL	0.96 + 0.038*CL	1.06 + 0.036*CL
	tF	5.40	1.16 + 0.085*CL	1.38 + 0.080*CL	1.56 + 0.078*CL
	tPLZ	0.91	0.91 + -0.000*CL	0.91 + -0.000*CL	0.91 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

4.5 5.0V-Tolerant Bidirectional I/O Buffers

5.0V-Tolerant Bidirectional Buffer Naming Conventions:

PTB xz u v

where

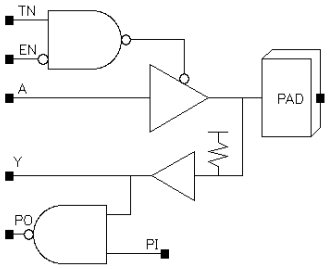
x = C -- CMOS levels
S -- CMOS Schmitt Trigger levels

z = (optional)
U -- pull-up resistor
D -- pull-down resistor

u = T -- Tristate non-inverting buffer
D -- Open-drain output

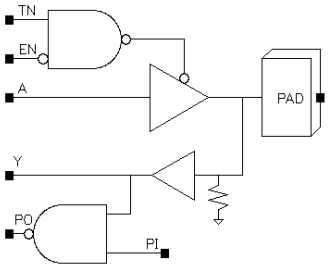
v = 1 -- 1mA drive
2 -- 2mA drive
4 -- 4mA drive
6 -- 6mA drive

e.g. PTBSUT6 - 5.0V Tolerant Schmitt Trigger input buffer and tristate output buffer with 6mA drive



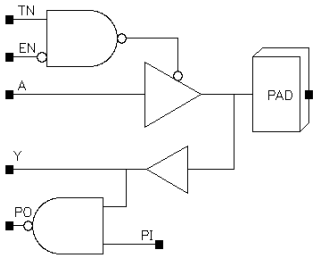
PTBxUTv

5.0V-Tolerant Bidirectional Tristate Buffer with Pull-Up, Non-Inverting Input



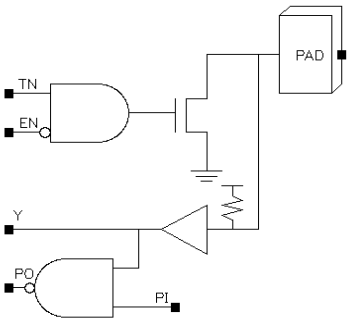
PTBxDTv

5.0V-Tolerant Bidirectional Tristate Buffer with Pull-Down, Non-Inverting Input



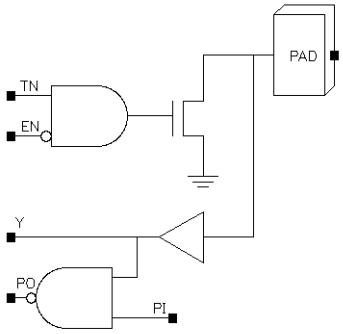
PTBxTv

5.0V-Tolerant Bidirectional Tristate Buffer with Non-Inverting Input



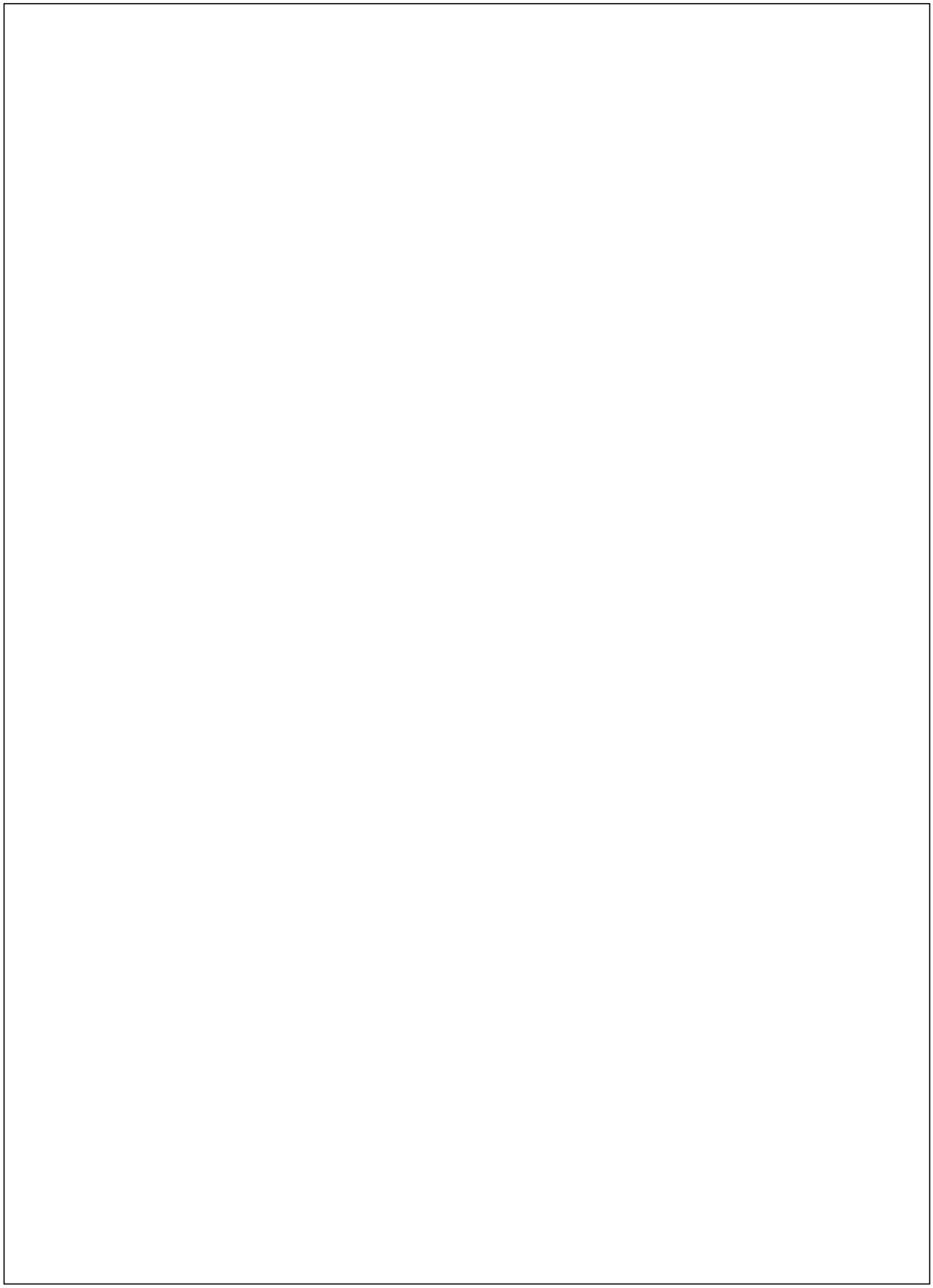
PTBxUDv

5.0V-Tolerant Bidirectional Open Drain Buffer with Pull-Up, Non-Inverting Input



PTBxDv

5.0V-Tolerant Bidirectional Open Drain Buffer with Non-Inverting Input



4.4 5.0V-Tolerant Clock Drivers

Clock Driver Naming Convention:

PTSCKD x y z

where x = C -- CMOS level

S -- CMOS Schmitt Trigger level

y = (optional)

U -- pull-up resistor

D -- pull-down resistor

z = Maximum Load

2 -- 5pF

4 -- 10pF

8 -- 20pF

12 -- 30pF

Cell Propagation Time:

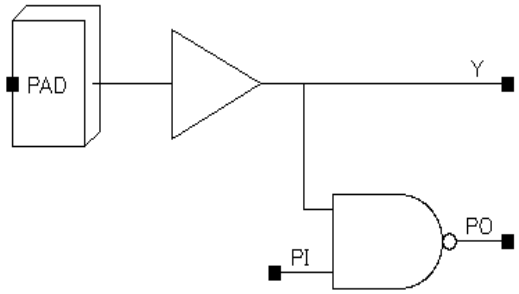
T_{PHL} 1ns (typical)

T_{PLH} 0.8ns (typical)

Inputs: PAD, PI
Outputs: Y, PO

Input Loading (SL): All:
PI: 3.3556

I/O Slots: 1



Symbol

Note: The timing tables for PTSCKDCD and PTSCKDCU are the same as for PTSCKDC.

PTSCKDC2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=5.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	t_{PLH}	3.26	0.14 + 0.646*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	t_{PHL}	3.78	0.15 + 0.747*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	t_R	4.44	0.52 + 0.798*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	t_F	5.65	0.49 + 1.044*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	t_{PLH}	3.12	0.24 + 0.591*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	t_{PHL}	3.35	0.06 + 0.675*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	t_R	4.33	0.59 + 0.758*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	t_F	5.30	0.52 + 0.956*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	t_{PLH}	2.35	1.73 + 0.130*CL	1.76 + 0.118*CL	1.77 + 0.115*CL
	t_{PHL}	1.50	0.88 + 0.124*CL	0.89 + 0.122*CL	0.89 + 0.122*CL
	t_R	1.45	0.35 + 0.213*CL	0.32 + 0.226*CL	0.30 + 0.230*CL
	t_F	1.22	0.11 + 0.218*CL	0.09 + 0.225*CL	0.08 + 0.228*CL

*Range1 : CL < 2.50, *Range2 : 2.50 ≦ CL ≦ 5.00, *Range3 : 5.00 < CL

PTSCKDC4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=10.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	6.26	0.14 + 0.623*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	tPHL	7.31	0.15 + 0.726*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	tR	8.31	0.52 + 0.785*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	tF	10.74	0.49 + 1.032*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	tPLH	5.91	0.24 + 0.575*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	tPHL	6.56	0.06 + 0.658*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	tR	8.03	0.59 + 0.749*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	tF	10.07	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	tPLH	2.64	1.95 + 0.072*CL	1.98 + 0.066*CL	1.99 + 0.064*CL
	tPHL	1.56	0.95 + 0.062*CL	0.95 + 0.061*CL	0.95 + 0.061*CL
	tR	1.65	0.43 + 0.117*CL	0.38 + 0.127*CL	0.35 + 0.130*CL
	tF	1.21	0.12 + 0.106*CL	0.09 + 0.112*CL	0.07 + 0.114*CL

*Range1 : CL < 5.00, *Range2 : 5.00 ≦ CL ≦ 10.00, *Range3 : 10.00 < CL

PTSCKDC8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=20.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	12.26	0.14 + 0.611*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	tPHL	14.36	0.15 + 0.716*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	tR	16.03	0.52 + 0.779*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	tF	20.94	0.49 + 1.026*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	tPLH	11.50	0.24 + 0.567*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	tPHL	12.97	0.06 + 0.650*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	tR	15.44	0.59 + 0.745*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	tF	19.62	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	tPLH	2.76	2.12 + 0.034*CL	2.17 + 0.030*CL	2.19 + 0.028*CL
	tPHL	1.76	1.14 + 0.031*CL	1.15 + 0.030*CL	1.15 + 0.030*CL
	tR	1.52	0.48 + 0.050*CL	0.44 + 0.054*CL	0.40 + 0.056*CL
	tF	1.22	0.12 + 0.054*CL	0.10 + 0.056*CL	0.09 + 0.057*CL

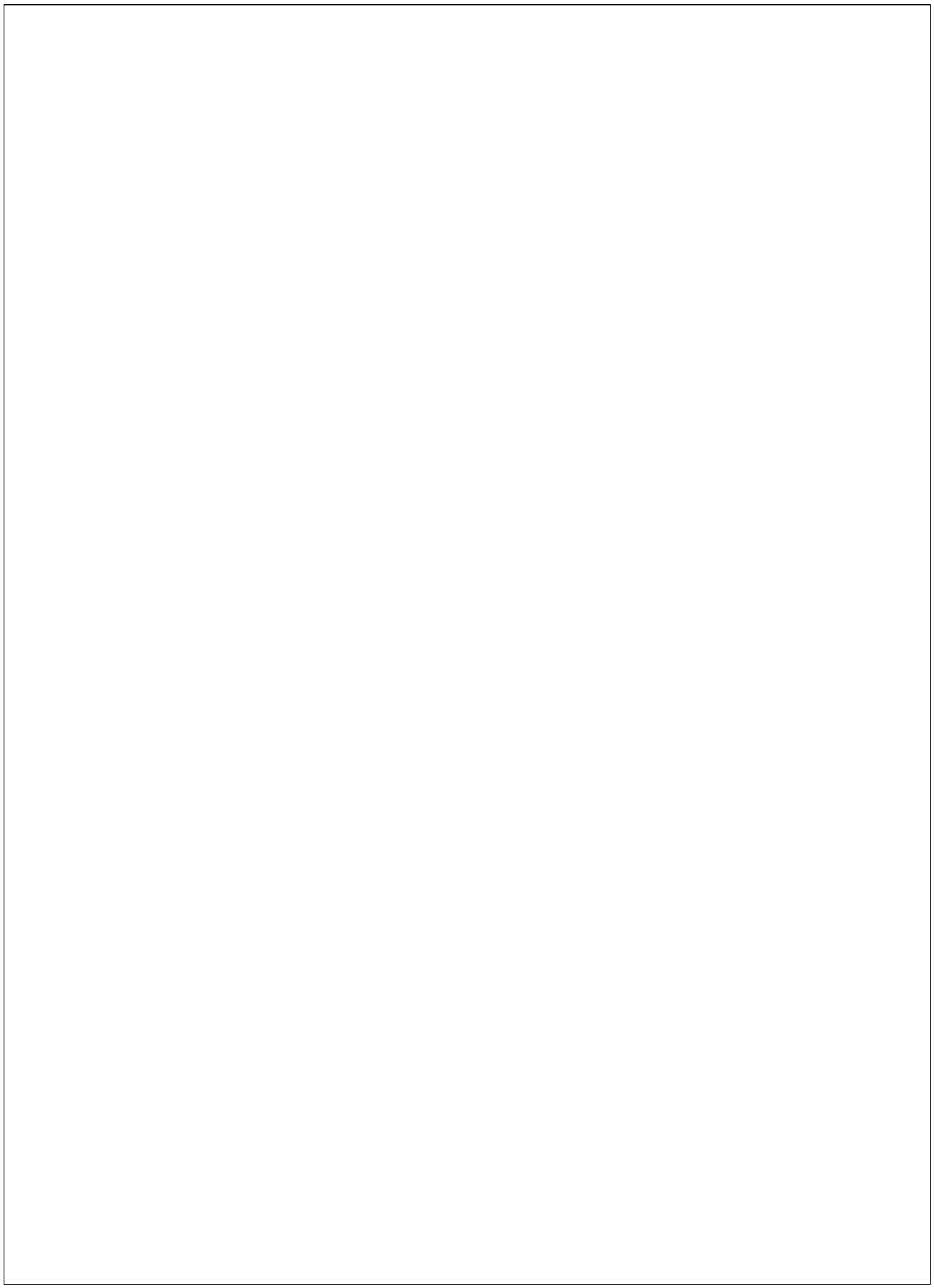
*Range1 : CL < 10.00, *Range2 : 10.00 ≦ CL ≦ 20.00, *Range3 : 20.00 < CL

PTSCKDC12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=30.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	t_{PLH}	18.26	0.14 + 0.608*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	t_{PHL}	21.41	0.15 + 0.712*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	t_R	23.76	0.52 + 0.777*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	t_F	31.14	0.49 + 1.024*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	t_{PLH}	17.09	0.24 + 0.564*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	t_{PHL}	19.38	0.06 + 0.647*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	t_R	22.84	0.59 + 0.743*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	t_F	29.17	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	t_{PLH}	3.00	2.32 + 0.024*CL	2.36 + 0.021*CL	2.39 + 0.020*CL
	t_{PHL}	1.82	1.21 + 0.021*CL	1.21 + 0.020*CL	1.21 + 0.020*CL
	t_R	1.67	0.56 + 0.036*CL	0.51 + 0.039*CL	0.48 + 0.040*CL
	t_F	1.22	0.15 + 0.034*CL	0.12 + 0.037*CL	0.10 + 0.037*CL

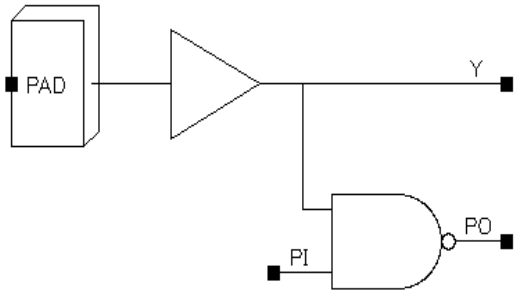
*Range1 : CL < 15.00, *Range2 : 15.00 ≦ CL ≦ 30.00, *Range3 : 30.00 < CL



Inputs: PAD, PI
Outputs: Y, PO

Input Loading (SL): All:
PI: 3.3556

I/O Slots: 1



Symbol

Note: The timing tables for PTSCKDSD and PTSCKDSU are the same as for PTSCKDS.

PTSCKDS2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=5.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	3.26	0.14 + 0.646*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	tPHL	3.78	0.15 + 0.747*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	tR	4.44	0.52 + 0.798*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	tF	5.65	0.49 + 1.044*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	tPLH	3.12	0.24 + 0.591*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	tPHL	3.35	0.06 + 0.675*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	tR	4.33	0.59 + 0.758*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	tF	5.30	0.52 + 0.956*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	tPLH	1.74	1.23 + 0.104*CL	1.25 + 0.097*CL	1.25 + 0.097*CL
	tPHL	2.48	1.85 + 0.130*CL	1.87 + 0.123*CL	1.88 + 0.121*CL
	tR	1.23	0.22 + 0.194*CL	0.19 + 0.208*CL	0.15 + 0.216*CL
	tF	1.25	0.19 + 0.207*CL	0.17 + 0.217*CL	0.14 + 0.223*CL

*Range1 : CL < 2.50, *Range2 : 2.50 ≦ CL ≦ 5.00, *Range3 : 5.00 < CL

PTSCKDS4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=10.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	6.26	0.14 + 0.623*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	tPHL	7.31	0.15 + 0.726*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	tR	8.31	0.52 + 0.785*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	tF	10.74	0.49 + 1.032*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	tPLH	5.91	0.24 + 0.575*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	tPHL	6.56	0.06 + 0.658*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	tR	8.03	0.59 + 0.749*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	tF	10.07	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	tPLH	2.06	1.48 + 0.061*CL	1.50 + 0.056*CL	1.51 + 0.055*CL
	tPHL	2.73	2.08 + 0.069*CL	2.11 + 0.063*CL	2.12 + 0.061*CL
	tR	1.43	0.29 + 0.111*CL	0.25 + 0.118*CL	0.20 + 0.122*CL
	tF	1.30	0.27 + 0.100*CL	0.24 + 0.106*CL	0.20 + 0.110*CL

*Range1 : CL < 5.00, *Range2 : 5.00 ≤ CL ≤ 10.00, *Range3 : 10.00 < CL

PTSCKDS8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=20.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	12.26	0.14 + 0.611*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	tPHL	14.36	0.15 + 0.716*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	tR	16.03	0.52 + 0.779*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	tF	20.94	0.49 + 1.026*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	tPLH	11.50	0.24 + 0.567*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	tPHL	12.97	0.06 + 0.650*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	tR	15.44	0.59 + 0.745*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	tF	19.62	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	tPLH	2.01	1.49 + 0.027*CL	1.51 + 0.025*CL	1.53 + 0.024*CL
	tPHL	3.08	2.42 + 0.035*CL	2.45 + 0.032*CL	2.47 + 0.031*CL
	tR	1.27	0.29 + 0.047*CL	0.24 + 0.051*CL	0.21 + 0.053*CL
	tF	1.32	0.29 + 0.049*CL	0.26 + 0.053*CL	0.23 + 0.055*CL

*Range1 : CL < 10.00, *Range2 : 10.00 ≤ CL ≤ 20.00, *Range3 : 20.00 < CL

PTSCKDS12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=30.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	18.26	0.14 + 0.608*CL	0.26 + 0.600*CL	0.26 + 0.600*CL
	tPHL	21.41	0.15 + 0.712*CL	0.25 + 0.705*CL	0.25 + 0.705*CL
	tR	23.76	0.52 + 0.777*CL	0.58 + 0.773*CL	0.58 + 0.773*CL
	tF	31.14	0.49 + 1.024*CL	0.55 + 1.020*CL	0.55 + 1.020*CL
PI to PO	tPLH	17.09	0.24 + 0.564*CL	0.32 + 0.559*CL	0.32 + 0.559*CL
	tPHL	19.38	0.06 + 0.647*CL	0.14 + 0.641*CL	0.14 + 0.641*CL
	tR	22.84	0.59 + 0.743*CL	0.63 + 0.740*CL	0.63 + 0.740*CL
	tF	29.17	0.52 + 0.955*CL	0.53 + 0.955*CL	0.53 + 0.955*CL
PAD to Y	tPLH	2.25	1.68 + 0.020*CL	1.71 + 0.018*CL	1.72 + 0.018*CL
	tPHL	3.32	2.63 + 0.024*CL	2.67 + 0.022*CL	2.70 + 0.021*CL
	tR	1.41	0.33 + 0.035*CL	0.31 + 0.037*CL	0.28 + 0.038*CL
	tF	1.38	0.35 + 0.034*CL	0.35 + 0.034*CL	0.31 + 0.036*CL

*Range1 : CL < 15.00, *Range2 : 15.00 ≦ CL ≦ 30.00, *Range3 : 30.00 < CL