



# **ASPEC Technology, Inc.**

**0.5 Micron**

**Gate Array Products**

**HDA<sup>®</sup> 9000**

**(TSMC SPTM 5.0V)**

**5.0V**

**Macrocell Databook**

**Rev. 1**

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## Chapter 1: Introduction to the 5.0V 0.5 $\mu$ m Products

This databook provides basic technical information on the 5.0V HDA9000 product line, including masterslice statistics, macrocell data sheets, input and output DC characteristics, cell name conventions and Application Notes on Power and Ground rules and clock skew management.

### 1.1 Product Description

HDA9000, based on an advanced array architecture, supports a triple layer metal HCMOS process. The high gate-density of this architecture results in lower on-chip noise, higher chip level performance, and lower component cost. HDA9000 is well-suited for cost-sensitive applications that also demand high circuit performance.

HDA9000 libraries support a de-facto standard set of macrocells. Power buffer and "Multiple Drive" versions of each macrocell are available for handling heavily loaded nets.

### 1.2 CAE Support

HDA9000 supports popular design platforms and environments such as Verilog, Viewlogic, Mentor, and Synopsys for front-end logic design capture and simulation, and Cadence Gate Ensemble and SVR GARDS for back-end place-and-route. For higher simulation accuracy, HDA9000 uses the ADVER2™ delay calculator. Macrocells are characterized using a 4 x 4 delay matrix in which the input slope and output fanout are independently varied. Signal interconnect delay is based on RC Tree analysis.

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## 1.3 Libraries

HDA9000 libraries include the following design elements:

- (a) 5.0V internal macrocells
- (b) 5.0V internal - 5.0V interface and 5.0V internal - 3.3V interface I/O cells
- (c) Megacells
- (d) Compiled cells
- (e) Macrofunctions
- (f) Megafunctions
- (g) Compiled functions

### 1.3.1 Macrocells

Macrocells are lowest level of logic functions e.g., NAND, NOR, FLIP-FLOP, etc., used for logic design. There are 309 internal macrocells and over 700 I/O cells in the standard library. Macrocells are available in 5.0V drive strengths and have many levels of representation -- logic symbol, logic model, timing model, transistor schematic, SPICE netlist, physical layout, and place-and-route model.

### 1.3.2 Megacells

Megacells are large logic functions, such as RAMs and ROMs, which have the same number of levels of representation as macrocells. Improved silicon area efficiency and device performance are the main reasons for using megacells. Megacells are offered in array-cell and full custom implementations.

### 1.3.3 Compiled Cells

Compiled cells are generated by parameter-driven compiler programs. MEMGEN™ generates single-port and dual-port RAMs and ROMs. FIFO Builder™ and Multiplier Builder™ programs generate RAM-based FIFO and multiplier netlists.

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### **1.3.4 Macrofunctions**

Macrofunctions are netlists of logic function which have the complexity of a standard MSI integrated circuits. Macrocells are the logic building blocks. There are forty-three 7400 (TTL) compatible functions in the library.

### **1.3.5 Megafunctions**

Megafunctions are also netlists of logic function, but with the higher logic complexity of a standard LSI circuit. Multipliers, barrel shifters, and 82XX Intel functions, etc., are supported in this library.

### **1.3.6 Compiled Functions**

Compiled functions are generated by parameter-driven programs that use the macrocell library for basic building blocks.

## 1.4 Product Lines

**Table 1.1: HDA9000 Products**

Device	Total Gates	DLM Usable Gates <sup>(1)</sup>	TLM Usable Gates <sup>(1)</sup>	Total I/O Pads	Max I/O
HDA9432	9,612	4,325	6,921	64	48
HDA9842	18,675	8,404	13,446	80	64
HDA9133	30,943	13,924	22,279	96	80
HDA9173	39,930	17,569	28,111	106	90
HDA9223	50,468	22,206	35,529	116	100
HDA9293	69,165	29,741	47,586	132	116
HDA9363	85,169	36,623	58,596	144	128
HDA9463	109,200	46,956	75,130	160	144
HDA9573	136,680	57,406	91,849	176	160
HDA9663	166,500	66,600	106,560	192	176
HDA9783	200,070	78,027	124,844	208	192
HDA9893	235,840	89,619	143,391	224	208
HDA9104	295,500	109,335	174,936	248	232
HDA9134	386,218	139,038	222,462	280	264
HDA9174	488,676	171,037	273,659	312	296
HDA9214	618,016	210,125	336,201	348	332
HDA9254	779,200	257,136	411,418	388	372
HDA9314	997,310	319,139	510,623	436	420
HDA9384	1,253,922	388,716	621,945	486	470
HDA9474	1,540,565	477,575	764,120	536	520
HDA9534	1,791,336	537,401	859,841	576	560

**Note:**

- (1) Usable gates are estimated; the actual number of usable gates is design dependant.
- (2) I/O pads can be used as VDD/VSS pads.
- (3) There are four (4) dedicated VDD/VSS pads for each corner cell in the chip.

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## 1.5 VDD and VSS Rules and Guidelines

There are three types of VDD and VSS in this product family, each with its related bus and pad cells.

1. Core Logic  
IVSS, IVDD
2. Input Buffers  
RVSS, RVDD
3. Output Buffers  
OVSS, OVDD

The number of VSS and VDD pads required for a specific design depends on the following factors:

- Number of input and output buffers
- Number of simultaneous switching inputs
- Number of simultaneous switching outputs
- Number of used gates and number of simultaneous switching gates
- Operating frequency of the design

### 1.5.1 Core Logic VSS Bus and IVSS Pad Allocation Guidelines

The purpose of these guidelines is to ensure that VDD/VSS bounce due to simultaneous gate switching is kept to a minimum. Voltage bounce on the power bus could have a negative impact on gate switching speed, and in an extreme case could even affect the functionality of the macrocells, e.g., flip-flops and latches. Because of variations in package inductance, the number of VDD/VSS pads required for a specific design is a function of the operating frequency of the chip, i.e., designs operating at high frequency should use more VDD/VSS pads.

- VDD Bus width and pad requirement is half that of VSS.
- VDD/VSS Bus and Pads should be distributed evenly in the core and on all sides of the chip.
- At least one (1) IVSS pad should be used on each side of the chip.
- The total number of IVDD pads required is half that of IVSS.

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## 1.5.1 Core Logic VSS Bus and IVSS Pad Allocation Guidelines (cont'd)

The number of IVSS pads required for a design can be calculated from the following expression:

$$\text{Number of IVSS pads} = G \times S \times F \times 2.72 \times (10^{\wedge} - 5)$$

where G = Total number of used gates (k)  
S = % of simultaneous switching gates  
F = Switching frequency in Mhz

## 1.6 Propagation Delays

Interconnect wire-length, temperature and supply voltage are the chief factors affecting propagation delay.

### 1.6.1 Wire Length Loading Estimation

Loading due to interconnect wire-length can be estimated with the following expression. The result is given in terms of number of equivalent standard loads.

$$C_{WL} = C_{fo} \times (0.049 \times \sqrt{A} + 0.48) + 0.079 \times \sqrt{A} + 0.33$$

where  $C_{fo}$  = number of fan-outs in standard load  
 $A$  = area of block size in  $\text{mm}^2$   
 $C_{WL}$  = number of equivalent standard loads due to interconnect

e.g.,  $C_{fo}$  = 7 (standard loads)  
 $A$  = 25  $\text{mm}^2$   
 $C_{WL}$  = 5.8 (standard load)

## 1.6.2 Temperature and Supply Voltage

Fig. 1.1 describes propagation delay correction factor ( $K_T$ ) as a function of on-chip junction temperature ( $T_j$ ), and voltage delay correction factor ( $K_V$ ) as a function of supply voltage ( $V_{DD}$ ). As a result of increasing CMOS power dissipation, ambient and junction temperature are generally not the same. The temperature of the die inside the package (junction temperature,  $T_j$ ), is calculated using chip power dissipation and the Thermal Resistance to Ambient ( $\theta_{ja}$ ) temperature of the package. Information on package thermal performance can be obtained from ASPEC Application Engineers.

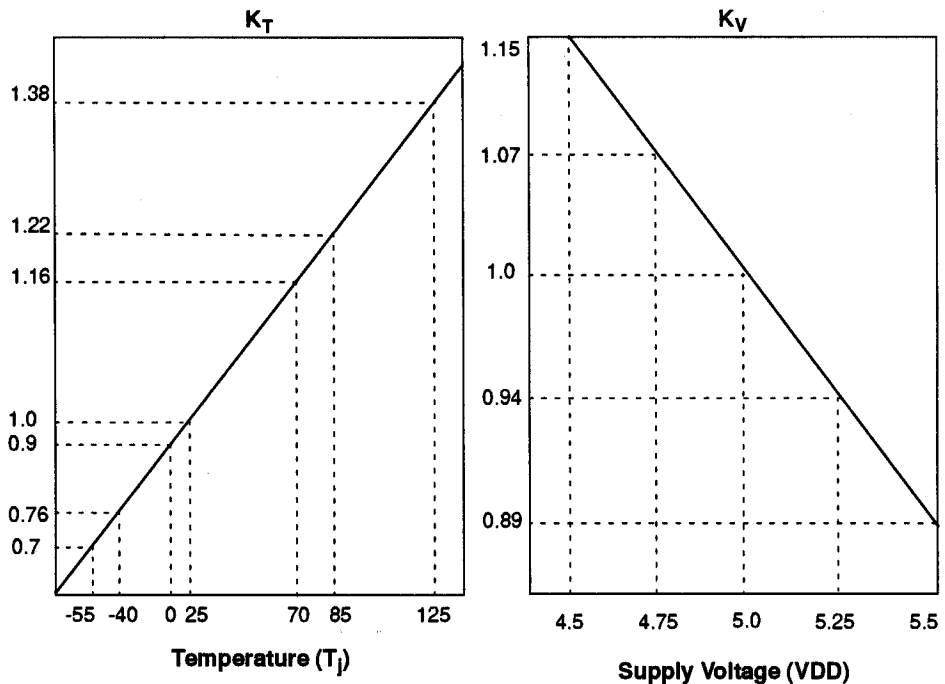


Figure 1.1: Effect of Temperature and Supply Voltage on Propagation Delay



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### 1.6.3 Propagation Delay

A circuit should be designed to operate properly within a given specification level, either commercial, industrial or military. It is recommended that circuits be simulated for Best Case, Nominal Case and Worst Case conditions at each specification level. The following expressions also allow for the effect of process variation on circuit performance.

Worst Case:

$$T_{WC} = K_{PWC} \times K_T \times K_V \times t_{nom} = K_{WC} \times t_{nom}$$

Best Case:

$$T_{BC} = K_{PBC} \times K_T \times K_V \times t_{nom} = K_{BC} \times t_{nom}$$

- $T_{WC}$  = Worst case propagation delay
- $T_{BC}$  = Best case propagation delay
- $t_{nom}$  = nominal propagation delay ( $T_j = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$   
and typical process parameters)
- $K_{PWC}$  = Worst case process correction factor
- $K_{PBC}$  = Best case process correction factor

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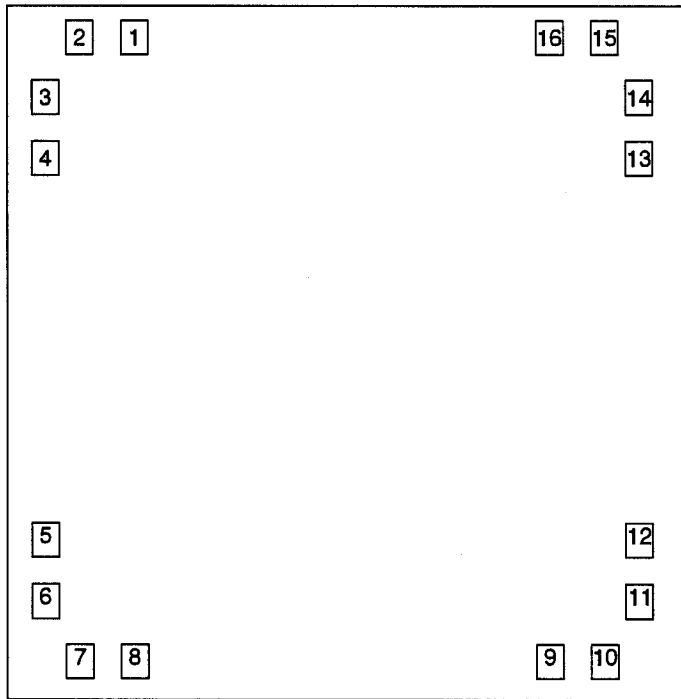
## 1.7 Packages

For package options for HDA9000 gate arrays, please consult your foundry representative.

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## 1.8 Dedicated Corner VSS/VDD Pads

The corner pads shown in Fig. 1.2 are well-suited for double bonding purposes. Pad 1 and Pad 2 can be bonded to the same package pin.



**Fig. 1.2: VDD/VSS Corner Pads**

## Chapter 2.0 DC Characteristics

### 2.1 VDD = 5V ± 10%, junction temperature range -55 to +125°C.

Table 2.1: DC CHARACTERISTICS AT VDD = 5v

Symbol	Parameter	Condition	Min	Typical	Max	Unit
<b>V<sub>IL</sub></b>	Input Low Voltage					
	CMOS				0.3V <sub>DD</sub>	V
	CMOS Schmitt Trigger				1.0	V
	TTL				0.8	V
	TTL Schmitt Trigger				0.8	V
<b>V<sub>IH</sub></b>	Input High Voltage					
	CMOS		0.7V <sub>DD</sub>			V
	CMOS Schmitt Trigger		4.0			V
	TTL		2.0			V
	TTL Schmitt Trigger		2.0			V
<b>I<sub>IH</sub></b>	Input High Current	V <sub>IN</sub> =V <sub>DD</sub>	-10		10	μA
	Input with pull-down	V <sub>IN</sub> =V <sub>DD</sub>	10		180	μA
<b>I<sub>IL</sub></b>	Input Low Current	V <sub>IN</sub> =V <sub>SS</sub>	-10		10	μA
	Input with pull-down	V <sub>IN</sub> =V <sub>SS</sub>	-180		-10	μA
<b>V<sub>OH</sub></b>	Output High Voltage					
	Type B1	I <sub>OH</sub> = -1mA	2.4			V
	Type B2	I <sub>OH</sub> = -2mA	2.4			V
	Type B4	I <sub>OH</sub> = -4mA	2.4			V
	Type B8	I <sub>OH</sub> = -8mA	2.4			V
	Type B12	I <sub>OH</sub> = -12mA	2.4			V
	Type B16	I <sub>OH</sub> = -16mA	2.4			V
	Type B20	I <sub>OH</sub> = -20mA	2.4			V
	Type B24	I <sub>OH</sub> = -24mA	2.4			V
<b>V<sub>OL</sub></b>	Output Low Voltage					
	Type B1	I <sub>OL</sub> = 1mA			0.4	V
	Type B2	I <sub>OL</sub> = 2mA			0.4	V
	Type B4	I <sub>OL</sub> = 4mA			0.4	V
	Type B8	I <sub>OL</sub> = 8mA			0.4	V
	Type B12	I <sub>OL</sub> = 12mA			0.4	V
	Type B16	I <sub>OL</sub> = 16mA			0.4	V
	Type B20	I <sub>OL</sub> = 20mA			0.4	V
	Type B24	I <sub>OL</sub> = 24mA			0.4	V
<b>I<sub>oz</sub></b>	3-State Output Leakage Current	V <sub>OH</sub> =V <sub>SS</sub> or V <sub>DD</sub>	-10		10	μA
<b>I<sub>DD</sub></b>	Quiescent Supply Current	V <sub>IN</sub> =V <sub>SS</sub> or V <sub>DD</sub>			100 <sup>1</sup>	μA

1. Depends on customer design

## 2.2 Absolute Maximum Ratings

**Table 2.2: Maximum Ratings**

	<b>Symbol</b>	<b>Parameter</b>	<b>Rating</b>	<b>Unit</b>
Absolute Maximum Ratings	$V_{DD}$	DC Supply Voltage	-0.3 to 7.0	V
	$V_{IN}$	DC Input Voltage	-0.3 to $V_{DD} + 0.3$	V
	$I_{IN}$	DC Input Current	$\pm 10$	mA
	$T_{STG}$	Storage Temperature	-40 to +125	$^{\circ}C$
Recommended Operating Conditions	$V_{DD}$	DC Supply Voltage	4.5 to 5.5	V
	$T_A$	Commercial Temperature	0 to 70	$^{\circ}C$
	$T_A$	Industrial Temperature	-40 to 85	$^{\circ}C$
	$T_A$	Military Temperature	-55 to 125	$^{\circ}C$

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## Chapter 3.0 5.0V Internal Macrocells

This chapter contains datasheets for 5.0V simple logic cells, multiplexers, decoders, adders, latches and flip-flops. Maximum fanout loading is given for each cell. This figure is the recommended standard load, including wire capacitance.

Tables 3.1 through 3.6 list 5.0V internal macrocells alphabetically by type, with size, input loading, description and the page number where the datasheet may be found.

**Table 3.1: Simple Logic Cells**

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
AD2D2	2	A,B = 1,1	2 Input AND 2X Drive	3-20
AD2D4	3	A,B = 1,1	2 Input AND 4X Drive	3-20
AD2D6	4	A,B = 1,1	2 Input AND 6X Drive	3-20
AD3	2	A,B,C = 1,1,1	3 Input AND 1X Drive	3-22
AD3D3	3	A,B,C = 1,1,1	3 Input AND 3X Drive	3-22
AD3D5	4	A,B,C = 1,1,1	3 Input AND 5X Drive	3-22
AD3D8	7	A,B,C = 2,2,2	3 Input AND 8X Drive	3-22
AD4D2	3	A,B,C,D = 1,1,1,1	4 Input AND 2X Drive	3-26
AD4D4	4	A,B,C,D = 1,1,1,1	4 Input AND 4X Drive	3-26
AD4D6	5	A,B,C,D = 2,2,2,2	4 Input AND 6X Drive	3-26
AD5	3	A,B,C,D,E = 1,1,1,1,1	5 Input AND 1X Drive	3-30
AD5D3	4	A,B,C,D,E = 1,1,1,1,1	5 Input AND 3X Drive	3-30
AD5D6	8	A,B,C,D,E = 2,2,2,2,2	5 Input AND 6X Drive	3-30
AO21	2	A,B,C = 1,1,1	2-AND into 2-NOR 1X Drive	3-34
AO21D2	3	A,B,C = 2,2,2	2-AND into 2-NOR 2X Drive	3-34
AO21D4	4	A,B,C = 1,1,1	2-AND into 2-NOR 4X Drive	3-34
AO21D6	5	A,B,C = 1,1,1	2-AND into 2-NOR 6X Drive	3-34
AO21I	2	A,B,C = 1,1,1	2-AND into 2-OR 1X Drive	3-38
AO21ID3	3	A,B,C = 1,1,1	2-AND into 2-OR 3X Drive	3-38
AO21ID5	4	A,B,C = 1,1,1	2-AND into 2-OR 5X Drive	3-38
AO21ID8	7	A,B,C = 1,1,1	2-AND into 2-OR 8X Drive	3-38
AO211	2	A,B,C,D = 1,1,1,1	2-AND into 3-NOR 1X Drive	3-42
AO211D2	4	A,B,C,D = 2,2,2,2	2-AND into 3-NOR 2X Drive	3-42
AO211D3	4	A,B,C,D = 1,1,1,1	2-AND into 3-NOR 3X Drive	3-42
AO211D7	6	A,B,C,D = 1,1,1,1	2-AND into 3-NOR 7X Drive	3-42
AO22	2	A,B,C,D = 1,1,1,1	2 2-AND into 2-NOR 1X Drive	3-46
AO22D2	4	A,B,C,D = 2,2,2,2	2 2-AND into 2-NOR 2X Drive	3-46
AO22D3	4	A,B,C,D = 1,1,1,1	2 2-AND into 2-NOR 3X Drive	3-46

**Table 3.1: Simple Logic Cells (Continued)**

<b>Cell Names</b>	<b>Size (gates)</b>	<b>Input Loading (In Standard loads)</b>	<b>Description</b>	<b>Page</b>
AO22D7	6	A,B,C,D = 1,1,1,1	2 2-AND into 2-NOR 7X Drive	3 - 46
AO22A	3	A,B,C,D = 1,1,1,1	2-AND and 2-invert-AND into 2-NOR 1X Drive	3 - 50
AO22D2A	5	A,B,C,D = 2,2,1,1	2-AND and 2-invert-AND into 2-NOR 2X Drive	3 - 50
AO222	3	A,B,C,D,E,F = 1,1,1,1,1,1	3 2-AND into 3-NOR 1X Drive	3 - 52
AO222D3	5	A,B,C,D,E,F = 1,1,1,1,1,1	3 2-AND into 3-NOR with 3X Drive	3 - 52
AO222D7	7	A,B,C,D,E,F = 1,1,1,1,1,1,1	3 2-AND into 3-NOR with 7X Drive	3 - 52
AO222A	3	A,B,C,D,E,F = 1,1,1,1,1,1	Inverting 2-of-3 majority 1X Drive	3 - 56
AO33	3	A,B,C,D,E,F = 1,1,1,1,1,1	2 3-AND into 2-NOR 1X Drive	3 - 58
AO33D2	5	A,B,C,D,E,F = 1,1,1,1,1,1	2 3-AND into 2-NOR 2X Drive	3 - 58
AO33D3	5	A,B,C,D,E,F = 1,1,1,1,1,1	2 3-AND into 2-NOR 3X Drive	3 - 58
AO33D7	7	A,B,C,D,E,F = 1,1,1,1,1,1,1	2 3-AND into 2-NOR 7X Drive	3 - 58
AO333	5	A,B,C,D,E,F,G,H,I = 1,1,1,1,1,1,1,1,1	3 3-AND into 3-NOR 1X Drive	3 - 62
AO333D2	6	A,B,C,D,E,F,G,H,I = 1,1,1,1,1,1,1,1,1	3 3-AND into 3-NOR 2X Drive	3 - 62
DL1D2	4	A = 1	1 ns non-inverting delay cell, 2X Drive	3 - 66
DL1D4	5	A = 1	1 ns non-inverting delay cell, 4X Drive	3 - 66
DL2D2	7	A = 1	2 ns non-inverting delay cell, 2X Drive	3 - 68
DL2D4	8	A = 1	2 ns non-inverting delay cell, 4X Drive	3 - 68
DL5D2	14	A = 1	5 ns non-inverting delay cell, 2X Drive	3 - 70



**Table 3.1: Simple Logic Cells (Continued)**

Cell Names	Size (gates)	Input Loading (In Standard loads)	Description	Page
DL5D4	15	A = 1	5 ns non-inverting delay cell, 4X Drive	3-70
IV	1	A = 1	Inverter 1X Drive	3-72
IVD2	1	A = 2	Inverter 2X Drive	3-72
IVD3	2	A = 3	Inverter 3X Drive	3-72
IVD4	2	A = 4	Inverter 4X Drive	3-72
IVD6	3	A = 6	Inverter 6X Drive	3-74
IVD8	4	A = 8	Inverter 8X Drive	3-74
IVD12	6	A = 12	Inverter 12X Drive	3-76
IVD16	8	A = 16	Inverter 16X Drive	3-76
IVA	1	A = 1.5	Inverter with 2X P, 1X N Transistors	3-78
IVD2A	2	A = 3	Inverter with 4X P, 2X N Transistors	3-78
IVD3A	3	A = 4.5	Inverter with 6X P, 3X N Transistors	3-78
IVD4A	4	A = 6	Inverter with 8X P, 4X N Transistors	3-78
IVD8A	8	A = 8	Inverter with 16X P, 8X N Transistors	3-80
IVD12A	12	A = 18	Inverter with 24X P, 12X N Transistors	3-80
IVCD11	1	A = 1	1X Inverter into Inverter	3-82
IVCD13	2	A = 1	1X Inverter into Inverter	3-82
IVCD22	2	A = 2	2X Inverter into Inverter	3-84
IVCD26	4	A = 2	2X Inverter into Inverter	3-84
IVCD39	6	A = 3	3X Inverter into 9X Inverter	3-86
IVCD44	4	A = 4	4X Inverter into 4X Inverter	3-88
IVCD11A	2	A = 2.5	Buffer with 1X Inverting and 1X Non-inverting Outputs	3-90
IVCD22A	3	A = 3.5	Buffer with 2X inverting and 2X Non-inverting Outputs	3-90
IVCD44A	5	A = 5.5	Buffer with 4X Inverting and 4X Non-inverting Outputs	3-90

**Table 3.1: Simple Logic Cells (Continued)**

Cell Names	Size (gates)	Input Loading (In Standard loads)	Description	Page
IVCD88A	9	A = 10	Buffer with 8X Inverting and 8X Non-inverting Outputs	3-90
IVT	3	A,E = 1,1,5	Inverting 3-State Buffer, Enable High, 1X Drive	3-92
IVTD2	4	A,E = 1,2	Inverting 3-State Buffer, Enable High, 2X Drive	3-92
IVTD5	5	A,E = 1,2	Inverting 3-State Buffer, Enable High, 5X Drive	3-92
IVTD9	7	A,E = 1,2	Inverting 3-State Buffer, Enable High, 9X Drive	3-92
ND2	1	A,B = 1,1	2 Input NAND 1X Drive	3-96
ND2D2	2	A,B = 2,2	2 Input NAND 2X Drive	3-96
ND2D5	4	A,B = 1,1	2 Input NAND 5X Drive	3-96
ND2D7	5	A,B = 1,1	2 Input NAND 7X Drive	3-96
ND3	2	A,B,C = 1,1,1	3 Input NAND 1X Drive	3-100
ND3D2	3	A,B,C = 2,2,2	3 Input NAND 2X Drive	3-100
ND3D4	4	A,B,C = 1,1,1	3 Input NAND 4X Drive	3-100
ND3D6	5	A,B,C = 1,1,1	3 Input NAND 6X Drive	3-100
ND4	2	A,B,C,D = 1,1,1,1	4 Input NAND 1X Drive	3-104
ND4D2	4	A,B,C,D = 2,2,2,2	4 Input NAND 2X Drive	3-104
ND4D5	5	A,B,C,D = 1,1,1,1	4 Input NAND 5X Drive	3-104
ND4D7	6	A,B,C,D = 1,1,1,1	4 Input NAND 7X Drive	3-104
ND5	3	A,B,C,D,E = 1,1,1,1,1	5 Input NAND 1X Drive	3-108
ND5D2	5	A,B,C,D,E = 2,2,2,2,2	5 Input NAND 2X Drive	3-108
ND5D4	5	A,B,C,D,E = 1,1,1,1,1	5 Input NAND 4X Drive	3-108
ND5D6	6	A,B,C,D,E = 1,1,1,1,1	5 Input NAND 6X Drive	3-108
ND6	5	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NAND 1X Drive	3-112
ND6D2	5	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NAND 2X Drive	3-112

**Table 3.1: Simple Logic Cells (Continued)**

<b>Cell Names</b>	<b>Size (gates)</b>	<b>Input Loading (in Standard loads)</b>	<b>Description</b>	<b>Page</b>
ND6D4	6	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NAND 4x Drive	3 - 112
ND6D8	9	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NAND 8x Drive	3 - 112
ND8	6	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NAND 1X Drive	3 - 116
ND8D2	6	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NAND 2X Drive	3 - 116
ND8D4	7	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NAND 4X Drive	3 - 116
ND8D8	10	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NAND 8X Drive	3 - 116
NID8	5	A = 2	Non-Inverting Buffer 8X Drive	3 - 122
NID12	7	A = 2	Non-Inverting Buffer 12X Drive	3 - 122
NID16	9	A = 2	Non-Inverting Buffer 16X Drive	3 - 122
NIT	2	A,E = 1,1.5	Non-Inverting Tri-State Buffer, Enable High, 1X Drive	3 - 124
NITD2	3	A,E = 1,2	Non-Inverting Tri-State Buffer, Enable High, 2X Drive	3 - 124
NITD5	5	A = 2	Non-Inverting Tri-State Buffer, Enable High, 5X Drive	3 - 124
NITD9	7	A = 2	Non-Inverting Tri-State Buffer, Enable High, 9X Drive	3 - 124
NR2	1	A,B = 1,1	2 Input NOR 1X Drive	3 - 128
NR2D2	2	A,B = 2,2	2 Input NOR 2X Drive	3 - 128
NR2D7	5	A,B = 1,1	2 Input NOR 7X Drive	3 - 128
NR3	2	A,B,C = 1,1,1	3 Input NOR 1X Drive	3 - 132
NR3D2	3	A,B,C = 2,2,2	3 Input NOR 2X Drive	3 - 132
NR3D3	4	A,B,C = 1,1,1	3 Input NOR 3X Drive	3 - 132
NR3D7	6	A,B,C = 1,1,1	3 Input NOR 7X Drive	3 - 132
NR4	2	A,B,C,D = 1,1,1,1	4 Input NOR 1X Drive	3 - 136
NR4D2	4	A,B,C,D = 1,1,1,1	4 Input NOR 2X Drive	3 - 136
NR4D6	6	A,B,C,D = 1,1,1,1	4 Input NOR 6X Drive	3 - 136

**Table 3.1: Simple Logic Cells (Continued)**

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
NR5	4	A,B,C,D,E = 1,1,1,1,1	5 Input NOR 1X Drive	3 - 140
NR5D2	5	A,B,C,D,E = 1,1,1,1,1	5 Input NOR 2X Drive	3 - 140
NR5D4	6	A,B,C,D,E = 1,1,1,1,1	5 Input NOR 5X Drive	3 - 140
NR5D6	7	A,B,C,D,E = 1,1,1,1,1	5 Input NOR 7X Drive	3 - 140
NR6	5	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NOR 1X Drive	3 - 144
NR6D2	6	A,B,C,D,E,F = 1,1,1,1,1,1	6 Input NOR 2x Drive	3 - 144
NR8	6	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NOR 1X Drive	3 - 148
NR8D2	7	A,B,C,D,E,F,G,H = 1,1,1,1,1,1,1,1	8 Input NOR 2X Drive	3 - 148
OA21	2	A,B,C = 1,1,1	2-OR into 2-NAND 1X Drive	3 - 152
OA21D2	3	A,B,C = 2,2,2	2-OR into 2-NAND 2X Drive	3 - 152
OA21D4	4	A,B,C = 1,1,1	2-OR into 2-NAND 4X Drive	3 - 152
OA21D6	5	A,B,C = 1,1,1	2-OR into 2-NAND 6X Drive	3 - 152
OA21I	2	A,B,C = 1,1,1	2-OR into 2-AND 1X Drive	3 - 156
OA21ID3	3	A,B,C = 1,1,1	2-OR into 2-AND 3X Drive	3 - 156
OA21ID5	4	A,B,C = 1,1,1	2-OR into 2-AND 5X Drive	3 - 156
OA21ID8	7	A,B,C = 2,2,2	2-OR into 2-AND 8X Drive	3 - 156
OA211	2	A,B,C,D = 1,1,1,1	2-OR into 3-NAND 1X Drive	3 - 160
OA211D2	4	A,B,C,D = 2,2,2,2	2-OR into 3-NAND 2X Drive	3 - 160
OA211D3	4	A,B,C,D = 1,1,1,1	2-OR into 3-NAND 3X Drive	3 - 160
OA211D7	6	A,B,C,D = 1,1,1,1	2-OR into 3-NAND 7X Drive	3 - 160
OA22	2	A,B,C = 1,1,1	2 2-OR into 2-NAND 1X Drive	3 - 164
OA22D2	4	A,B,C,D = 2,2,2,2	2 2-OR into 2-NAND 2X Drive	3 - 164
OA22D3	4	A,B,C,D = 1,1,1,1	2 2-OR into 2-NAND 3X Drive	3 - 164
OA22D7	6	A,B,C,D = 1,1,1,1	2 2-OR into 2-NAND 7X Drive	3 - 164
OA22A	3	A,B,C,D = 1,1,1,1	2 2-OR and 12-invert-OR into 2-NAND 1X Drive	3 - 168
OA22D2A	4	A,B,C,D = 2,2,1,1	2-OR and 2-invert-OR into 2-NAND 2X Drive	3 - 168

**Table 3.1: Simple Logic Cells (Continued)**

<b>Cell Names</b>	<b>Size (gates)</b>	<b>Input Loading (In Standard loads)</b>	<b>Description</b>	<b>Page</b>
OR2D2	2	A,B = 1,1	2 Input OR 2X Drive	3-170
OR2D4	3	A,B = 1,1	2 Input OR 4X Drive	3-170
OR2D8	6	A,B = 2,2	2 Input OR 8X Drive	3-170
OR3	2	A,B,C = 1,1,1	3 Input OR 1X Drive	3-172
OR3D3	3	A,B,C = 1,1,1	3 Input OR 3X Drive	3-172
OR3D6	6	A,B,C = 2,2,2	3 Input OR 6X Drive	3-172
OR3D8	7	A,B,C = 2,2,2	3 Input OR 8X Drive	3-172
OR4	3	A,B,C,D = 1,1,1,1	4 Input OR 1X Drive	3-176
OR4D2	4	A,B,C,D = 1,1,1,1	4 Input OR 2X Drive	3-176
OR4D5	6	A,B,C,D = 1,1,1,1	4 Input OR 5X Drive	3-176
OR4D7	7	A,B,C,D = 1,1,1,1	4 Input OR 7X Drive	3-176
OR5	4	A,B,C,D,E = 1,1,1,1,1	5 Input OR 1X Drive	3-180
OR5D2	5	A,B,C,D,E = 1,1,1,1,1	5 Input OR 2X Drive	3-180
XN2	3	A,B = 1,2	2 Input Exclusive NOR 1X Drive	3-182
XN2D2	4	A,B = 1,2	2 Input Exclusive NOR 2X Drive	3-182
XN2D3	4	A,B = 1,2	2 Input Exclusive NOR 3X Drive	3-182
XN2D5	5	A,B = 1,2	2 Input Exclusive NOR 5X Drive	3-182
XN3	5	A,B,C = 2,1,2	3 Input Exclusive NOR 1X Drive	3-186
XN3D3	6	A,B,C = 2,1,2	3 Input Exclusive NOR 3X Drive	3-186
XO2	3	A,B = 1,2	2 Input Exclusive OR 1X Drive	3-188
XO2D2	4	A,B = 1,2	2 Input Exclusive OR 2X Drive	3-188
XO2D3	4	A,B = 1,2	2 Input Exclusive OR 3X Drive	3-188
XO2D5	5	A,B = 1,2	2 Input Exclusive OR 5X Drive	3-188
XO3	5	A,B,C = 2,1,2	3 Input Exclusive OR 1X Drive	3-192
XO3D3	6	A,B,C = 2,1,2	3 Input Exclusive OR 3X Drive	3-192

**Table 3.2: Multiplexers and Decoders**

Cell Names	Size (gates)	Input Loading (In Standard loads)	Description	Page
DC4	7	S0,S1 = 3,3	2 > 4 Non-Inverting Decoder 1X Drive	3-194
DC4D2	9	S0,S1 = 3,3	2 > 4 Non-Inverting Decoder 2X Drive	3-194
DC4D4	13	S0,S1 = 3,3	2 > 4 Non-Inverting Decoder 4X Drive	3-194
DC4I	5	S0,S1 = 3,3	2 > 4 Inverting Decoder 1X Drive	3-198
DC4ID2	9	S0,S1 = 3,3	2 > 4 Inverting Decoder 2X Drive	3-198
DC4ID4	13	S0,S1 = 3,3	2 > 4 Inverting Decoder 4X Drive	3-198
MX2	3	D0,D1,S = 1,1,2	2 > 1 Non-Inverting Mux 1X Drive	3-202
MX2D3	4	D0,D1,S = 1,1,2	2 > 1 Non-Inverting Mux 3X Drive	3-202
MX2X4	11	D00,D10,D01,D11,D02, D12,D03,D13,S = 1,1,1,1,1,1,1,1	4-Bit 2 > 1 Non-Inverting Mux 1X Drive	3-204
MX2D2X4	13	D00,D10,D01,D11,D02, D12,D03,D13,S = 1,1,1,1,1,1,1,4	4-Bit 2 > 1 Non-Inverting Mux 2X Drive	3-204
MX2I	2	D0,D1,S = 3,3,2	2 > 1 Inverting Mux 1X Drive	3-210
MX2ID2	3	D0,D1,S = 4,4,2	2 > 1 Inverting Mux 2X Drive	3-210
MX2ID3	3	D0,D1,S = 5,5,2	2 > 1 Inverting Mux 3X Drive	3-210
MX2IX4	7	D00,D10,D01,D11,D02, D12,D03,D13,S = 3,3,3,3,3,3,3,1	4-Bit 2 > 1 Inverting Mux 1X Drive	3-214
MX2ID2X4	9	D00,D10,D01,D11,D02, D12,D03,D13,S = 4,4,4,4,4,4,4,1	4-Bit 2 > 1 Inverting Mux 2X Drive	3-214
MX2IA	2	D0,D1,S,SN = 3,3,1,1	2 > 1 Inverting Mux 1X Drive, separate S and SN inputs	3-220
MX2ID2A	2	D0,D1,S, SN = 4,4,1,1	2 > 1 Inverting Mux 2X Drive, separate S and SN inputs	3-220
MX2ID4A	3	D0,D1,S = 6,6,1,1	2 > 1 Inverting Mux 4X Drive, separate S and SN inputs	3-220

**Table 3.2: Multiplexers and Decoders**

<b>Cell Names</b>	<b>Size (gates)</b>	<b>Input Loading (In Standard loads)</b>	<b>Description</b>	<b>Page</b>
MX3I	4	D0,D1,D2,S0,S1 = 3,3,1,2,2	3 > 1 Inverting Mux 1X Drive	3-224
MX3ID2	4	D0,D1,D2,S0,S1 = 6,6,4,2,2	3 > 1 Inverting Mux 2X Drive	3-224
MX3ID4	6	D0,D1,D2,S0,S1 = 3,3,6,,2,2	3 > 1 Inverting Mux 4X Drive	3-224
MX4	6	D0,D1,D2,D3,S0,S1 = 3,3,3,3,3,2	4 > 1 Non-inverting Mux 1X Drive	3-228
MX4D2	6	D0,D1,D2,D3,S0,S1 = 3,3,3,3,3,2	4 > 1 Non-inverting Mux 2X Drive	3-228
MX8	12	D0,D1,D2,D3,D4,D5,D6, D7,S0,S1,S2 = 3,3,3,3,3,3,3,1,3,2	8 > 1 Non-inverting Mux 1X Drive	3-232
MX8D2	12	D0,D1,D2,D3,D4,D5,D6, D7,D8,S0,S1,S2 = 3,3,3,3,3,3,3,3,1,3,2	8 > 1 Non-inverting Mux 2X Drive	3-232

**Table 3.3: Adders**

<b>Cell Names</b>	<b>Size (gates)</b>	<b>Input Loading (In Standard loads)</b>	<b>Description</b>	<b>Page</b>
FA	7	C1,A,B = 2,1,2	Full Adder 1X Drive	3-296
FAD2	8	C1,A,B = 2,1,2	Full Adder 2X Drive	3-296
FAD4	10	C1,A,B = 2,1,2	Full Adder 4X Drive	3-296
FAD6	12	C1,A,B = 2,1,2	Full Adder 6X Drive	3-296
HA	5	A,B = 2,3	Half Adder 1X Drive	3-302
HAD2	6	A,B = 2,3	Half Adder 2X Drive	3-302
HAD4	8	A,B = 2,3	Half Adder 4X Drive	3-302

**Table 3.4: Miscellaneous Cells**

<b>Cell Names</b>	<b>Size (gates)</b>	<b>Input Loading (In Standard loads)</b>	<b>Description</b>	<b>Page</b>
Busholder	0	2	Busholder	3-480



**Table 3. 5: Latches**

Cell Names	Size (gates)	Input Loading (In Standard loads)	Description	Page
LD1	4	D,G = 3,1	D-Latch Active High Gate, 1X Drive	3-238
LD1D2	5	D,G = 3,1	D-Latch Active High Gate, 2X Drive	3-238
LD1D2Q	4	D,G = 3,1	D-Latch Active High Gate, Q Output Only, 2X Drive	3-242
LD1D4Q	5	D,G = 3,1	D-Latch Active High Gate, Q Output Only, 4X Drive	3-242
LD1A	5	D,G,E = 3,1,1.5	D-Latch Active High Gate, 3-State, 1X Drive	3-244
LD1B	4	D,WR,WRN,RD = 3,1,1,1.5	D-Latch, 3-State, with separate WR, WRN, commonly known as RAM1	3-246
LD1S	7	D,G,SI,SG = 1,2,1,2	D-Latch Active High Gate with Scan, 1X Drive	3-352
LD1SD2	8	D,G,SI,SG = 1,2,1,2	D-Latch Active High Gate with Scan, 2x Drive	3-252
LD1X4	13	D0,D1,D2,D3,G = 3,3,3,3,1	4-Bit D-Latch Active High Gate, 1X Drive	3-256
LD2	5	D,G,RN = 3,1,1	D-Latch Active High Gate with Reset, 1X Drive	3-260
LD2Q	4	D,G,RN = 3,1,1	D-Latch Active High Gate with Reset, Q Output Only, 1X Drive	3-262
LD2D3Q	5	D,G,RN = 3,1,1	D-Latch Active High Gate with Reset, Q Output Only, 3X Drive	3-262
LD4	6	D,G,RN,SN = 3,1,1,2	D-Latch Active High Gate with Set, Reset, 1X Drive	3-266
LD4D2Q	6	D,G,RN,SN = 3,1,1,2	D-Latch Active High Gate with Set, Reset, Q Output Only, 2X Drive	3-270
LD4D4Q	7	D,G,RN,SN = 3,1,1,2	D-Latch Active High Gate with Set, Reset, Q Output Only, 4X Drive	3-270
LD5	4	D,GN = 3,1	D-Latch Active Low Gate, 1X Drive	3-274
LD5D2	5	D,GN = 3,1	D-Latch Active Low Gate, 2X Drive	3-274
LD5D2Q	4	D,GN = 3,1	D-Latch Active Low Gate, Q Output Only, 2X Drive	3-278
LD5D4Q	5	D,GN = 3,1	D-Latch Active Low Gate, Q Output Only, 4X Drive	3-278

**Table 3.3: Adders**

Cell Names	Size (gates)	Input Loading (In Standard loads)	Description	Page
FA	7	CI,A,B = 2,1,2	Full Adder 1X Drive	3-296
FAD2	8	CI,A,B = 2,1,2	Full Adder 2X Drive	3-296
FAD4	10	CI,A,B = 2,1,2	Full Adder 4X Drive	3-296
FAD6	12	CI,A,B = 2,1,2	Full Adder 6X Drive	3-296
HA	5	A,B = 2,3	Half Adder 1X Drive	3-302
HAD2	6	A,B = 2,3	Half Adder 2X Drive	3-302
HAD4	8	A,B = 2,3	Half Adder 4X Drive	3-302

**Table 3.4: Miscellaneous Cells**

Cell Names	Size (gates)	Input Loading (In Standard loads)	Description	Page
Busholder	0	2	Busholder	3-480

**Table 3. 5: Latches**

Cell Names	Size (gates)	Input Loading (In Standard loads)	Description	Page
LD1	4	D,G = 3,1	D-Latch Active High Gate, 1X Drive	3-238
LD1D2	5	D,G = 3,1	D-Latch Active High Gate, 2X Drive	3-238
LD1D2Q	4	D,G = 3,1	D-Latch Active High Gate, Q Output Only, 2X Drive	3-242
LD1D4Q	5	D,G = 3,1	D-Latch Active High Gate, Q Output Only, 4X Drive	3-242
LD1A	5	D,G,E = 3,1,1.5	D-Latch Active High Gate, 3-State, 1X Drive	3-244
LD1B	4	D,WR,WRN,RD = 3,1,1,1.5	D-Latch, 3-State, with separate WR, WRN, commonly known as RAM1	3-246
LD1S	7	D,G,SI,SG = 1,2,1,2	D-Latch Active High Gate with Scan, 1X Drive	3-352
LD1SD2	8	D,G,SI,SG = 1,2,1,2	D-Latch Active High Gate with Scan, 2x Drive	3-252
LD1X4	13	D0,D1,D2,D3,G = 3,3,3,3,1	4-Bit D-Latch Active High Gate, 1X Drive	3-256
LD2	5	D,G,RN = 3,1,1	D-Latch Active High Gate with Reset, 1X Drive	3-260
LD2Q	4	D,G,RN = 3,1,1	D-Latch Active High Gate with Reset, Q Output Only, 1X Drive	3-262
LD2D3Q	5	D,G,RN = 3,1,1	D-Latch Active High Gate with Reset, Q Output Only, 3X Drive	3-262
LD4	6	D,G,RN,SN = 3,1,1,2	D-Latch Active High Gate with Set, Reset, 1X Drive	3-266
LD4D2Q	6	D,G,RN,SN = 3,1,1,2	D-Latch Active High Gate with Set, Reset, Q Output Only, 2X Drive	3-270
LD4D4Q	7	D,G,RN,SN = 3,1,1,2	D-Latch Active High Gate with Set, Reset, Q Output Only, 4X Drive	3-270
LD5	4	D,GN = 3,1	D-Latch Active Low Gate, 1X Drive	3-274
LD5D2	5	D,GN = 3,1	D-Latch Active Low Gate, 2X Drive	3-274
LD5D2Q	4	D,GN = 3,1	D-Latch Active Low Gate, Q Output Only, 2X Drive	3-278
LD5D4Q	5	D,GN = 3,1	D-Latch Active Low Gate, Q Output Only, 4X Drive	3-278

**Table 3. 5: Latches**

<b>Cell Names</b>	<b>Size (gates)</b>	<b>Input Loading (In Standard loads)</b>	<b>Description</b>	<b>Page</b>
LD5X4	13	D0,D1,D2,D3,G = 3,3,3,3,1	4-Bit D-Latch Active Low Gate, 1X Drive	3-280
LD6	5	D,GN,RN = 3,1,1	D-Latch Active Low Gate with Reset,1X Drive	3-284
LD6D2	6	D,GN,RN = 3,1,1	D-Latch Active Low Gate with Reset,2X Drive	3-284
LD6Q	4	D,GN,RN = 3,1,1	D-Latch Active Low Gate with Reset, Q Output Only, 1X Drive	3-288
LD6D3Q	5	D,GN,RN = 3,1,1	D-Latch Active Low Gate with Reset, Q Output Only, 3X Drive	3-288
LS1	4	SN1,SN2,SN,RN,RN1, RN2 = 1,1,1,1,1,1	SR Latch with separate Gate inputs, 1X Drive	3-292
LS1D3	8	SN1,SN2,SN,RN,RN1, RN2 = 1,1,1,1,1,1	SR Latch with separate Gate inputs,3X Drive	3-292

**Table 3.6: Flip-Flops**

Cell Names	Size (gates)	Input Loading (In Standard loads)	Description	Page
FD1	6	D,CK = 3,1	D Flip-Flop, Positive Edge Trigger, 1X Drive	3-306
FD1D2	7	D,CK = 3,1	D Flip-Flop, Positive Edge Trigger, 2X Drive	3-306
FD1D2Q	6	D,CK = 3,1	D Flip-Flop, Positive Edge Trigger, Q Output Only, 2X Drive	3-308
FD1D4Q	7	D,CK = 3,1	D Flip-Flop, Positive Edge Trigger, Q Output Only, 4X Drive	3-308
FD1S	9	D,TI,TE,CK = 1,1,2,1	D Flip-Flop with Scan, Positive Edge Trigger, 1X Drive	3-310
FD1SD2	10	D,TI,TE,CK = 1,1,2,1	D Flip-Flop with Scan, Positive Edge Trigger, 2X Drive	3-310
FD1SD2Q	9	D,TI,TE,CK = 1,1,2,1	D Flip-Flop with Scan, Positive Edge Trigger, Q Output Only, 2X Drive	3-314
FD1SD4Q	10	D,TI,TE,CK = 1,1,2,1	D Flip-Flop with Scan, Positive Edge Trigger, Q Output Only, 4X Drive	3-314
FD1X4	21	D0,D1,D2,D3,CK = 3,3,3,3,1	4-Bit D Flip-Flop, Positive Edge Trigger, 1X Drive	3-316
FD1D2X4Q	24	D0,D1,D2,D3,CK = 3,3,3,3,1	4-Bit D Flip-Flop, Positive Edge Trigger, Q Output Only, 2X Drive	3-320
FD1D4X4Q	28	D0,D1,D2,D3,CK = 3,3,3,3,1	4-Bit D Flip-Flop, Positive Edge Trigger, Q Output Only, 4X Drive	3-320
FD2	7	D,CK,RN = 3,1,2	D Flip-Flop with Reset, Positive Edge Trigger, 1X Drive	3-324
FD2D2	8	D,CK,RN = 3,1,2	D Flip-Flop with Reset, Positive Edge Trigger, 2X Drive	3-324
FD2D2Q	7	D,CK,RN = 3,1,2	D Flip-Flop with Reset, Positive Edge Trigger, Q Output Only, 2X Drive	3-328
FD2D4Q	8	D,CK,RN = 3,1,2	D Flip-Flop with Reset, Positive Edge Trigger, Q Output Only, 4X Drive	3-328
FD2S	10	D,TI,TE,CK,RN = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Positive Edge Trigger, 1X Drive	3-330
FD2SD2	11	D,TI,TE,CK,RN = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Positive Edge Trigger, 2X Drive	3-330

**Table 3.6: Flip-Flops (Continued)**

Cell Names	Size (gates)	Input Loading (In Standard loads)	Description	Page
FD2SD2Q	10	D,CK,RN, TI, TE = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Positive Edge Trigger, Q Output Only, 2X Drive	3-334
FD2SD4Q	11	D,CK,RN, TI, TE = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Positive Edge Trigger, Q Output Only, 4X Drive	3-334
FD2X4	25	D0,D1,D2,D3,CK,RN = 3,3,3,3,3,8	4-Bit D Flip-Flop with Reset, Positive Edge Trigger, 1X Drive	3-338
FD2D2X4Q	28	D0,D1,D2,D3,CK,RN = 3,3,3,3,1,8	4-Bit D Flip-Flop with Reset, Positive Edge Trigger, Q Output Only, 2X Drive	3-342
FD2D4X4Q	32	D0,D1,D2,D3,CK,RN = 3,3,3,3,1,8	4-Bit D Flip-Flop with Reset, Positive Edge Trigger, Q Output Only, 4X Drive	3-342
FD3	7	D,CK,SN = 3,1,2	D Flip-Flop with Set, Positive Edge Trigger, 1X Drive	3-348
FD3D2	8	D,CK,SN = 3,1,2	D Flip-Flop with Set, Positive Edge Trigger, 2X Drive	3-348
FD3S	10	D,TI,TE,CK,SN = 1,1,2,1,2	D Flip-Flop with Set, Scan, Positive Edge Trigger, 1X Drive	3-352
FD3SD2	11	D,TI,TE,CK,SN = 1,1,2,1,2	D Flip-Flop with Set, Scan, Positive Edge Trigger, 2X Drive	3-352
FD4	8	D,CK,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset, Positive Edge Trigger, 1X Drive	3-356
FD4D2	9	D,CK,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset, Positive Edge Trigger, 2X Drive	3-356
FD4D2Q	8	D,CK,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset, Positive Edge Trigger, Q Output Only, 2X Drive	3-360
FD4D4Q	9	D,CK,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset, Positive Edge Trigger, Q Output Only, 4X Drive	3-360
FD4S	11	D,TI,TE,CK,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, 1X Drive	3-364
FD4SD2	12	D,TI,TE,CK,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, 2X Drive	3-364

**Table 3.6: Flip-Flops (Continued)**

Cell Names	Size (gates)	Input Loading (In Standard loads)	Description	Page
FD4SD2Q	11	D,TI,TE,CK,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, Q Output On ly, 2X Drive	3-370
FD4SD4Q	12	D,TI,TE,CK,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, Q Output On ly, 4X Drive	3-370
FD4D2X4Q	32	DO,D1,D2,D3,CK,RN, SN = 3,3,3,3,1,8,8	4-Bit D Flip-Flop with Set and Reset, Positive Edge Trigger, Q Output Only, 2X Drive	3-374
FD4D4X4Q	36	DO,D1,D2,D3,CK,RN, SN = 3,3,3,3,1,8,8	4-Bit D Flip-Flop with Set and Reset, Positive Edge Trigger, Q Output Only, 4X Drive	3-374
FD5	6	D,CKN = 3,1	D Flip-Flop, Negative Edge Trigger, 1X Drive	3-380
FD5D2	7	D,CKN = 3,1	D Flip-Flop, Negative Edge Trigger, 2X Drive	3-380
FD5D2Q	6	D,CKN = 3,1	D Flip-Flop, Negative Edge Trigger, Q Output Only, 2X Drive	3-384
FD5D4Q	7	D,CKN = 3,1	D Flip-Flop, Negative Edge Trigger, Q Output Only, 4X Drive	3-384
FD5SD2Q	9	D,CKN,TI,TE = 1,1,1,2	D Flip-Flop, Scan, Negative Edge Trigger, Q Output Only, 2X Drive	3-386
FD5SD4Q	10	D,CKN,TI,TE = 1,1,1,2	D Flip-Flop, Scan, Negative Edge Trigger, Q Output Only, 4X Drive	3-386
FD5X4	21	D0, D1, D2, D3, CKN = 3, 3, 3, 3, 1	4-Bit Flip-Flop with Negative Edge Trigger	3-390
FD5D2X4Q	24	D0, D1, D2, D3, CKN = 3,3,3,3,1	4-Bit Flip-Flop with Negative Edge Trigger, Q Output Only, 2X Drive	3-394
FD5D4X4Q	28	D0, D1, D2, D3, CKN = 3,3,3,3,1	4-Bit Flip-Flop with Negative Edge Trigger, Q Output Only, 4X Drive	3-394
FD6	7	D,CKN,RN = 3,1,2	D Flip-Flop with Reset, Negative Edge Trigger, 1X Drive	3-398
FD6D2	8	D,CKN,RN = 3,1,2	D Flip-Flop with Reset, Negative Edge Trigger, 2X Drive	3-398
FD6D2Q	7	D,CKN,RN = 3,1,2	D Flip-Flop with Reset, Negative Edge Trigger, Q Output Only, 2X Drive	3-402
FD6D4Q	8	D,CKN,RN = 3,1,2	D Flip-Flop with Reset, Negative Edge Trigger, Q Output Only, 4X Drive	3-402

**Table 3.6: Flip-Flops (Continued)**

Cell Names	Size (gates)	Input Loading (In Standard loads)	Description	Page
FD6SD2Q	10	D,CKN,RN,TI,TE = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Negative Edge Trigger, Q Output Only, 2X Drive	3-406
FD6SD4Q	11	D,CKN,RN,TI,TE = 1,1,2,1,2	D Flip-Flop with Reset, Scan, Negative Edge Trigger, Q Output Only, 4X Drive	3-406
FD6D2X4Q	28	D0, D1, D2, D3, CKN, RN = 3,3,3,3,1, 8	4-Bit D Flip-Flop with Reset, Negative Edge Trigger, Q Output Only, 2X Drive	3-410
FD6D4X4Q	32	D0, D1, D2, D3, CKN, RN = 3,3,3,3,1, 8	4-Bit D Flip-Flop with Reset, Negative Edge Trigger, Q Output Only, 4X Drive	3-410
FD7	7	D,CKN,SN = 3,1,2	D Flip-Flop with Set, Negative Edge Trigger, 1X Drive	3-416
FD7D2	8	D,CKN,SN = 3,1,2	D Flip-Flop with Set, Negative Edge Trigger, 2X Drive	3-416
FD8	8	D,CKN,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset, Negative Edge Trigger, 1X Drive	3-420
FD8D2	9	D,CKN,SN,RN = 3,1,2,2	D Flip-Flop with Set and Reset, Negative Edge Trigger, 2X Drive	3-420
FD8D2Q	8	D,CKN,RN,SN = 3,1,2, 2	D Flip-Flop with Set and Reset, Negative Edge Trigger, Q Output Only, 2X Drive	3-424
FD8D4Q	9	D,CKN,RN,SN = 3,1,2, 2	D Flip-Flop with Set and Reset, Negative Edge Trigger, Q Output Only, 4X Drive	3-424
FD8SD2Q	11	D,TI,TE,CKN,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set and Reset, Scan, Negative Edge Trigger, Q Output Only, 2X Drive	3-428
FD8SD4Q	12	D,TI,TE,CKN,SN,RN = 1,1,2,1,2,2	D Flip-Flop with Set and Reset, Scan, Negative Edge Trigger, Q Output Only, 4X Drive	3-428
FD8D2X4Q	32	D0, D1, D2, D3, CKN, RN, SN = 3, 3, 3, 3, 1, 8, 8	4-Bit D Flip-Flop with Set and Reset, Negative Edge Trigger, Q Output Only, 2X Drive	3-432
FD8D4X4Q	36	D0, D1, D2, D3, CKN, RN, SN = 3, 3, 3, 3, 1, 8, 8	4-Bit D Flip-Flop with Set and Reset, Negative Edge Trigger, Q Output Only, 4X Drive	3-432
FG1	7	D,E,CK = 3,1,1	D Flip-Flop with CK Enable, Positive Edge Trigger, 1X Drive	3-438



**Table 3.6: Flip-Flops (Continued)**

Cell Names	Size (gates)	Input Loading (in Standard loads)	Description	Page
FG1X4	22	D0,D1,D2,D3,E,CK = 3,3,3,3,1,1	4-Bit D Flip-Flop with CK Enable, Positive Edge Trigger, 1X Drive	3-440
FG2	8	D,E,CK RN = 3,1,1,2	D Flip-Flop with Reset, CK Enable, Positive Edge Trigger, 1X Drive	3-444
FG2X4	26	D0,D1,D2,D3,E,CK,RN = 3,3,3,3,1,1,8	4-Bit D Flip-Flop with Reset, CK Enable, Positive Edge Trigger, 1X Drive	3-446
FJ1	9	J,K,CK = 1,1,1	JK Flip-Flop, Positive Edge Trigger, 1X Drive	3-450
FJ1D2	10	J,K,CK = 1,1,1	JK Flip-Flop, Positive Edge Trigger, 2X Drive	3-450
FJ1S	11	J,K,CK,TI,TE = 1,1,1,1,2	JK Flip-Flop with Scan, Positive Edge Trigger, 1X Drive	3-454
FJ1SD2	12	J,K,CK,TI,TE = 1,1,1,1,2	JK Flip-Flop with Scan, Positive Edge Trigger, 2X Drive	3-454
FJ2	10	J,K,CK,RN = 1,1,1,2	JK Flip-Flop with Reset, Positive Edge Trigger, 1X Drive	3-458
FJ2D2	11	J,K,CK,RN = 1,1,1,2	JK Flip-Flop with Reset, Positive Edge Trigger, 2X Drive	3-458
FJ2S	12	J,K,CK,TI,TE,RN = 1,1,1,1,2,2	JK Flip-Flop with Scan, Reset, Positive Edge Trigger, 1X Drive	3-462
FJ2SD2	13	J,K,CK,TI,TE,RN = 1,1,1,1,2,2	JK Flip-Flop with Reset, Scan, Positive Edge Trigger, 2X Drive	3-462
FJ4	11	J,K,CK,SN,RN = 1,1,1,2,2	JK Flip-Flop with Set, Reset, Positive Edge Trigger, 1X Drive	3-466
FJ4D2	12	J,K,CK,SN,RN = 1,1,1,2,2	JK Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, 1X Drive	3-466
FJ4S	13	J,K,CK,TI,TE,SN,RN = 1,1,1,1,2,2,2	JK Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, 1X Drive	3-470
FJ4SD2	14	J,K,CK,TI,TE,SN,RN = 1,1,1,1,2,2,2	JK Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, 2X Drive	3-470
FT2	7	CK,RN = 1,2	Toggle Flip-Flop with Reset, Positive Edge Trigger, 1X Drive	3-476
FT2D2	8	CK,RN = 1,2	Toggle Flip-Flop with Reset, Positive Edge Trigger, 2X Drive	3-476

Datasheets for HDA9000 5.0V Macrocells (5.0V Device) are on pages 3-20 to 3-480

# AD2D2/AD2D4/AD2D6

2 Input AND with 2X Drive, 4X Drive or 6X Drive

Inputs: A, B

Output: Y

Input Loading (SL):

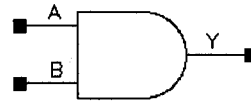
- AD2D2: All: 1
- AD2D4: All: 1
- AD2D6: All: 1

Maximum Fanout (Rec. SL):

- AD2D2: 56
- AD2D4: 112
- AD2D6: 168

Gate Count:

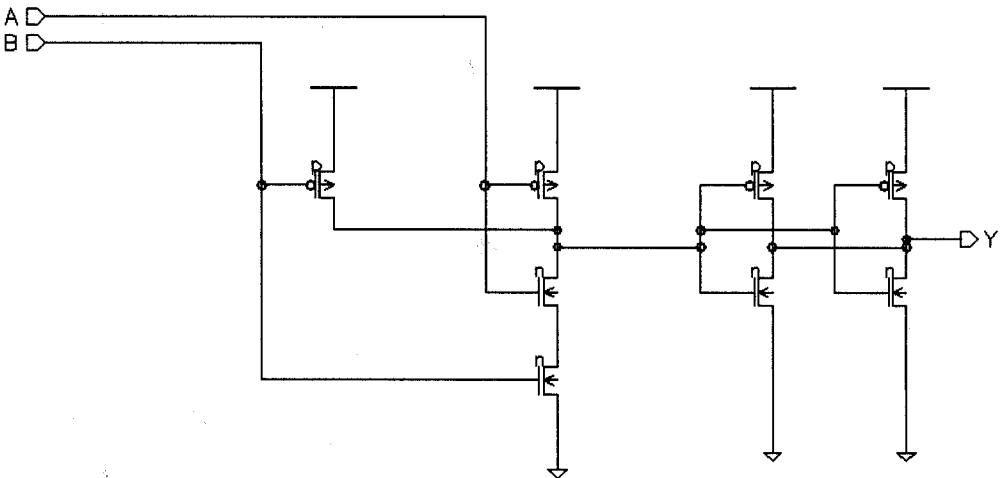
- AD2D2: 2
- AD2D4: 3
- AD2D6: 4



**Symbol**

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

**Truth Table**



**Schematic**

**AD2D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.31	$0.27 + 0.023 \cdot \text{SL}$	$0.27 + 0.022 \cdot \text{SL}$	$0.28 + 0.021 \cdot \text{SL}$
	tPHL	0.37	$0.34 + 0.017 \cdot \text{SL}$	$0.35 + 0.012 \cdot \text{SL}$	$0.38 + 0.010 \cdot \text{SL}$
	tR	0.24	$0.15 + 0.047 \cdot \text{SL}$	$0.14 + 0.051 \cdot \text{SL}$	$0.11 + 0.052 \cdot \text{SL}$
	tF	0.18	$0.14 + 0.018 \cdot \text{SL}$	$0.14 + 0.019 \cdot \text{SL}$	$0.11 + 0.020 \cdot \text{SL}$
B to Y	tPLH	0.28	$0.23 + 0.024 \cdot \text{SL}$	$0.24 + 0.022 \cdot \text{SL}$	$0.24 + 0.021 \cdot \text{SL}$
	tPHL	0.43	$0.39 + 0.019 \cdot \text{SL}$	$0.41 + 0.012 \cdot \text{SL}$	$0.45 + 0.010 \cdot \text{SL}$
	tR	0.24	$0.15 + 0.047 \cdot \text{SL}$	$0.14 + 0.051 \cdot \text{SL}$	$0.11 + 0.052 \cdot \text{SL}$
	tF	0.20	$0.17 + 0.016 \cdot \text{SL}$	$0.16 + 0.018 \cdot \text{SL}$	$0.13 + 0.020 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **AD2D4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.39	$0.36 + 0.013 \cdot \text{SL}$	$0.37 + 0.011 \cdot \text{SL}$	$0.38 + 0.011 \cdot \text{SL}$
	tPHL	0.44	$0.41 + 0.010 \cdot \text{SL}$	$0.42 + 0.007 \cdot \text{SL}$	$0.45 + 0.006 \cdot \text{SL}$
	tR	0.22	$0.18 + 0.022 \cdot \text{SL}$	$0.17 + 0.024 \cdot \text{SL}$	$0.15 + 0.025 \cdot \text{SL}$
	tF	0.20	$0.18 + 0.009 \cdot \text{SL}$	$0.18 + 0.009 \cdot \text{SL}$	$0.18 + 0.009 \cdot \text{SL}$
B to Y	tPLH	0.34	$0.32 + 0.013 \cdot \text{SL}$	$0.32 + 0.011 \cdot \text{SL}$	$0.33 + 0.011 \cdot \text{SL}$
	tPHL	0.48	$0.46 + 0.012 \cdot \text{SL}$	$0.47 + 0.008 \cdot \text{SL}$	$0.51 + 0.006 \cdot \text{SL}$
	tR	0.22	$0.18 + 0.021 \cdot \text{SL}$	$0.17 + 0.024 \cdot \text{SL}$	$0.15 + 0.025 \cdot \text{SL}$
	tF	0.22	$0.20 + 0.009 \cdot \text{SL}$	$0.20 + 0.009 \cdot \text{SL}$	$0.20 + 0.009 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **AD2D6 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.47	$0.45 + 0.009 \cdot \text{SL}$	$0.45 + 0.008 \cdot \text{SL}$	$0.46 + 0.007 \cdot \text{SL}$
	tPHL	0.50	$0.49 + 0.008 \cdot \text{SL}$	$0.49 + 0.006 \cdot \text{SL}$	$0.52 + 0.005 \cdot \text{SL}$
	tR	0.24	$0.22 + 0.012 \cdot \text{SL}$	$0.20 + 0.016 \cdot \text{SL}$	$0.18 + 0.017 \cdot \text{SL}$
	tF	0.23	$0.23 + 0.004 \cdot \text{SL}$	$0.22 + 0.006 \cdot \text{SL}$	$0.22 + 0.006 \cdot \text{SL}$
B to Y	tPLH	0.41	$0.39 + 0.010 \cdot \text{SL}$	$0.40 + 0.008 \cdot \text{SL}$	$0.41 + 0.007 \cdot \text{SL}$
	tPHL	0.54	$0.53 + 0.008 \cdot \text{SL}$	$0.53 + 0.006 \cdot \text{SL}$	$0.56 + 0.005 \cdot \text{SL}$
	tR	0.24	$0.22 + 0.013 \cdot \text{SL}$	$0.21 + 0.015 \cdot \text{SL}$	$0.19 + 0.016 \cdot \text{SL}$
	tF	0.25	$0.24 + 0.005 \cdot \text{SL}$	$0.24 + 0.006 \cdot \text{SL}$	$0.24 + 0.006 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

# AD3/AD3D3/AD3D5/AD3D8

3 Input AND with 1X Drive, 3X Drive, 5X Drive or 8X Drive

Inputs: A, B, C

Output: Y

Input Loading (SL):

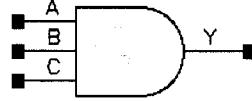
- AD3: All : 1
- AD3D3: All: 1
- AD3D5: All: 1
- AD3D8: All: 2

Maximum Fanout (Rec. SL):

- AD3: 28
- AD3D3: 84
- AD3D5: 140
- AD3D8: 224

Gate Count:

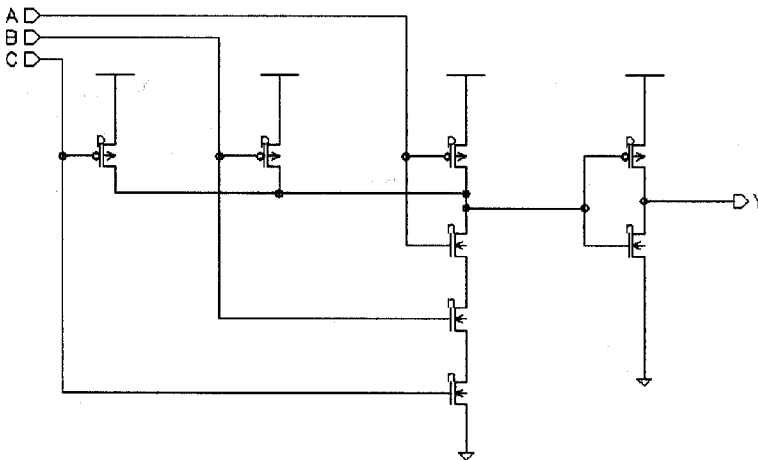
- AD3 : 2
- AD3D3 : 3
- AD3D5 : 4
- AD3D8 : 7



Symbol

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Truth Table



Schematic

**AD3 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.39	$0.30 + 0.046*SL$	$0.31 + 0.043*SL$	$0.31 + 0.043*SL$
	tPHL	0.35	$0.29 + 0.029*SL$	$0.31 + 0.021*SL$	$0.34 + 0.020*SL$
	tR	0.34	$0.15 + 0.097*SL$	$0.14 + 0.100*SL$	$0.11 + 0.102*SL$
	tF	0.20	$0.13 + 0.033*SL$	$0.12 + 0.036*SL$	$0.08 + 0.039*SL$
B to Y	tPLH	0.39	$0.30 + 0.046*SL$	$0.31 + 0.042*SL$	$0.31 + 0.042*SL$
	tPHL	0.41	$0.35 + 0.031*SL$	$0.38 + 0.021*SL$	$0.41 + 0.020*SL$
	tR	0.35	$0.16 + 0.096*SL$	$0.15 + 0.100*SL$	$0.11 + 0.102*SL$
	tF	0.22	$0.15 + 0.034*SL$	$0.14 + 0.036*SL$	$0.09 + 0.038*SL$
C to Y	tPLH	0.36	$0.27 + 0.046*SL$	$0.28 + 0.043*SL$	$0.28 + 0.042*SL$
	tPHL	0.45	$0.39 + 0.032*SL$	$0.42 + 0.022*SL$	$0.46 + 0.020*SL$
	tR	0.35	$0.16 + 0.096*SL$	$0.15 + 0.100*SL$	$0.11 + 0.102*SL$
	tF	0.24	$0.18 + 0.033*SL$	$0.17 + 0.035*SL$	$0.11 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **AD3D3 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.46	$0.42 + 0.018*SL$	$0.43 + 0.015*SL$	$0.45 + 0.014*SL$
	tPHL	0.40	$0.37 + 0.014*SL$	$0.39 + 0.009*SL$	$0.42 + 0.007*SL$
	tR	0.26	$0.20 + 0.029*SL$	$0.19 + 0.032*SL$	$0.17 + 0.034*SL$
	tF	0.19	$0.17 + 0.013*SL$	$0.17 + 0.012*SL$	$0.16 + 0.012*SL$
B to Y	tPLH	0.44	$0.41 + 0.018*SL$	$0.42 + 0.015*SL$	$0.43 + 0.014*SL$
	tPHL	0.45	$0.42 + 0.014*SL$	$0.43 + 0.010*SL$	$0.48 + 0.008*SL$
	tR	0.26	$0.20 + 0.029*SL$	$0.19 + 0.032*SL$	$0.17 + 0.034*SL$
	tF	0.21	$0.19 + 0.012*SL$	$0.19 + 0.012*SL$	$0.18 + 0.012*SL$
C to Y	tPLH	0.41	$0.37 + 0.018*SL$	$0.38 + 0.015*SL$	$0.39 + 0.014*SL$
	tPHL	0.49	$0.46 + 0.015*SL$	$0.47 + 0.010*SL$	$0.52 + 0.008*SL$
	tR	0.26	$0.21 + 0.029*SL$	$0.19 + 0.032*SL$	$0.17 + 0.034*SL$
	tF	0.24	$0.21 + 0.015*SL$	$0.21 + 0.012*SL$	$0.21 + 0.012*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# AD3D5/AD3D8

3 Input AND with 5X Drive or 8X Drive

## AD3D5 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.57	$0.54 + 0.013*SL$	$0.55 + 0.010*SL$	$0.57 + 0.009*SL$
	tPHL	0.47	$0.45 + 0.009*SL$	$0.46 + 0.007*SL$	$0.49 + 0.005*SL$
	tR	0.30	$0.26 + 0.016*SL$	$0.26 + 0.018*SL$	$0.23 + 0.020*SL$
	tF	0.22	$0.21 + 0.007*SL$	$0.21 + 0.007*SL$	$0.21 + 0.007*SL$
B to Y	tPLH	0.55	$0.52 + 0.012*SL$	$0.53 + 0.010*SL$	$0.55 + 0.009*SL$
	tPHL	0.51	$0.49 + 0.010*SL$	$0.50 + 0.007*SL$	$0.53 + 0.005*SL$
	tR	0.30	$0.27 + 0.015*SL$	$0.26 + 0.018*SL$	$0.23 + 0.020*SL$
	tF	0.24	$0.23 + 0.007*SL$	$0.23 + 0.008*SL$	$0.23 + 0.007*SL$
C to Y	tPLH	0.51	$0.48 + 0.012*SL$	$0.49 + 0.010*SL$	$0.51 + 0.009*SL$
	tPHL	0.55	$0.53 + 0.010*SL$	$0.53 + 0.007*SL$	$0.57 + 0.006*SL$
	tR	0.30	$0.27 + 0.015*SL$	$0.26 + 0.018*SL$	$0.23 + 0.020*SL$
	tF	0.26	$0.24 + 0.009*SL$	$0.25 + 0.008*SL$	$0.26 + 0.007*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

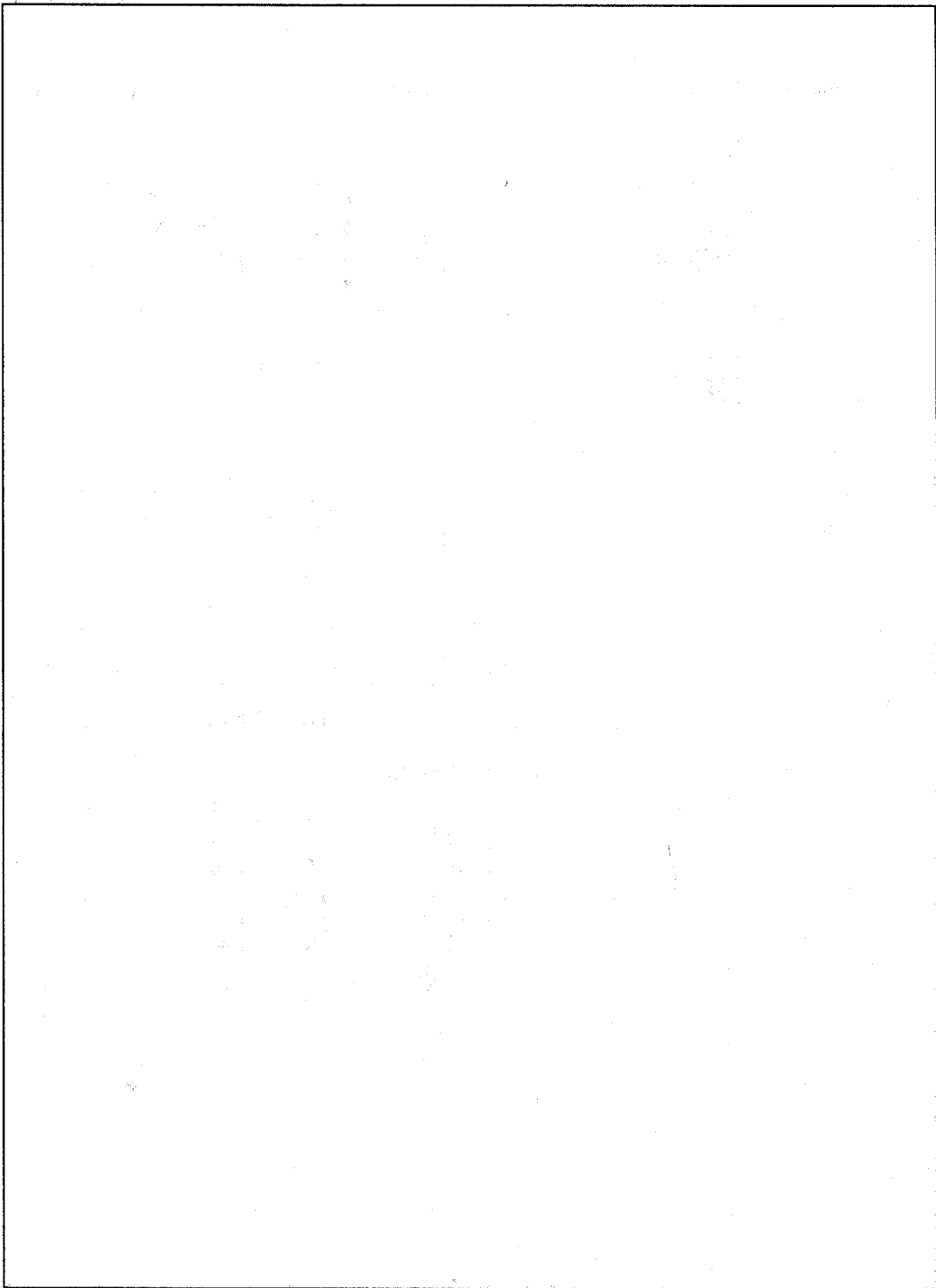
## AD3D8 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.52	$0.50 + 0.008*SL$	$0.51 + 0.006*SL$	$0.52 + 0.006*SL$
	tPHL	0.42	$0.41 + 0.005*SL$	$0.41 + 0.005*SL$	$0.43 + 0.004*SL$
	tR	0.26	$0.25 + 0.009*SL$	$0.24 + 0.011*SL$	$0.22 + 0.012*SL$
	tF	0.20	$0.20 + 0.004*SL$	$0.19 + 0.005*SL$	$0.20 + 0.005*SL$
B to Y	tPLH	0.50	$0.48 + 0.008*SL$	$0.49 + 0.006*SL$	$0.50 + 0.006*SL$
	tPHL	0.47	$0.45 + 0.006*SL$	$0.46 + 0.005*SL$	$0.48 + 0.004*SL$
	tR	0.27	$0.25 + 0.010*SL$	$0.24 + 0.011*SL$	$0.22 + 0.012*SL$
	tF	0.22	$0.21 + 0.006*SL$	$0.21 + 0.005*SL$	$0.22 + 0.004*SL$
C to Y	tPLH	0.46	$0.45 + 0.008*SL$	$0.45 + 0.006*SL$	$0.47 + 0.006*SL$
	tPHL	0.50	$0.49 + 0.006*SL$	$0.49 + 0.005*SL$	$0.52 + 0.004*SL$
	tR	0.27	$0.25 + 0.009*SL$	$0.25 + 0.011*SL$	$0.22 + 0.012*SL$
	tF	0.24	$0.24 + 0.003*SL$	$0.23 + 0.005*SL$	$0.24 + 0.005*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$





# AD4D2/AD4D4/AD4D6

4 Input AND with 2X Drive, 4X Drive or 6X Drive

Inputs: A, B, C, D

Output: Y

Input Loading (SL):

- AD4D2: All: 1

- AD4D4: All: 1

- AD4D6: All: 2

Maximum Fanout (Rec. SL):

- AD4D2: 56

- AD4D4: 112

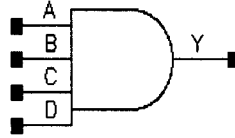
- AD4D6: 168

Gate Count:

- AD4D2: 3

- AD4D4: 4

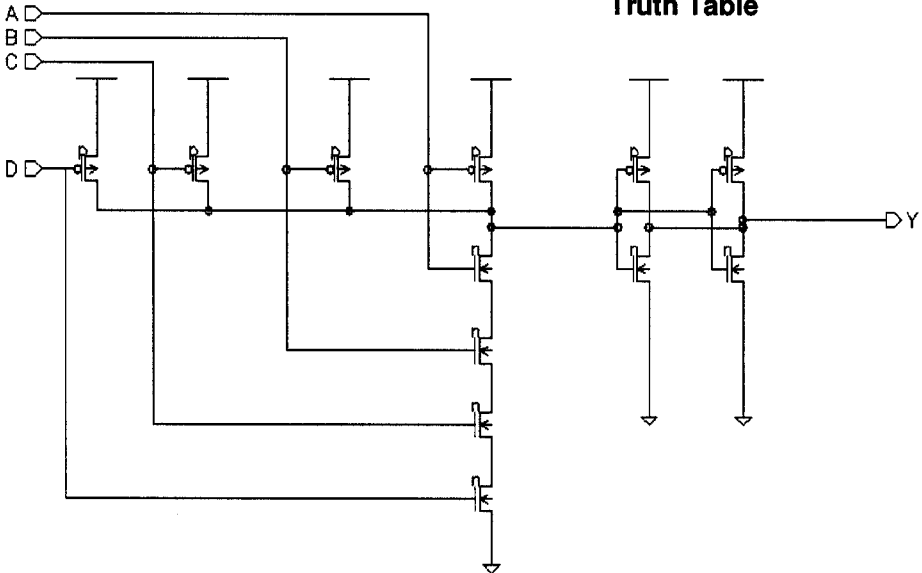
- AD4D6: 7



**Symbol**

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

**Truth Table**



**Schematic**

**AD4D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.52	$0.47 + 0.027 \cdot \text{SL}$	$0.48 + 0.023 \cdot \text{SL}$	$0.51 + 0.022 \cdot \text{SL}$
	tPHL	0.37	$0.34 + 0.019 \cdot \text{SL}$	$0.36 + 0.013 \cdot \text{SL}$	$0.40 + 0.011 \cdot \text{SL}$
	tR	0.31	$0.22 + 0.046 \cdot \text{SL}$	$0.21 + 0.050 \cdot \text{SL}$	$0.18 + 0.051 \cdot \text{SL}$
	tF	0.20	$0.16 + 0.018 \cdot \text{SL}$	$0.16 + 0.019 \cdot \text{SL}$	$0.14 + 0.020 \cdot \text{SL}$
B to Y	tPLH	0.53	$0.48 + 0.028 \cdot \text{SL}$	$0.49 + 0.023 \cdot \text{SL}$	$0.52 + 0.022 \cdot \text{SL}$
	tPHL	0.43	$0.39 + 0.020 \cdot \text{SL}$	$0.41 + 0.013 \cdot \text{SL}$	$0.45 + 0.011 \cdot \text{SL}$
	tR	0.32	$0.23 + 0.045 \cdot \text{SL}$	$0.21 + 0.050 \cdot \text{SL}$	$0.18 + 0.051 \cdot \text{SL}$
	tF	0.22	$0.19 + 0.017 \cdot \text{SL}$	$0.18 + 0.018 \cdot \text{SL}$	$0.16 + 0.020 \cdot \text{SL}$
C to Y	tPLH	0.52	$0.47 + 0.027 \cdot \text{SL}$	$0.48 + 0.023 \cdot \text{SL}$	$0.51 + 0.022 \cdot \text{SL}$
	tPHL	0.47	$0.43 + 0.021 \cdot \text{SL}$	$0.45 + 0.014 \cdot \text{SL}$	$0.50 + 0.011 \cdot \text{SL}$
	tR	0.32	$0.23 + 0.044 \cdot \text{SL}$	$0.21 + 0.050 \cdot \text{SL}$	$0.18 + 0.051 \cdot \text{SL}$
	tF	0.24	$0.20 + 0.018 \cdot \text{SL}$	$0.20 + 0.018 \cdot \text{SL}$	$0.18 + 0.019 \cdot \text{SL}$
D to Y	tPLH	0.51	$0.45 + 0.028 \cdot \text{SL}$	$0.47 + 0.023 \cdot \text{SL}$	$0.49 + 0.022 \cdot \text{SL}$
	tPHL	0.50	$0.45 + 0.022 \cdot \text{SL}$	$0.47 + 0.014 \cdot \text{SL}$	$0.54 + 0.011 \cdot \text{SL}$
	tR	0.32	$0.23 + 0.044 \cdot \text{SL}$	$0.21 + 0.050 \cdot \text{SL}$	$0.18 + 0.051 \cdot \text{SL}$
	tF	0.26	$0.23 + 0.017 \cdot \text{SL}$	$0.22 + 0.018 \cdot \text{SL}$	$0.21 + 0.019 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

# AD4D4/AD4D6

4 Input AND with 4X Drive or 6X Drive

## AD4D4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.64	$0.60 + 0.016*SL$	$0.62 + 0.012*SL$	$0.64 + 0.011*SL$
	tPHL	0.44	$0.42 + 0.011*SL$	$0.43 + 0.008*SL$	$0.46 + 0.006*SL$
	tR	0.34	$0.30 + 0.018*SL$	$0.29 + 0.023*SL$	$0.26 + 0.025*SL$
	tF	0.22	$0.20 + 0.010*SL$	$0.20 + 0.009*SL$	$0.19 + 0.010*SL$
B to Y	tPLH	0.64	$0.61 + 0.016*SL$	$0.62 + 0.012*SL$	$0.65 + 0.011*SL$
	tPHL	0.48	$0.46 + 0.012*SL$	$0.47 + 0.008*SL$	$0.51 + 0.006*SL$
	tR	0.34	$0.31 + 0.019*SL$	$0.29 + 0.023*SL$	$0.26 + 0.025*SL$
	tF	0.24	$0.22 + 0.010*SL$	$0.22 + 0.009*SL$	$0.21 + 0.009*SL$
C to Y	tPLH	0.63	$0.60 + 0.016*SL$	$0.61 + 0.012*SL$	$0.63 + 0.011*SL$
	tPHL	0.52	$0.49 + 0.013*SL$	$0.51 + 0.009*SL$	$0.55 + 0.007*SL$
	tR	0.34	$0.31 + 0.019*SL$	$0.29 + 0.023*SL$	$0.26 + 0.025*SL$
	tF	0.25	$0.23 + 0.011*SL$	$0.24 + 0.010*SL$	$0.24 + 0.009*SL$
D to Y	tPLH	0.61	$0.58 + 0.016*SL$	$0.59 + 0.012*SL$	$0.62 + 0.011*SL$
	tPHL	0.55	$0.52 + 0.013*SL$	$0.53 + 0.009*SL$	$0.58 + 0.007*SL$
	tR	0.34	$0.30 + 0.020*SL$	$0.29 + 0.023*SL$	$0.26 + 0.025*SL$
	tF	0.27	$0.25 + 0.011*SL$	$0.25 + 0.010*SL$	$0.26 + 0.009*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

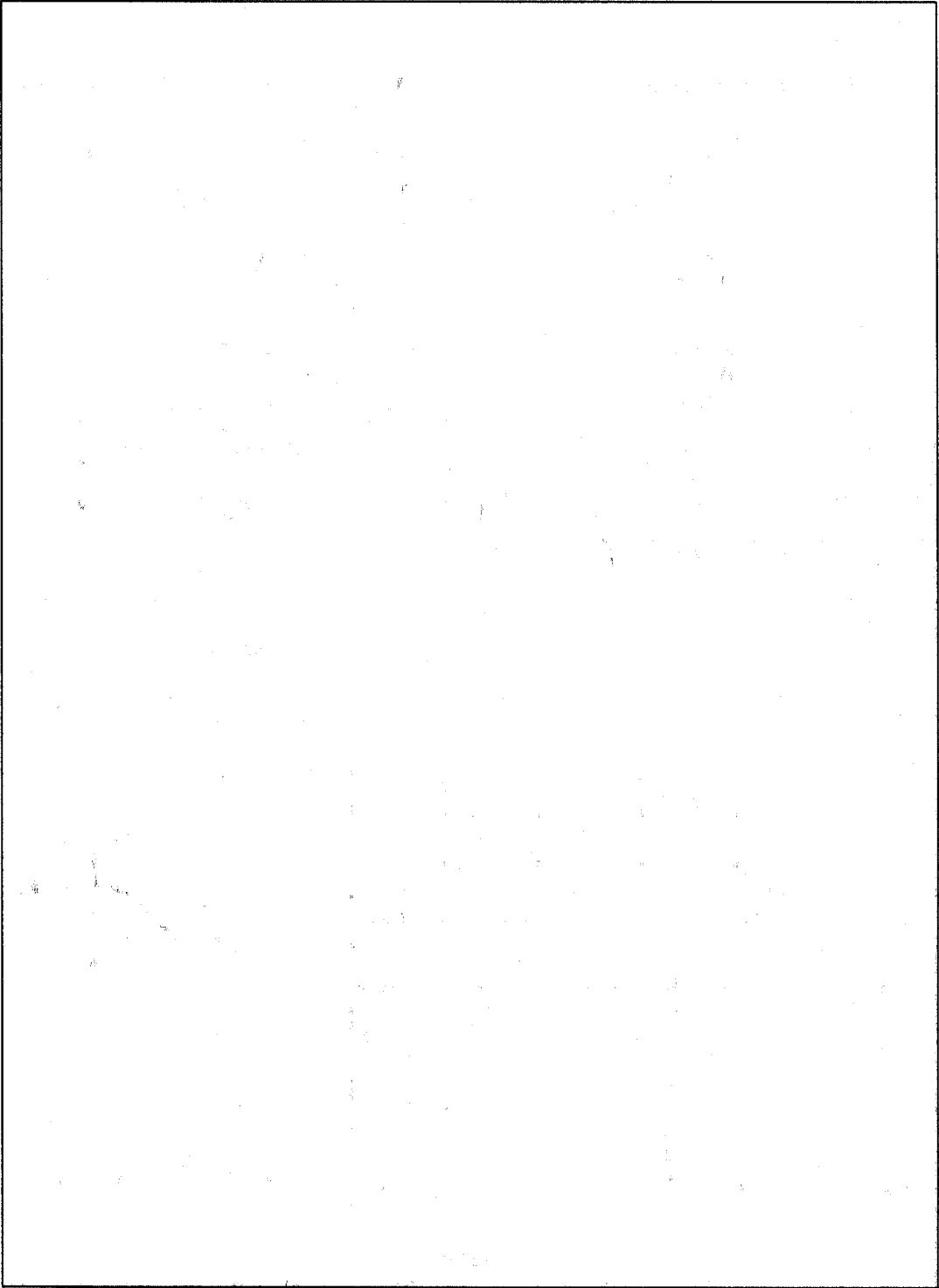
## AD4D6 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.58	$0.56 + 0.011*SL$	$0.57 + 0.009*SL$	$0.59 + 0.008*SL$
	tPHL	0.39	$0.37 + 0.008*SL$	$0.38 + 0.006*SL$	$0.40 + 0.004*SL$
	tR	0.31	$0.28 + 0.013*SL$	$0.27 + 0.015*SL$	$0.25 + 0.016*SL$
	tF	0.19	$0.17 + 0.010*SL$	$0.19 + 0.006*SL$	$0.18 + 0.006*SL$
B to Y	tPLH	0.59	$0.57 + 0.011*SL$	$0.57 + 0.009*SL$	$0.60 + 0.008*SL$
	tPHL	0.44	$0.42 + 0.008*SL$	$0.43 + 0.006*SL$	$0.45 + 0.005*SL$
	tR	0.31	$0.28 + 0.014*SL$	$0.28 + 0.015*SL$	$0.25 + 0.016*SL$
	tF	0.21	$0.20 + 0.006*SL$	$0.20 + 0.006*SL$	$0.20 + 0.006*SL$
C to Y	tPLH	0.58	$0.56 + 0.011*SL$	$0.57 + 0.009*SL$	$0.59 + 0.008*SL$
	tPHL	0.47	$0.45 + 0.009*SL$	$0.46 + 0.006*SL$	$0.49 + 0.005*SL$
	tR	0.31	$0.28 + 0.013*SL$	$0.28 + 0.015*SL$	$0.25 + 0.016*SL$
	tF	0.23	$0.22 + 0.007*SL$	$0.22 + 0.006*SL$	$0.23 + 0.006*SL$
D to Y	tPLH	0.56	$0.54 + 0.011*SL$	$0.55 + 0.009*SL$	$0.57 + 0.008*SL$
	tPHL	0.50	$0.48 + 0.009*SL$	$0.49 + 0.007*SL$	$0.52 + 0.005*SL$
	tR	0.31	$0.28 + 0.014*SL$	$0.28 + 0.015*SL$	$0.25 + 0.016*SL$
	tF	0.26	$0.24 + 0.006*SL$	$0.24 + 0.007*SL$	$0.25 + 0.006*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# AD5/AD5D3/AD5D6

5 Input AND with 1X Drive, 3X Drive or 6X Drive

Inputs: A, B, C, D,E

Output: Y

Input Loading (SL):

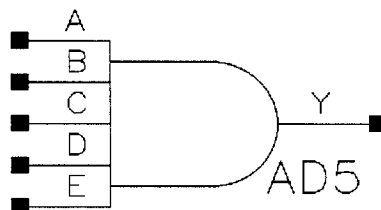
- AD5: All: 1
- AD5D3: All: 1
- AD5D6: All: 2

Maximum Fanout (Rec. SL):

- AD5: 28
- AD5D3: 72
- AD5D6: 144

Gate Count:

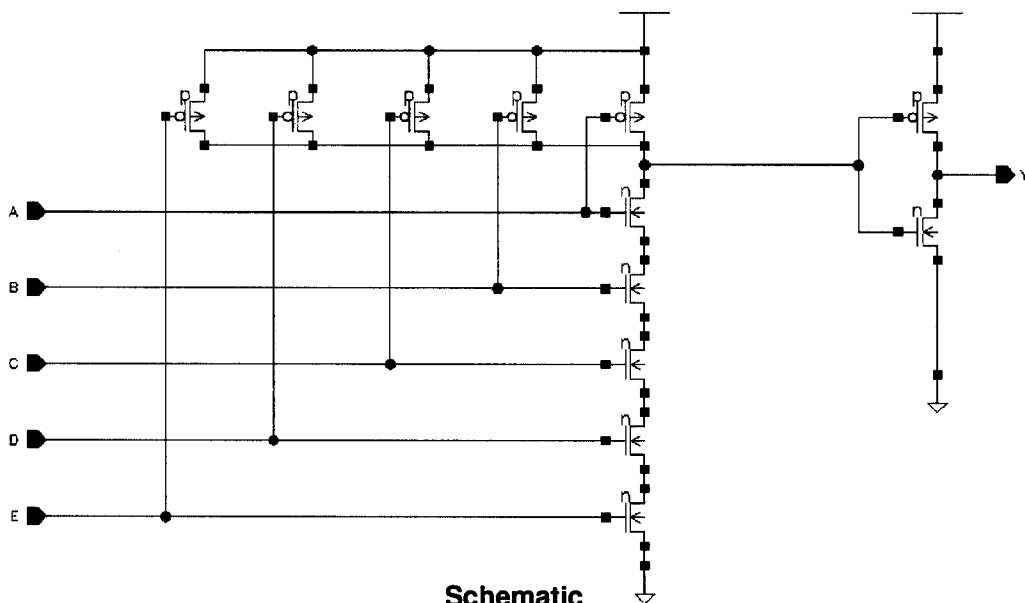
- AD5: 3
- AD5D3: 4
- AD5D6: 8



Symbol

A	B	C	D	E	Y
0	x	x	x	x	0
x	0	x	x	x	0
x	x	0	x	x	0
x	x	x	0	x	0
1	1	1	1	1	1

Truth Table



Schematic

**AD5 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.59	$0.48 + 0.051 * SL$	$0.51 + 0.044 * SL$	$0.54 + 0.042 * SL$
	tPHL	0.37	$0.30 + 0.031 * SL$	$0.33 + 0.022 * SL$	$0.37 + 0.020 * SL$
	tR	0.41	$0.22 + 0.096 * SL$	$0.21 + 0.099 * SL$	$0.18 + 0.101 * SL$
	tF	0.21	$0.14 + 0.035 * SL$	$0.13 + 0.036 * SL$	$0.10 + 0.038 * SL$
B to Y	tPLH	0.62	$0.52 + 0.051 * SL$	$0.54 + 0.044 * SL$	$0.57 + 0.042 * SL$
	tPHL	0.42	$0.36 + 0.032 * SL$	$0.39 + 0.022 * SL$	$0.43 + 0.020 * SL$
	tR	0.42	$0.23 + 0.096 * SL$	$0.22 + 0.099 * SL$	$0.18 + 0.101 * SL$
	tF	0.23	$0.16 + 0.035 * SL$	$0.16 + 0.036 * SL$	$0.11 + 0.038 * SL$
C to Y	tPLH	0.63	$0.53 + 0.051 * SL$	$0.55 + 0.044 * SL$	$0.58 + 0.042 * SL$
	tPHL	0.46	$0.39 + 0.034 * SL$	$0.43 + 0.023 * SL$	$0.48 + 0.020 * SL$
	tR	0.42	$0.23 + 0.096 * SL$	$0.22 + 0.099 * SL$	$0.18 + 0.101 * SL$
	tF	0.25	$0.18 + 0.035 * SL$	$0.18 + 0.035 * SL$	$0.13 + 0.038 * SL$
D to Y	tPLH	0.64	$0.53 + 0.051 * SL$	$0.56 + 0.044 * SL$	$0.59 + 0.042 * SL$
	tPHL	0.49	$0.42 + 0.036 * SL$	$0.46 + 0.023 * SL$	$0.52 + 0.020 * SL$
	tR	0.42	$0.23 + 0.095 * SL$	$0.22 + 0.099 * SL$	$0.18 + 0.101 * SL$
	tF	0.28	$0.21 + 0.034 * SL$	$0.21 + 0.035 * SL$	$0.16 + 0.037 * SL$
E to Y	tPLH	0.62	$0.52 + 0.051 * SL$	$0.54 + 0.044 * SL$	$0.57 + 0.042 * SL$
	tPHL	0.51	$0.43 + 0.038 * SL$	$0.47 + 0.024 * SL$	$0.54 + 0.020 * SL$
	tR	0.42	$0.23 + 0.095 * SL$	$0.22 + 0.099 * SL$	$0.18 + 0.101 * SL$
	tF	0.30	$0.23 + 0.037 * SL$	$0.24 + 0.035 * SL$	$0.19 + 0.037 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# AD5D3

## 5 Input AND with 3X Drive

### AD5D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.68	$0.64 + 0.022*SL$	$0.66 + 0.017*SL$	$0.69 + 0.015*SL$
	tPHL	0.41	$0.38 + 0.014*SL$	$0.40 + 0.010*SL$	$0.44 + 0.008*SL$
	tR	0.38	$0.33 + 0.027*SL$	$0.31 + 0.031*SL$	$0.28 + 0.033*SL$
	tF	0.21	$0.18 + 0.011*SL$	$0.18 + 0.012*SL$	$0.17 + 0.013*SL$
B to Y	tPLH	0.71	$0.67 + 0.022*SL$	$0.68 + 0.017*SL$	$0.72 + 0.015*SL$
	tPHL	0.46	$0.43 + 0.015*SL$	$0.44 + 0.010*SL$	$0.49 + 0.008*SL$
	tR	0.38	$0.33 + 0.027*SL$	$0.32 + 0.031*SL$	$0.28 + 0.033*SL$
	tF	0.23	$0.20 + 0.012*SL$	$0.20 + 0.012*SL$	$0.20 + 0.012*SL$
C to Y	tPLH	0.72	$0.68 + 0.022*SL$	$0.69 + 0.017*SL$	$0.73 + 0.015*SL$
	tPHL	0.49	$0.46 + 0.015*SL$	$0.48 + 0.011*SL$	$0.53 + 0.008*SL$
	tR	0.38	$0.33 + 0.027*SL$	$0.32 + 0.031*SL$	$0.28 + 0.033*SL$
	tF	0.24	$0.22 + 0.012*SL$	$0.22 + 0.012*SL$	$0.22 + 0.012*SL$
D to Y	tPLH	0.73	$0.68 + 0.022*SL$	$0.70 + 0.017*SL$	$0.73 + 0.015*SL$
	tPHL	0.52	$0.49 + 0.016*SL$	$0.50 + 0.011*SL$	$0.56 + 0.008*SL$
	tR	0.38	$0.33 + 0.028*SL$	$0.32 + 0.031*SL$	$0.28 + 0.033*SL$
	tF	0.26	$0.24 + 0.014*SL$	$0.24 + 0.012*SL$	$0.24 + 0.012*SL$
E to Y	tPLH	0.72	$0.67 + 0.022*SL$	$0.69 + 0.017*SL$	$0.72 + 0.015*SL$
	tPHL	0.54	$0.51 + 0.017*SL$	$0.52 + 0.011*SL$	$0.58 + 0.008*SL$
	tR	0.38	$0.33 + 0.028*SL$	$0.32 + 0.031*SL$	$0.28 + 0.033*SL$
	tF	0.29	$0.26 + 0.015*SL$	$0.27 + 0.013*SL$	$0.27 + 0.012*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**AD5D6 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.70	$0.68 + 0.012 \cdot \text{SL}$	$0.68 + 0.010 \cdot \text{SL}$	$0.72 + 0.008 \cdot \text{SL}$
	tPHL	0.40	$0.38 + 0.008 \cdot \text{SL}$	$0.39 + 0.006 \cdot \text{SL}$	$0.41 + 0.004 \cdot \text{SL}$
	tR	0.38	$0.36 + 0.012 \cdot \text{SL}$	$0.35 + 0.015 \cdot \text{SL}$	$0.32 + 0.016 \cdot \text{SL}$
	tF	0.20	$0.18 + 0.007 \cdot \text{SL}$	$0.18 + 0.006 \cdot \text{SL}$	$0.18 + 0.006 \cdot \text{SL}$
B to Y	tPLH	0.73	$0.71 + 0.013 \cdot \text{SL}$	$0.71 + 0.010 \cdot \text{SL}$	$0.75 + 0.008 \cdot \text{SL}$
	tPHL	0.44	$0.43 + 0.008 \cdot \text{SL}$	$0.43 + 0.006 \cdot \text{SL}$	$0.46 + 0.005 \cdot \text{SL}$
	tR	0.39	$0.36 + 0.012 \cdot \text{SL}$	$0.36 + 0.015 \cdot \text{SL}$	$0.32 + 0.016 \cdot \text{SL}$
	tF	0.22	$0.21 + 0.006 \cdot \text{SL}$	$0.20 + 0.006 \cdot \text{SL}$	$0.21 + 0.006 \cdot \text{SL}$
C to Y	tPLH	0.75	$0.72 + 0.013 \cdot \text{SL}$	$0.73 + 0.010 \cdot \text{SL}$	$0.76 + 0.008 \cdot \text{SL}$
	tPHL	0.48	$0.46 + 0.009 \cdot \text{SL}$	$0.47 + 0.006 \cdot \text{SL}$	$0.50 + 0.005 \cdot \text{SL}$
	tR	0.39	$0.36 + 0.012 \cdot \text{SL}$	$0.36 + 0.014 \cdot \text{SL}$	$0.32 + 0.016 \cdot \text{SL}$
	tF	0.24	$0.22 + 0.007 \cdot \text{SL}$	$0.22 + 0.007 \cdot \text{SL}$	$0.23 + 0.006 \cdot \text{SL}$
D to Y	tPLH	0.75	$0.73 + 0.013 \cdot \text{SL}$	$0.74 + 0.010 \cdot \text{SL}$	$0.77 + 0.008 \cdot \text{SL}$
	tPHL	0.50	$0.49 + 0.009 \cdot \text{SL}$	$0.49 + 0.007 \cdot \text{SL}$	$0.53 + 0.005 \cdot \text{SL}$
	tR	0.39	$0.36 + 0.012 \cdot \text{SL}$	$0.35 + 0.015 \cdot \text{SL}$	$0.32 + 0.016 \cdot \text{SL}$
	tF	0.26	$0.24 + 0.007 \cdot \text{SL}$	$0.24 + 0.007 \cdot \text{SL}$	$0.26 + 0.006 \cdot \text{SL}$
E to Y	tPLH	0.75	$0.72 + 0.013 \cdot \text{SL}$	$0.73 + 0.010 \cdot \text{SL}$	$0.76 + 0.008 \cdot \text{SL}$
	tPHL	0.52	$0.50 + 0.010 \cdot \text{SL}$	$0.51 + 0.007 \cdot \text{SL}$	$0.55 + 0.005 \cdot \text{SL}$
	tR	0.39	$0.36 + 0.012 \cdot \text{SL}$	$0.35 + 0.015 \cdot \text{SL}$	$0.32 + 0.016 \cdot \text{SL}$
	tF	0.28	$0.26 + 0.008 \cdot \text{SL}$	$0.27 + 0.007 \cdot \text{SL}$	$0.28 + 0.006 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$



# AO21/AO21D2/AO21D4/AO21D6

2-AND into 2-NOR with 1X Drive, 2X Drive, 4X Drive or 6X Drive

Inputs: A, B, C

Output: Y

Input Loading(SL):

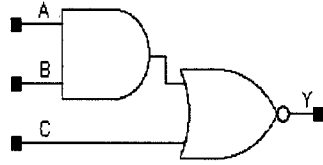
- AO21: All : 1
- AO21D2: All : 2
- AO21D4: All : 1
- AO21D6: All : 1

Maximum Fanout (Rec. SL):

- AO21: 14
- AO21D2: 28
- AO21D4: 112
- AO21D6: 168

Gate Count:

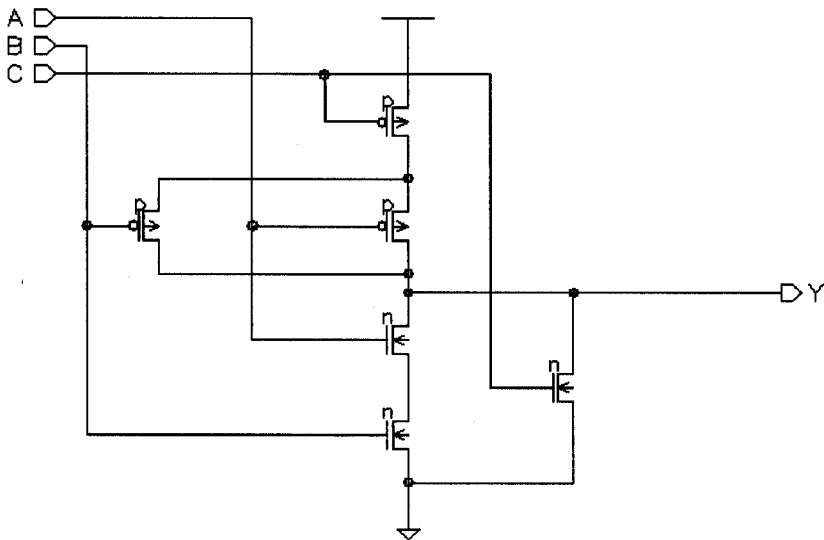
- AO21 : 2
- AO21D2 : 3
- AO21D4 : 4
- AO21D6 : 5



**Symbol**

A	B	C	Y
x	x	1	0
0	x	0	1
x	0	0	1
1	1	x	0

**Truth Table**



**Schematic**

**AO21 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.50	$0.34 + 0.078*SL$	$0.34 + 0.079*SL$	$0.30 + 0.081*SL$
	tPHL	0.16	$0.06 + 0.050*SL$	$0.11 + 0.034*SL$	$0.17 + 0.031*SL$
	tR	0.83	$0.47 + 0.182*SL$	$0.43 + 0.194*SL$	$0.36 + 0.198*SL$
	tF	0.44	$0.32 + 0.063*SL$	$0.32 + 0.063*SL$	$0.23 + 0.067*SL$
B to Y	tPLH	0.58	$0.43 + 0.076*SL$	$0.42 + 0.079*SL$	$0.39 + 0.080*SL$
	tPHL	0.12	$0.04 + 0.043*SL$	$0.07 + 0.032*SL$	$0.10 + 0.031*SL$
	tR	0.97	$0.61 + 0.182*SL$	$0.57 + 0.194*SL$	$0.50 + 0.198*SL$
	tF	0.41	$0.30 + 0.058*SL$	$0.28 + 0.064*SL$	$0.19 + 0.068*SL$
C to Y	tPLH	0.58	$0.43 + 0.077*SL$	$0.42 + 0.079*SL$	$0.39 + 0.081*SL$
	tPHL	0.13	$0.05 + 0.037*SL$	$0.09 + 0.024*SL$	$0.17 + 0.020*SL$
	tR	0.94	$0.57 + 0.188*SL$	$0.55 + 0.196*SL$	$0.50 + 0.198*SL$
	tF	0.45	$0.38 + 0.032*SL$	$0.38 + 0.033*SL$	$0.31 + 0.036*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**AO21D2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.40	$0.33 + 0.039*SL$	$0.33 + 0.037*SL$	$0.32 + 0.038*SL$
	tPHL	0.11	$0.05 + 0.029*SL$	$0.08 + 0.019*SL$	$0.15 + 0.015*SL$
	tR	0.62	$0.46 + 0.084*SL$	$0.44 + 0.089*SL$	$0.37 + 0.092*SL$
	tF	0.38	$0.31 + 0.032*SL$	$0.32 + 0.029*SL$	$0.29 + 0.031*SL$
B to Y	tPLH	0.49	$0.42 + 0.036*SL$	$0.42 + 0.036*SL$	$0.40 + 0.037*SL$
	tPHL	0.08	$0.03 + 0.023*SL$	$0.05 + 0.017*SL$	$0.09 + 0.015*SL$
	tR	0.76	$0.59 + 0.083*SL$	$0.57 + 0.089*SL$	$0.50 + 0.092*SL$
	tF	0.35	$0.29 + 0.028*SL$	$0.29 + 0.029*SL$	$0.24 + 0.031*SL$
C to Y	tPLH	0.49	$0.42 + 0.036*SL$	$0.42 + 0.037*SL$	$0.40 + 0.038*SL$
	tPHL	0.09	$0.05 + 0.020*SL$	$0.07 + 0.014*SL$	$0.14 + 0.011*SL$
	tR	0.72	$0.55 + 0.086*SL$	$0.54 + 0.090*SL$	$0.49 + 0.092*SL$
	tF	0.42	$0.38 + 0.016*SL$	$0.38 + 0.016*SL$	$0.36 + 0.017*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# AO21D4/AO21D6

2-AND into 2-NOR with 4X Drive or 6X Drive

## AO21D4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{q}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.67	$0.64 + 0.012 \cdot \text{SL}$	$0.65 + 0.011 \cdot \text{SL}$	$0.65 + 0.011 \cdot \text{SL}$
	tPHL	0.41	$0.39 + 0.010 \cdot \text{SL}$	$0.40 + 0.007 \cdot \text{SL}$	$0.43 + 0.006 \cdot \text{SL}$
	tR	0.18	$0.13 + 0.023 \cdot \text{SL}$	$0.13 + 0.025 \cdot \text{SL}$	$0.11 + 0.026 \cdot \text{SL}$
	tF	0.17	$0.16 + 0.008 \cdot \text{SL}$	$0.15 + 0.009 \cdot \text{SL}$	$0.15 + 0.010 \cdot \text{SL}$
B to Y	tPLH	0.77	$0.74 + 0.012 \cdot \text{SL}$	$0.75 + 0.011 \cdot \text{SL}$	$0.75 + 0.011 \cdot \text{SL}$
	tPHL	0.39	$0.36 + 0.010 \cdot \text{SL}$	$0.37 + 0.007 \cdot \text{SL}$	$0.40 + 0.006 \cdot \text{SL}$
	tR	0.18	$0.14 + 0.023 \cdot \text{SL}$	$0.13 + 0.025 \cdot \text{SL}$	$0.12 + 0.026 \cdot \text{SL}$
	tF	0.18	$0.16 + 0.008 \cdot \text{SL}$	$0.16 + 0.009 \cdot \text{SL}$	$0.15 + 0.010 \cdot \text{SL}$
C to Y	tPLH	0.76	$0.74 + 0.012 \cdot \text{SL}$	$0.74 + 0.011 \cdot \text{SL}$	$0.74 + 0.011 \cdot \text{SL}$
	tPHL	0.41	$0.39 + 0.010 \cdot \text{SL}$	$0.40 + 0.007 \cdot \text{SL}$	$0.42 + 0.006 \cdot \text{SL}$
	tR	0.19	$0.14 + 0.022 \cdot \text{SL}$	$0.13 + 0.025 \cdot \text{SL}$	$0.11 + 0.026 \cdot \text{SL}$
	tF	0.17	$0.16 + 0.009 \cdot \text{SL}$	$0.16 + 0.009 \cdot \text{SL}$	$0.15 + 0.010 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

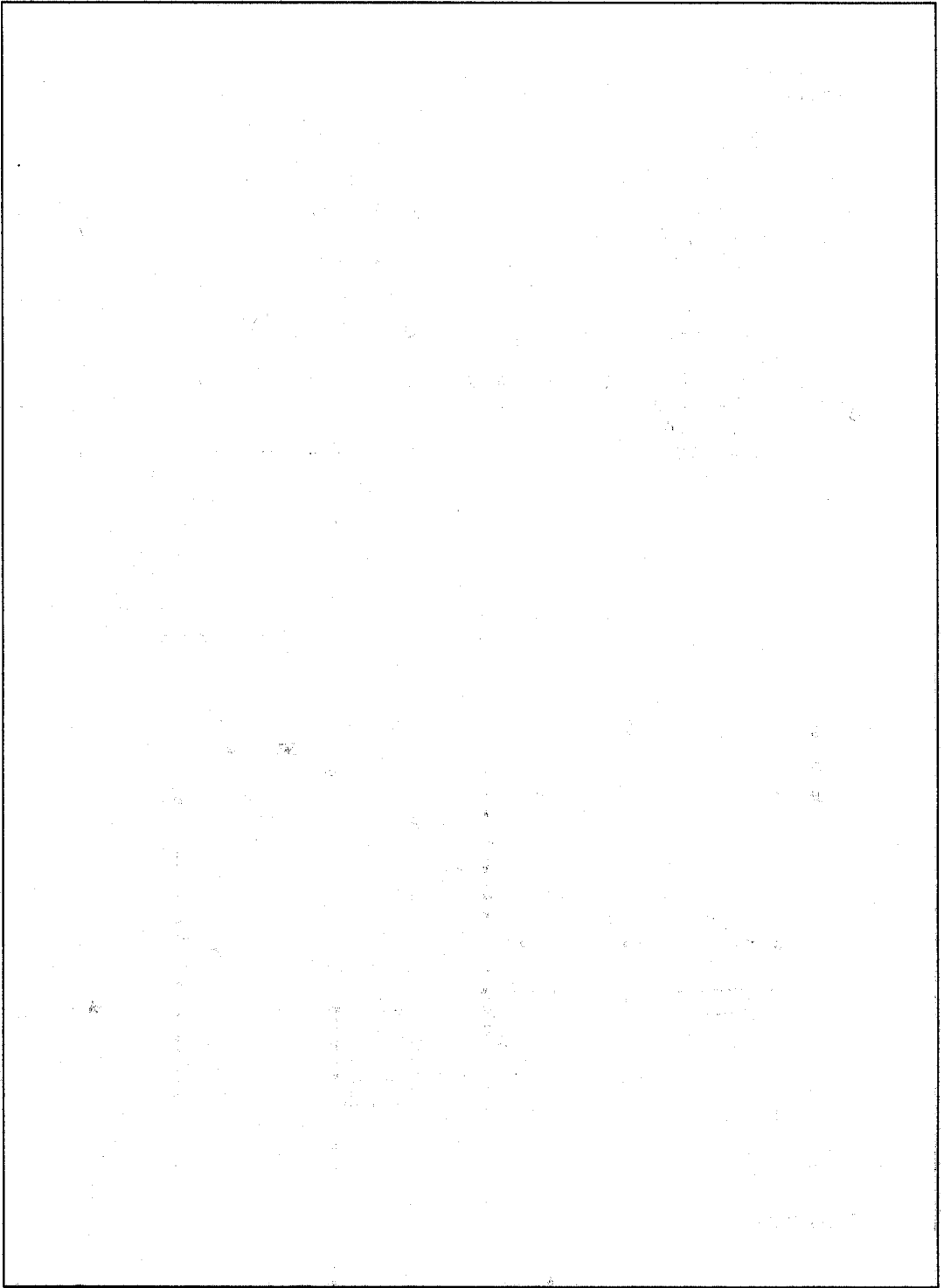
## AO21D6 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{q}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.72	$0.70 + 0.008 \cdot \text{SL}$	$0.71 + 0.007 \cdot \text{SL}$	$0.71 + 0.007 \cdot \text{SL}$
	tPHL	0.47	$0.45 + 0.008 \cdot \text{SL}$	$0.46 + 0.006 \cdot \text{SL}$	$0.49 + 0.005 \cdot \text{SL}$
	tR	0.18	$0.15 + 0.015 \cdot \text{SL}$	$0.15 + 0.016 \cdot \text{SL}$	$0.13 + 0.017 \cdot \text{SL}$
	tF	0.21	$0.20 + 0.006 \cdot \text{SL}$	$0.20 + 0.006 \cdot \text{SL}$	$0.20 + 0.006 \cdot \text{SL}$
B to Y	tPLH	0.82	$0.81 + 0.009 \cdot \text{SL}$	$0.81 + 0.007 \cdot \text{SL}$	$0.82 + 0.007 \cdot \text{SL}$
	tPHL	0.45	$0.43 + 0.008 \cdot \text{SL}$	$0.44 + 0.006 \cdot \text{SL}$	$0.47 + 0.004 \cdot \text{SL}$
	tR	0.19	$0.15 + 0.016 \cdot \text{SL}$	$0.15 + 0.016 \cdot \text{SL}$	$0.14 + 0.017 \cdot \text{SL}$
	tF	0.21	$0.19 + 0.010 \cdot \text{SL}$	$0.20 + 0.006 \cdot \text{SL}$	$0.20 + 0.006 \cdot \text{SL}$
C to Y	tPLH	0.82	$0.80 + 0.008 \cdot \text{SL}$	$0.80 + 0.007 \cdot \text{SL}$	$0.81 + 0.007 \cdot \text{SL}$
	tPHL	0.47	$0.45 + 0.008 \cdot \text{SL}$	$0.46 + 0.006 \cdot \text{SL}$	$0.49 + 0.004 \cdot \text{SL}$
	tR	0.19	$0.16 + 0.015 \cdot \text{SL}$	$0.15 + 0.016 \cdot \text{SL}$	$0.14 + 0.017 \cdot \text{SL}$
	tF	0.21	$0.19 + 0.007 \cdot \text{SL}$	$0.20 + 0.007 \cdot \text{SL}$	$0.20 + 0.006 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$



# AO21I/AO21ID3/AO21ID5/AO21ID8

2-AND into 2-OR with 1X Drive, 3X Drive, 5X Drive or 8X Drive

Inputs: A, B, C

Output: Y

Input Loading(SL):

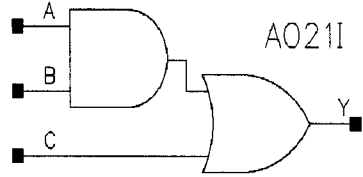
- AO21I: All: 1
- AO21ID3: All: 1
- AO21ID5: All: 1
- AO21ID8: All: 2

Maximum Fanout (Rec. SL):

- AO21I: 28
- AO21ID3: 84
- AO21ID5: 120
- AO21ID8: 224

Gate Count:

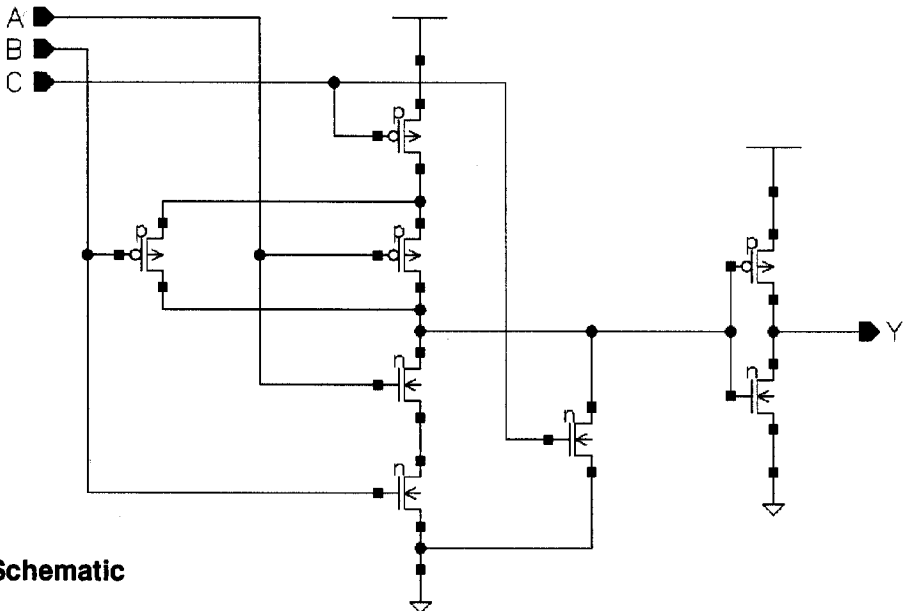
- AO21I: 2
- AO21ID3: 3
- AO21ID5: 4
- AO21ID8: 7



**Symbol**

A	B	C	Y
x	x	1	1
0	x	0	0
x	0	0	0
1	1	x	1

**Truth Table**



**Schematic**

**AO211 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.30	$0.21 + 0.044*SL$	$0.22 + 0.043*SL$	$0.22 + 0.043*SL$
	tPHL	0.50	$0.43 + 0.033*SL$	$0.46 + 0.023*SL$	$0.52 + 0.020*SL$
	tR	0.33	$0.13 + 0.098*SL$	$0.12 + 0.101*SL$	$0.09 + 0.102*SL$
	tF	0.23	$0.16 + 0.038*SL$	$0.16 + 0.037*SL$	$0.14 + 0.038*SL$
B to Y	tPLH	0.28	$0.19 + 0.045*SL$	$0.19 + 0.043*SL$	$0.19 + 0.043*SL$
	tPHL	0.59	$0.51 + 0.037*SL$	$0.55 + 0.024*SL$	$0.63 + 0.020*SL$
	tR	0.33	$0.13 + 0.098*SL$	$0.12 + 0.101*SL$	$0.09 + 0.102*SL$
	tF	0.27	$0.19 + 0.040*SL$	$0.20 + 0.036*SL$	$0.18 + 0.037*SL$
C to Y	tPLH	0.29	$0.21 + 0.043*SL$	$0.21 + 0.042*SL$	$0.20 + 0.042*SL$
	tPHL	0.58	$0.51 + 0.038*SL$	$0.55 + 0.024*SL$	$0.62 + 0.020*SL$
	tR	0.33	$0.14 + 0.096*SL$	$0.12 + 0.100*SL$	$0.09 + 0.102*SL$
	tF	0.28	$0.20 + 0.039*SL$	$0.21 + 0.036*SL$	$0.19 + 0.037*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **AO21ID3 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.35	$0.31 + 0.016*SL$	$0.32 + 0.014*SL$	$0.33 + 0.014*SL$
	tPHL	0.57	$0.54 + 0.016*SL$	$0.55 + 0.011*SL$	$0.61 + 0.008*SL$
	tR	0.22	$0.16 + 0.029*SL$	$0.16 + 0.031*SL$	$0.13 + 0.032*SL$
	tF	0.25	$0.22 + 0.015*SL$	$0.23 + 0.013*SL$	$0.24 + 0.013*SL$
B to Y	tPLH	0.31	$0.27 + 0.016*SL$	$0.28 + 0.014*SL$	$0.29 + 0.014*SL$
	tPHL	0.65	$0.61 + 0.017*SL$	$0.63 + 0.012*SL$	$0.69 + 0.009*SL$
	tR	0.22	$0.16 + 0.029*SL$	$0.16 + 0.031*SL$	$0.13 + 0.032*SL$
	tF	0.29	$0.26 + 0.016*SL$	$0.26 + 0.013*SL$	$0.28 + 0.013*SL$
C to Y	tPLH	0.31	$0.28 + 0.015*SL$	$0.28 + 0.014*SL$	$0.28 + 0.013*SL$
	tPHL	0.64	$0.60 + 0.017*SL$	$0.62 + 0.012*SL$	$0.68 + 0.009*SL$
	tR	0.21	$0.15 + 0.029*SL$	$0.15 + 0.031*SL$	$0.12 + 0.032*SL$
	tF	0.29	$0.26 + 0.016*SL$	$0.26 + 0.013*SL$	$0.28 + 0.013*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# AO21ID5/AO21ID8

2-AND into 2-OR with 5X Drive or 8X Drive

## AO21ID5 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.43	$0.41 + 0.011 * SL$	$0.42 + 0.009 * SL$	$0.43 + 0.009 * SL$
	tPHL	0.70	$0.68 + 0.011 * SL$	$0.68 + 0.008 * SL$	$0.72 + 0.006 * SL$
	tR	0.23	$0.20 + 0.016 * SL$	$0.19 + 0.019 * SL$	$0.17 + 0.020 * SL$
	tF	0.34	$0.32 + 0.009 * SL$	$0.32 + 0.009 * SL$	$0.34 + 0.008 * SL$
B to Y	tPLH	0.38	$0.36 + 0.011 * SL$	$0.36 + 0.009 * SL$	$0.38 + 0.009 * SL$
	tPHL	0.77	$0.74 + 0.012 * SL$	$0.75 + 0.009 * SL$	$0.80 + 0.007 * SL$
	tR	0.23	$0.20 + 0.016 * SL$	$0.19 + 0.019 * SL$	$0.18 + 0.020 * SL$
	tF	0.37	$0.35 + 0.010 * SL$	$0.35 + 0.009 * SL$	$0.38 + 0.008 * SL$
C to Y	tPLH	0.37	$0.35 + 0.010 * SL$	$0.36 + 0.009 * SL$	$0.37 + 0.008 * SL$
	tPHL	0.77	$0.74 + 0.012 * SL$	$0.75 + 0.009 * SL$	$0.80 + 0.007 * SL$
	tR	0.21	$0.18 + 0.017 * SL$	$0.17 + 0.019 * SL$	$0.15 + 0.020 * SL$
	tF	0.38	$0.36 + 0.010 * SL$	$0.36 + 0.009 * SL$	$0.38 + 0.008 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## AO21ID8 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.39	$0.38 + 0.007 * SL$	$0.38 + 0.006 * SL$	$0.39 + 0.005 * SL$
	tPHL	0.63	$0.62 + 0.007 * SL$	$0.62 + 0.006 * SL$	$0.65 + 0.004 * SL$
	tR	0.21	$0.19 + 0.010 * SL$	$0.19 + 0.012 * SL$	$0.18 + 0.012 * SL$
	tF	0.29	$0.28 + 0.005 * SL$	$0.28 + 0.006 * SL$	$0.29 + 0.005 * SL$
B to Y	tPLH	0.35	$0.33 + 0.008 * SL$	$0.34 + 0.006 * SL$	$0.34 + 0.006 * SL$
	tPHL	0.71	$0.69 + 0.007 * SL$	$0.70 + 0.006 * SL$	$0.72 + 0.005 * SL$
	tR	0.22	$0.20 + 0.010 * SL$	$0.19 + 0.012 * SL$	$0.18 + 0.012 * SL$
	tF	0.33	$0.32 + 0.005 * SL$	$0.32 + 0.006 * SL$	$0.33 + 0.005 * SL$
C to Y	tPLH	0.34	$0.32 + 0.007 * SL$	$0.32 + 0.006 * SL$	$0.33 + 0.005 * SL$
	tPHL	0.71	$0.69 + 0.008 * SL$	$0.70 + 0.006 * SL$	$0.73 + 0.005 * SL$
	tR	0.19	$0.17 + 0.012 * SL$	$0.17 + 0.012 * SL$	$0.16 + 0.012 * SL$
	tF	0.33	$0.31 + 0.009 * SL$	$0.32 + 0.006 * SL$	$0.33 + 0.005 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$





# AO211/AO211D2/AO211D3/AO211D7

2-AND into 3-NOR with 1X Drive, 2X Drive, 3X Drive or 7X Drive

Inputs: A, B, C, D

Output: Y

Input Loading(SL):

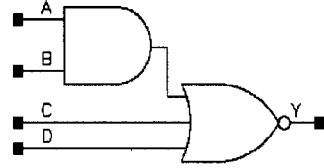
- AO211: All : 1
- AO211D2: All : 2
- AO211D3: All: 1
- AO211D7: All: 1

Maximum Fanout (Rec. SL):

- AO211: 9
- AO211D2: 18
- AO211D3: 84
- AO211D7: 196

Gate Count:

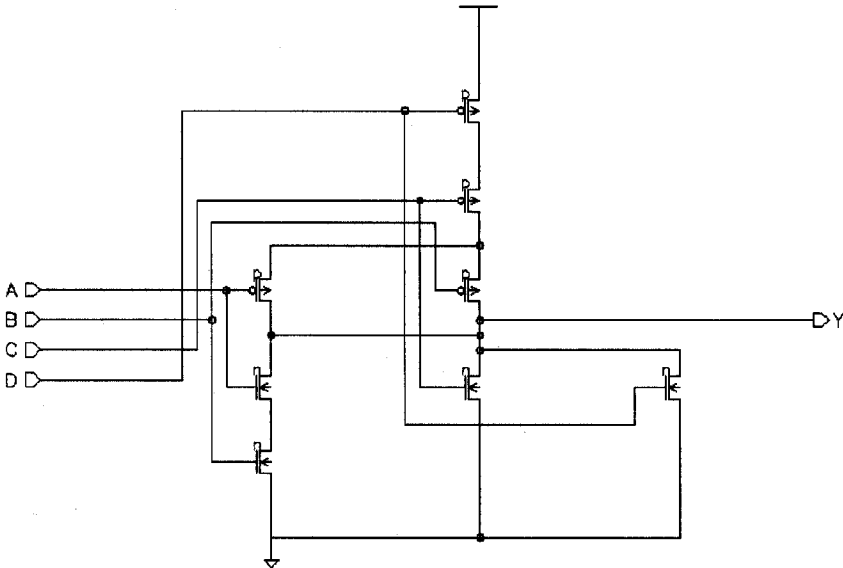
- AO211: 2
- AO211D2: 4
- AO211D3: 4
- AO211D7: 6



**Symbol**

A	B	C	D	Y
1	1	x	x	0
x	x	1	x	0
x	x	x	1	0
x	0	0	0	1
0	x	0	0	1

**Truth Table**



**Schematic**

**AO211 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.65	$0.43 + 0.110 \cdot \text{SL}$	$0.41 + 0.114 \cdot \text{SL}$	$0.37 + 0.116 \cdot \text{SL}$
	tPHL	0.17	$0.08 + 0.049 \cdot \text{SL}$	$0.12 + 0.034 \cdot \text{SL}$	$0.18 + 0.031 \cdot \text{SL}$
	tR	1.30	$0.75 + 0.275 \cdot \text{SL}$	$0.72 + 0.285 \cdot \text{SL}$	$0.70 + 0.286 \cdot \text{SL}$
	tF	0.46	$0.33 + 0.064 \cdot \text{SL}$	$0.33 + 0.063 \cdot \text{SL}$	$0.25 + 0.067 \cdot \text{SL}$
B to Y	tPLH	0.77	$0.55 + 0.109 \cdot \text{SL}$	$0.54 + 0.114 \cdot \text{SL}$	$0.49 + 0.116 \cdot \text{SL}$
	tPHL	0.14	$0.05 + 0.041 \cdot \text{SL}$	$0.08 + 0.032 \cdot \text{SL}$	$0.11 + 0.031 \cdot \text{SL}$
	tR	1.49	$0.94 + 0.275 \cdot \text{SL}$	$0.92 + 0.285 \cdot \text{SL}$	$0.89 + 0.286 \cdot \text{SL}$
	tF	0.43	$0.31 + 0.059 \cdot \text{SL}$	$0.29 + 0.064 \cdot \text{SL}$	$0.21 + 0.068 \cdot \text{SL}$
C to Y	tPLH	0.83	$0.61 + 0.113 \cdot \text{SL}$	$0.60 + 0.115 \cdot \text{SL}$	$0.58 + 0.117 \cdot \text{SL}$
	tPHL	0.14	$0.07 + 0.037 \cdot \text{SL}$	$0.11 + 0.024 \cdot \text{SL}$	$0.18 + 0.020 \cdot \text{SL}$
	tR	1.51	$0.95 + 0.278 \cdot \text{SL}$	$0.93 + 0.284 \cdot \text{SL}$	$0.90 + 0.286 \cdot \text{SL}$
	tF	0.46	$0.39 + 0.035 \cdot \text{SL}$	$0.39 + 0.035 \cdot \text{SL}$	$0.33 + 0.039 \cdot \text{SL}$
D to Y	tPLH	0.83	$0.60 + 0.114 \cdot \text{SL}$	$0.60 + 0.116 \cdot \text{SL}$	$0.58 + 0.117 \cdot \text{SL}$
	tPHL	0.15	$0.07 + 0.038 \cdot \text{SL}$	$0.11 + 0.025 \cdot \text{SL}$	$0.19 + 0.021 \cdot \text{SL}$
	tR	1.50	$0.94 + 0.279 \cdot \text{SL}$	$0.93 + 0.285 \cdot \text{SL}$	$0.90 + 0.286 \cdot \text{SL}$
	tF	0.49	$0.42 + 0.035 \cdot \text{SL}$	$0.42 + 0.036 \cdot \text{SL}$	$0.36 + 0.039 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **AO211D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.53	$0.42 + 0.053 \cdot \text{SL}$	$0.42 + 0.055 \cdot \text{SL}$	$0.39 + 0.056 \cdot \text{SL}$
	tPHL	0.12	$0.07 + 0.027 \cdot \text{SL}$	$0.09 + 0.019 \cdot \text{SL}$	$0.16 + 0.015 \cdot \text{SL}$
	tR	1.01	$0.74 + 0.132 \cdot \text{SL}$	$0.73 + 0.136 \cdot \text{SL}$	$0.68 + 0.139 \cdot \text{SL}$
	tF	0.39	$0.33 + 0.033 \cdot \text{SL}$	$0.34 + 0.030 \cdot \text{SL}$	$0.31 + 0.031 \cdot \text{SL}$
B to Y	tPLH	0.65	$0.55 + 0.052 \cdot \text{SL}$	$0.54 + 0.054 \cdot \text{SL}$	$0.51 + 0.056 \cdot \text{SL}$
	tPHL	0.09	$0.05 + 0.023 \cdot \text{SL}$	$0.06 + 0.017 \cdot \text{SL}$	$0.10 + 0.015 \cdot \text{SL}$
	tR	1.20	$0.93 + 0.132 \cdot \text{SL}$	$0.92 + 0.137 \cdot \text{SL}$	$0.88 + 0.139 \cdot \text{SL}$
	tF	0.36	$0.31 + 0.028 \cdot \text{SL}$	$0.30 + 0.030 \cdot \text{SL}$	$0.26 + 0.032 \cdot \text{SL}$
C to Y	tPLH	0.71	$0.60 + 0.055 \cdot \text{SL}$	$0.60 + 0.056 \cdot \text{SL}$	$0.59 + 0.056 \cdot \text{SL}$
	tPHL	0.10	$0.06 + 0.020 \cdot \text{SL}$	$0.08 + 0.014 \cdot \text{SL}$	$0.15 + 0.011 \cdot \text{SL}$
	tR	1.20	$0.94 + 0.134 \cdot \text{SL}$	$0.93 + 0.137 \cdot \text{SL}$	$0.90 + 0.138 \cdot \text{SL}$
	tF	0.42	$0.39 + 0.017 \cdot \text{SL}$	$0.39 + 0.017 \cdot \text{SL}$	$0.37 + 0.017 \cdot \text{SL}$
D to Y	tPLH	0.71	$0.60 + 0.055 \cdot \text{SL}$	$0.60 + 0.056 \cdot \text{SL}$	$0.58 + 0.056 \cdot \text{SL}$
	tPHL	0.11	$0.07 + 0.021 \cdot \text{SL}$	$0.08 + 0.015 \cdot \text{SL}$	$0.16 + 0.011 \cdot \text{SL}$
	tR	1.20	$0.93 + 0.134 \cdot \text{SL}$	$0.92 + 0.137 \cdot \text{SL}$	$0.89 + 0.138 \cdot \text{SL}$
	tF	0.45	$0.42 + 0.017 \cdot \text{SL}$	$0.42 + 0.016 \cdot \text{SL}$	$0.40 + 0.017 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

# AO211D3/AO211D7

2-AND into 3-NOR with 3X Drive or 7X Drive

## AO211D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	$t_{PLH}$	0.77	$0.74 + 0.015*SL$	$0.74 + 0.014*SL$	$0.74 + 0.014*SL$
	$t_{PHL}$	0.39	$0.37 + 0.012*SL$	$0.38 + 0.009*SL$	$0.41 + 0.007*SL$
	$t_R$	0.20	$0.13 + 0.032*SL$	$0.13 + 0.033*SL$	$0.10 + 0.034*SL$
	$t_F$	0.16	$0.14 + 0.011*SL$	$0.13 + 0.013*SL$	$0.12 + 0.013*SL$
B to Y	$t_{PLH}$	0.89	$0.86 + 0.015*SL$	$0.87 + 0.014*SL$	$0.87 + 0.014*SL$
	$t_{PHL}$	0.37	$0.35 + 0.012*SL$	$0.35 + 0.009*SL$	$0.39 + 0.007*SL$
	$t_R$	0.20	$0.14 + 0.031*SL$	$0.14 + 0.033*SL$	$0.11 + 0.034*SL$
	$t_F$	0.16	$0.13 + 0.012*SL$	$0.13 + 0.013*SL$	$0.12 + 0.013*SL$
C to Y	$t_{PLH}$	0.95	$0.92 + 0.015*SL$	$0.92 + 0.014*SL$	$0.92 + 0.014*SL$
	$t_{PHL}$	0.39	$0.36 + 0.013*SL$	$0.37 + 0.009*SL$	$0.40 + 0.007*SL$
	$t_R$	0.20	$0.14 + 0.030*SL$	$0.14 + 0.033*SL$	$0.11 + 0.034*SL$
	$t_F$	0.16	$0.13 + 0.012*SL$	$0.13 + 0.013*SL$	$0.12 + 0.013*SL$
D to Y	$t_{PLH}$	0.95	$0.92 + 0.015*SL$	$0.92 + 0.014*SL$	$0.92 + 0.014*SL$
	$t_{PHL}$	0.40	$0.38 + 0.012*SL$	$0.39 + 0.009*SL$	$0.42 + 0.007*SL$
	$t_R$	0.20	$0.14 + 0.032*SL$	$0.14 + 0.033*SL$	$0.11 + 0.034*SL$
	$t_F$	0.16	$0.13 + 0.012*SL$	$0.13 + 0.013*SL$	$0.12 + 0.013*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

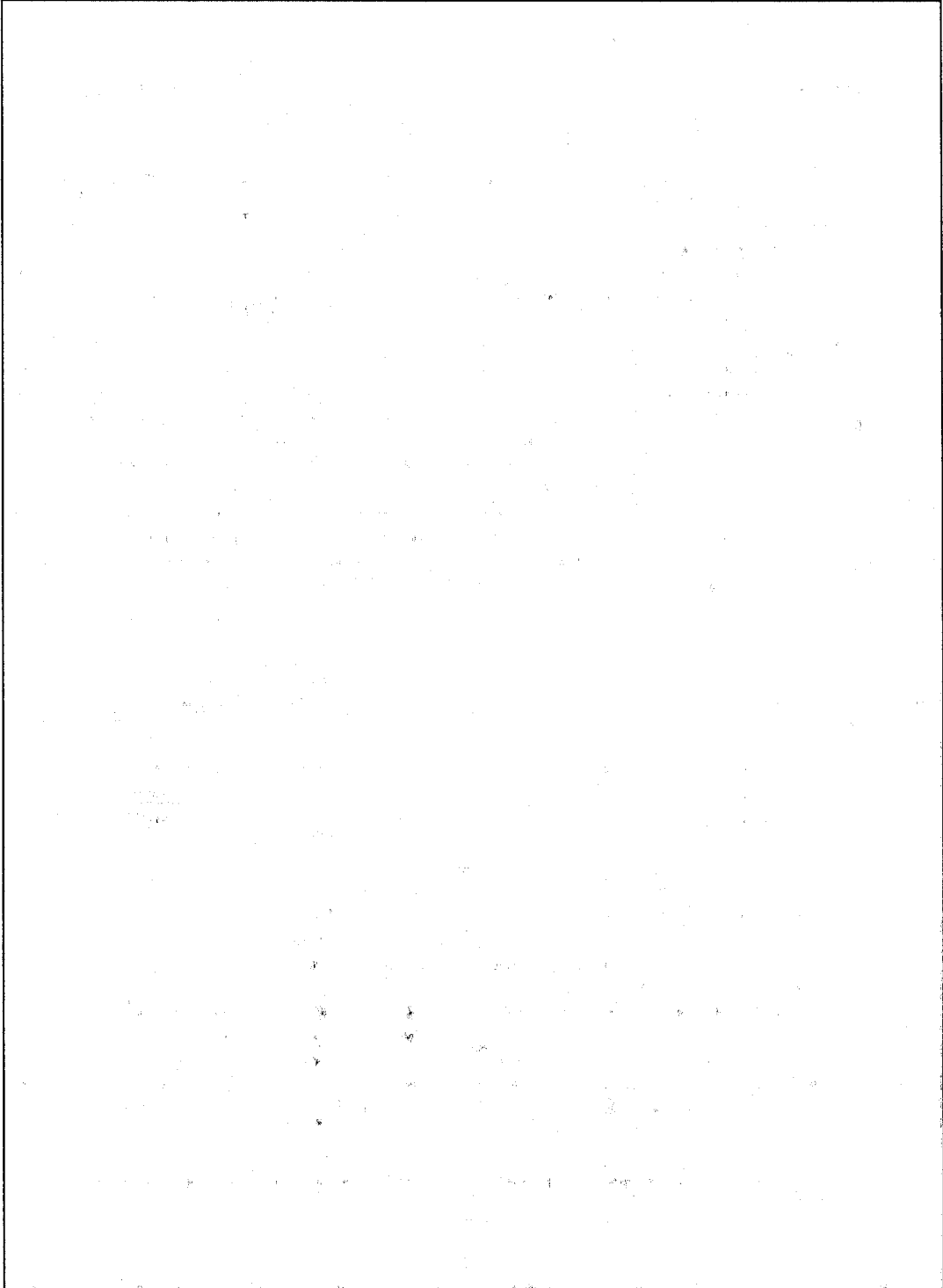
## AO211D7 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	$t_{PLH}$	0.90	$0.88 + 0.007*SL$	$0.88 + 0.006*SL$	$0.89 + 0.006*SL$
	$t_{PHL}$	0.52	$0.51 + 0.007*SL$	$0.51 + 0.005*SL$	$0.54 + 0.004*SL$
	$t_R$	0.20	$0.18 + 0.012*SL$	$0.17 + 0.013*SL$	$0.16 + 0.014*SL$
	$t_F$	0.23	$0.22 + 0.006*SL$	$0.22 + 0.006*SL$	$0.23 + 0.005*SL$
B to Y	$t_{PLH}$	1.03	$1.02 + 0.007*SL$	$1.02 + 0.006*SL$	$1.03 + 0.006*SL$
	$t_{PHL}$	0.50	$0.48 + 0.007*SL$	$0.49 + 0.005*SL$	$0.51 + 0.004*SL$
	$t_R$	0.21	$0.19 + 0.011*SL$	$0.18 + 0.013*SL$	$0.17 + 0.014*SL$
	$t_F$	0.23	$0.22 + 0.005*SL$	$0.22 + 0.006*SL$	$0.23 + 0.005*SL$
C to Y	$t_{PLH}$	1.09	$1.07 + 0.007*SL$	$1.08 + 0.006*SL$	$1.08 + 0.006*SL$
	$t_{PHL}$	0.51	$0.50 + 0.007*SL$	$0.51 + 0.005*SL$	$0.53 + 0.004*SL$
	$t_R$	0.21	$0.18 + 0.013*SL$	$0.18 + 0.013*SL$	$0.17 + 0.014*SL$
	$t_F$	0.23	$0.23 + 0.003*SL$	$0.22 + 0.006*SL$	$0.23 + 0.005*SL$
D to Y	$t_{PLH}$	1.09	$1.07 + 0.007*SL$	$1.07 + 0.006*SL$	$1.08 + 0.006*SL$
	$t_{PHL}$	0.53	$0.52 + 0.007*SL$	$0.52 + 0.005*SL$	$0.54 + 0.004*SL$
	$t_R$	0.21	$0.19 + 0.012*SL$	$0.18 + 0.013*SL$	$0.17 + 0.014*SL$
	$t_F$	0.23	$0.22 + 0.006*SL$	$0.22 + 0.006*SL$	$0.23 + 0.005*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# AO22/AO22D2/AO22D3/AO22D7

2 2-AND into 2-NOR with 1X Drive, 2X Drive, 3X Drive Or 7X Drive

Inputs: A, B, C, D

Output: Y

Input Loading(SL):

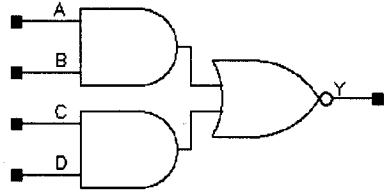
- AO22: All : 1
- AO22D2: All : 2
- AO22D3: All : 1
- AO22D7: All : 1

Maximum Fanout (Rec. SL):

- AO22: 14
- AO22D2: 28
- AO22D3: 84
- AO22D7: 196

Gate Count:

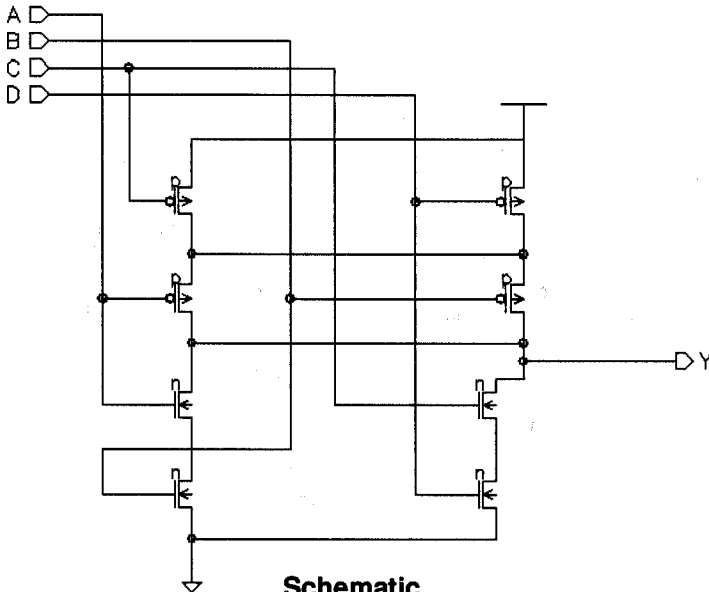
- AO22: 2
- AO22D2: 4
- AO22D3: 5
- AO22D7: 7



**Symbol**

A	B	C	D	Y
1	1	x	x	0
x	x	1	1	0
0	x	0	x	1
0	x	x	0	1
x	0	x	0	1
x	0	0	x	1

**Truth Table**



**Schematic**

**AO22 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.55	$0.40 + 0.072*SL$	$0.40 + 0.073*SL$	$0.37 + 0.074*SL$
	tPHL	0.19	$0.10 + 0.047*SL$	$0.14 + 0.033*SL$	$0.18 + 0.031*SL$
	tR	0.89	$0.56 + 0.167*SL$	$0.53 + 0.176*SL$	$0.47 + 0.180*SL$
	tF	0.52	$0.41 + 0.057*SL$	$0.39 + 0.062*SL$	$0.30 + 0.067*SL$
B to Y	tPLH	0.63	$0.49 + 0.070*SL$	$0.48 + 0.073*SL$	$0.45 + 0.074*SL$
	tPHL	0.15	$0.07 + 0.040*SL$	$0.09 + 0.032*SL$	$0.12 + 0.031*SL$
	tR	1.02	$0.69 + 0.166*SL$	$0.66 + 0.176*SL$	$0.59 + 0.180*SL$
	tF	0.48	$0.37 + 0.055*SL$	$0.35 + 0.063*SL$	$0.26 + 0.068*SL$
C to Y	tPLH	0.56	$0.41 + 0.075*SL$	$0.41 + 0.075*SL$	$0.39 + 0.076*SL$
	tPHL	0.25	$0.16 + 0.043*SL$	$0.19 + 0.033*SL$	$0.23 + 0.031*SL$
	tR	0.91	$0.57 + 0.171*SL$	$0.54 + 0.180*SL$	$0.48 + 0.183*SL$
	tF	0.63	$0.52 + 0.054*SL$	$0.50 + 0.062*SL$	$0.39 + 0.067*SL$
D to Y	tPLH	0.63	$0.49 + 0.072*SL$	$0.48 + 0.074*SL$	$0.46 + 0.075*SL$
	tPHL	0.20	$0.12 + 0.039*SL$	$0.14 + 0.032*SL$	$0.16 + 0.031*SL$
	tR	1.02	$0.68 + 0.168*SL$	$0.65 + 0.177*SL$	$0.59 + 0.180*SL$
	tF	0.58	$0.48 + 0.053*SL$	$0.45 + 0.063*SL$	$0.35 + 0.068*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **AO22D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.49	$0.41 + 0.038*SL$	$0.41 + 0.037*SL$	$0.40 + 0.038*SL$
	tPHL	0.14	$0.09 + 0.026*SL$	$0.11 + 0.019*SL$	$0.17 + 0.015*SL$
	tR	0.76	$0.58 + 0.086*SL$	$0.57 + 0.091*SL$	$0.51 + 0.094*SL$
	tF	0.46	$0.40 + 0.029*SL$	$0.40 + 0.029*SL$	$0.36 + 0.031*SL$
B to Y	tPLH	0.57	$0.50 + 0.036*SL$	$0.50 + 0.037*SL$	$0.48 + 0.038*SL$
	tPHL	0.10	$0.06 + 0.022*SL$	$0.07 + 0.017*SL$	$0.11 + 0.015*SL$
	tR	0.88	$0.71 + 0.085*SL$	$0.69 + 0.089*SL$	$0.64 + 0.092*SL$
	tF	0.42	$0.37 + 0.026*SL$	$0.36 + 0.029*SL$	$0.31 + 0.032*SL$
C to Y	tPLH	0.49	$0.41 + 0.038*SL$	$0.41 + 0.038*SL$	$0.40 + 0.038*SL$
	tPHL	0.20	$0.15 + 0.023*SL$	$0.17 + 0.018*SL$	$0.22 + 0.015*SL$
	tR	0.75	$0.58 + 0.085*SL$	$0.57 + 0.090*SL$	$0.52 + 0.093*SL$
	tF	0.57	$0.52 + 0.025*SL$	$0.51 + 0.028*SL$	$0.46 + 0.031*SL$
D to Y	tPLH	0.57	$0.50 + 0.036*SL$	$0.50 + 0.037*SL$	$0.48 + 0.038*SL$
	tPHL	0.15	$0.11 + 0.021*SL$	$0.12 + 0.017*SL$	$0.15 + 0.015*SL$
	tR	0.87	$0.70 + 0.086*SL$	$0.69 + 0.089*SL$	$0.64 + 0.092*SL$
	tF	0.52	$0.47 + 0.024*SL$	$0.46 + 0.029*SL$	$0.40 + 0.031*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# AO22D3/AO22D7

2 2-AND into 2-NOR with 3X Drive Or 7X Drive

## AO22D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.73	$0.70 + 0.016*SL$	$0.70 + 0.014*SL$	$0.70 + 0.014*SL$
	tPHL	0.43	$0.41 + 0.012*SL$	$0.42 + 0.009*SL$	$0.45 + 0.007*SL$
	tR	0.19	$0.13 + 0.032*SL$	$0.12 + 0.033*SL$	$0.10 + 0.034*SL$
	tF	0.16	$0.14 + 0.013*SL$	$0.14 + 0.012*SL$	$0.13 + 0.013*SL$
B to Y	tPLH	0.82	$0.79 + 0.016*SL$	$0.79 + 0.014*SL$	$0.79 + 0.014*SL$
	tPHL	0.40	$0.37 + 0.012*SL$	$0.38 + 0.009*SL$	$0.42 + 0.007*SL$
	tR	0.20	$0.13 + 0.032*SL$	$0.13 + 0.033*SL$	$0.10 + 0.034*SL$
	tF	0.16	$0.14 + 0.011*SL$	$0.13 + 0.013*SL$	$0.13 + 0.013*SL$
C to Y	tPLH	0.73	$0.70 + 0.015*SL$	$0.70 + 0.014*SL$	$0.70 + 0.014*SL$
	tPHL	0.51	$0.49 + 0.013*SL$	$0.50 + 0.009*SL$	$0.53 + 0.007*SL$
	tR	0.19	$0.13 + 0.030*SL$	$0.12 + 0.033*SL$	$0.10 + 0.034*SL$
	tF	0.16	$0.14 + 0.013*SL$	$0.14 + 0.012*SL$	$0.13 + 0.013*SL$
D to Y	tPLH	0.82	$0.79 + 0.015*SL$	$0.80 + 0.014*SL$	$0.79 + 0.014*SL$
	tPHL	0.47	$0.44 + 0.013*SL$	$0.45 + 0.009*SL$	$0.48 + 0.007*SL$
	tR	0.20	$0.13 + 0.031*SL$	$0.13 + 0.033*SL$	$0.10 + 0.034*SL$
	tF	0.17	$0.14 + 0.012*SL$	$0.14 + 0.012*SL$	$0.13 + 0.013*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

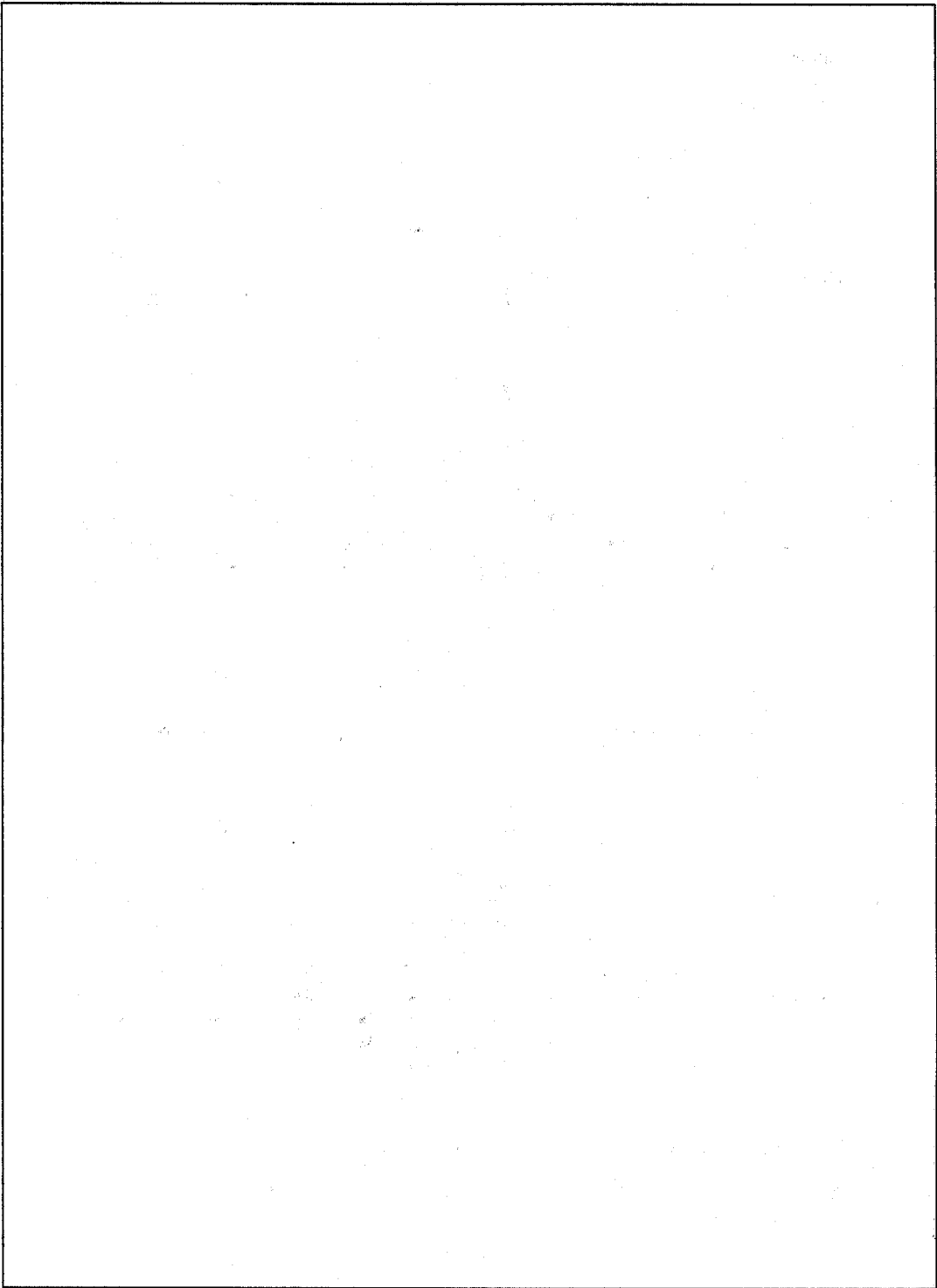
## AO22D7 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.85	$0.83 + 0.007*SL$	$0.84 + 0.006*SL$	$0.84 + 0.006*SL$
	tPHL	0.56	$0.55 + 0.007*SL$	$0.55 + 0.005*SL$	$0.58 + 0.004*SL$
	tR	0.19	$0.17 + 0.012*SL$	$0.16 + 0.013*SL$	$0.15 + 0.014*SL$
	tF	0.24	$0.23 + 0.002*SL$	$0.22 + 0.006*SL$	$0.23 + 0.005*SL$
B to Y	tPLH	0.95	$0.93 + 0.007*SL$	$0.94 + 0.006*SL$	$0.94 + 0.006*SL$
	tPHL	0.53	$0.52 + 0.007*SL$	$0.52 + 0.005*SL$	$0.54 + 0.004*SL$
	tR	0.20	$0.18 + 0.011*SL$	$0.17 + 0.013*SL$	$0.16 + 0.014*SL$
	tF	0.24	$0.22 + 0.006*SL$	$0.22 + 0.006*SL$	$0.23 + 0.005*SL$
C to Y	tPLH	0.85	$0.84 + 0.007*SL$	$0.84 + 0.006*SL$	$0.85 + 0.006*SL$
	tPHL	0.64	$0.63 + 0.007*SL$	$0.63 + 0.005*SL$	$0.66 + 0.004*SL$
	tR	0.19	$0.17 + 0.012*SL$	$0.16 + 0.013*SL$	$0.15 + 0.014*SL$
	tF	0.24	$0.23 + 0.005*SL$	$0.23 + 0.006*SL$	$0.23 + 0.005*SL$
D to Y	tPLH	0.95	$0.93 + 0.007*SL$	$0.94 + 0.006*SL$	$0.95 + 0.006*SL$
	tPHL	0.60	$0.59 + 0.006*SL$	$0.59 + 0.005*SL$	$0.61 + 0.004*SL$
	tR	0.20	$0.17 + 0.012*SL$	$0.17 + 0.013*SL$	$0.15 + 0.014*SL$
	tF	0.24	$0.24 + 0.003*SL$	$0.23 + 0.006*SL$	$0.24 + 0.005*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$





# AO22A/AO22D2A

2-AND and 2-invert-AND into 2-NOR with 1X Drive or 2X Drive

Inputs: A, B, C, D

Output: Y

Input Loading (SL):

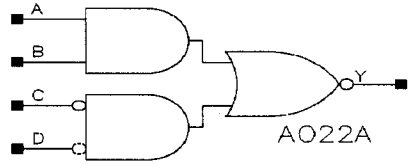
- AO22A: All : 1
- AO22D2A: A,B : 2  
C,D : 1

Maximum Fanout (Rec. SL):

- AO22A: 14
- AO22D2A: 28

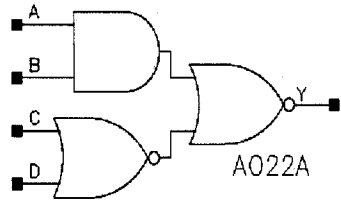
Gate Count:

- AO22A: 3
- AO22D2A: 5

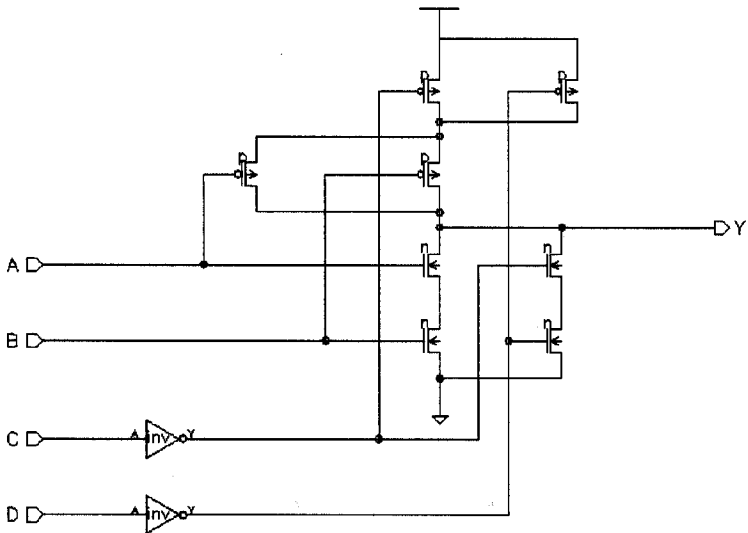


A	B	C	D	Y
1	1	x	x	0
0	x	1	x	1
0	x	x	1	1
x	0	1	x	1
x	0	x	1	1
x	x	0	0	0

**Truth Table**



**Symbols**



**Schematic**

**AO22A Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.55	$0.41 + 0.073*SL$	$0.40 + 0.074*SL$	$0.38 + 0.075*SL$
	tPHL	0.18	$0.08 + 0.046*SL$	$0.13 + 0.032*SL$	$0.18 + 0.029*SL$
	tR	0.90	$0.56 + 0.169*SL$	$0.53 + 0.179*SL$	$0.47 + 0.182*SL$
	tF	0.50	$0.39 + 0.054*SL$	$0.38 + 0.057*SL$	$0.29 + 0.062*SL$
B to Y	tPLH	0.63	$0.49 + 0.071*SL$	$0.48 + 0.074*SL$	$0.45 + 0.075*SL$
	tPHL	0.14	$0.06 + 0.040*SL$	$0.08 + 0.031*SL$	$0.12 + 0.029*SL$
	tR	1.02	$0.68 + 0.169*SL$	$0.66 + 0.179*SL$	$0.60 + 0.182*SL$
	tF	0.46	$0.36 + 0.051*SL$	$0.34 + 0.058*SL$	$0.25 + 0.063*SL$
C to Y	tPLH	0.49	$0.33 + 0.078*SL$	$0.34 + 0.076*SL$	$0.35 + 0.076*SL$
	tPHL	0.46	$0.39 + 0.035*SL$	$0.41 + 0.031*SL$	$0.42 + 0.031*SL$
	tR	0.84	$0.49 + 0.178*SL$	$0.48 + 0.181*SL$	$0.47 + 0.182*SL$
	tF	0.45	$0.33 + 0.061*SL$	$0.31 + 0.065*SL$	$0.28 + 0.067*SL$
D to Y	tPLH	0.56	$0.41 + 0.077*SL$	$0.41 + 0.076*SL$	$0.42 + 0.076*SL$
	tPHL	0.46	$0.39 + 0.035*SL$	$0.40 + 0.031*SL$	$0.42 + 0.031*SL$
	tR	0.97	$0.61 + 0.179*SL$	$0.60 + 0.181*SL$	$0.59 + 0.182*SL$
	tF	0.44	$0.31 + 0.061*SL$	$0.30 + 0.065*SL$	$0.28 + 0.067*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **AO22D2A Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.50	$0.42 + 0.040*SL$	$0.42 + 0.040*SL$	$0.41 + 0.040*SL$
	tPHL	0.13	$0.08 + 0.026*SL$	$0.10 + 0.019*SL$	$0.17 + 0.015*SL$
	tR	0.80	$0.62 + 0.092*SL$	$0.60 + 0.097*SL$	$0.55 + 0.100*SL$
	tF	0.46	$0.40 + 0.028*SL$	$0.40 + 0.029*SL$	$0.36 + 0.031*SL$
B to Y	tPLH	0.59	$0.51 + 0.038*SL$	$0.51 + 0.039*SL$	$0.49 + 0.040*SL$
	tPHL	0.10	$0.05 + 0.022*SL$	$0.07 + 0.017*SL$	$0.11 + 0.015*SL$
	tR	0.92	$0.74 + 0.091*SL$	$0.73 + 0.095*SL$	$0.67 + 0.098*SL$
	tF	0.42	$0.37 + 0.026*SL$	$0.36 + 0.029*SL$	$0.30 + 0.031*SL$
C to Y	tPLH	0.46	$0.38 + 0.040*SL$	$0.38 + 0.039*SL$	$0.39 + 0.039*SL$
	tPHL	0.50	$0.46 + 0.019*SL$	$0.46 + 0.017*SL$	$0.48 + 0.016*SL$
	tR	0.69	$0.51 + 0.091*SL$	$0.50 + 0.093*SL$	$0.49 + 0.093*SL$
	tF	0.42	$0.37 + 0.029*SL$	$0.36 + 0.032*SL$	$0.32 + 0.034*SL$
D to Y	tPLH	0.55	$0.47 + 0.042*SL$	$0.47 + 0.041*SL$	$0.48 + 0.041*SL$
	tPHL	0.49	$0.46 + 0.019*SL$	$0.46 + 0.017*SL$	$0.48 + 0.016*SL$
	tR	0.87	$0.68 + 0.095*SL$	$0.67 + 0.097*SL$	$0.66 + 0.098*SL$
	tF	0.41	$0.35 + 0.031*SL$	$0.34 + 0.033*SL$	$0.32 + 0.034*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# AO222/AO222D3/AO222D7

3 2-AND into 3-NOR with 3X Drive ans 7X Drive

Inputs: A, B, C, D, E, F

Output: Y

Input Loading (SL):

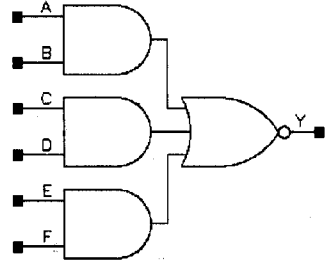
- AO222: All : 1
- AO222D3: All : 1
- AO222D7: All: 1

Maximum Fanout (Rec. SL):

- AO222: 9
- AO222D3: 84
- AO222D7: 196

Gate Count:

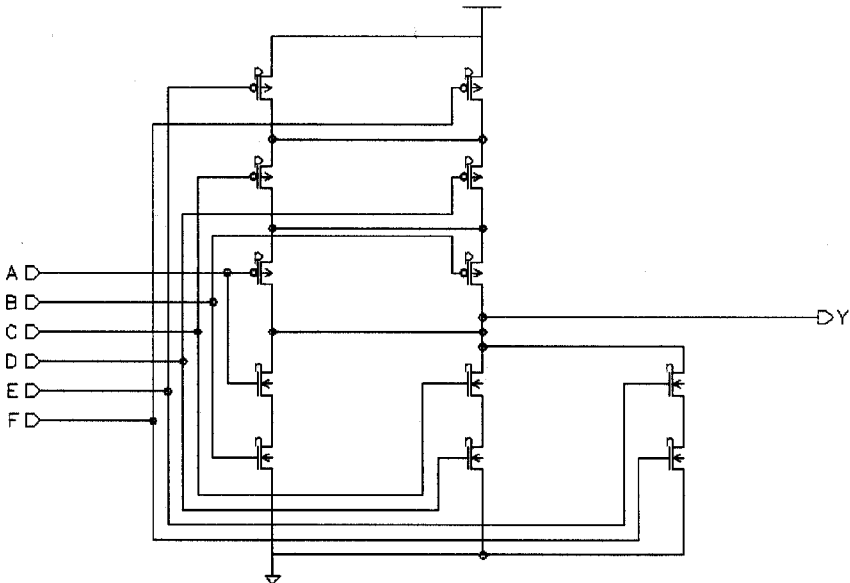
- AO222: 3
- AO222D3: 5
- AO222D7: 7



**Symbol**

A	B	C	D	E	F	Y
1	1	x	x	x	x	0
x	x	1	1	x	x	0
x	x	x	x	1	1	0
other states						1

**Truth Table**



**Schematic**

**AO222 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	$t_{PLH}$	0.85	$0.63 + 0.108*SL$	$0.63 + 0.111*SL$	$0.60 + 0.112*SL$
	$t_{PHL}$	0.22	$0.14 + 0.044*SL$	$0.17 + 0.033*SL$	$0.21 + 0.031*SL$
	$t_R$	1.65	$1.11 + 0.268*SL$	$1.09 + 0.274*SL$	$1.09 + 0.274*SL$
	$t_F$	0.61	$0.50 + 0.057*SL$	$0.48 + 0.063*SL$	$0.39 + 0.067*SL$
B to Y	$t_{PLH}$	0.97	$0.75 + 0.107*SL$	$0.74 + 0.110*SL$	$0.71 + 0.112*SL$
	$t_{PHL}$	0.18	$0.10 + 0.038*SL$	$0.12 + 0.032*SL$	$0.14 + 0.031*SL$
	$t_R$	1.83	$1.29 + 0.269*SL$	$1.28 + 0.274*SL$	$1.27 + 0.275*SL$
	$t_F$	0.57	$0.46 + 0.055*SL$	$0.43 + 0.064*SL$	$0.35 + 0.068*SL$
C to Y	$t_{PLH}$	0.96	$0.73 + 0.114*SL$	$0.73 + 0.115*SL$	$0.72 + 0.116*SL$
	$t_{PHL}$	0.28	$0.20 + 0.041*SL$	$0.22 + 0.033*SL$	$0.26 + 0.031*SL$
	$t_R$	1.73	$1.18 + 0.276*SL$	$1.16 + 0.281*SL$	$1.13 + 0.283*SL$
	$t_F$	0.71	$0.60 + 0.055*SL$	$0.58 + 0.062*SL$	$0.48 + 0.067*SL$
D to Y	$t_{PLH}$	1.05	$0.83 + 0.110*SL$	$0.83 + 0.112*SL$	$0.82 + 0.112*SL$
	$t_{PHL}$	0.22	$0.15 + 0.038*SL$	$0.17 + 0.032*SL$	$0.19 + 0.031*SL$
	$t_R$	1.86	$1.32 + 0.268*SL$	$1.31 + 0.273*SL$	$1.28 + 0.274*SL$
	$t_F$	0.66	$0.55 + 0.055*SL$	$0.53 + 0.063*SL$	$0.44 + 0.068*SL$
E to Y	$t_{PLH}$	0.99	$0.76 + 0.114*SL$	$0.76 + 0.114*SL$	$0.77 + 0.114*SL$
	$t_{PHL}$	0.30	$0.21 + 0.043*SL$	$0.24 + 0.034*SL$	$0.28 + 0.031*SL$
	$t_R$	1.70	$1.16 + 0.272*SL$	$1.14 + 0.277*SL$	$1.12 + 0.278*SL$
	$t_F$	0.81	$0.70 + 0.055*SL$	$0.68 + 0.062*SL$	$0.58 + 0.067*SL$
F to Y	$t_{PLH}$	1.10	$0.87 + 0.112*SL$	$0.87 + 0.112*SL$	$0.87 + 0.112*SL$
	$t_{PHL}$	0.24	$0.16 + 0.040*SL$	$0.17 + 0.033*SL$	$0.22 + 0.031*SL$
	$t_R$	1.86	$1.32 + 0.269*SL$	$1.30 + 0.273*SL$	$1.28 + 0.274*SL$
	$t_F$	0.76	$0.65 + 0.056*SL$	$0.62 + 0.064*SL$	$0.54 + 0.068*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# AO222D3

3 2-AND into 3-NOR with 3X Drive

## AO222D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	1.00	$0.97 + 0.016 * SL$	$0.98 + 0.014 * SL$	$0.98 + 0.014 * SL$
	tPHL	0.49	$0.47 + 0.012 * SL$	$0.48 + 0.009 * SL$	$0.51 + 0.007 * SL$
	tR	0.21	$0.15 + 0.030 * SL$	$0.14 + 0.033 * SL$	$0.12 + 0.034 * SL$
	tF	0.16	$0.14 + 0.011 * SL$	$0.14 + 0.013 * SL$	$0.13 + 0.013 * SL$
B to Y	tPLH	1.12	$1.09 + 0.016 * SL$	$1.09 + 0.014 * SL$	$1.09 + 0.014 * SL$
	tPHL	0.46	$0.43 + 0.012 * SL$	$0.44 + 0.009 * SL$	$0.47 + 0.007 * SL$
	tR	0.22	$0.16 + 0.031 * SL$	$0.15 + 0.033 * SL$	$0.13 + 0.034 * SL$
	tF	0.16	$0.14 + 0.012 * SL$	$0.14 + 0.013 * SL$	$0.13 + 0.013 * SL$
C to Y	tPLH	1.10	$1.06 + 0.016 * SL$	$1.07 + 0.014 * SL$	$1.07 + 0.014 * SL$
	tPHL	0.57	$0.55 + 0.012 * SL$	$0.56 + 0.009 * SL$	$0.59 + 0.007 * SL$
	tR	0.21	$0.15 + 0.031 * SL$	$0.14 + 0.033 * SL$	$0.12 + 0.034 * SL$
	tF	0.17	$0.14 + 0.012 * SL$	$0.14 + 0.012 * SL$	$0.13 + 0.013 * SL$
D to Y	tPLH	1.21	$1.18 + 0.016 * SL$	$1.19 + 0.014 * SL$	$1.19 + 0.014 * SL$
	tPHL	0.52	$0.50 + 0.013 * SL$	$0.51 + 0.009 * SL$	$0.54 + 0.007 * SL$
	tR	0.22	$0.16 + 0.031 * SL$	$0.15 + 0.033 * SL$	$0.13 + 0.034 * SL$
	tF	0.17	$0.15 + 0.010 * SL$	$0.14 + 0.012 * SL$	$0.13 + 0.013 * SL$
E to Y	tPLH	1.14	$1.11 + 0.015 * SL$	$1.11 + 0.014 * SL$	$1.11 + 0.014 * SL$
	tPHL	0.61	$0.58 + 0.013 * SL$	$0.60 + 0.009 * SL$	$0.63 + 0.007 * SL$
	tR	0.21	$0.15 + 0.031 * SL$	$0.14 + 0.033 * SL$	$0.12 + 0.034 * SL$
	tF	0.17	$0.15 + 0.012 * SL$	$0.15 + 0.012 * SL$	$0.14 + 0.013 * SL$
F to Y	tPLH	1.26	$1.23 + 0.016 * SL$	$1.23 + 0.014 * SL$	$1.23 + 0.014 * SL$
	tPHL	0.55	$0.53 + 0.012 * SL$	$0.54 + 0.009 * SL$	$0.57 + 0.007 * SL$
	tR	0.22	$0.16 + 0.031 * SL$	$0.15 + 0.033 * SL$	$0.13 + 0.034 * SL$
	tF	0.17	$0.15 + 0.010 * SL$	$0.15 + 0.012 * SL$	$0.14 + 0.013 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**AO222D7 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

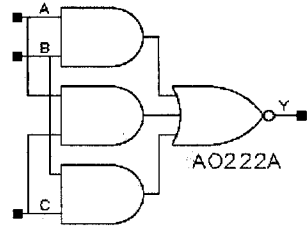
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	1.16	$1.14 + 0.008*SL$	$1.15 + 0.006*SL$	$1.16 + 0.006*SL$
	tPHL	0.63	$0.61 + 0.007*SL$	$0.62 + 0.005*SL$	$0.64 + 0.004*SL$
	tR	0.22	$0.20 + 0.011*SL$	$0.20 + 0.013*SL$	$0.18 + 0.014*SL$
	tF	0.24	$0.23 + 0.004*SL$	$0.23 + 0.006*SL$	$0.23 + 0.005*SL$
B to Y	tPLH	1.29	$1.27 + 0.007*SL$	$1.27 + 0.006*SL$	$1.28 + 0.006*SL$
	tPHL	0.59	$0.57 + 0.007*SL$	$0.58 + 0.005*SL$	$0.60 + 0.004*SL$
	tR	0.23	$0.21 + 0.011*SL$	$0.21 + 0.013*SL$	$0.19 + 0.014*SL$
	tF	0.24	$0.23 + 0.005*SL$	$0.23 + 0.006*SL$	$0.24 + 0.005*SL$
C to Y	tPLH	1.25	$1.23 + 0.008*SL$	$1.24 + 0.006*SL$	$1.25 + 0.006*SL$
	tPHL	0.71	$0.69 + 0.007*SL$	$0.70 + 0.005*SL$	$0.72 + 0.004*SL$
	tR	0.22	$0.20 + 0.011*SL$	$0.20 + 0.013*SL$	$0.18 + 0.014*SL$
	tF	0.24	$0.24 + 0.004*SL$	$0.23 + 0.006*SL$	$0.24 + 0.005*SL$
D to Y	tPLH	1.38	$1.36 + 0.008*SL$	$1.37 + 0.006*SL$	$1.38 + 0.006*SL$
	tPHL	0.66	$0.64 + 0.007*SL$	$0.65 + 0.005*SL$	$0.67 + 0.004*SL$
	tR	0.23	$0.21 + 0.010*SL$	$0.21 + 0.013*SL$	$0.19 + 0.014*SL$
	tF	0.25	$0.24 + 0.003*SL$	$0.23 + 0.006*SL$	$0.24 + 0.005*SL$
E to Y	tPLH	1.30	$1.28 + 0.007*SL$	$1.28 + 0.006*SL$	$1.29 + 0.006*SL$
	tPHL	0.75	$0.73 + 0.007*SL$	$0.74 + 0.005*SL$	$0.76 + 0.004*SL$
	tR	0.22	$0.20 + 0.011*SL$	$0.20 + 0.013*SL$	$0.18 + 0.014*SL$
	tF	0.25	$0.24 + 0.004*SL$	$0.24 + 0.006*SL$	$0.25 + 0.005*SL$
F to Y	tPLH	1.43	$1.41 + 0.008*SL$	$1.41 + 0.006*SL$	$1.42 + 0.006*SL$
	tPHL	0.69	$0.68 + 0.007*SL$	$0.69 + 0.005*SL$	$0.71 + 0.004*SL$
	tR	0.23	$0.21 + 0.011*SL$	$0.21 + 0.013*SL$	$0.19 + 0.014*SL$
	tF	0.25	$0.24 + 0.004*SL$	$0.24 + 0.006*SL$	$0.25 + 0.005*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# AO222A

## Inverting 2-of-3 Majority

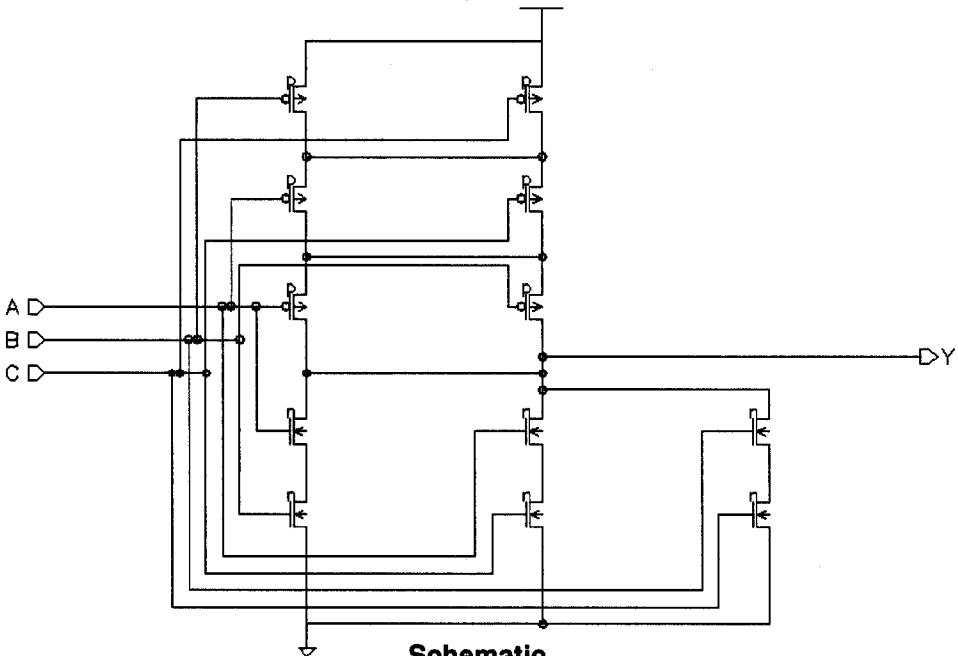
Inputs: A, B, C  
Output: Y  
Input Loading (SL): All : 2  
Maximum Fanout (Rec. SL): 9  
Gate Count: 3



Symbol

A	B	C	Y
1	1	x	0
1	x	1	0
x	1	1	0
0	0	x	1
0	x	0	1
x	0	0	1

Truth Table



Schematic

**AO222A Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.67	$0.47 + 0.095 \cdot \text{SL}$	$0.48 + 0.094 \cdot \text{SL}$	$0.48 + 0.094 \cdot \text{SL}$
	tPHL	0.25	$0.16 + 0.045 \cdot \text{SL}$	$0.20 + 0.033 \cdot \text{SL}$	$0.25 + 0.031 \cdot \text{SL}$
	tR	1.23	$0.80 + 0.216 \cdot \text{SL}$	$0.77 + 0.223 \cdot \text{SL}$	$0.74 + 0.224 \cdot \text{SL}$
	tF	0.59	$0.47 + 0.061 \cdot \text{SL}$	$0.46 + 0.063 \cdot \text{SL}$	$0.38 + 0.067 \cdot \text{SL}$
B to Y	tPLH	0.78	$0.60 + 0.088 \cdot \text{SL}$	$0.60 + 0.091 \cdot \text{SL}$	$0.58 + 0.092 \cdot \text{SL}$
	tPHL	0.27	$0.18 + 0.047 \cdot \text{SL}$	$0.22 + 0.034 \cdot \text{SL}$	$0.27 + 0.031 \cdot \text{SL}$
	tR	1.32	$0.89 + 0.215 \cdot \text{SL}$	$0.87 + 0.220 \cdot \text{SL}$	$0.85 + 0.221 \cdot \text{SL}$
	tF	0.63	$0.51 + 0.062 \cdot \text{SL}$	$0.51 + 0.063 \cdot \text{SL}$	$0.43 + 0.067 \cdot \text{SL}$
C to Y	tPLH	0.80	$0.62 + 0.089 \cdot \text{SL}$	$0.62 + 0.091 \cdot \text{SL}$	$0.60 + 0.092 \cdot \text{SL}$
	tPHL	0.21	$0.12 + 0.043 \cdot \text{SL}$	$0.15 + 0.034 \cdot \text{SL}$	$0.20 + 0.031 \cdot \text{SL}$
	tR	1.34	$0.92 + 0.212 \cdot \text{SL}$	$0.90 + 0.219 \cdot \text{SL}$	$0.85 + 0.221 \cdot \text{SL}$
	tF	0.62	$0.50 + 0.058 \cdot \text{SL}$	$0.48 + 0.064 \cdot \text{SL}$	$0.41 + 0.068 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$



# AO33/AO33D2/AO33D3/AO33D7

2 3-AND into 2-NOR with 1X Drive 2X Drive, 3X Drive or 7X Drive

Inputs: A, B, C, D, E, F

Output: Y

Input Loading (SL):

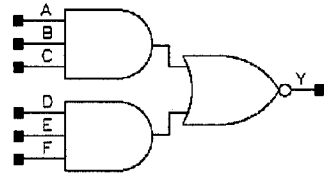
- AO33: All : 1
- AO33D2: All: 1
- AO33D3: All: 1
- AO33D7: All: 1

Maximum Fanout (Rec. SL):

- AO33: 14
- AO33D2: 28
- AO33D3: 84
- AO33D7: 196

Gate Count:

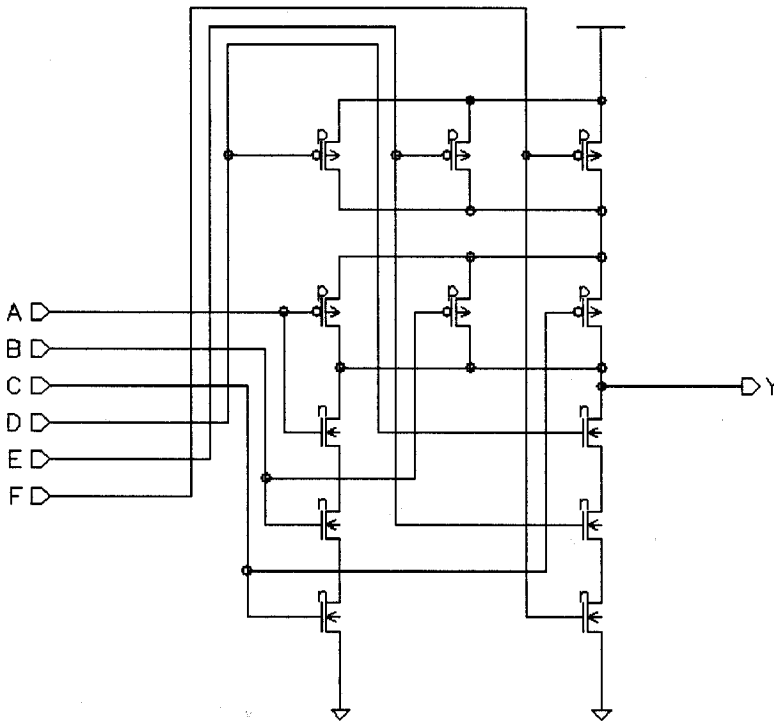
- AO33: 3
- AO33D2: 5
- AO33D3: 5
- AO33D7: 7



**Symbol**

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	1	0
other states						1

**Truth Table**



**Schematic**

**AO33 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.62	$0.47 + 0.073 \cdot SL$	$0.47 + 0.073 \cdot SL$	$0.46 + 0.074 \cdot SL$
	tPHL	0.29	$0.19 + 0.053 \cdot SL$	$0.21 + 0.043 \cdot SL$	$0.24 + 0.042 \cdot SL$
	tR	1.10	$0.77 + 0.165 \cdot SL$	$0.74 + 0.174 \cdot SL$	$0.68 + 0.177 \cdot SL$
	tF	0.78	$0.62 + 0.082 \cdot SL$	$0.59 + 0.091 \cdot SL$	$0.48 + 0.097 \cdot SL$
B to Y	tPLH	0.70	$0.56 + 0.073 \cdot SL$	$0.55 + 0.074 \cdot SL$	$0.54 + 0.075 \cdot SL$
	tPHL	0.27	$0.17 + 0.049 \cdot SL$	$0.19 + 0.043 \cdot SL$	$0.20 + 0.042 \cdot SL$
	tR	1.23	$0.90 + 0.167 \cdot SL$	$0.87 + 0.177 \cdot SL$	$0.81 + 0.180 \cdot SL$
	tF	0.76	$0.60 + 0.081 \cdot SL$	$0.56 + 0.092 \cdot SL$	$0.47 + 0.097 \cdot SL$
C to Y	tPLH	0.77	$0.63 + 0.073 \cdot SL$	$0.63 + 0.074 \cdot SL$	$0.61 + 0.075 \cdot SL$
	tPHL	0.24	$0.14 + 0.047 \cdot SL$	$0.16 + 0.043 \cdot SL$	$0.17 + 0.042 \cdot SL$
	tR	1.37	$1.04 + 0.165 \cdot SL$	$1.01 + 0.176 \cdot SL$	$0.93 + 0.180 \cdot SL$
	tF	0.72	$0.56 + 0.083 \cdot SL$	$0.53 + 0.094 \cdot SL$	$0.45 + 0.097 \cdot SL$
D to Y	tPLH	0.68	$0.53 + 0.077 \cdot SL$	$0.53 + 0.076 \cdot SL$	$0.53 + 0.076 \cdot SL$
	tPHL	0.39	$0.29 + 0.049 \cdot SL$	$0.31 + 0.044 \cdot SL$	$0.33 + 0.043 \cdot SL$
	tR	1.12	$0.78 + 0.173 \cdot SL$	$0.75 + 0.181 \cdot SL$	$0.70 + 0.183 \cdot SL$
	tF	0.97	$0.82 + 0.080 \cdot SL$	$0.78 + 0.090 \cdot SL$	$0.66 + 0.096 \cdot SL$
E to Y	tPLH	0.76	$0.61 + 0.076 \cdot SL$	$0.61 + 0.076 \cdot SL$	$0.61 + 0.076 \cdot SL$
	tPHL	0.36	$0.27 + 0.048 \cdot SL$	$0.28 + 0.043 \cdot SL$	$0.30 + 0.043 \cdot SL$
	tR	1.25	$0.90 + 0.175 \cdot SL$	$0.88 + 0.181 \cdot SL$	$0.83 + 0.183 \cdot SL$
	tF	0.94	$0.78 + 0.080 \cdot SL$	$0.75 + 0.092 \cdot SL$	$0.65 + 0.097 \cdot SL$
F to Y	tPLH	0.82	$0.67 + 0.075 \cdot SL$	$0.67 + 0.075 \cdot SL$	$0.67 + 0.075 \cdot SL$
	tPHL	0.33	$0.23 + 0.048 \cdot SL$	$0.24 + 0.043 \cdot SL$	$0.26 + 0.043 \cdot SL$
	tR	1.36	$1.02 + 0.170 \cdot SL$	$1.00 + 0.177 \cdot SL$	$0.94 + 0.180 \cdot SL$
	tF	0.91	$0.74 + 0.083 \cdot SL$	$0.71 + 0.093 \cdot SL$	$0.63 + 0.097 \cdot SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **AO33D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.88	$0.83 + 0.023 \cdot SL$	$0.84 + 0.021 \cdot SL$	$0.84 + 0.021 \cdot SL$
	tPHL	0.50	$0.47 + 0.016 \cdot SL$	$0.48 + 0.011 \cdot SL$	$0.51 + 0.010 \cdot SL$
	tR	0.23	$0.13 + 0.049 \cdot SL$	$0.12 + 0.051 \cdot SL$	$0.10 + 0.052 \cdot SL$
	tF	0.15	$0.11 + 0.018 \cdot SL$	$0.11 + 0.019 \cdot SL$	$0.08 + 0.020 \cdot SL$
B to Y	tPLH	0.98	$0.93 + 0.023 \cdot SL$	$0.93 + 0.021 \cdot SL$	$0.93 + 0.021 \cdot SL$
	tPHL	0.48	$0.45 + 0.015 \cdot SL$	$0.46 + 0.011 \cdot SL$	$0.49 + 0.010 \cdot SL$
	tR	0.23	$0.14 + 0.048 \cdot SL$	$0.13 + 0.051 \cdot SL$	$0.10 + 0.052 \cdot SL$
	tF	0.15	$0.11 + 0.017 \cdot SL$	$0.11 + 0.019 \cdot SL$	$0.08 + 0.020 \cdot SL$
C to Y	tPLH	1.06	$1.01 + 0.023 \cdot SL$	$1.02 + 0.021 \cdot SL$	$1.02 + 0.021 \cdot SL$
	tPHL	0.45	$0.42 + 0.015 \cdot SL$	$0.43 + 0.011 \cdot SL$	$0.46 + 0.010 \cdot SL$
	tR	0.24	$0.14 + 0.048 \cdot SL$	$0.13 + 0.051 \cdot SL$	$0.10 + 0.052 \cdot SL$
	tF	0.15	$0.11 + 0.022 \cdot SL$	$0.12 + 0.019 \cdot SL$	$0.08 + 0.020 \cdot SL$
D to Y	tPLH	0.94	$0.90 + 0.022 \cdot SL$	$0.90 + 0.021 \cdot SL$	$0.90 + 0.021 \cdot SL$
	tPHL	0.63	$0.60 + 0.016 \cdot SL$	$0.62 + 0.011 \cdot SL$	$0.64 + 0.010 \cdot SL$
	tR	0.23	$0.13 + 0.047 \cdot SL$	$0.12 + 0.051 \cdot SL$	$0.10 + 0.052 \cdot SL$
	tF	0.15	$0.11 + 0.019 \cdot SL$	$0.11 + 0.019 \cdot SL$	$0.08 + 0.020 \cdot SL$
E to Y	tPLH	1.03	$0.98 + 0.023 \cdot SL$	$0.99 + 0.021 \cdot SL$	$0.99 + 0.021 \cdot SL$
	tPHL	0.61	$0.58 + 0.016 \cdot SL$	$0.59 + 0.011 \cdot SL$	$0.61 + 0.010 \cdot SL$
	tR	0.23	$0.13 + 0.049 \cdot SL$	$0.13 + 0.051 \cdot SL$	$0.10 + 0.052 \cdot SL$
	tF	0.15	$0.11 + 0.017 \cdot SL$	$0.11 + 0.019 \cdot SL$	$0.08 + 0.020 \cdot SL$
F to Y	tPLH	1.11	$1.06 + 0.023 \cdot SL$	$1.07 + 0.021 \cdot SL$	$1.07 + 0.021 \cdot SL$
	tPHL	0.57	$0.54 + 0.016 \cdot SL$	$0.55 + 0.012 \cdot SL$	$0.57 + 0.010 \cdot SL$
	tR	0.24	$0.14 + 0.048 \cdot SL$	$0.13 + 0.051 \cdot SL$	$0.10 + 0.052 \cdot SL$
	tF	0.16	$0.12 + 0.019 \cdot SL$	$0.12 + 0.019 \cdot SL$	$0.09 + 0.020 \cdot SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# AO33D3

2 3-AND into 2-NOR with 3X Drive

## AO33D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.82	$0.79 + 0.015*SL$	$0.79 + 0.014*SL$	$0.79 + 0.014*SL$
	tPHL	0.60	$0.58 + 0.013*SL$	$0.59 + 0.009*SL$	$0.62 + 0.007*SL$
	tR	0.20	$0.13 + 0.032*SL$	$0.13 + 0.033*SL$	$0.11 + 0.034*SL$
	tF	0.18	$0.15 + 0.011*SL$	$0.15 + 0.012*SL$	$0.14 + 0.013*SL$
B to Y	tPLH	0.90	$0.87 + 0.015*SL$	$0.87 + 0.014*SL$	$0.87 + 0.014*SL$
	tPHL	0.59	$0.57 + 0.013*SL$	$0.58 + 0.009*SL$	$0.61 + 0.007*SL$
	tR	0.20	$0.14 + 0.033*SL$	$0.14 + 0.033*SL$	$0.11 + 0.034*SL$
	tF	0.18	$0.15 + 0.013*SL$	$0.15 + 0.012*SL$	$0.14 + 0.013*SL$
C to Y	tPLH	0.96	$0.93 + 0.016*SL$	$0.93 + 0.014*SL$	$0.93 + 0.014*SL$
	tPHL	0.56	$0.54 + 0.012*SL$	$0.55 + 0.009*SL$	$0.58 + 0.007*SL$
	tR	0.21	$0.15 + 0.029*SL$	$0.14 + 0.033*SL$	$0.11 + 0.034*SL$
	tF	0.18	$0.15 + 0.011*SL$	$0.15 + 0.012*SL$	$0.14 + 0.013*SL$
D to Y	tPLH	0.87	$0.84 + 0.015*SL$	$0.84 + 0.014*SL$	$0.84 + 0.014*SL$
	tPHL	0.74	$0.72 + 0.012*SL$	$0.73 + 0.009*SL$	$0.76 + 0.007*SL$
	tR	0.20	$0.14 + 0.032*SL$	$0.13 + 0.033*SL$	$0.11 + 0.034*SL$
	tF	0.18	$0.16 + 0.011*SL$	$0.16 + 0.012*SL$	$0.14 + 0.013*SL$
E to Y	tPLH	0.95	$0.92 + 0.015*SL$	$0.92 + 0.014*SL$	$0.92 + 0.014*SL$
	tPHL	0.73	$0.70 + 0.012*SL$	$0.71 + 0.009*SL$	$0.74 + 0.007*SL$
	tR	0.20	$0.14 + 0.031*SL$	$0.14 + 0.033*SL$	$0.11 + 0.034*SL$
	tF	0.18	$0.16 + 0.010*SL$	$0.16 + 0.012*SL$	$0.14 + 0.013*SL$
F to Y	tPLH	1.01	$0.98 + 0.016*SL$	$0.98 + 0.014*SL$	$0.98 + 0.014*SL$
	tPHL	0.69	$0.66 + 0.012*SL$	$0.67 + 0.009*SL$	$0.71 + 0.007*SL$
	tR	0.21	$0.15 + 0.029*SL$	$0.14 + 0.033*SL$	$0.11 + 0.034*SL$
	tF	0.19	$0.16 + 0.015*SL$	$0.17 + 0.012*SL$	$0.14 + 0.013*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**AO33D7 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.95	$0.93 + 0.007 \cdot \text{SL}$	$0.94 + 0.006 \cdot \text{SL}$	$0.94 + 0.006 \cdot \text{SL}$
	tPHL	0.74	$0.73 + 0.007 \cdot \text{SL}$	$0.73 + 0.005 \cdot \text{SL}$	$0.76 + 0.004 \cdot \text{SL}$
	tR	0.20	$0.18 + 0.012 \cdot \text{SL}$	$0.17 + 0.013 \cdot \text{SL}$	$0.16 + 0.014 \cdot \text{SL}$
	tF	0.25	$0.25 + 0.003 \cdot \text{SL}$	$0.24 + 0.006 \cdot \text{SL}$	$0.25 + 0.005 \cdot \text{SL}$
B to Y	tPLH	1.04	$1.03 + 0.007 \cdot \text{SL}$	$1.03 + 0.006 \cdot \text{SL}$	$1.04 + 0.006 \cdot \text{SL}$
	tPHL	0.73	$0.72 + 0.007 \cdot \text{SL}$	$0.73 + 0.005 \cdot \text{SL}$	$0.75 + 0.004 \cdot \text{SL}$
	tR	0.21	$0.18 + 0.012 \cdot \text{SL}$	$0.18 + 0.013 \cdot \text{SL}$	$0.16 + 0.014 \cdot \text{SL}$
	tF	0.25	$0.25 + 0.004 \cdot \text{SL}$	$0.24 + 0.006 \cdot \text{SL}$	$0.25 + 0.005 \cdot \text{SL}$
C to Y	tPLH	1.10	$1.09 + 0.007 \cdot \text{SL}$	$1.09 + 0.006 \cdot \text{SL}$	$1.10 + 0.006 \cdot \text{SL}$
	tPHL	0.70	$0.69 + 0.007 \cdot \text{SL}$	$0.69 + 0.005 \cdot \text{SL}$	$0.71 + 0.004 \cdot \text{SL}$
	tR	0.22	$0.19 + 0.012 \cdot \text{SL}$	$0.19 + 0.013 \cdot \text{SL}$	$0.17 + 0.014 \cdot \text{SL}$
	tF	0.26	$0.25 + 0.003 \cdot \text{SL}$	$0.24 + 0.005 \cdot \text{SL}$	$0.25 + 0.005 \cdot \text{SL}$
D to Y	tPLH	1.00	$0.98 + 0.007 \cdot \text{SL}$	$0.99 + 0.006 \cdot \text{SL}$	$0.99 + 0.006 \cdot \text{SL}$
	tPHL	0.89	$0.87 + 0.007 \cdot \text{SL}$	$0.88 + 0.005 \cdot \text{SL}$	$0.90 + 0.004 \cdot \text{SL}$
	tR	0.20	$0.18 + 0.012 \cdot \text{SL}$	$0.18 + 0.013 \cdot \text{SL}$	$0.16 + 0.014 \cdot \text{SL}$
	tF	0.26	$0.25 + 0.005 \cdot \text{SL}$	$0.25 + 0.006 \cdot \text{SL}$	$0.26 + 0.005 \cdot \text{SL}$
E to Y	tPLH	1.09	$1.08 + 0.007 \cdot \text{SL}$	$1.08 + 0.006 \cdot \text{SL}$	$1.09 + 0.006 \cdot \text{SL}$
	tPHL	0.87	$0.85 + 0.007 \cdot \text{SL}$	$0.86 + 0.005 \cdot \text{SL}$	$0.88 + 0.004 \cdot \text{SL}$
	tR	0.21	$0.19 + 0.012 \cdot \text{SL}$	$0.18 + 0.013 \cdot \text{SL}$	$0.16 + 0.014 \cdot \text{SL}$
	tF	0.26	$0.26 + 0.002 \cdot \text{SL}$	$0.25 + 0.006 \cdot \text{SL}$	$0.26 + 0.005 \cdot \text{SL}$
F to Y	tPLH	1.16	$1.14 + 0.007 \cdot \text{SL}$	$1.14 + 0.006 \cdot \text{SL}$	$1.15 + 0.006 \cdot \text{SL}$
	tPHL	0.83	$0.82 + 0.006 \cdot \text{SL}$	$0.82 + 0.005 \cdot \text{SL}$	$0.85 + 0.004 \cdot \text{SL}$
	tR	0.22	$0.19 + 0.012 \cdot \text{SL}$	$0.19 + 0.013 \cdot \text{SL}$	$0.17 + 0.014 \cdot \text{SL}$
	tF	0.26	$0.24 + 0.007 \cdot \text{SL}$	$0.25 + 0.005 \cdot \text{SL}$	$0.26 + 0.005 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

# AO333/AO333D2

3 3-AND into 3-NOR 1X Drive or 2X Drive

Inputs: A, B, C, D, E, F, G, H, I

Output: Y

Input Loading (SL): All : 1

Maximum Fanout (Rec. SL):

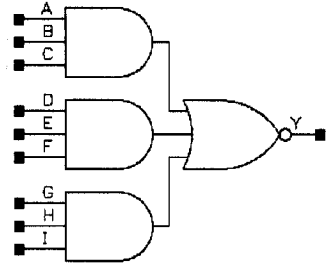
AO333: 9

AO333D2: 18

Gate Count:

AO333: 5

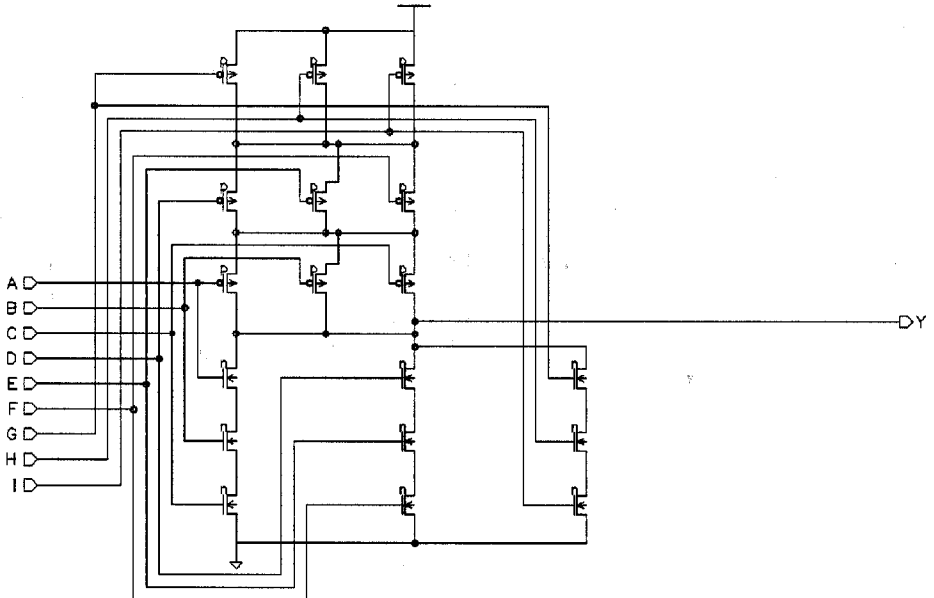
AO333D2: 6



Symbol

A	B	C	D	E	F	G	H	I	Y
1	1	1	x	x	x	x	x	x	0
x	x	x	1	1	1	x	x	x	0
x	x	x	x	x	x	1	1	1	0
other states									1

Truth Table



Schematic

**AO333 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	1.04	$0.83 + 0.108 \cdot SL$	$0.83 + 0.109 \cdot SL$	$0.82 + 0.109 \cdot SL$
	tPHL	0.36	$0.26 + 0.050 \cdot SL$	$0.28 + 0.044 \cdot SL$	$0.30 + 0.043 \cdot SL$
	tR	2.13	$1.62 + 0.259 \cdot SL$	$1.60 + 0.264 \cdot SL$	$1.60 + 0.263 \cdot SL$
	tF	1.03	$0.86 + 0.085 \cdot SL$	$0.83 + 0.094 \cdot SL$	$0.72 + 0.099 \cdot SL$
B to Y	tPLH	1.16	$0.95 + 0.108 \cdot SL$	$0.95 + 0.109 \cdot SL$	$0.93 + 0.110 \cdot SL$
	tPHL	0.33	$0.24 + 0.048 \cdot SL$	$0.25 + 0.044 \cdot SL$	$0.26 + 0.043 \cdot SL$
	tR	2.33	$1.80 + 0.262 \cdot SL$	$1.79 + 0.266 \cdot SL$	$1.80 + 0.266 \cdot SL$
	tF	1.00	$0.83 + 0.084 \cdot SL$	$0.80 + 0.095 \cdot SL$	$0.71 + 0.099 \cdot SL$
C to Y	tPLH	1.26	$1.05 + 0.107 \cdot SL$	$1.05 + 0.108 \cdot SL$	$1.03 + 0.109 \cdot SL$
	tPHL	0.30	$0.21 + 0.047 \cdot SL$	$0.22 + 0.043 \cdot SL$	$0.23 + 0.043 \cdot SL$
	tR	2.50	$1.98 + 0.257 \cdot SL$	$1.96 + 0.263 \cdot SL$	$1.97 + 0.263 \cdot SL$
	tF	0.96	$0.79 + 0.087 \cdot SL$	$0.76 + 0.096 \cdot SL$	$0.70 + 0.100 \cdot SL$
D to Y	tPLH	1.23	$1.01 + 0.112 \cdot SL$	$1.01 + 0.111 \cdot SL$	$1.02 + 0.111 \cdot SL$
	tPHL	0.46	$0.37 + 0.048 \cdot SL$	$0.38 + 0.044 \cdot SL$	$0.40 + 0.043 \cdot SL$
	tR	2.21	$1.69 + 0.260 \cdot SL$	$1.68 + 0.264 \cdot SL$	$1.64 + 0.266 \cdot SL$
	tF	1.21	$1.05 + 0.083 \cdot SL$	$1.02 + 0.093 \cdot SL$	$0.90 + 0.099 \cdot SL$
E to Y	tPLH	1.35	$1.13 + 0.112 \cdot SL$	$1.13 + 0.111 \cdot SL$	$1.13 + 0.111 \cdot SL$
	tPHL	0.43	$0.34 + 0.046 \cdot SL$	$0.35 + 0.044 \cdot SL$	$0.36 + 0.043 \cdot SL$
	tR	2.39	$1.86 + 0.261 \cdot SL$	$1.85 + 0.264 \cdot SL$	$1.83 + 0.266 \cdot SL$
	tF	1.18	$1.01 + 0.085 \cdot SL$	$0.98 + 0.095 \cdot SL$	$0.89 + 0.099 \cdot SL$
F to Y	tPLH	1.44	$1.22 + 0.110 \cdot SL$	$1.23 + 0.109 \cdot SL$	$1.23 + 0.109 \cdot SL$
	tPHL	0.40	$0.30 + 0.046 \cdot SL$	$0.31 + 0.044 \cdot SL$	$0.33 + 0.043 \cdot SL$
	tR	2.54	$2.02 + 0.258 \cdot SL$	$2.01 + 0.261 \cdot SL$	$1.99 + 0.262 \cdot SL$
	tF	1.14	$0.97 + 0.088 \cdot SL$	$0.94 + 0.096 \cdot SL$	$0.88 + 0.099 \cdot SL$
G to Y	tPLH	1.34	$1.11 + 0.114 \cdot SL$	$1.12 + 0.112 \cdot SL$	$1.13 + 0.111 \cdot SL$
	tPHL	0.50	$0.40 + 0.049 \cdot SL$	$0.41 + 0.045 \cdot SL$	$0.45 + 0.043 \cdot SL$
	tR	2.22	$1.70 + 0.260 \cdot SL$	$1.68 + 0.264 \cdot SL$	$1.65 + 0.266 \cdot SL$
	tF	1.38	$1.22 + 0.081 \cdot SL$	$1.19 + 0.090 \cdot SL$	$1.08 + 0.096 \cdot SL$
H to Y	tPLH	1.46	$1.23 + 0.113 \cdot SL$	$1.23 + 0.112 \cdot SL$	$1.25 + 0.111 \cdot SL$
	tPHL	0.47	$0.37 + 0.048 \cdot SL$	$0.38 + 0.045 \cdot SL$	$0.42 + 0.043 \cdot SL$
	tR	2.39	$1.87 + 0.262 \cdot SL$	$1.86 + 0.265 \cdot SL$	$1.83 + 0.266 \cdot SL$
	tF	1.35	$1.18 + 0.083 \cdot SL$	$1.15 + 0.092 \cdot SL$	$1.07 + 0.096 \cdot SL$
I to Y	tPLH	1.55	$1.32 + 0.111 \cdot SL$	$1.33 + 0.110 \cdot SL$	$1.34 + 0.109 \cdot SL$
	tPHL	0.42	$0.33 + 0.049 \cdot SL$	$0.34 + 0.045 \cdot SL$	$0.38 + 0.043 \cdot SL$
	tR	2.54	$2.02 + 0.258 \cdot SL$	$2.01 + 0.261 \cdot SL$	$1.99 + 0.262 \cdot SL$
	tF	1.31	$1.14 + 0.085 \cdot SL$	$1.12 + 0.093 \cdot SL$	$1.05 + 0.096 \cdot SL$

\*Range1:  $SL < 3.00$ , \*Range2:  $3.00 \leq SL \leq 20.00$ , \*Range3:  $20.00 < SL$

# AO333D2

3 3-AND into 3-NOR with 2X Drive

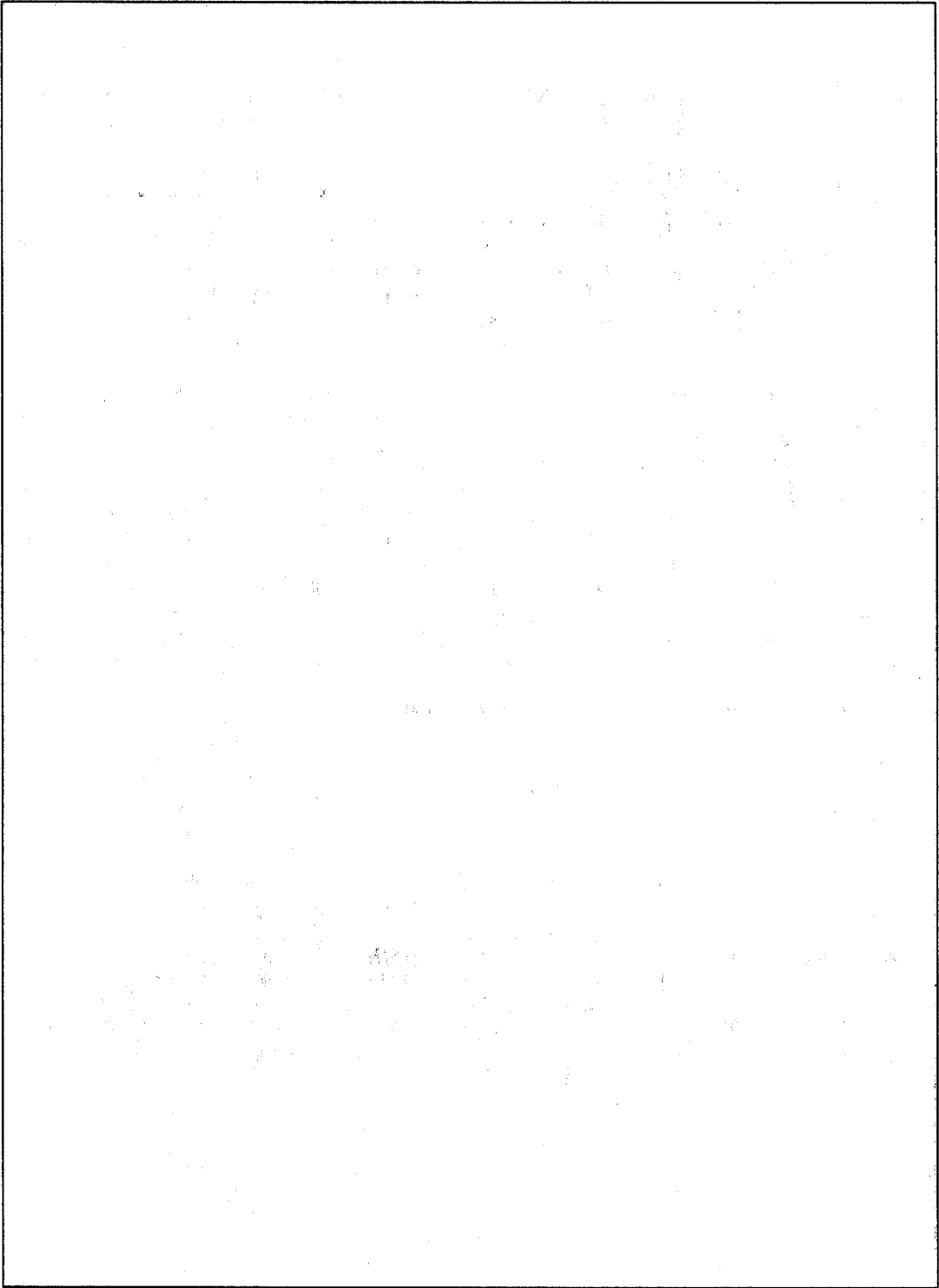
## AO333D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{p}$  and  $t_{f}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t <sub>PLH</sub>	1.11	1.06 + 0.021*SL	1.07 + 0.020*SL	1.07 + 0.020*SL
	t <sub>PHL</sub>	0.69	0.66 + 0.016*SL	0.67 + 0.011*SL	0.70 + 0.010*SL
	t <sub>R</sub>	0.23	0.14 + 0.044*SL	0.13 + 0.045*SL	0.11 + 0.047*SL
	t <sub>F</sub>	0.17	0.13 + 0.016*SL	0.13 + 0.017*SL	0.10 + 0.019*SL
B to Y	t <sub>PLH</sub>	1.21	1.17 + 0.021*SL	1.17 + 0.020*SL	1.17 + 0.020*SL
	t <sub>PHL</sub>	0.67	0.64 + 0.016*SL	0.65 + 0.011*SL	0.68 + 0.010*SL
	t <sub>R</sub>	0.23	0.15 + 0.041*SL	0.14 + 0.046*SL	0.11 + 0.047*SL
	t <sub>F</sub>	0.17	0.14 + 0.014*SL	0.13 + 0.017*SL	0.10 + 0.019*SL
C to Y	t <sub>PLH</sub>	1.30	1.26 + 0.022*SL	1.27 + 0.020*SL	1.26 + 0.020*SL
	t <sub>PHL</sub>	0.64	0.60 + 0.016*SL	0.62 + 0.011*SL	0.65 + 0.010*SL
	t <sub>R</sub>	0.24	0.15 + 0.043*SL	0.14 + 0.046*SL	0.12 + 0.047*SL
	t <sub>F</sub>	0.17	0.14 + 0.014*SL	0.13 + 0.017*SL	0.10 + 0.019*SL
D to Y	t <sub>PLH</sub>	1.29	1.25 + 0.021*SL	1.26 + 0.020*SL	1.26 + 0.020*SL
	t <sub>PHL</sub>	0.83	0.79 + 0.016*SL	0.81 + 0.011*SL	0.84 + 0.010*SL
	t <sub>R</sub>	0.23	0.14 + 0.042*SL	0.13 + 0.046*SL	0.11 + 0.047*SL
	t <sub>F</sub>	0.17	0.15 + 0.014*SL	0.14 + 0.017*SL	0.11 + 0.019*SL
E to Y	t <sub>PLH</sub>	1.40	1.36 + 0.021*SL	1.36 + 0.020*SL	1.36 + 0.020*SL
	t <sub>PHL</sub>	0.80	0.77 + 0.017*SL	0.78 + 0.011*SL	0.81 + 0.010*SL
	t <sub>R</sub>	0.23	0.15 + 0.043*SL	0.14 + 0.045*SL	0.12 + 0.047*SL
	t <sub>F</sub>	0.17	0.14 + 0.017*SL	0.14 + 0.017*SL	0.11 + 0.019*SL
F to Y	t <sub>PLH</sub>	1.48	1.44 + 0.021*SL	1.44 + 0.020*SL	1.44 + 0.020*SL
	t <sub>PHL</sub>	0.77	0.73 + 0.017*SL	0.75 + 0.011*SL	0.78 + 0.010*SL
	t <sub>R</sub>	0.24	0.15 + 0.043*SL	0.14 + 0.045*SL	0.12 + 0.047*SL
	t <sub>F</sub>	0.17	0.14 + 0.016*SL	0.14 + 0.017*SL	0.11 + 0.019*SL
G to Y	t <sub>PLH</sub>	1.40	1.35 + 0.022*SL	1.36 + 0.020*SL	1.36 + 0.020*SL
	t <sub>PHL</sub>	0.89	0.86 + 0.017*SL	0.88 + 0.011*SL	0.91 + 0.010*SL
	t <sub>R</sub>	0.23	0.14 + 0.043*SL	0.13 + 0.046*SL	0.11 + 0.047*SL
	t <sub>F</sub>	0.18	0.14 + 0.018*SL	0.15 + 0.017*SL	0.11 + 0.019*SL
H to Y	t <sub>PLH</sub>	1.51	1.46 + 0.021*SL	1.47 + 0.020*SL	1.47 + 0.020*SL
	t <sub>PHL</sub>	0.87	0.84 + 0.017*SL	0.85 + 0.011*SL	0.88 + 0.010*SL
	t <sub>R</sub>	0.23	0.15 + 0.042*SL	0.14 + 0.046*SL	0.12 + 0.047*SL
	t <sub>F</sub>	0.17	0.14 + 0.016*SL	0.14 + 0.017*SL	0.11 + 0.019*SL
I to Y	t <sub>PLH</sub>	1.58	1.54 + 0.021*SL	1.54 + 0.020*SL	1.54 + 0.020*SL
	t <sub>PHL</sub>	0.83	0.79 + 0.016*SL	0.81 + 0.012*SL	0.84 + 0.010*SL
	t <sub>R</sub>	0.24	0.15 + 0.042*SL	0.14 + 0.046*SL	0.12 + 0.047*SL
	t <sub>F</sub>	0.18	0.14 + 0.018*SL	0.14 + 0.017*SL	0.11 + 0.019*SL

\*Range1 : SL < 3.00, \*Range2 : 3.00 ≤ SL ≤ 20.00, \*Range3 : 20.00 < SL





# DL1D2/DL1D4

1ns Non-Inverting Delay Cell with 2X Drive or 4X Drive

Input: A

Output: Y

Input Loading (SL):

- DL1D2: A : 1

- DL1D4: A : 1

Maximum Fanout (Rec. SL):

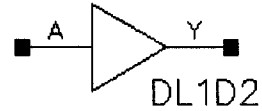
- DL1D2: 56

- DL1D4: 112

Gate Count:

- DL1D2: 4

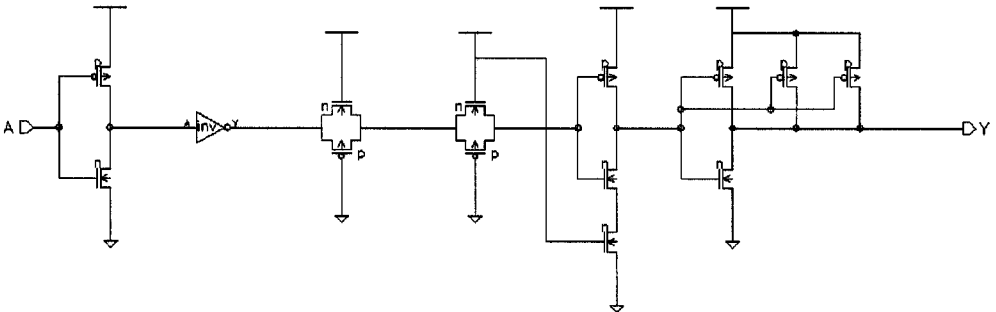
- DL1D4: 5



Symbol

A	Y
0	0
1	1

Truth Table



Schematic

**DL1D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_P$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.56	$0.53 + 0.017*SL$	$0.54 + 0.014*SL$	$0.55 + 0.013*SL$
	tPHL	0.78	$0.73 + 0.023*SL$	$0.74 + 0.020*SL$	$0.75 + 0.020*SL$
	tR	0.19	$0.13 + 0.028*SL$	$0.13 + 0.029*SL$	$0.10 + 0.031*SL$
	tF	0.20	$0.13 + 0.033*SL$	$0.12 + 0.037*SL$	$0.09 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **DL1D4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_P$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.62	$0.59 + 0.012*SL$	$0.60 + 0.009*SL$	$0.62 + 0.008*SL$
	tPHL	0.82	$0.80 + 0.014*SL$	$0.80 + 0.011*SL$	$0.83 + 0.010*SL$
	tR	0.19	$0.17 + 0.013*SL$	$0.16 + 0.017*SL$	$0.13 + 0.018*SL$
	tF	0.20	$0.17 + 0.016*SL$	$0.16 + 0.017*SL$	$0.14 + 0.018*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# DL2D2/DL2D4

2ns Non-Inverting Delay Cell with 2X Drive or 4X Drive

Input: A

Output: Y

Input Loading (SL):

- DL2D2: A : 1

- DL2D4: A : 1

Maximum Fanout Rec. SL):

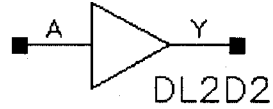
- DL2D2: 56

- DL2D4: 112

Gate Count:

- DL2D2: 7

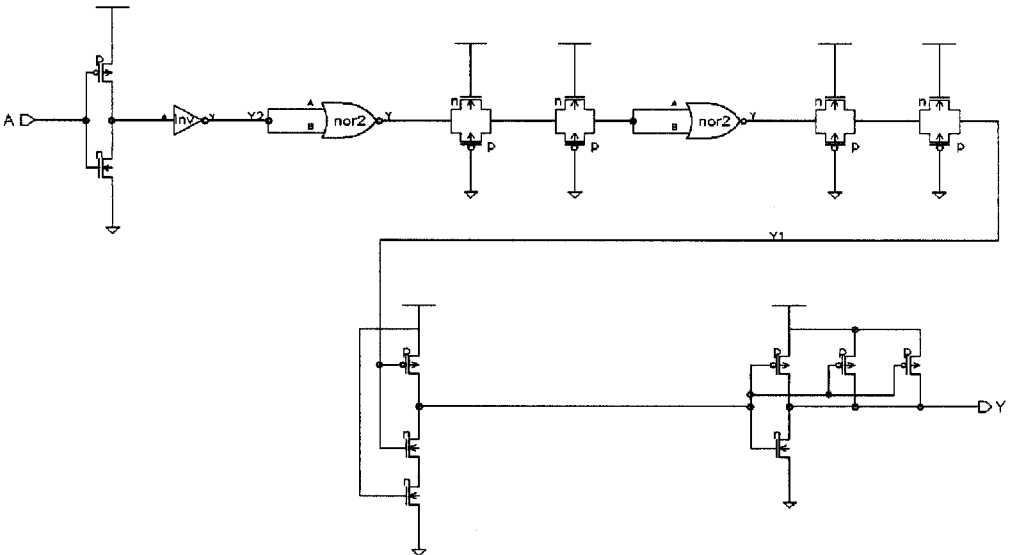
- DL2D4: 8



Symbol

A	Y
0	0
1	1

Truth Table



Schematic

**DL2D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	1.34	$1.31 + 0.018*SL$	$1.32 + 0.015*SL$	$1.33 + 0.014*SL$
	tPHL	1.46	$1.41 + 0.023*SL$	$1.42 + 0.020*SL$	$1.43 + 0.020*SL$
	tR	0.21	$0.16 + 0.025*SL$	$0.14 + 0.030*SL$	$0.11 + 0.031*SL$
	tF	0.19	$0.12 + 0.033*SL$	$0.11 + 0.037*SL$	$0.08 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **DL2D4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	1.31	$1.29 + 0.012*SL$	$1.30 + 0.009*SL$	$1.31 + 0.008*SL$
	tPHL	1.50	$1.47 + 0.014*SL$	$1.48 + 0.011*SL$	$1.50 + 0.010*SL$
	tR	0.18	$0.15 + 0.015*SL$	$0.15 + 0.017*SL$	$0.12 + 0.018*SL$
	tF	0.19	$0.16 + 0.016*SL$	$0.15 + 0.017*SL$	$0.13 + 0.018*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# DL5D2/DL5D4

5ns Non-Inverting Delay Cell with 2X Drive or 4X Drive

Input: A

Output: Y

Input Loading (SL):

- DL5D2: All : 1

- DL5D4: All : 1

Maximum Fanout (Rec. SL):

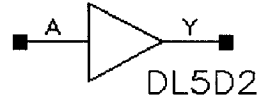
- DL5D2: 56

- DL5D4: 112

Gate Count:

- DL5D2: 14

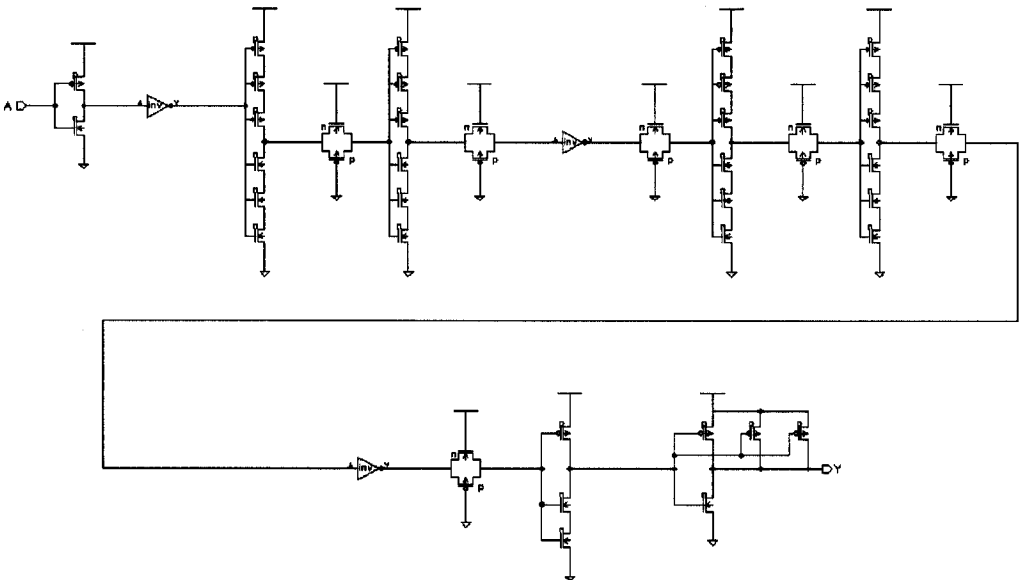
- DL5D4: 15



Symbol

A	Y
0	0
1	1

Truth Table



Schematic

**DL5D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	3.69	$3.66 + 0.016*SL$	$3.67 + 0.014*SL$	$3.67 + 0.013*SL$
	tPHL	3.82	$3.77 + 0.023*SL$	$3.78 + 0.020*SL$	$3.79 + 0.020*SL$
	tR	0.16	$0.11 + 0.026*SL$	$0.10 + 0.030*SL$	$0.07 + 0.031*SL$
	tF	0.19	$0.12 + 0.033*SL$	$0.11 + 0.037*SL$	$0.08 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **DL5D4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	3.73	$3.71 + 0.010*SL$	$3.71 + 0.008*SL$	$3.72 + 0.008*SL$
	tPHL	3.86	$3.83 + 0.013*SL$	$3.84 + 0.011*SL$	$3.85 + 0.010*SL$
	tR	0.15	$0.12 + 0.016*SL$	$0.12 + 0.017*SL$	$0.09 + 0.018*SL$
	tF	0.19	$0.16 + 0.014*SL$	$0.15 + 0.017*SL$	$0.13 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# IV/IVD2/IVD3/IVD4

Inverter with 1X Drive, 2X Drive, 3X Drive or 4x Drive

Input: A  
Output: Y  
Input Loading (SL):

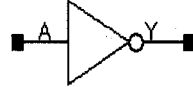
- IV: 1
- IVD2: 2
- IVD3: 3
- IVD4: 4

Maximum Fanout (Rec. SL):

- IV: 28
- IVD2: 56
- IVD3: 84
- IVD4: 112

Gate Count:

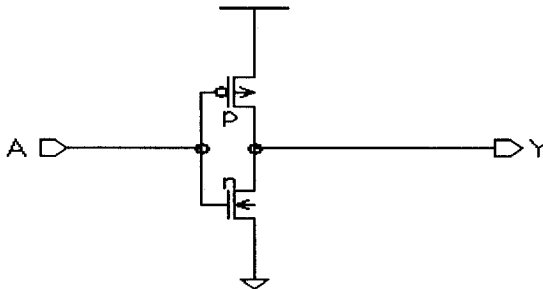
- IV, IVD2: 1
- IVD3, IVD4: 2



**Symbol**

A	Y
0	1
1	0

**Truth Table**



**Schematic**

**IV Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.36	$0.26 + 0.047 * SL$	$0.28 + 0.041 * SL$	$0.26 + 0.042 * SL$
	tPHL	0.10	$0.02 + 0.040 * SL$	$0.06 + 0.024 * SL$	$0.15 + 0.020 * SL$
	tR	0.48	$0.30 + 0.090 * SL$	$0.28 + 0.097 * SL$	$0.19 + 0.101 * SL$
	tF	0.36	$0.28 + 0.038 * SL$	$0.29 + 0.036 * SL$	$0.23 + 0.039 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVD2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.27	$0.22 + 0.028 * SL$	$0.24 + 0.021 * SL$	$0.25 + 0.021 * SL$
	tPHL	0.02	$-0.03 + 0.026 * SL$	$0.00 + 0.016 * SL$	$0.10 + 0.011 * SL$
	tR	0.34	$0.25 + 0.045 * SL$	$0.24 + 0.048 * SL$	$0.18 + 0.051 * SL$
	tF	0.29	$0.25 + 0.020 * SL$	$0.26 + 0.018 * SL$	$0.26 + 0.018 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVD3 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.26	$0.22 + 0.020 * SL$	$0.23 + 0.015 * SL$	$0.26 + 0.014 * SL$
	tPHL	0.00	$-0.03 + 0.019 * SL$	$-0.01 + 0.012 * SL$	$0.06 + 0.008 * SL$
	tR	0.31	$0.25 + 0.031 * SL$	$0.25 + 0.031 * SL$	$0.21 + 0.033 * SL$
	tF	0.27	$0.24 + 0.018 * SL$	$0.25 + 0.012 * SL$	$0.27 + 0.011 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVD4 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.24	$0.21 + 0.016 * SL$	$0.22 + 0.011 * SL$	$0.25 + 0.010 * SL$
	tPHL	-0.00	$-0.03 + 0.015 * SL$	$-0.02 + 0.010 * SL$	$0.04 + 0.007 * SL$
	tR	0.29	$0.24 + 0.022 * SL$	$0.24 + 0.021 * SL$	$0.22 + 0.022 * SL$
	tF	0.26	$0.23 + 0.014 * SL$	$0.24 + 0.010 * SL$	$0.27 + 0.008 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# IVD6/IVD8

Inverter with 6X Drive or 8X Drive

Input: A

Output: Y

Input Loading (SL):

- IVD6: 6

- IVD8: 8

Maximum Fanout (Rec. SL):

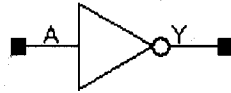
- IVD6: 168

- IVD8: 224

Gate Count:

- IVD6: 3

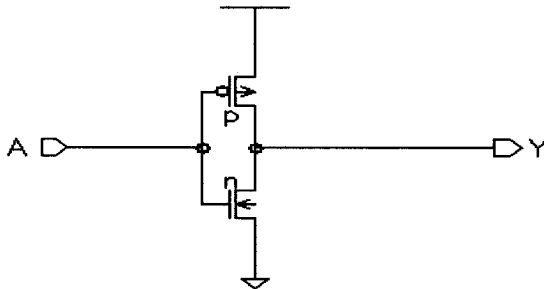
- IVD8: 4



Symbol

A	Y
0	1
1	0

Truth Table



Schematic

**IVD6 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.23	$0.21 + 0.011*SL$	$0.22 + 0.008*SL$	$0.25 + 0.007*SL$
	tPHL	-0.01	$-0.03 + 0.010*SL$	$-0.02 + 0.007*SL$	$0.02 + 0.005*SL$
	tR	0.27	$0.24 + 0.014*SL$	$0.24 + 0.014*SL$	$0.23 + 0.015*SL$
	tF	0.26	$0.23 + 0.011*SL$	$0.25 + 0.007*SL$	$0.26 + 0.006*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVD8 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

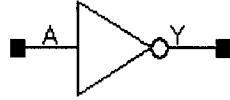
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.23	$0.21 + 0.009*SL$	$0.22 + 0.007*SL$	$0.24 + 0.005*SL$
	tPHL	-0.02	$-0.03 + 0.008*SL$	$-0.03 + 0.006*SL$	$0.01 + 0.004*SL$
	tR	0.26	$0.24 + 0.010*SL$	$0.24 + 0.011*SL$	$0.24 + 0.011*SL$
	tF	0.25	$0.23 + 0.008*SL$	$0.24 + 0.005*SL$	$0.26 + 0.005*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# IVD12/IVD16

Inverter with 12X Drive or 16X Drive

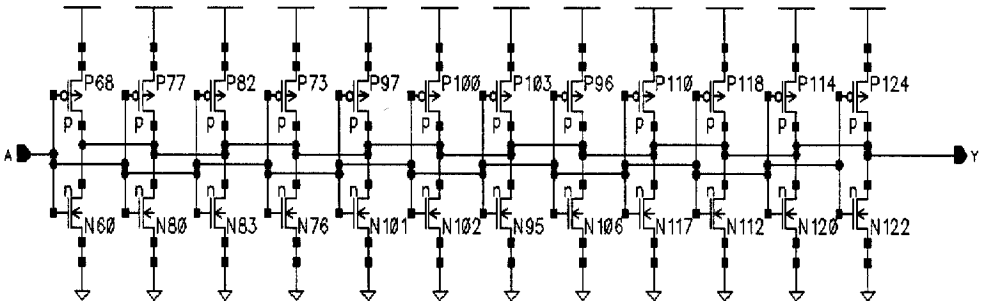
- Input: A
- Outputs: Y
- Input Loading (SL):
  - IVD12: 12
  - IVD16: 16
- Maximum Fanout (Rec. SL):
  - IVD12: 336
  - IVD16: 448
- Gate Count:
  - IVD12: 6
  - IVD16: 8



**Symbol**

A	Y
0	1
1	0

**Truth Table**



**Schematic**

**IVD12 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.22	$0.21 + 0.006*SL$	$0.22 + 0.005*SL$	$0.23 + 0.004*SL$
	tPHL	-0.02	$-0.03 + 0.006*SL$	$-0.03 + 0.004*SL$	$-0.01 + 0.003*SL$
	tR	0.27	$0.25 + 0.007*SL$	$0.25 + 0.008*SL$	$0.25 + 0.008*SL$
	tF	0.25	$0.24 + 0.004*SL$	$0.24 + 0.004*SL$	$0.26 + 0.003*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVD16 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.22	$0.21 + 0.005*SL$	$0.21 + 0.004*SL$	$0.23 + 0.003*SL$
	tPHL	-0.03	$-0.03 + 0.004*SL$	$-0.03 + 0.004*SL$	$-0.02 + 0.003*SL$
	tR	0.26	$0.25 + 0.006*SL$	$0.25 + 0.006*SL$	$0.25 + 0.006*SL$
	tF	0.25	$0.24 + 0.005*SL$	$0.25 + 0.003*SL$	$0.25 + 0.003*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# IVA/IVD2A/IVD3A/IVD4A

Inverter with 2X P, 1X N; 4X P, 2X N; 6X P, 3X N; 8X P, 4X N Transistors

Input: A

Output: Y

Input Loading (SL):

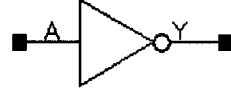
- IVA: 1.5
- IVD2A: 3
- IVD3A: 4.5
- IVD4A: 6

Maximum Fanout (Rec. SL):

- IVA: 56
- IVD2A: 112
- IVD3A: 168
- IVD4A: 224

Gate Count:

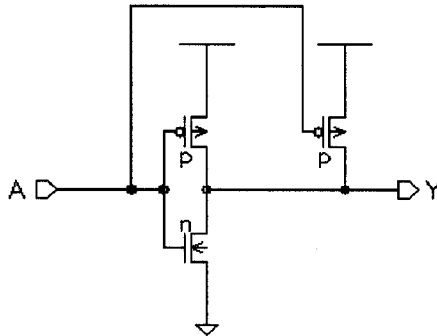
- IVA: 1
- IVD2A: 2
- IVD3A: 3
- IVD4A: 4



**Symbol**

A	Y
0	1
1	0

**Truth Table**



**Schematic**

**IVA Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.22	$0.15 + 0.033*SL$	$0.18 + 0.023*SL$	$0.22 + 0.021*SL$
	tPHL	0.15	$0.08 + 0.034*SL$	$0.12 + 0.023*SL$	$0.17 + 0.020*SL$
	tR	0.39	$0.30 + 0.044*SL$	$0.30 + 0.046*SL$	$0.22 + 0.050*SL$
	tF	0.36	$0.29 + 0.036*SL$	$0.29 + 0.035*SL$	$0.22 + 0.039*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVD2A Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.16	$0.12 + 0.020*SL$	$0.14 + 0.013*SL$	$0.20 + 0.010*SL$
	tPHL	0.11	$0.07 + 0.020*SL$	$0.09 + 0.014*SL$	$0.15 + 0.010*SL$
	tR	0.33	$0.29 + 0.022*SL$	$0.29 + 0.020*SL$	$0.26 + 0.021*SL$
	tF	0.31	$0.27 + 0.020*SL$	$0.27 + 0.018*SL$	$0.26 + 0.018*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVD3A Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.15	$0.12 + 0.014*SL$	$0.13 + 0.010*SL$	$0.18 + 0.007*SL$
	tPHL	0.09	$0.06 + 0.014*SL$	$0.08 + 0.010*SL$	$0.13 + 0.007*SL$
	tR	0.31	$0.28 + 0.015*SL$	$0.29 + 0.013*SL$	$0.28 + 0.014*SL$
	tF	0.29	$0.26 + 0.016*SL$	$0.27 + 0.012*SL$	$0.27 + 0.011*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVD4A Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

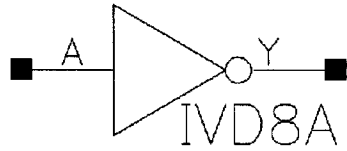
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.14	$0.12 + 0.011*SL$	$0.13 + 0.008*SL$	$0.17 + 0.006*SL$
	tPHL	0.09	$0.06 + 0.012*SL$	$0.07 + 0.008*SL$	$0.11 + 0.006*SL$
	tR	0.31	$0.29 + 0.011*SL$	$0.29 + 0.010*SL$	$0.29 + 0.010*SL$
	tF	0.28	$0.26 + 0.011*SL$	$0.27 + 0.009*SL$	$0.28 + 0.009*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# IVD8AIVD12A

Inverter with 16X P, 8X N Transistors; 24X P, 12X N Transistors

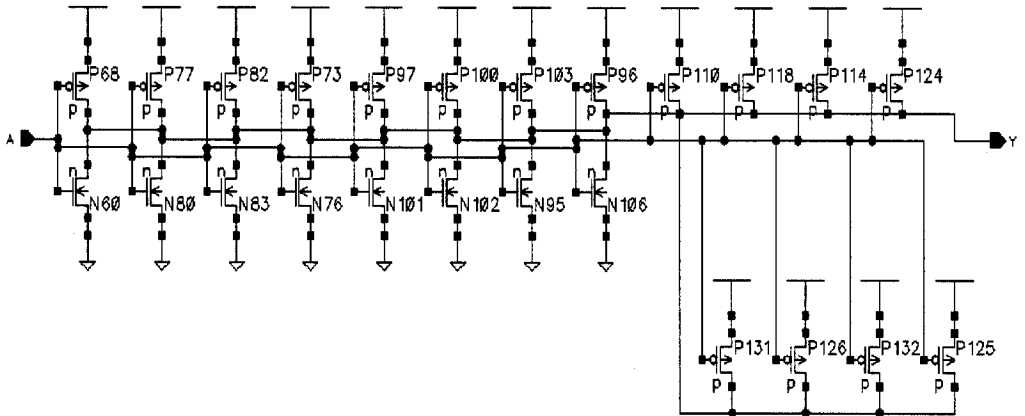
- Input: A  
Outputs: Y  
Input Loading (SL):  
- IVD8A: 8  
- IVD12A: 18  
Maximum Fanout (Rec. SL):  
- IVD8A: 448  
- IVD12A: 672  
Gate Count:  
- IVD8A: 8  
- IVD12A: 12



Symbol

A	Y
0	1
1	0

Truth Table



Schematic

**IVD8A Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.13	$0.12 + 0.006*SL$	$0.12 + 0.005*SL$	$0.15 + 0.004*SL$
	tPHL	0.07	$0.06 + 0.006*SL$	$0.07 + 0.005*SL$	$0.09 + 0.004*SL$
	tR	0.30	$0.29 + 0.005*SL$	$0.29 + 0.005*SL$	$0.30 + 0.005*SL$
	tF	0.28	$0.26 + 0.005*SL$	$0.27 + 0.005*SL$	$0.28 + 0.004*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVD12A Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.13	$0.12 + 0.004*SL$	$0.12 + 0.003*SL$	$0.14 + 0.003*SL$
	tPHL	0.07	$0.06 + 0.004*SL$	$0.07 + 0.003*SL$	$0.08 + 0.003*SL$
	tR	0.30	$0.29 + 0.003*SL$	$0.29 + 0.004*SL$	$0.30 + 0.003*SL$
	tF	0.27	$0.26 + 0.003*SL$	$0.26 + 0.004*SL$	$0.28 + 0.003*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

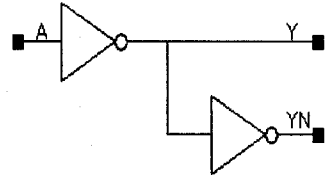


# IVCD11/IVCD13

## 1X Inverter into Inverter

Input: A  
Outputs: Y, YN  
Input Loading (SL): All : 1  
Maximum Fanout (Rec. SL):  
- IVCD11: All : 28  
- IVCD13: Y : 28  
YN: 84

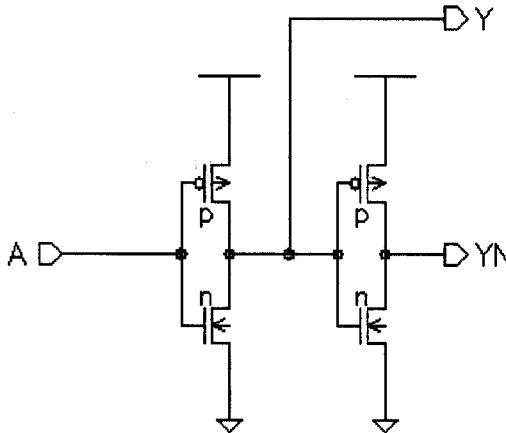
Gate Count:  
- IVCD11: 1  
- IVCD13: 2



**Symbol**

A	Y	YN
1	0	1
0	1	0

**Truth Table**



**Schematic**

**IVCD11 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.37	$0.28 + 0.045*SL$	$0.30 + 0.041*SL$	$0.28 + 0.042*SL$
	tPHL	0.10	$0.02 + 0.038*SL$	$0.06 + 0.024*SL$	$0.15 + 0.020*SL$
	tR	0.52	$0.34 + 0.091*SL$	$0.32 + 0.097*SL$	$0.24 + 0.101*SL$
	tF	0.36	$0.28 + 0.037*SL$	$0.30 + 0.033*SL$	$0.24 + 0.036*SL$
Y to YN	tPLH	0.32	$0.22 + 0.049*SL$	$0.25 + 0.041*SL$	$0.24 + 0.041*SL$
	tPHL	0.07	$-0.01 + 0.043*SL$	$0.04 + 0.025*SL$	$0.13 + 0.020*SL$
	tR	0.43	$0.25 + 0.090*SL$	$0.23 + 0.096*SL$	$0.14 + 0.101*SL$
	tF	0.33	$0.25 + 0.039*SL$	$0.26 + 0.034*SL$	$0.21 + 0.037*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVCD13 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.46	$0.38 + 0.040*SL$	$0.38 + 0.041*SL$	$0.36 + 0.042*SL$
	tPHL	0.16	$0.09 + 0.032*SL$	$0.12 + 0.023*SL$	$0.18 + 0.020*SL$
	tR	0.70	$0.52 + 0.092*SL$	$0.50 + 0.098*SL$	$0.43 + 0.102*SL$
	tF	0.44	$0.39 + 0.028*SL$	$0.37 + 0.033*SL$	$0.30 + 0.036*SL$
Y to YN	tPLH	0.25	$0.21 + 0.021*SL$	$0.23 + 0.015*SL$	$0.26 + 0.014*SL$
	tPHL	0.01	$-0.03 + 0.019*SL$	$-0.01 + 0.012*SL$	$0.07 + 0.008*SL$
	tR	0.31	$0.25 + 0.031*SL$	$0.25 + 0.031*SL$	$0.21 + 0.033*SL$
	tF	0.27	$0.24 + 0.017*SL$	$0.25 + 0.012*SL$	$0.27 + 0.012*SL$

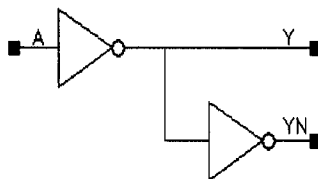
\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# IVCD22/IVCD26

## 2X Inverter into Inverter

Input: A  
Outputs: Y, YN  
Input Loading (SL): All : 2  
Maximum Fanout (Rec. SL):  
- IVCD22: All : 56  
- IVCD26: Y : 56  
YN: 168

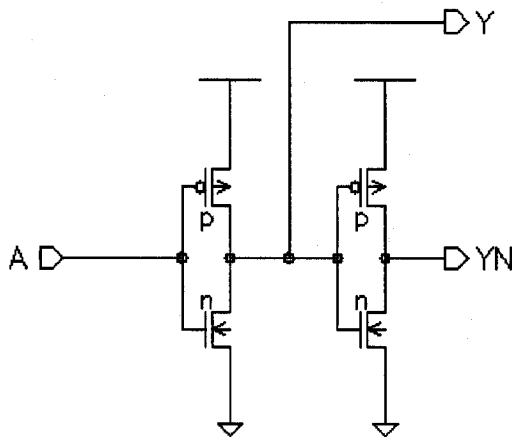
Gate Count:  
- IVCD22: 2  
- IVCD26: 4



**Symbol**

A	Y	YN
1	0	1
0	1	0

**Truth Table**



**Schematic**

**IVCD22 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.32	$0.28 + 0.024*SL$	$0.28 + 0.021*SL$	$0.29 + 0.021*SL$
	tPHL	0.06	$0.02 + 0.022*SL$	$0.04 + 0.015*SL$	$0.12 + 0.011*SL$
	tR	0.45	$0.35 + 0.047*SL$	$0.35 + 0.048*SL$	$0.30 + 0.051*SL$
	tF	0.34	$0.30 + 0.019*SL$	$0.30 + 0.018*SL$	$0.29 + 0.018*SL$
Y to YN	tPLH	0.27	$0.22 + 0.028*SL$	$0.24 + 0.021*SL$	$0.25 + 0.021*SL$
	tPHL	0.02	$-0.03 + 0.026*SL$	$0.00 + 0.016*SL$	$0.10 + 0.011*SL$
	tR	0.34	$0.25 + 0.045*SL$	$0.24 + 0.047*SL$	$0.18 + 0.051*SL$
	tF	0.29	$0.25 + 0.021*SL$	$0.26 + 0.018*SL$	$0.26 + 0.018*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVCD26 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

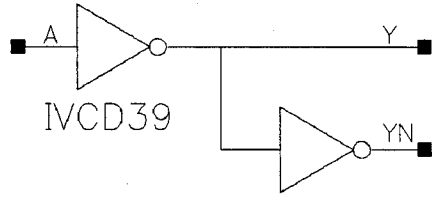
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.42	$0.37 + 0.021*SL$	$0.38 + 0.020*SL$	$0.37 + 0.021*SL$
	tPHL	0.13	$0.09 + 0.018*SL$	$0.11 + 0.013*SL$	$0.16 + 0.011*SL$
	tR	0.63	$0.53 + 0.046*SL$	$0.53 + 0.049*SL$	$0.48 + 0.051*SL$
	tF	0.43	$0.40 + 0.016*SL$	$0.40 + 0.017*SL$	$0.36 + 0.018*SL$
Y to YN	tPLH	0.23	$0.21 + 0.011*SL$	$0.22 + 0.008*SL$	$0.25 + 0.007*SL$
	tPHL	-0.01	$-0.03 + 0.010*SL$	$-0.02 + 0.008*SL$	$0.02 + 0.005*SL$
	tR	0.28	$0.25 + 0.015*SL$	$0.25 + 0.015*SL$	$0.24 + 0.016*SL$
	tF	0.26	$0.24 + 0.009*SL$	$0.25 + 0.007*SL$	$0.27 + 0.006*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# IVCD39

3X Inverter into 9X Inverter

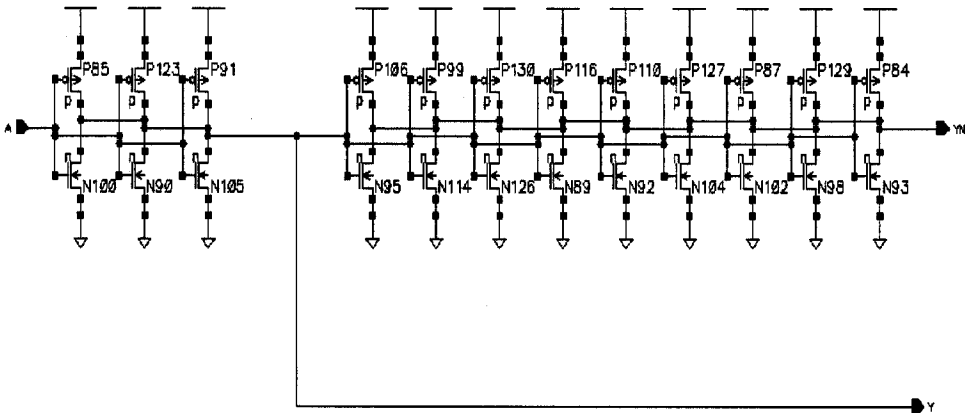
Input: A  
 Outputs: Y, YN  
 Input Loading (SL): 3  
 Maximum Fanout (Rec. SL): Y: 84, YN: 252  
 Gate Count: 6



Symbol

A	Y	YN
1	0	1
0	1	0

Truth Table



Schematic

**IVCD39 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

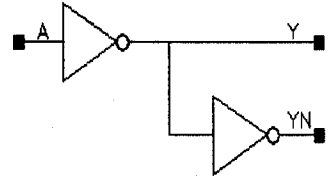
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.39	$0.36 + 0.014 * SL$	$0.37 + 0.013 * SL$	$0.37 + 0.013 * SL$
	tPHL	0.11	$0.09 + 0.012 * SL$	$0.10 + 0.010 * SL$	$0.14 + 0.008 * SL$
	tR	0.55	$0.50 + 0.029 * SL$	$0.50 + 0.029 * SL$	$0.46 + 0.031 * SL$
	tF	0.40	$0.39 + 0.009 * SL$	$0.38 + 0.011 * SL$	$0.36 + 0.012 * SL$
Y to YN	tPLH	0.18	$0.17 + 0.008 * SL$	$0.17 + 0.006 * SL$	$0.20 + 0.005 * SL$
	tPHL	0.05	$0.03 + 0.007 * SL$	$0.04 + 0.005 * SL$	$0.07 + 0.004 * SL$
	tR	0.28	$0.26 + 0.009 * SL$	$0.26 + 0.009 * SL$	$0.26 + 0.009 * SL$
	tF	0.26	$0.24 + 0.007 * SL$	$0.25 + 0.005 * SL$	$0.27 + 0.004 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# IVCD44

## 4X Inverter into Inverter

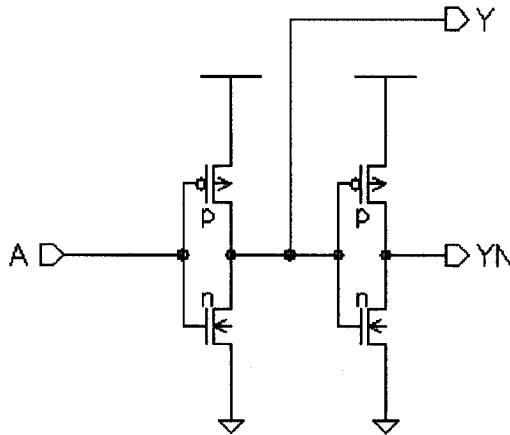
Inputs: A  
Outputs: Y, YN  
Input Loading (SL): All : 4  
Maximum Fanout (Rec. SL): All : 112  
Gate Count: 4



**Symbol**

A	Y	YN
1	0	1
0	1	0

**Truth Table**



**Schematic**

**IVCD44 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.30	$0.27 + 0.013*SL$	$0.28 + 0.011*SL$	$0.29 + 0.010*SL$
	tPHL	0.04	$0.02 + 0.012*SL$	$0.03 + 0.009*SL$	$0.07 + 0.007*SL$
	tR	0.40	$0.35 + 0.023*SL$	$0.35 + 0.024*SL$	$0.33 + 0.024*SL$
	tF	0.32	$0.30 + 0.009*SL$	$0.30 + 0.009*SL$	$0.30 + 0.009*SL$
Y to YN	tPLH	0.25	$0.21 + 0.016*SL$	$0.23 + 0.012*SL$	$0.26 + 0.010*SL$
	tPHL	-0.00	$-0.03 + 0.015*SL$	$-0.02 + 0.010*SL$	$0.04 + 0.007*SL$
	tR	0.30	$0.25 + 0.023*SL$	$0.25 + 0.023*SL$	$0.23 + 0.024*SL$
	tF	0.27	$0.24 + 0.014*SL$	$0.25 + 0.010*SL$	$0.27 + 0.009*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# IVCD11A/IVCD22A/IVCD44A/IVCD88A

Buffer with 1X, 2X, 4X and 8X Inverting and 1X, 2X, 4X and 8X Non-inverting Outputs

Input: A

Outputs: Y, YN

Input Loading (SL):

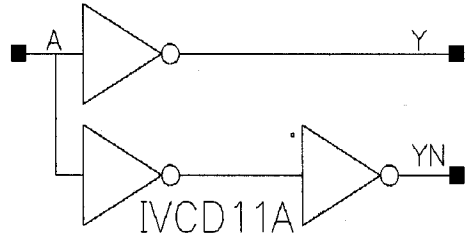
- IVCD11A: 2.5
- IVCD22A: 3.5
- IVCD44A: 5.5
- IVCD88A: 10

Maximum Fanout (Rec. SL):

- IVCD11A: 28
- IVCD22A: 56
- IVCD44A: 114
- IVCD88A: 224

Gate Count:

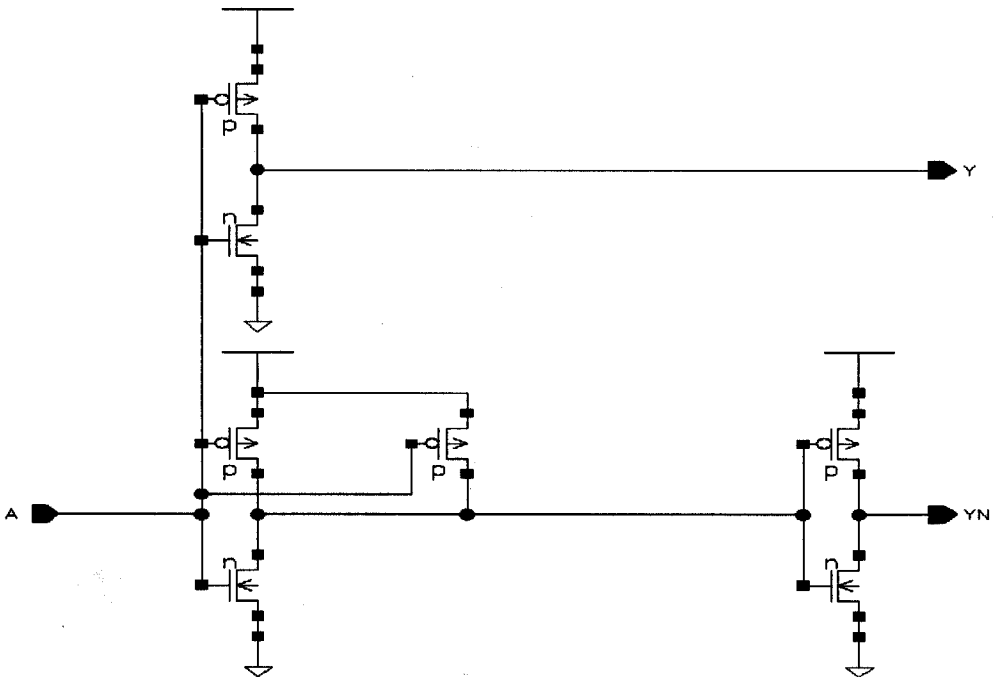
- IVCD11A: 2
- IVCD22A: 3
- IVCD44A: 5
- IVCD88A: 9



Symbol

A	Y	YN
1	0	1
0	1	0

Truth Table



Schematic

# IVCD11A/IVCD22A/IVCD44A/IVCD88A

Buffer with 1X, 2X, 4X and 8X Inverting and 1X, 2X, 4X and 8X Non-inverting Outputs

## IVCD11A Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.32	$0.22 + 0.049 \cdot \text{SL}$	$0.25 + 0.041 \cdot \text{SL}$	$0.23 + 0.042 \cdot \text{SL}$
	tPHL	0.07	$-0.02 + 0.043 \cdot \text{SL}$	$0.04 + 0.025 \cdot \text{SL}$	$0.13 + 0.020 \cdot \text{SL}$
	tR	0.43	$0.25 + 0.088 \cdot \text{SL}$	$0.23 + 0.096 \cdot \text{SL}$	$0.13 + 0.101 \cdot \text{SL}$
	tF	0.33	$0.25 + 0.041 \cdot \text{SL}$	$0.26 + 0.036 \cdot \text{SL}$	$0.21 + 0.039 \cdot \text{SL}$
A to YN	tPLH	0.29	$0.20 + 0.043 \cdot \text{SL}$	$0.21 + 0.042 \cdot \text{SL}$	$0.20 + 0.043 \cdot \text{SL}$
	tPHL	0.27	$0.21 + 0.026 \cdot \text{SL}$	$0.23 + 0.021 \cdot \text{SL}$	$0.24 + 0.020 \cdot \text{SL}$
	tR	0.31	$0.12 + 0.099 \cdot \text{SL}$	$0.11 + 0.101 \cdot \text{SL}$	$0.09 + 0.102 \cdot \text{SL}$
	tF	0.18	$0.11 + 0.034 \cdot \text{SL}$	$0.09 + 0.039 \cdot \text{SL}$	$0.06 + 0.041 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

## IVCD22A Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.27	$0.22 + 0.029 \cdot \text{SL}$	$0.24 + 0.021 \cdot \text{SL}$	$0.25 + 0.021 \cdot \text{SL}$
	tPHL	0.02	$-0.03 + 0.026 \cdot \text{SL}$	$0.00 + 0.016 \cdot \text{SL}$	$0.10 + 0.011 \cdot \text{SL}$
	tR	0.34	$0.25 + 0.045 \cdot \text{SL}$	$0.25 + 0.047 \cdot \text{SL}$	$0.18 + 0.051 \cdot \text{SL}$
	tF	0.29	$0.25 + 0.024 \cdot \text{SL}$	$0.26 + 0.018 \cdot \text{SL}$	$0.26 + 0.018 \cdot \text{SL}$
A to YN	tPLH	0.29	$0.24 + 0.022 \cdot \text{SL}$	$0.24 + 0.021 \cdot \text{SL}$	$0.24 + 0.021 \cdot \text{SL}$
	tPHL	0.27	$0.24 + 0.016 \cdot \text{SL}$	$0.25 + 0.011 \cdot \text{SL}$	$0.28 + 0.010 \cdot \text{SL}$
	tR	0.22	$0.13 + 0.048 \cdot \text{SL}$	$0.12 + 0.051 \cdot \text{SL}$	$0.09 + 0.052 \cdot \text{SL}$
	tF	0.16	$0.12 + 0.018 \cdot \text{SL}$	$0.12 + 0.019 \cdot \text{SL}$	$0.09 + 0.020 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

## IVCD44A Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.24	$0.21 + 0.016 \cdot \text{SL}$	$0.22 + 0.011 \cdot \text{SL}$	$0.25 + 0.010 \cdot \text{SL}$
	tPHL	-0.00	$-0.03 + 0.015 \cdot \text{SL}$	$-0.02 + 0.010 \cdot \text{SL}$	$0.04 + 0.007 \cdot \text{SL}$
	tR	0.28	$0.24 + 0.022 \cdot \text{SL}$	$0.24 + 0.021 \cdot \text{SL}$	$0.22 + 0.022 \cdot \text{SL}$
	tF	0.26	$0.23 + 0.014 \cdot \text{SL}$	$0.24 + 0.010 \cdot \text{SL}$	$0.27 + 0.008 \cdot \text{SL}$
A to YN	tPLH	0.32	$0.30 + 0.011 \cdot \text{SL}$	$0.30 + 0.010 \cdot \text{SL}$	$0.31 + 0.010 \cdot \text{SL}$
	tPHL	0.30	$0.29 + 0.009 \cdot \text{SL}$	$0.29 + 0.006 \cdot \text{SL}$	$0.32 + 0.005 \cdot \text{SL}$
	tR	0.18	$0.13 + 0.022 \cdot \text{SL}$	$0.13 + 0.023 \cdot \text{SL}$	$0.11 + 0.023 \cdot \text{SL}$
	tF	0.15	$0.13 + 0.010 \cdot \text{SL}$	$0.14 + 0.008 \cdot \text{SL}$	$0.12 + 0.009 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

## IVCD88A Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.22	$0.21 + 0.009 \cdot \text{SL}$	$0.21 + 0.007 \cdot \text{SL}$	$0.24 + 0.005 \cdot \text{SL}$
	tPHL	-0.02	$-0.03 + 0.008 \cdot \text{SL}$	$-0.03 + 0.006 \cdot \text{SL}$	$0.01 + 0.004 \cdot \text{SL}$
	tR	0.26	$0.24 + 0.011 \cdot \text{SL}$	$0.24 + 0.011 \cdot \text{SL}$	$0.24 + 0.011 \cdot \text{SL}$
	tF	0.25	$0.23 + 0.008 \cdot \text{SL}$	$0.24 + 0.005 \cdot \text{SL}$	$0.26 + 0.004 \cdot \text{SL}$
A to YN	tPLH	0.24	$0.23 + 0.006 \cdot \text{SL}$	$0.23 + 0.005 \cdot \text{SL}$	$0.24 + 0.005 \cdot \text{SL}$
	tPHL	0.43	$0.42 + 0.005 \cdot \text{SL}$	$0.42 + 0.004 \cdot \text{SL}$	$0.44 + 0.003 \cdot \text{SL}$
	tR	0.16	$0.14 + 0.011 \cdot \text{SL}$	$0.14 + 0.011 \cdot \text{SL}$	$0.12 + 0.011 \cdot \text{SL}$
	tF	0.17	$0.16 + 0.005 \cdot \text{SL}$	$0.17 + 0.004 \cdot \text{SL}$	$0.16 + 0.004 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

# IVT/IVTD2/IVTD5/IVTD9

Inverting 3-State Buffer, Enable High, with 1X Drive, 2X Drive, 5X Drive or 9X Drive

Inputs: A, E

Output: Y

Input Loading (SL):

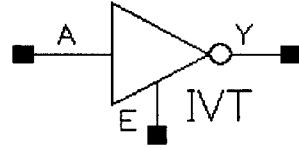
- IVT: A : 1, E : 1.5
- IVTD2: A : 1, E : 2
- IVTD5: A : 1, E : 2
- IVTD9: A : 1, E : 2

Maximum Fanout (Rec. SL):

- IVT: 28
- IVTD2: 56
- IVTD5: 120
- IVTD9: 232

Gate Count:

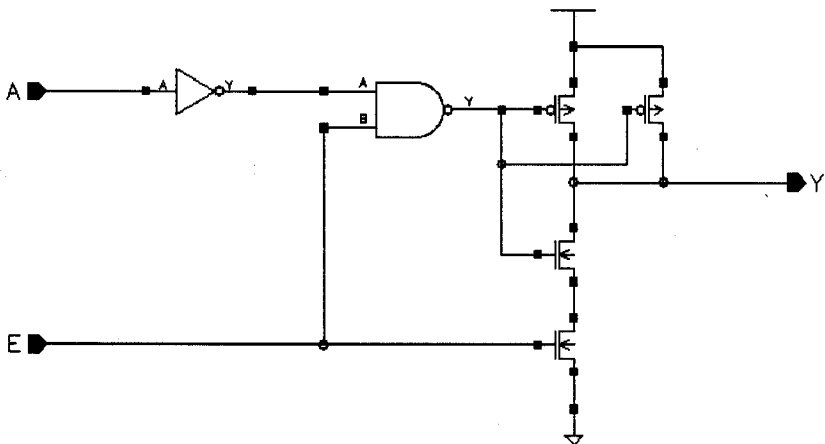
- IVT : 3
- IVTD2 : 4
- IVTD5 : 5
- IVTD9 : 7



Symbol

A	E	Y
x	0	hi-z
0	1	1
1	1	0

Truth Table



Schematic

**IVT Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.47	$0.42 + 0.024*SL$	$0.44 + 0.020*SL$	$0.44 + 0.020*SL$
	tPHL	0.32	$0.25 + 0.033*SL$	$0.26 + 0.030*SL$	$0.27 + 0.030*SL$
	tR	0.19	$0.11 + 0.043*SL$	$0.10 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.25	$0.13 + 0.061*SL$	$0.12 + 0.063*SL$	$0.10 + 0.064*SL$
E to Y	tPLH	0.21	$0.16 + 0.026*SL$	$0.17 + 0.021*SL$	$0.19 + 0.020*SL$
	tPHL	0.05	$-0.04 + 0.048*SL$	$0.00 + 0.032*SL$	$0.06 + 0.030*SL$
	tR	0.24	$0.15 + 0.041*SL$	$0.14 + 0.044*SL$	$0.11 + 0.046*SL$
	tF	0.36	$0.24 + 0.060*SL$	$0.24 + 0.059*SL$	$0.17 + 0.063*SL$
	tPLZ	0.40	$0.40 + -0.000*SL$	$0.40 + -0.000*SL$	$0.40 + -0.000*SL$
	tPHZ	0.52	$0.52 + -0.000*SL$	$0.52 + -0.000*SL$	$0.52 + -0.000*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**IVTD2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.50	$0.47 + 0.014*SL$	$0.48 + 0.011*SL$	$0.49 + 0.010*SL$
	tPHL	0.35	$0.31 + 0.019*SL$	$0.32 + 0.016*SL$	$0.34 + 0.015*SL$
	tR	0.17	$0.13 + 0.020*SL$	$0.12 + 0.023*SL$	$0.11 + 0.023*SL$
	tF	0.22	$0.16 + 0.030*SL$	$0.16 + 0.031*SL$	$0.13 + 0.032*SL$
E to Y	tPLH	0.24	$0.21 + 0.015*SL$	$0.22 + 0.011*SL$	$0.24 + 0.010*SL$
	tPHL	0.00	$-0.06 + 0.029*SL$	$-0.03 + 0.019*SL$	$0.04 + 0.016*SL$
	tR	0.20	$0.17 + 0.019*SL$	$0.16 + 0.022*SL$	$0.13 + 0.023*SL$
	tF	0.29	$0.23 + 0.034*SL$	$0.24 + 0.030*SL$	$0.22 + 0.031*SL$
	tPLZ	0.40	$0.40 + -0.000*SL$	$0.40 + -0.000*SL$	$0.40 + -0.000*SL$
	tPHZ	0.62	$0.62 + -0.000*SL$	$0.62 + -0.000*SL$	$0.62 + 0.000*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# IVTD5/IVTD9

Inverting 3-State Buffer, Enable High, with 5X Drive or 9X Drive

## IVTD5 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{p}$  and  $t_{f}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t <sub>PLH</sub>	0.54	0.52 + 0.011*SL	0.52 + 0.009*SL	0.54 + 0.008*SL
	t <sub>PHL</sub>	0.40	0.39 + 0.007*SL	0.39 + 0.006*SL	0.41 + 0.004*SL
	t <sub>R</sub>	0.16	0.12 + 0.021*SL	0.13 + 0.019*SL	0.13 + 0.019*SL
	t <sub>F</sub>	0.15	0.14 + 0.007*SL	0.13 + 0.007*SL	0.13 + 0.008*SL
E to Y	t <sub>PLH</sub>	0.19	0.16 + 0.015*SL	0.17 + 0.011*SL	0.21 + 0.009*SL
	t <sub>PHL</sub>	0.31	0.29 + 0.010*SL	0.30 + 0.006*SL	0.33 + 0.005*SL
	t <sub>R</sub>	0.20	0.16 + 0.019*SL	0.16 + 0.018*SL	0.15 + 0.018*SL
	t <sub>F</sub>	0.12	0.09 + 0.011*SL	0.10 + 0.009*SL	0.11 + 0.008*SL
	t <sub>PLZ</sub>	0.40	0.40 + -0.000*SL	0.40 + -0.000*SL	0.40 + -0.000*SL
	t <sub>PHZ</sub>	0.67	0.67 + -0.000*SL	0.67 + -0.000*SL	0.67 + -0.000*SL

\*Range1 : SL < 3.00, \*Range2 : 3.00 ≤ SL ≤ 20.00, \*Range3 : 20.00 < SL

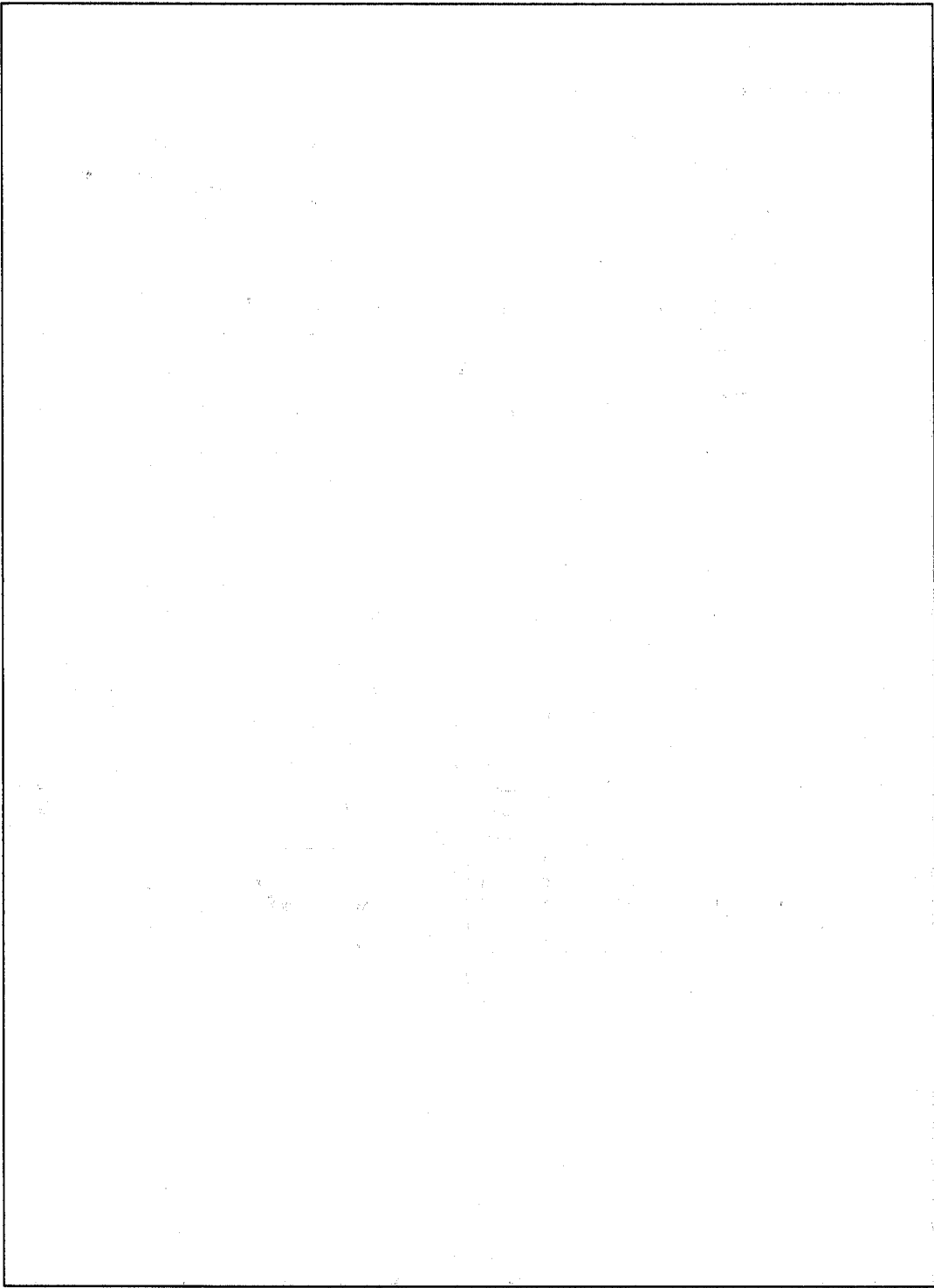
## IVTD9 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{p}$  and  $t_{f}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t <sub>PLH</sub>	0.60	0.59 + 0.007*SL	0.59 + 0.006*SL	0.60 + 0.005*SL
	t <sub>PHL</sub>	0.46	0.45 + 0.004*SL	0.45 + 0.004*SL	0.47 + 0.003*SL
	t <sub>R</sub>	0.17	0.14 + 0.013*SL	0.15 + 0.012*SL	0.15 + 0.011*SL
	t <sub>F</sub>	0.20	0.19 + 0.003*SL	0.19 + 0.004*SL	0.19 + 0.004*SL
E to Y	t <sub>PLH</sub>	0.23	0.21 + 0.010*SL	0.22 + 0.007*SL	0.25 + 0.006*SL
	t <sub>PHL</sub>	0.35	0.33 + 0.007*SL	0.34 + 0.005*SL	0.37 + 0.004*SL
	t <sub>R</sub>	0.21	0.19 + 0.012*SL	0.19 + 0.011*SL	0.19 + 0.011*SL
	t <sub>F</sub>	0.13	0.11 + 0.008*SL	0.12 + 0.006*SL	0.14 + 0.005*SL
	t <sub>PLZ</sub>	0.40	0.40 + -0.000*SL	0.40 + -0.000*SL	0.40 + -0.000*SL
	t <sub>PHZ</sub>	0.86	0.86 + 0.000*SL	0.86 + 0.000*SL	0.86 + -0.000*SL

\*Range1 : SL < 3.00, \*Range2 : 3.00 ≤ SL ≤ 20.00, \*Range3 : 20.00 < SL



# ND2/ND2D2/ND2D5/ND2D7

2 Input NAND with 1X Drive, 2X Drive, 5X Drive or 7X Drive

Inputs: A, B

Output: Y

Input Loading (SL):

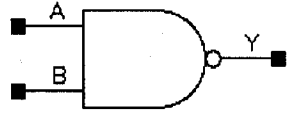
- ND2 : All : 1
- ND2D2: All : 2
- ND2D5: All: 1
- ND2D7: All: 1

Maximum Fanout (Rec. SL):

- ND2 : 28
- ND2D2 : 56
- ND2D5: 140
- ND2D7: 196

Gate Count:

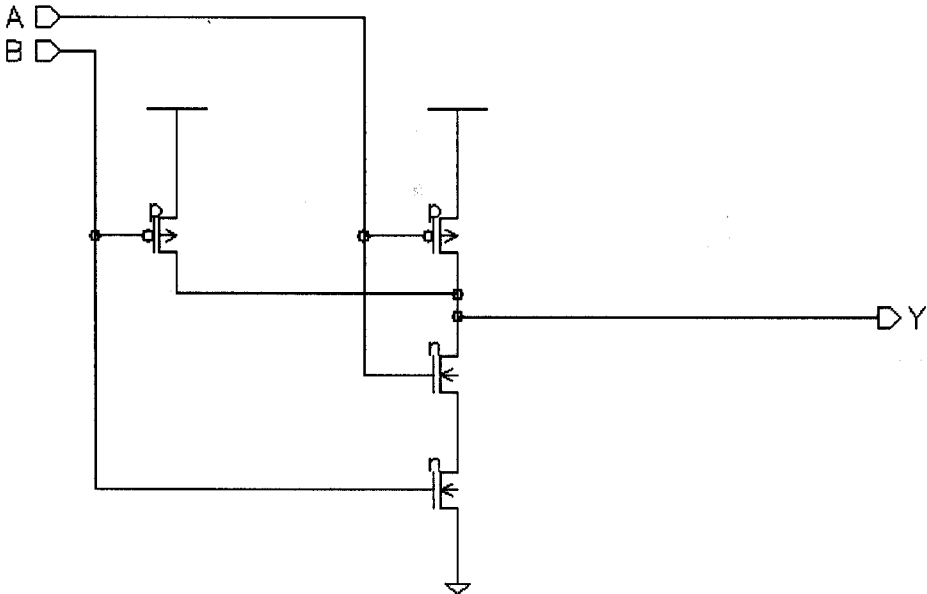
- ND2 : 1
- ND2D2 : 2
- ND2D5: 4
- ND2D7: 5



Symbol

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table



Schematic

**ND2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.32	$0.21 + 0.051 * SL$	$0.24 + 0.042 * SL$	$0.24 + 0.042 * SL$
	tPHL	0.16	$0.07 + 0.049 * SL$	$0.11 + 0.033 * SL$	$0.16 + 0.031 * SL$
	tR	0.49	$0.32 + 0.085 * SL$	$0.29 + 0.095 * SL$	$0.17 + 0.101 * SL$
	tF	0.44	$0.32 + 0.060 * SL$	$0.31 + 0.062 * SL$	$0.21 + 0.067 * SL$
B to Y	tPLH	0.38	$0.29 + 0.045 * SL$	$0.30 + 0.041 * SL$	$0.28 + 0.042 * SL$
	tPHL	0.12	$0.04 + 0.042 * SL$	$0.07 + 0.032 * SL$	$0.10 + 0.031 * SL$
	tR	0.57	$0.40 + 0.083 * SL$	$0.37 + 0.095 * SL$	$0.24 + 0.101 * SL$
	tF	0.41	$0.30 + 0.053 * SL$	$0.27 + 0.063 * SL$	$0.17 + 0.068 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**ND2D2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.26	$0.20 + 0.028 * SL$	$0.22 + 0.021 * SL$	$0.25 + 0.020 * SL$
	tPHL	0.11	$0.06 + 0.028 * SL$	$0.09 + 0.019 * SL$	$0.15 + 0.015 * SL$
	tR	0.39	$0.31 + 0.039 * SL$	$0.30 + 0.042 * SL$	$0.24 + 0.046 * SL$
	tF	0.37	$0.31 + 0.030 * SL$	$0.31 + 0.029 * SL$	$0.27 + 0.031 * SL$
B to Y	tPLH	0.33	$0.28 + 0.023 * SL$	$0.29 + 0.020 * SL$	$0.29 + 0.020 * SL$
	tPHL	0.08	$0.03 + 0.023 * SL$	$0.05 + 0.017 * SL$	$0.09 + 0.015 * SL$
	tR	0.48	$0.40 + 0.038 * SL$	$0.39 + 0.042 * SL$	$0.31 + 0.045 * SL$
	tF	0.35	$0.30 + 0.025 * SL$	$0.29 + 0.028 * SL$	$0.23 + 0.031 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# ND2D5/ND2D7

2 Input NAND with 5X Drive or 7X Drive

## ND2D5 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.52	$0.50 + 0.010 * SL$	$0.50 + 0.009 * SL$	$0.51 + 0.009 * SL$
	tPHL	0.44	$0.42 + 0.009 * SL$	$0.43 + 0.006 * SL$	$0.46 + 0.005 * SL$
	tR	0.17	$0.14 + 0.017 * SL$	$0.13 + 0.020 * SL$	$0.12 + 0.020 * SL$
	tF	0.19	$0.18 + 0.008 * SL$	$0.18 + 0.008 * SL$	$0.17 + 0.008 * SL$
B to Y	tPLH	0.59	$0.57 + 0.010 * SL$	$0.58 + 0.009 * SL$	$0.58 + 0.009 * SL$
	tPHL	0.42	$0.40 + 0.008 * SL$	$0.40 + 0.006 * SL$	$0.43 + 0.005 * SL$
	tR	0.17	$0.13 + 0.020 * SL$	$0.13 + 0.020 * SL$	$0.12 + 0.020 * SL$
	tF	0.19	$0.18 + 0.006 * SL$	$0.18 + 0.008 * SL$	$0.18 + 0.008 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

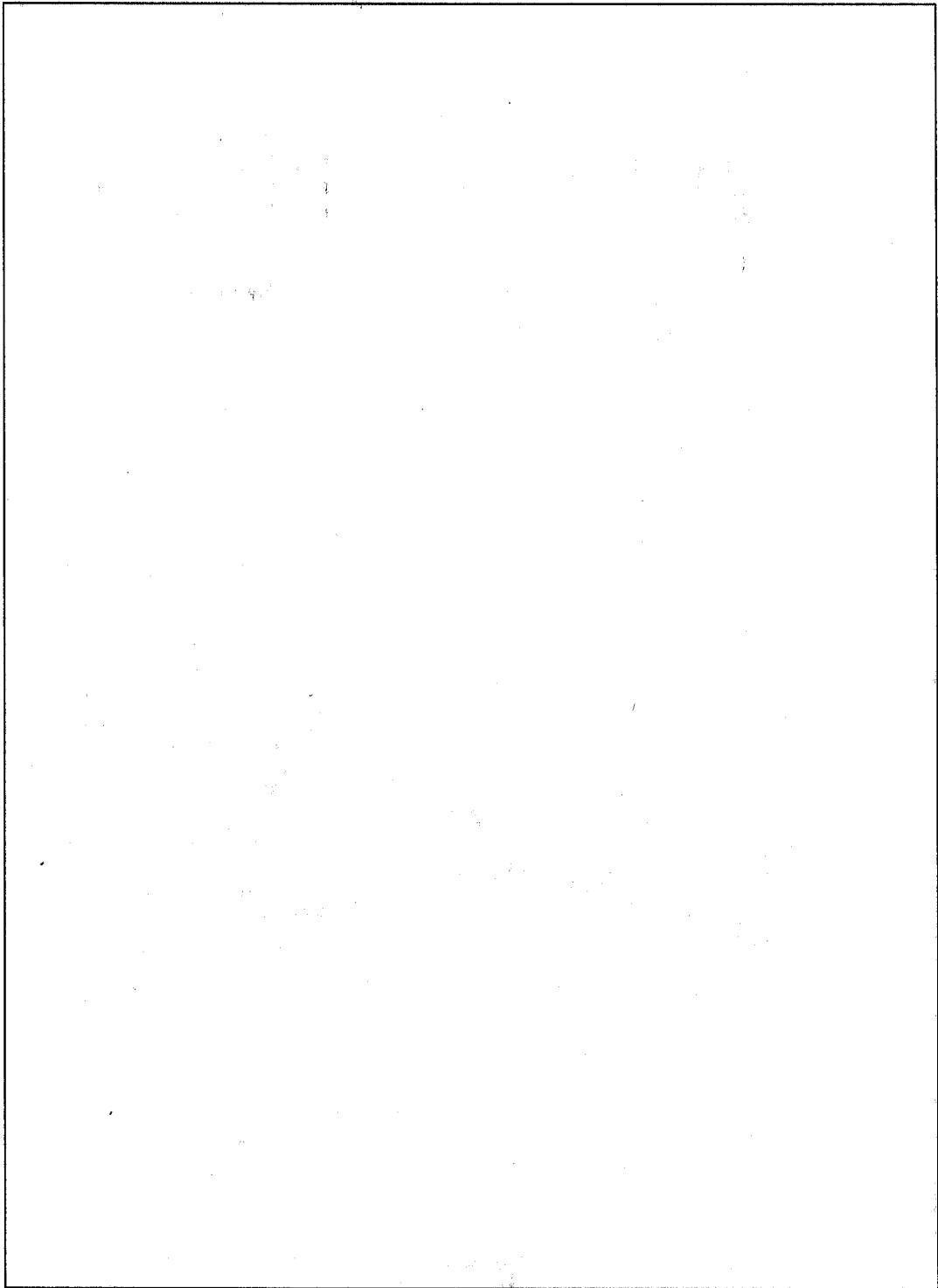
## ND2D7 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.57	$0.55 + 0.007 * SL$	$0.55 + 0.006 * SL$	$0.56 + 0.006 * SL$
	tPHL	0.50	$0.49 + 0.007 * SL$	$0.49 + 0.005 * SL$	$0.52 + 0.004 * SL$
	tR	0.18	$0.15 + 0.012 * SL$	$0.15 + 0.014 * SL$	$0.13 + 0.014 * SL$
	tF	0.23	$0.22 + 0.007 * SL$	$0.22 + 0.006 * SL$	$0.23 + 0.005 * SL$
B to Y	tPLH	0.64	$0.63 + 0.007 * SL$	$0.63 + 0.006 * SL$	$0.64 + 0.006 * SL$
	tPHL	0.48	$0.47 + 0.007 * SL$	$0.47 + 0.005 * SL$	$0.49 + 0.004 * SL$
	tR	0.18	$0.16 + 0.012 * SL$	$0.15 + 0.014 * SL$	$0.14 + 0.014 * SL$
	tF	0.23	$0.23 + 0.002 * SL$	$0.22 + 0.006 * SL$	$0.23 + 0.005 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# ND3/ND3D2/ND3D4/ND3D6

3 Input NAND with 1X Drive, 2X Drive, 4X Drive or 6X Drive

Inputs: A, B, C

Output: Y

Input Loading (SL):

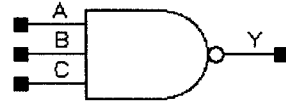
- ND3 : All : 1
- ND3D2 : All : 2
- ND3D4: All: 1
- ND3D6:All: 1

Maximum Fanout (Rec. SL):

- ND3 : 18
- ND3D2 : 40
- ND3D4: 112
- ND3D6: 168

Gate Count:

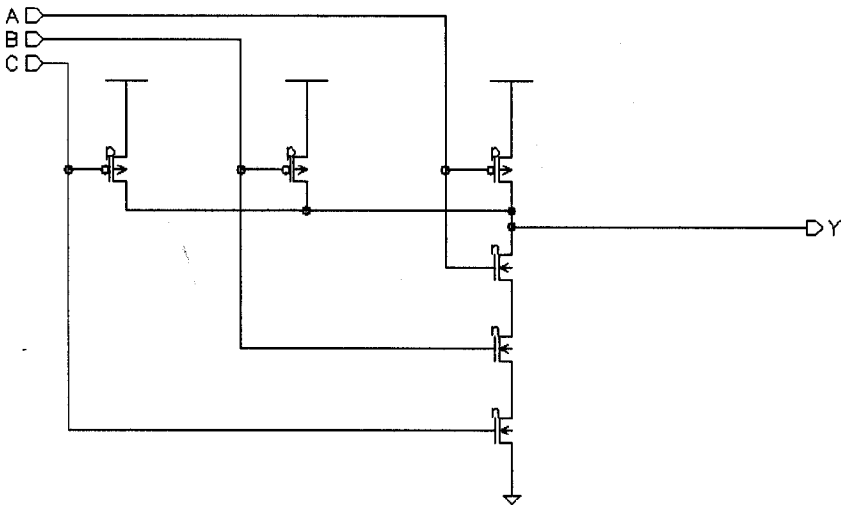
- ND3 : 2
- ND3D2 : 3
- ND3D4: 4
- ND3D6: 5



Symbol

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table



Schematic

**ND3 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{p}$  and  $t_{f}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.32	$0.21 + 0.052*SL$	$0.24 + 0.042*SL$	$0.24 + 0.042*SL$
	tPHL	0.25	$0.14 + 0.054*SL$	$0.17 + 0.043*SL$	$0.19 + 0.043*SL$
	tR	0.53	$0.36 + 0.084*SL$	$0.32 + 0.095*SL$	$0.21 + 0.101*SL$
	tF	0.57	$0.40 + 0.086*SL$	$0.38 + 0.093*SL$	$0.26 + 0.099*SL$
B to Y	tPLH	0.37	$0.28 + 0.047*SL$	$0.29 + 0.042*SL$	$0.29 + 0.042*SL$
	tPHL	0.23	$0.13 + 0.050*SL$	$0.15 + 0.043*SL$	$0.16 + 0.043*SL$
	tR	0.61	$0.44 + 0.082*SL$	$0.41 + 0.095*SL$	$0.28 + 0.101*SL$
	tF	0.56	$0.40 + 0.080*SL$	$0.36 + 0.094*SL$	$0.25 + 0.100*SL$
C to Y	tPLH	0.42	$0.33 + 0.043*SL$	$0.34 + 0.042*SL$	$0.33 + 0.042*SL$
	tPHL	0.20	$0.10 + 0.047*SL$	$0.12 + 0.043*SL$	$0.12 + 0.043*SL$
	tR	0.70	$0.54 + 0.080*SL$	$0.50 + 0.094*SL$	$0.36 + 0.101*SL$
	tF	0.52	$0.36 + 0.081*SL$	$0.32 + 0.096*SL$	$0.24 + 0.100*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**ND3D2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{p}$  and  $t_{f}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.25	$0.20 + 0.029*SL$	$0.22 + 0.021*SL$	$0.25 + 0.020*SL$
	tPHL	0.20	$0.14 + 0.030*SL$	$0.16 + 0.023*SL$	$0.19 + 0.021*SL$
	tR	0.44	$0.36 + 0.037*SL$	$0.35 + 0.042*SL$	$0.27 + 0.046*SL$
	tF	0.48	$0.40 + 0.041*SL$	$0.39 + 0.045*SL$	$0.33 + 0.048*SL$
B to Y	tPLH	0.32	$0.27 + 0.024*SL$	$0.28 + 0.021*SL$	$0.29 + 0.020*SL$
	tPHL	0.18	$0.12 + 0.026*SL$	$0.14 + 0.022*SL$	$0.16 + 0.021*SL$
	tR	0.52	$0.45 + 0.038*SL$	$0.43 + 0.042*SL$	$0.35 + 0.046*SL$
	tF	0.47	$0.39 + 0.038*SL$	$0.37 + 0.045*SL$	$0.30 + 0.048*SL$
C to Y	tPLH	0.36	$0.32 + 0.022*SL$	$0.33 + 0.020*SL$	$0.33 + 0.020*SL$
	tPHL	0.15	$0.10 + 0.025*SL$	$0.11 + 0.022*SL$	$0.12 + 0.021*SL$
	tR	0.61	$0.54 + 0.036*SL$	$0.52 + 0.041*SL$	$0.44 + 0.045*SL$
	tF	0.44	$0.36 + 0.038*SL$	$0.34 + 0.045*SL$	$0.27 + 0.049*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# ND3D4/ND3D6

3 Input NAND with 4X Drive or 6X Drive

## ND3D4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{RQ}$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.50	$0.47 + 0.012 \cdot SL$	$0.48 + 0.011 \cdot SL$	$0.48 + 0.011 \cdot SL$
	tPHL	0.51	$0.49 + 0.010 \cdot SL$	$0.50 + 0.007 \cdot SL$	$0.53 + 0.006 \cdot SL$
	tR	0.17	$0.13 + 0.022 \cdot SL$	$0.12 + 0.025 \cdot SL$	$0.10 + 0.026 \cdot SL$
	tF	0.18	$0.16 + 0.009 \cdot SL$	$0.16 + 0.009 \cdot SL$	$0.15 + 0.010 \cdot SL$
B to Y	tPLH	0.57	$0.54 + 0.012 \cdot SL$	$0.55 + 0.011 \cdot SL$	$0.55 + 0.011 \cdot SL$
	tPHL	0.51	$0.49 + 0.010 \cdot SL$	$0.50 + 0.007 \cdot SL$	$0.53 + 0.006 \cdot SL$
	tR	0.17	$0.13 + 0.024 \cdot SL$	$0.12 + 0.025 \cdot SL$	$0.11 + 0.026 \cdot SL$
	tF	0.18	$0.16 + 0.007 \cdot SL$	$0.16 + 0.009 \cdot SL$	$0.15 + 0.010 \cdot SL$
C to Y	tPLH	0.62	$0.59 + 0.011 \cdot SL$	$0.60 + 0.011 \cdot SL$	$0.60 + 0.011 \cdot SL$
	tPHL	0.47	$0.45 + 0.011 \cdot SL$	$0.46 + 0.007 \cdot SL$	$0.49 + 0.006 \cdot SL$
	tR	0.18	$0.13 + 0.023 \cdot SL$	$0.13 + 0.025 \cdot SL$	$0.11 + 0.026 \cdot SL$
	tF	0.18	$0.16 + 0.009 \cdot SL$	$0.16 + 0.010 \cdot SL$	$0.16 + 0.010 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

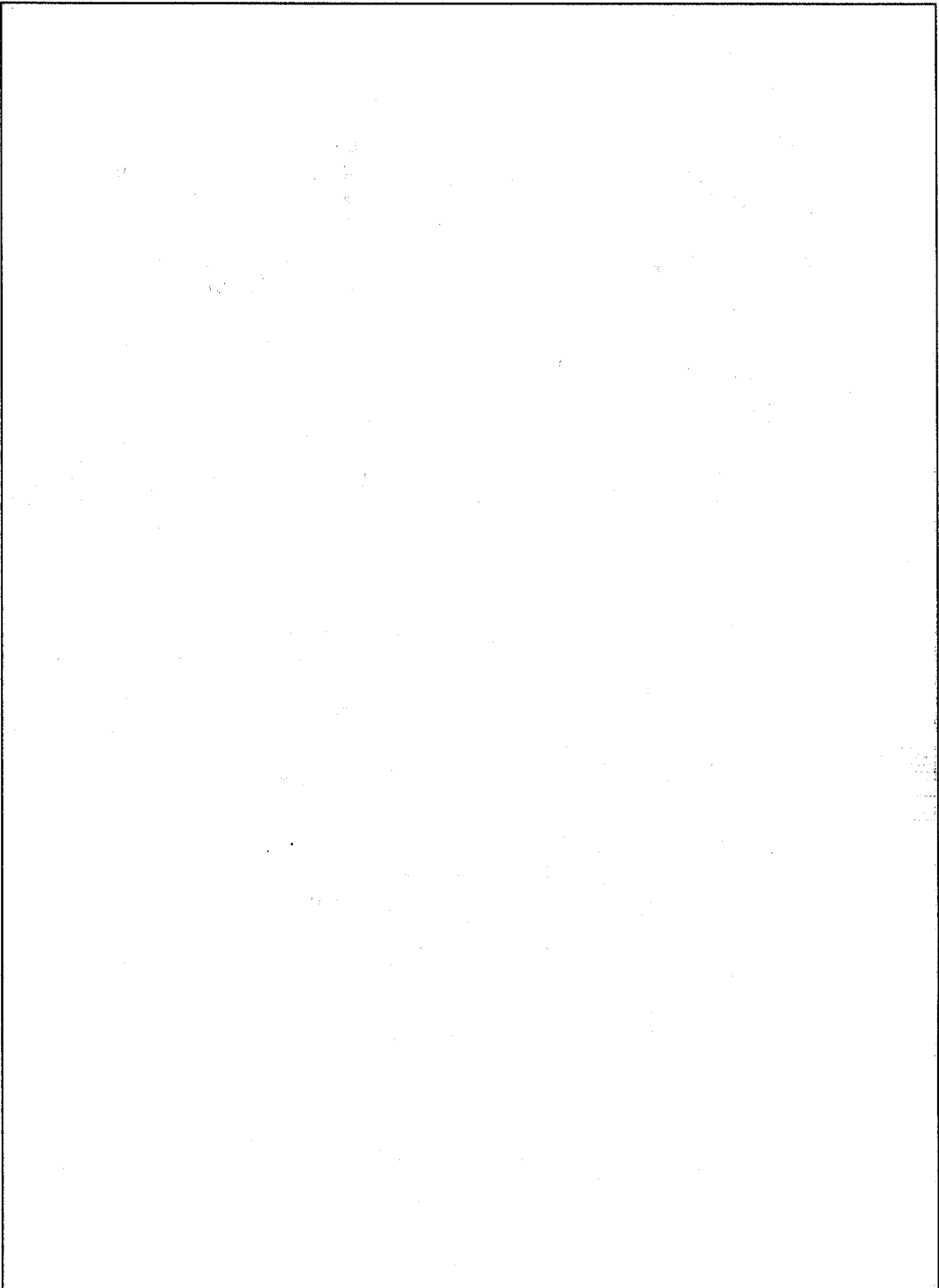
## ND3D6 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{RQ}$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.54	$0.53 + 0.008 \cdot SL$	$0.53 + 0.007 \cdot SL$	$0.54 + 0.007 \cdot SL$
	tPHL	0.58	$0.56 + 0.008 \cdot SL$	$0.57 + 0.006 \cdot SL$	$0.59 + 0.005 \cdot SL$
	tR	0.18	$0.15 + 0.014 \cdot SL$	$0.14 + 0.016 \cdot SL$	$0.13 + 0.017 \cdot SL$
	tF	0.22	$0.21 + 0.004 \cdot SL$	$0.20 + 0.006 \cdot SL$	$0.20 + 0.006 \cdot SL$
B to Y	tPLH	0.61	$0.60 + 0.008 \cdot SL$	$0.60 + 0.007 \cdot SL$	$0.61 + 0.007 \cdot SL$
	tPHL	0.57	$0.56 + 0.007 \cdot SL$	$0.56 + 0.006 \cdot SL$	$0.59 + 0.005 \cdot SL$
	tR	0.18	$0.15 + 0.014 \cdot SL$	$0.14 + 0.016 \cdot SL$	$0.13 + 0.017 \cdot SL$
	tF	0.22	$0.21 + 0.002 \cdot SL$	$0.20 + 0.007 \cdot SL$	$0.21 + 0.006 \cdot SL$
C to Y	tPLH	0.67	$0.65 + 0.008 \cdot SL$	$0.65 + 0.007 \cdot SL$	$0.66 + 0.007 \cdot SL$
	tPHL	0.54	$0.52 + 0.008 \cdot SL$	$0.53 + 0.006 \cdot SL$	$0.56 + 0.005 \cdot SL$
	tR	0.18	$0.15 + 0.015 \cdot SL$	$0.14 + 0.016 \cdot SL$	$0.13 + 0.017 \cdot SL$
	tF	0.22	$0.20 + 0.007 \cdot SL$	$0.20 + 0.006 \cdot SL$	$0.21 + 0.006 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# ND4/ND4D2/ND4D5/ND4D7

4 Input NAND with 1X Drive, 2X Drive, 5X Drive or 7X Drive

Inputs: A, B, C, D

Output: Y

Input Loading (SL):

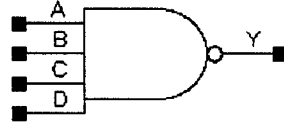
- ND4: All : 1
- ND4D2: All : 2
- ND4D5: All: 1
- ND4D7: All: 1

Maximum Fanout (Rec. SL):

- ND4: 14
- ND4D2: 28
- ND4D5: 140
- ND4D7: 196

Gate Count:

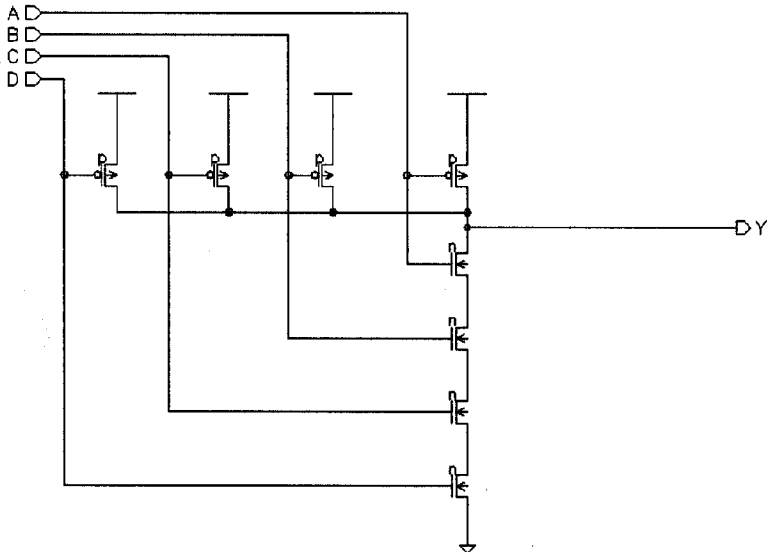
- ND4 : 2
- ND4D2 : 4
- ND4D5: 5
- ND4D7: 6



Symbol

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Truth Table



Schematic

**ND4 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{q}$  and  $t_{f} = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.32	$0.22 + 0.052*SL$	$0.25 + 0.043*SL$	$0.25 + 0.042*SL$
	tPHL	0.32	$0.20 + 0.060*SL$	$0.22 + 0.054*SL$	$0.21 + 0.054*SL$
	tR	0.56	$0.39 + 0.085*SL$	$0.36 + 0.095*SL$	$0.25 + 0.101*SL$
	tF	0.73	$0.50 + 0.113*SL$	$0.47 + 0.123*SL$	$0.36 + 0.129*SL$
B to Y	tPLH	0.38	$0.28 + 0.048*SL$	$0.30 + 0.042*SL$	$0.30 + 0.042*SL$
	tPHL	0.32	$0.20 + 0.058*SL$	$0.22 + 0.054*SL$	$0.21 + 0.054*SL$
	tR	0.64	$0.47 + 0.083*SL$	$0.44 + 0.095*SL$	$0.32 + 0.101*SL$
	tF	0.72	$0.50 + 0.110*SL$	$0.46 + 0.124*SL$	$0.36 + 0.129*SL$
C to Y	tPLH	0.42	$0.33 + 0.045*SL$	$0.34 + 0.042*SL$	$0.34 + 0.042*SL$
	tPHL	0.31	$0.19 + 0.057*SL$	$0.20 + 0.054*SL$	$0.19 + 0.054*SL$
	tR	0.73	$0.56 + 0.082*SL$	$0.53 + 0.094*SL$	$0.40 + 0.101*SL$
	tF	0.70	$0.48 + 0.112*SL$	$0.44 + 0.125*SL$	$0.36 + 0.129*SL$
D to Y	tPLH	0.45	$0.37 + 0.045*SL$	$0.37 + 0.042*SL$	$0.37 + 0.042*SL$
	tPHL	0.29	$0.18 + 0.056*SL$	$0.18 + 0.054*SL$	$0.18 + 0.054*SL$
	tR	0.81	$0.65 + 0.082*SL$	$0.61 + 0.094*SL$	$0.48 + 0.100*SL$
	tF	0.68	$0.45 + 0.114*SL$	$0.41 + 0.126*SL$	$0.35 + 0.129*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**ND4D2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{q}$  and  $t_{f} = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.26	$0.21 + 0.028*SL$	$0.23 + 0.022*SL$	$0.26 + 0.020*SL$
	tPHL	0.25	$0.19 + 0.031*SL$	$0.20 + 0.027*SL$	$0.22 + 0.026*SL$
	tR	0.46	$0.38 + 0.039*SL$	$0.37 + 0.042*SL$	$0.30 + 0.046*SL$
	tF	0.60	$0.49 + 0.055*SL$	$0.48 + 0.057*SL$	$0.42 + 0.060*SL$
B to Y	tPLH	0.33	$0.28 + 0.025*SL$	$0.29 + 0.021*SL$	$0.30 + 0.020*SL$
	tPHL	0.26	$0.20 + 0.029*SL$	$0.21 + 0.026*SL$	$0.21 + 0.026*SL$
	tR	0.54	$0.47 + 0.039*SL$	$0.45 + 0.043*SL$	$0.38 + 0.046*SL$
	tF	0.60	$0.49 + 0.051*SL$	$0.48 + 0.057*SL$	$0.40 + 0.061*SL$
C to Y	tPLH	0.37	$0.32 + 0.023*SL$	$0.33 + 0.021*SL$	$0.34 + 0.020*SL$
	tPHL	0.25	$0.19 + 0.029*SL$	$0.20 + 0.026*SL$	$0.20 + 0.026*SL$
	tR	0.63	$0.56 + 0.038*SL$	$0.54 + 0.042*SL$	$0.47 + 0.046*SL$
	tF	0.57	$0.47 + 0.051*SL$	$0.45 + 0.058*SL$	$0.38 + 0.061*SL$
D to Y	tPLH	0.40	$0.36 + 0.022*SL$	$0.36 + 0.021*SL$	$0.37 + 0.020*SL$
	tPHL	0.23	$0.17 + 0.028*SL$	$0.18 + 0.026*SL$	$0.18 + 0.026*SL$
	tR	0.71	$0.64 + 0.036*SL$	$0.62 + 0.041*SL$	$0.55 + 0.045*SL$
	tF	0.55	$0.44 + 0.052*SL$	$0.42 + 0.059*SL$	$0.37 + 0.061*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# ND4D5/ND4D7

4 Input NAND with 5X Drive or 7X Drive

## ND4D5 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.53	$0.51 + 0.009*SL$	$0.52 + 0.009*SL$	$0.52 + 0.008*SL$
	tPHL	0.64	$0.62 + 0.009*SL$	$0.63 + 0.006*SL$	$0.66 + 0.005*SL$
	tR	0.17	$0.14 + 0.018*SL$	$0.13 + 0.020*SL$	$0.12 + 0.020*SL$
	tF	0.21	$0.19 + 0.008*SL$	$0.19 + 0.007*SL$	$0.19 + 0.007*SL$
B to Y	tPLH	0.60	$0.58 + 0.009*SL$	$0.58 + 0.009*SL$	$0.58 + 0.008*SL$
	tPHL	0.66	$0.64 + 0.008*SL$	$0.65 + 0.007*SL$	$0.68 + 0.005*SL$
	tR	0.18	$0.14 + 0.020*SL$	$0.14 + 0.019*SL$	$0.12 + 0.020*SL$
	tF	0.21	$0.19 + 0.010*SL$	$0.20 + 0.007*SL$	$0.19 + 0.008*SL$
C to Y	tPLH	0.65	$0.63 + 0.009*SL$	$0.63 + 0.009*SL$	$0.64 + 0.008*SL$
	tPHL	0.65	$0.63 + 0.008*SL$	$0.64 + 0.006*SL$	$0.67 + 0.005*SL$
	tR	0.18	$0.14 + 0.019*SL$	$0.14 + 0.019*SL$	$0.12 + 0.020*SL$
	tF	0.21	$0.19 + 0.008*SL$	$0.20 + 0.007*SL$	$0.19 + 0.008*SL$
D to Y	tPLH	0.69	$0.67 + 0.009*SL$	$0.67 + 0.009*SL$	$0.67 + 0.008*SL$
	tPHL	0.63	$0.62 + 0.008*SL$	$0.62 + 0.006*SL$	$0.65 + 0.005*SL$
	tR	0.18	$0.15 + 0.017*SL$	$0.14 + 0.019*SL$	$0.12 + 0.020*SL$
	tF	0.21	$0.20 + 0.005*SL$	$0.19 + 0.007*SL$	$0.19 + 0.008*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

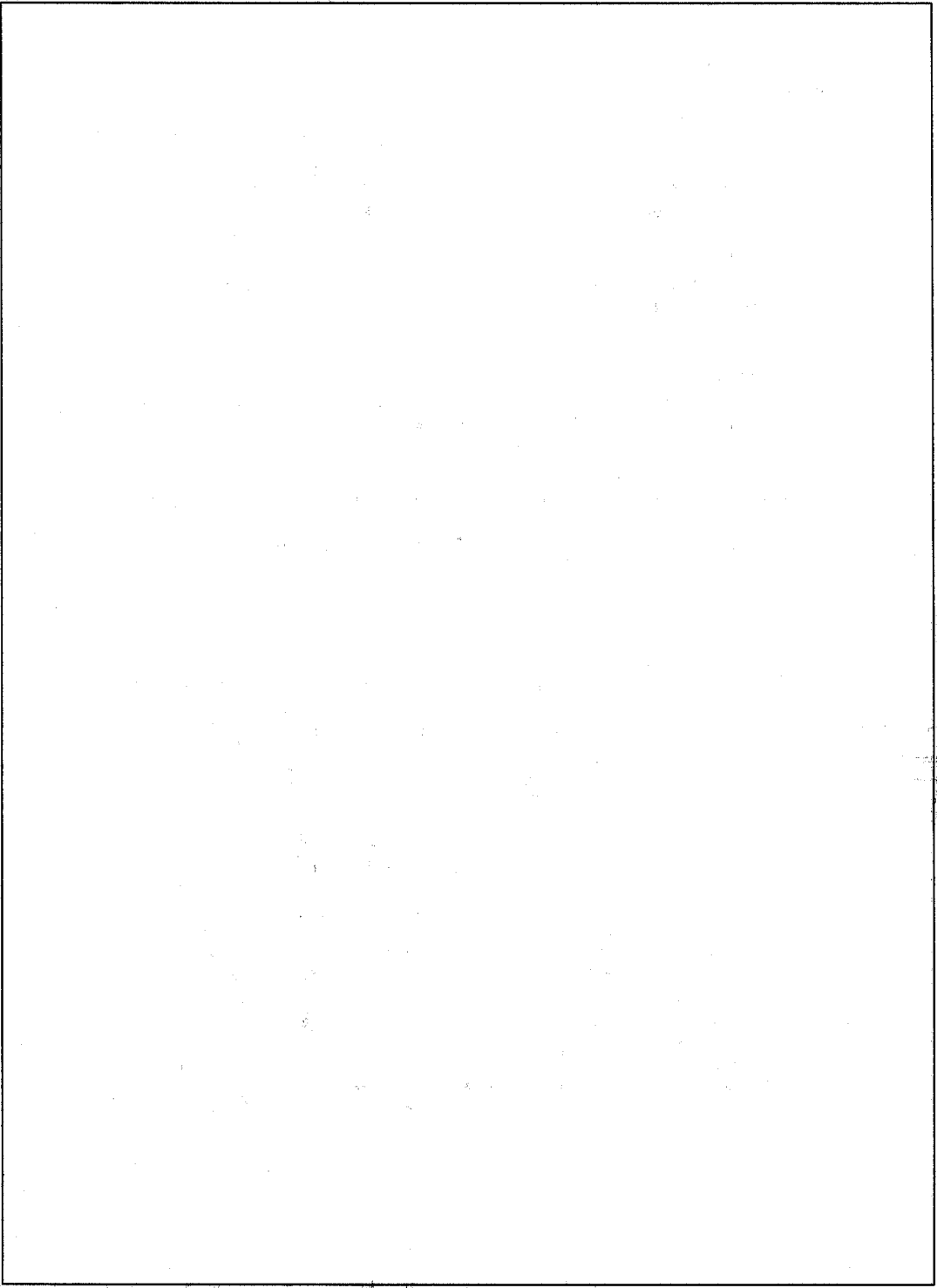
## ND4D7 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.58	$0.57 + 0.007*SL$	$0.57 + 0.006*SL$	$0.58 + 0.006*SL$
	tPHL	0.71	$0.70 + 0.007*SL$	$0.70 + 0.005*SL$	$0.73 + 0.004*SL$
	tR	0.18	$0.16 + 0.011*SL$	$0.15 + 0.014*SL$	$0.14 + 0.014*SL$
	tF	0.24	$0.23 + 0.006*SL$	$0.23 + 0.006*SL$	$0.24 + 0.005*SL$
B to Y	tPLH	0.65	$0.63 + 0.007*SL$	$0.63 + 0.006*SL$	$0.64 + 0.006*SL$
	tPHL	0.73	$0.71 + 0.006*SL$	$0.72 + 0.005*SL$	$0.74 + 0.004*SL$
	tR	0.18	$0.16 + 0.012*SL$	$0.15 + 0.014*SL$	$0.14 + 0.014*SL$
	tF	0.25	$0.24 + 0.002*SL$	$0.23 + 0.006*SL$	$0.24 + 0.005*SL$
C to Y	tPLH	0.70	$0.69 + 0.007*SL$	$0.69 + 0.006*SL$	$0.69 + 0.006*SL$
	tPHL	0.72	$0.70 + 0.007*SL$	$0.71 + 0.005*SL$	$0.73 + 0.004*SL$
	tR	0.18	$0.16 + 0.011*SL$	$0.16 + 0.014*SL$	$0.14 + 0.014*SL$
	tF	0.25	$0.25 + 0.001*SL$	$0.23 + 0.006*SL$	$0.24 + 0.005*SL$
D to Y	tPLH	0.74	$0.73 + 0.007*SL$	$0.73 + 0.006*SL$	$0.74 + 0.006*SL$
	tPHL	0.70	$0.69 + 0.007*SL$	$0.69 + 0.005*SL$	$0.71 + 0.004*SL$
	tR	0.19	$0.16 + 0.012*SL$	$0.16 + 0.013*SL$	$0.14 + 0.014*SL$
	tF	0.25	$0.24 + 0.003*SL$	$0.23 + 0.006*SL$	$0.24 + 0.005*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# ND5/ND5D2/ND5D4/ND5D6

5 Input NAND with 1X Drive, 2X Drive, 4X Drive or 6X Drive

Inputs: A, B, C, D, E

Output: Y

Input Loading (SL):

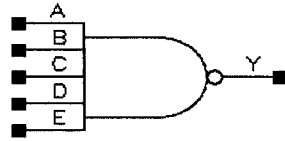
- ND5: All : 1
- ND5D2: All: 2
- ND5D4: All: 1
- ND5D6: All: 1

Maximum Fanout (Rec. SL):

- ND5: 12
- ND5D2: 24
- ND5D4: 112
- ND5D6: 168

Gate Count:

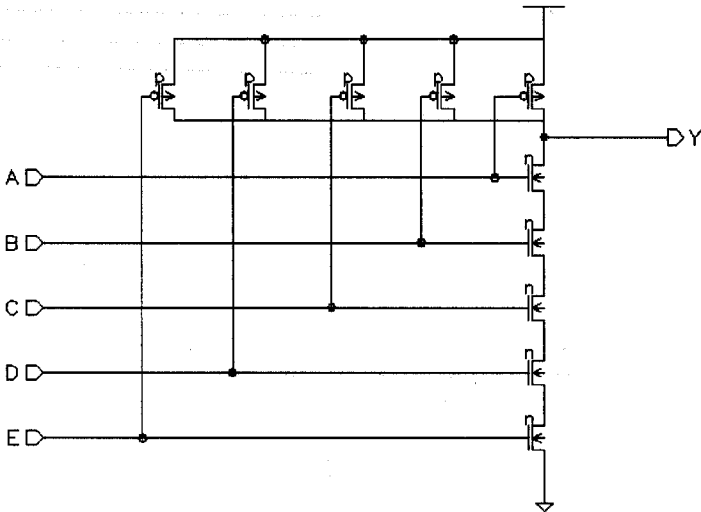
- ND5: 3
- ND5D2: 5
- ND5D4: 5
- ND5D6: 6



**Symbol**

A	B	C	D	E	Y
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

**Truth Table**



**Schematic**

**ND5 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.33	$0.23 + 0.052*SL$	$0.26 + 0.043*SL$	$0.27 + 0.042*SL$
	tPHL	0.38	$0.25 + 0.066*SL$	$0.25 + 0.065*SL$	$0.24 + 0.065*SL$
	tR	0.59	$0.41 + 0.087*SL$	$0.39 + 0.096*SL$	$0.28 + 0.101*SL$
	tF	0.92	$0.64 + 0.142*SL$	$0.60 + 0.153*SL$	$0.50 + 0.158*SL$
B to Y	tPLH	0.39	$0.29 + 0.048*SL$	$0.31 + 0.042*SL$	$0.31 + 0.042*SL$
	tPHL	0.40	$0.27 + 0.066*SL$	$0.27 + 0.065*SL$	$0.26 + 0.065*SL$
	tR	0.67	$0.50 + 0.085*SL$	$0.46 + 0.095*SL$	$0.35 + 0.101*SL$
	tF	0.92	$0.64 + 0.140*SL$	$0.60 + 0.153*SL$	$0.51 + 0.158*SL$
C to Y	tPLH	0.43	$0.34 + 0.046*SL$	$0.35 + 0.042*SL$	$0.35 + 0.042*SL$
	tPHL	0.41	$0.27 + 0.066*SL$	$0.28 + 0.065*SL$	$0.27 + 0.066*SL$
	tR	0.75	$0.59 + 0.084*SL$	$0.55 + 0.095*SL$	$0.43 + 0.101*SL$
	tF	0.91	$0.63 + 0.141*SL$	$0.59 + 0.154*SL$	$0.51 + 0.158*SL$
D to Y	tPLH	0.46	$0.37 + 0.046*SL$	$0.38 + 0.043*SL$	$0.38 + 0.043*SL$
	tPHL	0.41	$0.28 + 0.066*SL$	$0.28 + 0.065*SL$	$0.27 + 0.066*SL$
	tR	0.84	$0.67 + 0.084*SL$	$0.64 + 0.094*SL$	$0.52 + 0.101*SL$
	tF	0.89	$0.60 + 0.144*SL$	$0.57 + 0.155*SL$	$0.51 + 0.158*SL$
E to Y	tPLH	0.48	$0.39 + 0.047*SL$	$0.40 + 0.043*SL$	$0.41 + 0.043*SL$
	tPHL	0.40	$0.27 + 0.066*SL$	$0.27 + 0.065*SL$	$0.26 + 0.066*SL$
	tR	0.93	$0.76 + 0.084*SL$	$0.73 + 0.094*SL$	$0.61 + 0.100*SL$
	tF	0.88	$0.58 + 0.146*SL$	$0.56 + 0.155*SL$	$0.51 + 0.158*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**ND5D2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.27	$0.22 + 0.027*SL$	$0.24 + 0.022*SL$	$0.27 + 0.020*SL$
	tPHL	0.31	$0.24 + 0.033*SL$	$0.25 + 0.031*SL$	$0.25 + 0.032*SL$
	tR	0.49	$0.41 + 0.040*SL$	$0.40 + 0.043*SL$	$0.33 + 0.046*SL$
	tF	0.76	$0.62 + 0.068*SL$	$0.61 + 0.072*SL$	$0.54 + 0.075*SL$
B to Y	tPLH	0.33	$0.28 + 0.025*SL$	$0.29 + 0.021*SL$	$0.31 + 0.020*SL$
	tPHL	0.33	$0.26 + 0.033*SL$	$0.26 + 0.032*SL$	$0.26 + 0.032*SL$
	tR	0.57	$0.49 + 0.040*SL$	$0.48 + 0.043*SL$	$0.41 + 0.047*SL$
	tF	0.76	$0.63 + 0.065*SL$	$0.61 + 0.072*SL$	$0.54 + 0.075*SL$
C to Y	tPLH	0.38	$0.33 + 0.024*SL$	$0.34 + 0.021*SL$	$0.35 + 0.020*SL$
	tPHL	0.33	$0.27 + 0.034*SL$	$0.27 + 0.032*SL$	$0.27 + 0.032*SL$
	tR	0.65	$0.58 + 0.038*SL$	$0.56 + 0.043*SL$	$0.49 + 0.046*SL$
	tF	0.75	$0.62 + 0.065*SL$	$0.60 + 0.072*SL$	$0.54 + 0.075*SL$
D to Y	tPLH	0.41	$0.36 + 0.023*SL$	$0.37 + 0.021*SL$	$0.38 + 0.021*SL$
	tPHL	0.34	$0.27 + 0.033*SL$	$0.28 + 0.032*SL$	$0.28 + 0.032*SL$
	tR	0.74	$0.66 + 0.038*SL$	$0.65 + 0.043*SL$	$0.58 + 0.046*SL$
	tF	0.73	$0.59 + 0.067*SL$	$0.58 + 0.073*SL$	$0.52 + 0.076*SL$
E to Y	tPLH	0.43	$0.38 + 0.023*SL$	$0.38 + 0.021*SL$	$0.40 + 0.021*SL$
	tPHL	0.33	$0.26 + 0.033*SL$	$0.27 + 0.032*SL$	$0.27 + 0.032*SL$
	tR	0.81	$0.74 + 0.038*SL$	$0.72 + 0.042*SL$	$0.66 + 0.045*SL$
	tF	0.71	$0.57 + 0.069*SL$	$0.56 + 0.074*SL$	$0.52 + 0.076*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# ND5D4

## 5 Input NAND with 4X Drive

### ND5D4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.52	$0.49 + 0.012*SL$	$0.50 + 0.011*SL$	$0.50 + 0.011*SL$
	tPHL	0.70	$0.68 + 0.010*SL$	$0.69 + 0.007*SL$	$0.72 + 0.006*SL$
	tR	0.17	$0.12 + 0.024*SL$	$0.12 + 0.025*SL$	$0.10 + 0.026*SL$
	tF	0.19	$0.17 + 0.009*SL$	$0.18 + 0.009*SL$	$0.17 + 0.010*SL$
B to Y	tPLH	0.58	$0.56 + 0.011*SL$	$0.56 + 0.011*SL$	$0.56 + 0.011*SL$
	tPHL	0.74	$0.72 + 0.010*SL$	$0.72 + 0.007*SL$	$0.76 + 0.006*SL$
	tR	0.17	$0.13 + 0.023*SL$	$0.12 + 0.025*SL$	$0.11 + 0.026*SL$
	tF	0.19	$0.18 + 0.008*SL$	$0.18 + 0.009*SL$	$0.17 + 0.010*SL$
C to Y	tPLH	0.62	$0.60 + 0.012*SL$	$0.60 + 0.011*SL$	$0.61 + 0.011*SL$
	tPHL	0.75	$0.72 + 0.011*SL$	$0.73 + 0.007*SL$	$0.76 + 0.006*SL$
	tR	0.18	$0.13 + 0.022*SL$	$0.13 + 0.025*SL$	$0.11 + 0.026*SL$
	tF	0.19	$0.18 + 0.009*SL$	$0.18 + 0.009*SL$	$0.17 + 0.009*SL$
D to Y	tPLH	0.66	$0.64 + 0.012*SL$	$0.64 + 0.011*SL$	$0.64 + 0.011*SL$
	tPHL	0.75	$0.73 + 0.010*SL$	$0.74 + 0.007*SL$	$0.77 + 0.006*SL$
	tR	0.18	$0.13 + 0.023*SL$	$0.13 + 0.025*SL$	$0.11 + 0.026*SL$
	tF	0.20	$0.18 + 0.009*SL$	$0.18 + 0.009*SL$	$0.17 + 0.010*SL$
E to Y	tPLH	0.68	$0.66 + 0.012*SL$	$0.66 + 0.011*SL$	$0.66 + 0.011*SL$
	tPHL	0.74	$0.71 + 0.011*SL$	$0.72 + 0.007*SL$	$0.76 + 0.006*SL$
	tR	0.18	$0.14 + 0.021*SL$	$0.13 + 0.025*SL$	$0.11 + 0.026*SL$
	tF	0.19	$0.17 + 0.010*SL$	$0.18 + 0.009*SL$	$0.17 + 0.010*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**ND5D6 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.57	$0.56 + 0.008*SL$	$0.56 + 0.007*SL$	$0.56 + 0.007*SL$
	tPHL	0.78	$0.77 + 0.007*SL$	$0.77 + 0.006*SL$	$0.80 + 0.005*SL$
	tR	0.18	$0.15 + 0.014*SL$	$0.14 + 0.016*SL$	$0.13 + 0.017*SL$
	tF	0.24	$0.23 + 0.004*SL$	$0.22 + 0.006*SL$	$0.22 + 0.006*SL$
B to Y	tPLH	0.63	$0.62 + 0.008*SL$	$0.62 + 0.007*SL$	$0.63 + 0.007*SL$
	tPHL	0.81	$0.80 + 0.007*SL$	$0.80 + 0.006*SL$	$0.83 + 0.005*SL$
	tR	0.18	$0.15 + 0.015*SL$	$0.15 + 0.016*SL$	$0.13 + 0.017*SL$
	tF	0.24	$0.23 + 0.004*SL$	$0.22 + 0.006*SL$	$0.22 + 0.006*SL$
C to Y	tPLH	0.68	$0.67 + 0.008*SL$	$0.67 + 0.007*SL$	$0.68 + 0.007*SL$
	tPHL	0.82	$0.81 + 0.008*SL$	$0.81 + 0.006*SL$	$0.84 + 0.005*SL$
	tR	0.18	$0.15 + 0.014*SL$	$0.15 + 0.016*SL$	$0.13 + 0.017*SL$
	tF	0.24	$0.22 + 0.005*SL$	$0.22 + 0.006*SL$	$0.23 + 0.006*SL$
D to Y	tPLH	0.72	$0.70 + 0.008*SL$	$0.71 + 0.007*SL$	$0.71 + 0.007*SL$
	tPHL	0.83	$0.81 + 0.008*SL$	$0.82 + 0.006*SL$	$0.85 + 0.005*SL$
	tR	0.18	$0.15 + 0.015*SL$	$0.15 + 0.016*SL$	$0.13 + 0.017*SL$
	tF	0.24	$0.23 + 0.005*SL$	$0.22 + 0.006*SL$	$0.22 + 0.006*SL$
E to Y	tPLH	0.74	$0.73 + 0.008*SL$	$0.73 + 0.007*SL$	$0.74 + 0.007*SL$
	tPHL	0.82	$0.80 + 0.008*SL$	$0.81 + 0.006*SL$	$0.83 + 0.005*SL$
	tR	0.19	$0.15 + 0.016*SL$	$0.15 + 0.016*SL$	$0.14 + 0.017*SL$
	tF	0.24	$0.23 + 0.004*SL$	$0.22 + 0.006*SL$	$0.22 + 0.006*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# ND6/ND6D2/ND6D4/ND6D8

6 Input NAND with 2X Drive, 4X Drive or 8X Drive

Inputs: A, B, C, D, E, F

Output: Y

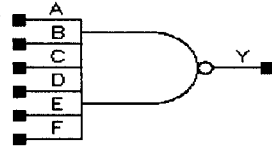
Input Loading (SL): All : 1

Maximum Fanout (Rec. SL):

- ND6: 28
- ND6D2: 56
- ND6D4: 112
- ND6D8: 224

Gate Count:

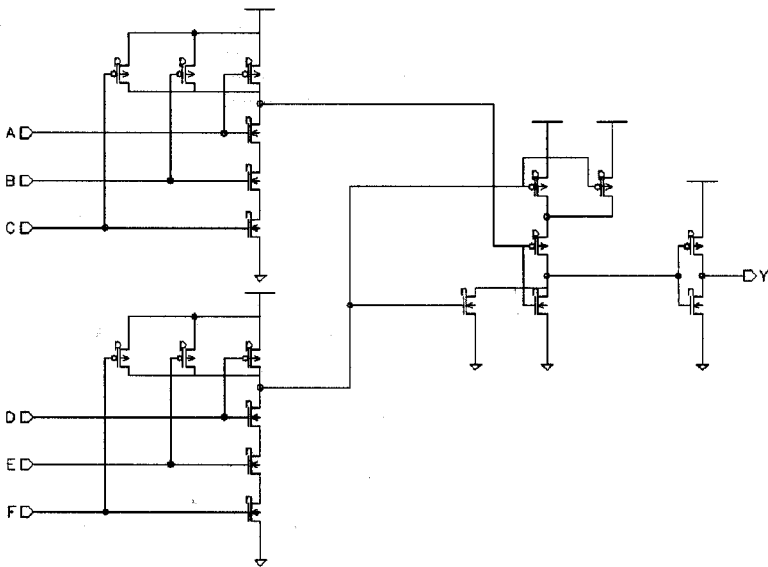
- ND6: 5
- ND6D2: 5
- ND6D4: 6
- ND6D8: 9



**Symbol**

A	B	C	D	E	F	Y
0	x	x	x	x	x	1
x	0	x	x	x	x	1
x	x	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
1	1	1	1	1	1	0

**Truth Table**



**Schematic**

**ND6 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.47	$0.39 + 0.041 \cdot SL$	$0.39 + 0.040 \cdot SL$	$0.39 + 0.040 \cdot SL$
	tPHL	0.49	$0.44 + 0.028 \cdot SL$	$0.46 + 0.021 \cdot SL$	$0.48 + 0.020 \cdot SL$
	tR	0.28	$0.10 + 0.089 \cdot SL$	$0.09 + 0.092 \cdot SL$	$0.08 + 0.092 \cdot SL$
	tF	0.18	$0.11 + 0.034 \cdot SL$	$0.11 + 0.037 \cdot SL$	$0.08 + 0.038 \cdot SL$
B to Y	tPLH	0.53	$0.45 + 0.040 \cdot SL$	$0.45 + 0.040 \cdot SL$	$0.45 + 0.040 \cdot SL$
	tPHL	0.49	$0.43 + 0.028 \cdot SL$	$0.45 + 0.021 \cdot SL$	$0.48 + 0.020 \cdot SL$
	tR	0.28	$0.10 + 0.089 \cdot SL$	$0.09 + 0.092 \cdot SL$	$0.08 + 0.092 \cdot SL$
	tF	0.18	$0.11 + 0.035 \cdot SL$	$0.11 + 0.037 \cdot SL$	$0.08 + 0.038 \cdot SL$
C to Y	tPLH	0.58	$0.50 + 0.040 \cdot SL$	$0.51 + 0.040 \cdot SL$	$0.51 + 0.040 \cdot SL$
	tPHL	0.45	$0.40 + 0.028 \cdot SL$	$0.42 + 0.021 \cdot SL$	$0.45 + 0.020 \cdot SL$
	tR	0.28	$0.10 + 0.088 \cdot SL$	$0.09 + 0.092 \cdot SL$	$0.08 + 0.092 \cdot SL$
	tF	0.18	$0.11 + 0.037 \cdot SL$	$0.11 + 0.037 \cdot SL$	$0.08 + 0.038 \cdot SL$
D to Y	tPLH	0.54	$0.46 + 0.041 \cdot SL$	$0.47 + 0.040 \cdot SL$	$0.46 + 0.040 \cdot SL$
	tPHL	0.51	$0.45 + 0.028 \cdot SL$	$0.47 + 0.021 \cdot SL$	$0.50 + 0.020 \cdot SL$
	tR	0.28	$0.11 + 0.089 \cdot SL$	$0.10 + 0.092 \cdot SL$	$0.08 + 0.092 \cdot SL$
	tF	0.18	$0.11 + 0.036 \cdot SL$	$0.11 + 0.037 \cdot SL$	$0.08 + 0.038 \cdot SL$
E to Y	tPLH	0.61	$0.53 + 0.040 \cdot SL$	$0.53 + 0.040 \cdot SL$	$0.53 + 0.040 \cdot SL$
	tPHL	0.50	$0.44 + 0.028 \cdot SL$	$0.46 + 0.021 \cdot SL$	$0.49 + 0.020 \cdot SL$
	tR	0.29	$0.11 + 0.086 \cdot SL$	$0.10 + 0.092 \cdot SL$	$0.08 + 0.092 \cdot SL$
	tF	0.18	$0.11 + 0.036 \cdot SL$	$0.11 + 0.037 \cdot SL$	$0.08 + 0.038 \cdot SL$
F to Y	tPLH	0.66	$0.58 + 0.040 \cdot SL$	$0.58 + 0.040 \cdot SL$	$0.58 + 0.040 \cdot SL$
	tPHL	0.46	$0.41 + 0.028 \cdot SL$	$0.43 + 0.021 \cdot SL$	$0.46 + 0.020 \cdot SL$
	tR	0.29	$0.11 + 0.087 \cdot SL$	$0.10 + 0.092 \cdot SL$	$0.08 + 0.092 \cdot SL$
	tF	0.19	$0.12 + 0.032 \cdot SL$	$0.11 + 0.037 \cdot SL$	$0.08 + 0.038 \cdot SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**ND6D2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.47	$0.43 + 0.022 \cdot SL$	$0.44 + 0.020 \cdot SL$	$0.43 + 0.020 \cdot SL$
	tPHL	0.57	$0.53 + 0.020 \cdot SL$	$0.55 + 0.013 \cdot SL$	$0.60 + 0.011 \cdot SL$
	tR	0.19	$0.11 + 0.044 \cdot SL$	$0.10 + 0.047 \cdot SL$	$0.08 + 0.048 \cdot SL$
	tF	0.20	$0.16 + 0.021 \cdot SL$	$0.17 + 0.018 \cdot SL$	$0.17 + 0.018 \cdot SL$
B to Y	tPLH	0.54	$0.50 + 0.021 \cdot SL$	$0.50 + 0.020 \cdot SL$	$0.50 + 0.020 \cdot SL$
	tPHL	0.56	$0.53 + 0.020 \cdot SL$	$0.54 + 0.013 \cdot SL$	$0.59 + 0.011 \cdot SL$
	tR	0.20	$0.11 + 0.046 \cdot SL$	$0.10 + 0.047 \cdot SL$	$0.08 + 0.048 \cdot SL$
	tF	0.20	$0.16 + 0.021 \cdot SL$	$0.17 + 0.018 \cdot SL$	$0.17 + 0.018 \cdot SL$
C to Y	tPLH	0.59	$0.55 + 0.021 \cdot SL$	$0.55 + 0.020 \cdot SL$	$0.55 + 0.020 \cdot SL$
	tPHL	0.53	$0.49 + 0.020 \cdot SL$	$0.51 + 0.013 \cdot SL$	$0.56 + 0.011 \cdot SL$
	tR	0.20	$0.11 + 0.044 \cdot SL$	$0.10 + 0.047 \cdot SL$	$0.08 + 0.048 \cdot SL$
	tF	0.20	$0.17 + 0.020 \cdot SL$	$0.17 + 0.018 \cdot SL$	$0.17 + 0.018 \cdot SL$
D to Y	tPLH	0.49	$0.45 + 0.021 \cdot SL$	$0.45 + 0.020 \cdot SL$	$0.45 + 0.020 \cdot SL$
	tPHL	0.57	$0.53 + 0.020 \cdot SL$	$0.55 + 0.013 \cdot SL$	$0.60 + 0.011 \cdot SL$
	tR	0.20	$0.11 + 0.045 \cdot SL$	$0.11 + 0.047 \cdot SL$	$0.09 + 0.048 \cdot SL$
	tF	0.21	$0.17 + 0.019 \cdot SL$	$0.17 + 0.018 \cdot SL$	$0.17 + 0.018 \cdot SL$
E to Y	tPLH	0.56	$0.51 + 0.022 \cdot SL$	$0.52 + 0.020 \cdot SL$	$0.52 + 0.020 \cdot SL$
	tPHL	0.57	$0.53 + 0.020 \cdot SL$	$0.55 + 0.013 \cdot SL$	$0.60 + 0.011 \cdot SL$
	tR	0.20	$0.11 + 0.045 \cdot SL$	$0.11 + 0.047 \cdot SL$	$0.09 + 0.048 \cdot SL$
	tF	0.20	$0.16 + 0.020 \cdot SL$	$0.17 + 0.018 \cdot SL$	$0.17 + 0.018 \cdot SL$
F to Y	tPLH	0.61	$0.57 + 0.021 \cdot SL$	$0.57 + 0.020 \cdot SL$	$0.57 + 0.020 \cdot SL$
	tPHL	0.53	$0.50 + 0.020 \cdot SL$	$0.51 + 0.013 \cdot SL$	$0.56 + 0.011 \cdot SL$
	tR	0.20	$0.12 + 0.044 \cdot SL$	$0.11 + 0.047 \cdot SL$	$0.09 + 0.048 \cdot SL$
	tF	0.21	$0.17 + 0.018 \cdot SL$	$0.17 + 0.018 \cdot SL$	$0.17 + 0.018 \cdot SL$



# ND6D4

6 Input NAND with 4X Drive

## ND6D4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.52	$0.49 + 0.012 * SL$	$0.50 + 0.011 * SL$	$0.50 + 0.011 * SL$
	tPHL	0.69	$0.67 + 0.013 * SL$	$0.68 + 0.009 * SL$	$0.72 + 0.007 * SL$
	tR	0.18	$0.13 + 0.023 * SL$	$0.12 + 0.025 * SL$	$0.11 + 0.026 * SL$
	tF	0.27	$0.25 + 0.012 * SL$	$0.26 + 0.010 * SL$	$0.26 + 0.010 * SL$
B to Y	tPLH	0.58	$0.56 + 0.012 * SL$	$0.56 + 0.011 * SL$	$0.57 + 0.011 * SL$
	tPHL	0.69	$0.66 + 0.013 * SL$	$0.68 + 0.009 * SL$	$0.72 + 0.007 * SL$
	tR	0.18	$0.13 + 0.024 * SL$	$0.13 + 0.025 * SL$	$0.11 + 0.026 * SL$
	tF	0.28	$0.25 + 0.012 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$
C to Y	tPLH	0.63	$0.61 + 0.012 * SL$	$0.61 + 0.011 * SL$	$0.62 + 0.011 * SL$
	tPHL	0.66	$0.63 + 0.012 * SL$	$0.64 + 0.009 * SL$	$0.69 + 0.007 * SL$
	tR	0.18	$0.13 + 0.024 * SL$	$0.13 + 0.025 * SL$	$0.11 + 0.026 * SL$
	tF	0.28	$0.25 + 0.014 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$
D to Y	tPLH	0.53	$0.51 + 0.012 * SL$	$0.51 + 0.011 * SL$	$0.51 + 0.011 * SL$
	tPHL	0.69	$0.67 + 0.013 * SL$	$0.68 + 0.009 * SL$	$0.72 + 0.007 * SL$
	tR	0.18	$0.13 + 0.024 * SL$	$0.13 + 0.025 * SL$	$0.11 + 0.026 * SL$
	tF	0.27	$0.25 + 0.012 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$
E to Y	tPLH	0.60	$0.58 + 0.012 * SL$	$0.58 + 0.011 * SL$	$0.58 + 0.011 * SL$
	tPHL	0.69	$0.66 + 0.013 * SL$	$0.68 + 0.009 * SL$	$0.72 + 0.007 * SL$
	tR	0.18	$0.14 + 0.024 * SL$	$0.13 + 0.025 * SL$	$0.12 + 0.026 * SL$
	tF	0.28	$0.25 + 0.013 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$
F to Y	tPLH	0.65	$0.63 + 0.012 * SL$	$0.63 + 0.011 * SL$	$0.64 + 0.011 * SL$
	tPHL	0.66	$0.63 + 0.013 * SL$	$0.64 + 0.009 * SL$	$0.69 + 0.007 * SL$
	tR	0.19	$0.14 + 0.025 * SL$	$0.14 + 0.025 * SL$	$0.12 + 0.026 * SL$
	tF	0.28	$0.25 + 0.013 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**ND6D8 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.56	$0.55 + 0.006 * SL$	$0.55 + 0.006 * SL$	$0.55 + 0.005 * SL$
	tPHL	0.76	$0.75 + 0.007 * SL$	$0.75 + 0.005 * SL$	$0.78 + 0.004 * SL$
	tR	0.15	$0.13 + 0.011 * SL$	$0.13 + 0.012 * SL$	$0.12 + 0.013 * SL$
	tF	0.28	$0.27 + 0.005 * SL$	$0.27 + 0.006 * SL$	$0.28 + 0.005 * SL$
B to Y	tPLH	0.62	$0.61 + 0.006 * SL$	$0.61 + 0.006 * SL$	$0.61 + 0.005 * SL$
	tPHL	0.75	$0.74 + 0.007 * SL$	$0.75 + 0.005 * SL$	$0.77 + 0.004 * SL$
	tR	0.16	$0.14 + 0.011 * SL$	$0.13 + 0.012 * SL$	$0.12 + 0.013 * SL$
	tF	0.28	$0.27 + 0.006 * SL$	$0.27 + 0.006 * SL$	$0.28 + 0.005 * SL$
C to Y	tPLH	0.67	$0.65 + 0.006 * SL$	$0.66 + 0.006 * SL$	$0.66 + 0.005 * SL$
	tPHL	0.72	$0.71 + 0.007 * SL$	$0.71 + 0.005 * SL$	$0.73 + 0.004 * SL$
	tR	0.16	$0.14 + 0.012 * SL$	$0.14 + 0.012 * SL$	$0.13 + 0.013 * SL$
	tF	0.28	$0.27 + 0.006 * SL$	$0.27 + 0.006 * SL$	$0.28 + 0.005 * SL$
D to Y	tPLH	0.57	$0.56 + 0.007 * SL$	$0.56 + 0.006 * SL$	$0.57 + 0.005 * SL$
	tPHL	0.77	$0.75 + 0.007 * SL$	$0.76 + 0.005 * SL$	$0.78 + 0.004 * SL$
	tR	0.16	$0.14 + 0.010 * SL$	$0.14 + 0.012 * SL$	$0.13 + 0.013 * SL$
	tF	0.28	$0.27 + 0.005 * SL$	$0.27 + 0.005 * SL$	$0.28 + 0.005 * SL$
E to Y	tPLH	0.64	$0.62 + 0.007 * SL$	$0.63 + 0.006 * SL$	$0.63 + 0.005 * SL$
	tPHL	0.76	$0.74 + 0.007 * SL$	$0.75 + 0.005 * SL$	$0.77 + 0.004 * SL$
	tR	0.17	$0.15 + 0.010 * SL$	$0.14 + 0.012 * SL$	$0.13 + 0.013 * SL$
	tF	0.28	$0.27 + 0.005 * SL$	$0.27 + 0.006 * SL$	$0.28 + 0.005 * SL$
F to Y	tPLH	0.69	$0.67 + 0.006 * SL$	$0.68 + 0.006 * SL$	$0.68 + 0.005 * SL$
	tPHL	0.72	$0.71 + 0.007 * SL$	$0.71 + 0.005 * SL$	$0.74 + 0.004 * SL$
	tR	0.17	$0.14 + 0.013 * SL$	$0.15 + 0.012 * SL$	$0.14 + 0.012 * SL$
	tF	0.28	$0.27 + 0.005 * SL$	$0.27 + 0.005 * SL$	$0.28 + 0.005 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# ND8/ND8D2/ND8D4/ND8D8

8 Input NAND with 1X Drive, 2X Drive, 4X Drive or 8X Drive

Inputs: A, B, C, D, E, F, G, H

Output: Y

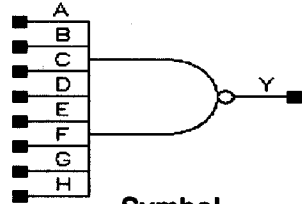
Input Loading (SL): All : 1

Maximum Fanout (Rec. SL):

- ND8: 28
- ND8D2: 56
- ND8D4: 112
- ND8D8: 224

Gate Count:

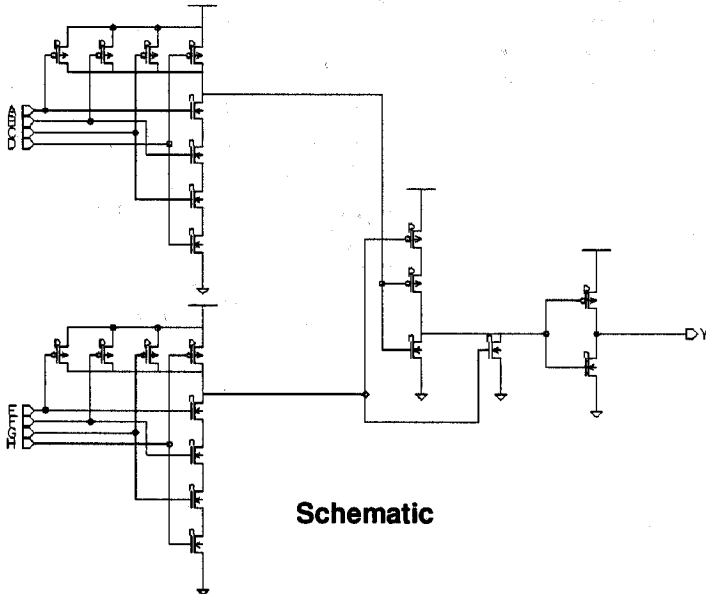
- ND8: 6
- ND8D2: 6
- ND8D4: 7
- ND8D8: 10



**Symbol**

A	B	C	D	E	F	G	H	Y
0	x	x	x	x	x	x	x	1
x	0	x	x	x	x	x	x	1
x	x	0	x	x	x	x	x	1
x	x	x	0	x	x	x	x	1
x	x	x	x	0	x	x	x	1
x	x	x	x	x	0	x	x	1
x	x	x	x	x	x	0	x	1
x	x	x	x	x	x	x	0	1
1	1	1	1	1	1	1	1	0

**Truth Table**



**Schematic**

**ND8 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.50	$0.42 + 0.040*SL$	$0.42 + 0.040*SL$	$0.42 + 0.040*SL$
	tPHL	0.64	$0.59 + 0.028*SL$	$0.61 + 0.022*SL$	$0.64 + 0.020*SL$
	tR	0.33	$0.15 + 0.090*SL$	$0.15 + 0.092*SL$	$0.14 + 0.093*SL$
	tF	0.23	$0.15 + 0.037*SL$	$0.15 + 0.037*SL$	$0.13 + 0.038*SL$
B to Y	tPLH	0.56	$0.48 + 0.040*SL$	$0.48 + 0.040*SL$	$0.48 + 0.040*SL$
	tPHL	0.66	$0.60 + 0.029*SL$	$0.62 + 0.022*SL$	$0.66 + 0.020*SL$
	tR	0.33	$0.15 + 0.090*SL$	$0.15 + 0.092*SL$	$0.14 + 0.093*SL$
	tF	0.23	$0.15 + 0.037*SL$	$0.15 + 0.037*SL$	$0.13 + 0.038*SL$
C to Y	tPLH	0.60	$0.52 + 0.040*SL$	$0.52 + 0.040*SL$	$0.52 + 0.040*SL$
	tPHL	0.65	$0.59 + 0.029*SL$	$0.62 + 0.022*SL$	$0.65 + 0.020*SL$
	tR	0.34	$0.16 + 0.089*SL$	$0.15 + 0.092*SL$	$0.14 + 0.093*SL$
	tF	0.23	$0.15 + 0.037*SL$	$0.15 + 0.037*SL$	$0.13 + 0.038*SL$
D to Y	tPLH	0.63	$0.55 + 0.040*SL$	$0.55 + 0.040*SL$	$0.55 + 0.040*SL$
	tPHL	0.64	$0.58 + 0.029*SL$	$0.60 + 0.022*SL$	$0.64 + 0.020*SL$
	tR	0.34	$0.16 + 0.089*SL$	$0.15 + 0.092*SL$	$0.14 + 0.093*SL$
	tF	0.23	$0.15 + 0.037*SL$	$0.15 + 0.037*SL$	$0.13 + 0.038*SL$
E to Y	tPLH	0.53	$0.45 + 0.040*SL$	$0.45 + 0.040*SL$	$0.45 + 0.040*SL$
	tPHL	0.65	$0.60 + 0.028*SL$	$0.62 + 0.022*SL$	$0.65 + 0.020*SL$
	tR	0.34	$0.16 + 0.090*SL$	$0.15 + 0.092*SL$	$0.14 + 0.093*SL$
	tF	0.23	$0.16 + 0.036*SL$	$0.15 + 0.037*SL$	$0.13 + 0.038*SL$
F to Y	tPLH	0.59	$0.51 + 0.040*SL$	$0.51 + 0.040*SL$	$0.51 + 0.040*SL$
	tPHL	0.67	$0.61 + 0.029*SL$	$0.63 + 0.022*SL$	$0.67 + 0.020*SL$
	tR	0.34	$0.16 + 0.091*SL$	$0.15 + 0.092*SL$	$0.14 + 0.093*SL$
	tF	0.23	$0.15 + 0.037*SL$	$0.16 + 0.037*SL$	$0.13 + 0.038*SL$
G to Y	tPLH	0.63	$0.55 + 0.039*SL$	$0.55 + 0.040*SL$	$0.55 + 0.040*SL$
	tPHL	0.66	$0.60 + 0.029*SL$	$0.62 + 0.022*SL$	$0.66 + 0.020*SL$
	tR	0.34	$0.16 + 0.089*SL$	$0.15 + 0.092*SL$	$0.14 + 0.093*SL$
	tF	0.23	$0.15 + 0.037*SL$	$0.15 + 0.037*SL$	$0.13 + 0.038*SL$
H to Y	tPLH	0.67	$0.59 + 0.040*SL$	$0.59 + 0.040*SL$	$0.59 + 0.040*SL$
	tPHL	0.64	$0.58 + 0.029*SL$	$0.60 + 0.022*SL$	$0.64 + 0.020*SL$
	tR	0.34	$0.16 + 0.089*SL$	$0.15 + 0.092*SL$	$0.14 + 0.093*SL$
	tF	0.23	$0.16 + 0.037*SL$	$0.16 + 0.037*SL$	$0.13 + 0.038*SL$

\*Range1: SL < 3.00, \*Range2:  $3.00 \leq SL \leq 20.00$ , \*Range3:  $20.00 < SL$

# ND8D2

## 8 Input NAND with 2X Drive

### ND8D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{q}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.47	$0.43 + 0.021*SL$	$0.43 + 0.020*SL$	$0.43 + 0.020*SL$
	tPHL	0.66	$0.62 + 0.019*SL$	$0.64 + 0.013*SL$	$0.69 + 0.011*SL$
	tR	0.19	$0.11 + 0.043*SL$	$0.09 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.20	$0.16 + 0.019*SL$	$0.17 + 0.018*SL$	$0.17 + 0.018*SL$
B to Y	tPLH	0.53	$0.49 + 0.021*SL$	$0.49 + 0.020*SL$	$0.49 + 0.020*SL$
	tPHL	0.67	$0.64 + 0.020*SL$	$0.65 + 0.013*SL$	$0.70 + 0.011*SL$
	tR	0.19	$0.10 + 0.045*SL$	$0.10 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.20	$0.16 + 0.020*SL$	$0.17 + 0.018*SL$	$0.16 + 0.018*SL$
C to Y	tPLH	0.57	$0.53 + 0.021*SL$	$0.54 + 0.020*SL$	$0.53 + 0.020*SL$
	tPHL	0.67	$0.63 + 0.020*SL$	$0.65 + 0.013*SL$	$0.69 + 0.011*SL$
	tR	0.19	$0.11 + 0.044*SL$	$0.10 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.20	$0.16 + 0.021*SL$	$0.17 + 0.018*SL$	$0.17 + 0.018*SL$
D to Y	tPLH	0.61	$0.57 + 0.021*SL$	$0.57 + 0.020*SL$	$0.57 + 0.020*SL$
	tPHL	0.65	$0.61 + 0.019*SL$	$0.63 + 0.013*SL$	$0.68 + 0.011*SL$
	tR	0.20	$0.11 + 0.044*SL$	$0.11 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.21	$0.17 + 0.019*SL$	$0.17 + 0.018*SL$	$0.16 + 0.018*SL$
E to Y	tPLH	0.50	$0.46 + 0.021*SL$	$0.46 + 0.020*SL$	$0.46 + 0.020*SL$
	tPHL	0.66	$0.62 + 0.020*SL$	$0.64 + 0.013*SL$	$0.69 + 0.011*SL$
	tR	0.20	$0.11 + 0.043*SL$	$0.10 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.20	$0.16 + 0.020*SL$	$0.17 + 0.018*SL$	$0.17 + 0.018*SL$
F to Y	tPLH	0.56	$0.52 + 0.021*SL$	$0.52 + 0.020*SL$	$0.52 + 0.020*SL$
	tPHL	0.67	$0.64 + 0.020*SL$	$0.65 + 0.013*SL$	$0.70 + 0.011*SL$
	tR	0.20	$0.11 + 0.044*SL$	$0.11 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.20	$0.16 + 0.020*SL$	$0.17 + 0.018*SL$	$0.17 + 0.018*SL$
G to Y	tPLH	0.61	$0.57 + 0.020*SL$	$0.57 + 0.020*SL$	$0.57 + 0.020*SL$
	tPHL	0.66	$0.63 + 0.020*SL$	$0.64 + 0.013*SL$	$0.69 + 0.011*SL$
	tR	0.20	$0.12 + 0.043*SL$	$0.11 + 0.046*SL$	$0.09 + 0.047*SL$
	tF	0.20	$0.16 + 0.021*SL$	$0.17 + 0.018*SL$	$0.17 + 0.018*SL$
H to Y	tPLH	0.64	$0.60 + 0.021*SL$	$0.60 + 0.020*SL$	$0.60 + 0.020*SL$
	tPHL	0.65	$0.61 + 0.019*SL$	$0.63 + 0.013*SL$	$0.68 + 0.011*SL$
	tR	0.20	$0.12 + 0.041*SL$	$0.11 + 0.046*SL$	$0.09 + 0.047*SL$
	tF	0.21	$0.17 + 0.020*SL$	$0.17 + 0.018*SL$	$0.17 + 0.018*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**ND8D4 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.53	$0.50 + 0.012 * SL$	$0.51 + 0.011 * SL$	$0.51 + 0.011 * SL$
	tPHL	0.80	$0.77 + 0.013 * SL$	$0.78 + 0.009 * SL$	$0.83 + 0.007 * SL$
	tR	0.18	$0.13 + 0.023 * SL$	$0.13 + 0.025 * SL$	$0.11 + 0.026 * SL$
	tF	0.28	$0.26 + 0.011 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$
B to Y	tPLH	0.59	$0.56 + 0.012 * SL$	$0.57 + 0.011 * SL$	$0.57 + 0.011 * SL$
	tPHL	0.81	$0.79 + 0.013 * SL$	$0.80 + 0.009 * SL$	$0.84 + 0.007 * SL$
	tR	0.18	$0.13 + 0.025 * SL$	$0.13 + 0.025 * SL$	$0.11 + 0.026 * SL$
	tF	0.28	$0.26 + 0.011 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$
C to Y	tPLH	0.64	$0.61 + 0.012 * SL$	$0.62 + 0.011 * SL$	$0.62 + 0.011 * SL$
	tPHL	0.80	$0.78 + 0.012 * SL$	$0.79 + 0.009 * SL$	$0.83 + 0.007 * SL$
	tR	0.18	$0.14 + 0.022 * SL$	$0.13 + 0.025 * SL$	$0.11 + 0.026 * SL$
	tF	0.28	$0.26 + 0.011 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$
D to Y	tPLH	0.67	$0.65 + 0.012 * SL$	$0.65 + 0.011 * SL$	$0.66 + 0.011 * SL$
	tPHL	0.79	$0.76 + 0.013 * SL$	$0.77 + 0.009 * SL$	$0.82 + 0.007 * SL$
	tR	0.18	$0.14 + 0.023 * SL$	$0.13 + 0.025 * SL$	$0.11 + 0.026 * SL$
	tF	0.28	$0.26 + 0.011 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$
E to Y	tPLH	0.54	$0.52 + 0.012 * SL$	$0.52 + 0.011 * SL$	$0.53 + 0.011 * SL$
	tPHL	0.78	$0.76 + 0.012 * SL$	$0.77 + 0.009 * SL$	$0.81 + 0.007 * SL$
	tR	0.18	$0.14 + 0.022 * SL$	$0.13 + 0.025 * SL$	$0.12 + 0.026 * SL$
	tF	0.28	$0.26 + 0.012 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$
F to Y	tPLH	0.61	$0.58 + 0.012 * SL$	$0.59 + 0.011 * SL$	$0.59 + 0.011 * SL$
	tPHL	0.80	$0.77 + 0.013 * SL$	$0.78 + 0.009 * SL$	$0.83 + 0.007 * SL$
	tR	0.19	$0.14 + 0.024 * SL$	$0.14 + 0.025 * SL$	$0.12 + 0.026 * SL$
	tF	0.28	$0.25 + 0.012 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$
G to Y	tPLH	0.66	$0.63 + 0.012 * SL$	$0.64 + 0.011 * SL$	$0.64 + 0.011 * SL$
	tPHL	0.79	$0.76 + 0.013 * SL$	$0.77 + 0.009 * SL$	$0.82 + 0.007 * SL$
	tR	0.19	$0.15 + 0.021 * SL$	$0.14 + 0.025 * SL$	$0.12 + 0.026 * SL$
	tF	0.28	$0.25 + 0.012 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$
H to Y	tPLH	0.69	$0.67 + 0.012 * SL$	$0.67 + 0.011 * SL$	$0.68 + 0.011 * SL$
	tPHL	0.77	$0.74 + 0.013 * SL$	$0.75 + 0.009 * SL$	$0.80 + 0.007 * SL$
	tR	0.19	$0.15 + 0.021 * SL$	$0.14 + 0.025 * SL$	$0.12 + 0.026 * SL$
	tF	0.28	$0.26 + 0.012 * SL$	$0.26 + 0.010 * SL$	$0.27 + 0.010 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# ND8D8

## 8 Input NAND with 8X Drive

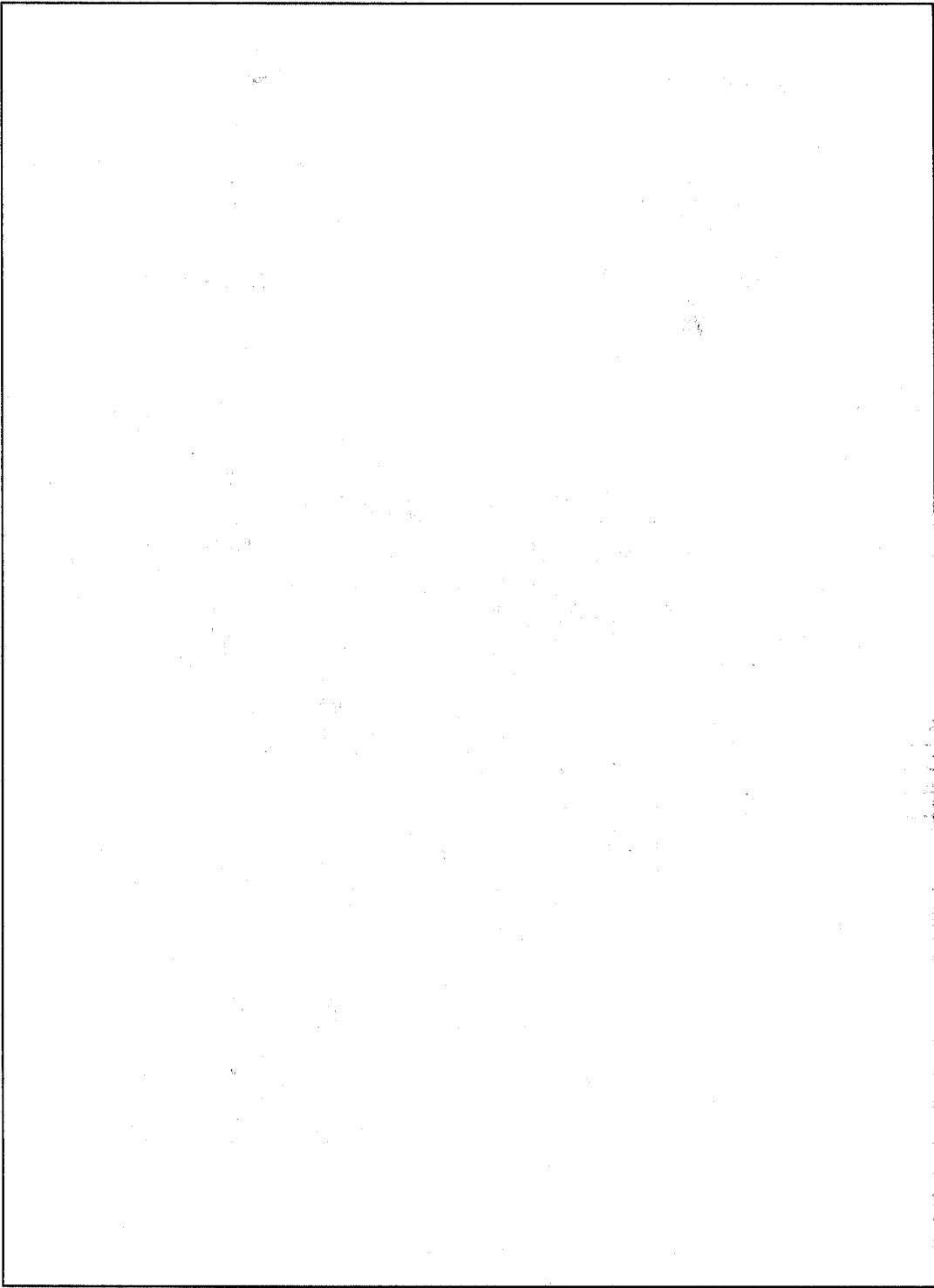
### ND8D8 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.57	$0.56 + 0.006*SL$	$0.56 + 0.006*SL$	$0.56 + 0.005*SL$
	tPHL	0.88	$0.87 + 0.007*SL$	$0.87 + 0.005*SL$	$0.89 + 0.004*SL$
	tR	0.16	$0.14 + 0.010*SL$	$0.13 + 0.012*SL$	$0.12 + 0.013*SL$
	tF	0.28	$0.27 + 0.006*SL$	$0.27 + 0.005*SL$	$0.29 + 0.005*SL$
B to Y	tPLH	0.63	$0.61 + 0.006*SL$	$0.61 + 0.006*SL$	$0.62 + 0.005*SL$
	tPHL	0.89	$0.88 + 0.007*SL$	$0.88 + 0.005*SL$	$0.91 + 0.004*SL$
	tR	0.16	$0.14 + 0.011*SL$	$0.14 + 0.012*SL$	$0.12 + 0.013*SL$
	tF	0.29	$0.28 + 0.004*SL$	$0.27 + 0.006*SL$	$0.29 + 0.005*SL$
C to Y	tPLH	0.67	$0.66 + 0.006*SL$	$0.66 + 0.006*SL$	$0.67 + 0.005*SL$
	tPHL	0.88	$0.87 + 0.006*SL$	$0.87 + 0.005*SL$	$0.89 + 0.004*SL$
	tR	0.16	$0.14 + 0.011*SL$	$0.14 + 0.012*SL$	$0.13 + 0.013*SL$
	tF	0.29	$0.28 + 0.004*SL$	$0.27 + 0.006*SL$	$0.28 + 0.005*SL$
D to Y	tPLH	0.70	$0.69 + 0.006*SL$	$0.69 + 0.006*SL$	$0.70 + 0.005*SL$
	tPHL	0.86	$0.85 + 0.007*SL$	$0.85 + 0.005*SL$	$0.88 + 0.004*SL$
	tR	0.17	$0.15 + 0.009*SL$	$0.14 + 0.012*SL$	$0.13 + 0.013*SL$
	tF	0.29	$0.28 + 0.005*SL$	$0.28 + 0.005*SL$	$0.28 + 0.005*SL$
E to Y	tPLH	0.58	$0.57 + 0.007*SL$	$0.57 + 0.006*SL$	$0.58 + 0.005*SL$
	tPHL	0.86	$0.85 + 0.007*SL$	$0.85 + 0.005*SL$	$0.88 + 0.004*SL$
	tR	0.17	$0.14 + 0.010*SL$	$0.14 + 0.012*SL$	$0.13 + 0.013*SL$
	tF	0.28	$0.28 + 0.005*SL$	$0.27 + 0.006*SL$	$0.28 + 0.005*SL$
F to Y	tPLH	0.64	$0.63 + 0.006*SL$	$0.63 + 0.006*SL$	$0.64 + 0.005*SL$
	tPHL	0.87	$0.86 + 0.007*SL$	$0.86 + 0.005*SL$	$0.89 + 0.004*SL$
	tR	0.17	$0.15 + 0.009*SL$	$0.14 + 0.012*SL$	$0.14 + 0.012*SL$
	tF	0.28	$0.27 + 0.006*SL$	$0.27 + 0.006*SL$	$0.29 + 0.005*SL$
G to Y	tPLH	0.69	$0.68 + 0.006*SL$	$0.68 + 0.006*SL$	$0.68 + 0.005*SL$
	tPHL	0.86	$0.85 + 0.007*SL$	$0.85 + 0.005*SL$	$0.88 + 0.004*SL$
	tR	0.17	$0.15 + 0.010*SL$	$0.14 + 0.012*SL$	$0.13 + 0.013*SL$
	tF	0.28	$0.27 + 0.006*SL$	$0.27 + 0.005*SL$	$0.28 + 0.005*SL$
H to Y	tPLH	0.73	$0.71 + 0.006*SL$	$0.72 + 0.006*SL$	$0.72 + 0.005*SL$
	tPHL	0.84	$0.83 + 0.007*SL$	$0.83 + 0.005*SL$	$0.86 + 0.004*SL$
	tR	0.17	$0.15 + 0.010*SL$	$0.15 + 0.012*SL$	$0.14 + 0.012*SL$
	tF	0.29	$0.27 + 0.005*SL$	$0.27 + 0.005*SL$	$0.29 + 0.005*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



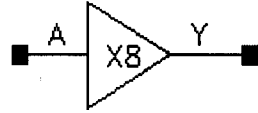


# NID8/NID12/NID16

Non-Inverting Buffer with 8X Drive, 12X Drive or 16X Drive

Input: A  
Output: Y  
Input Loading (SL): All : 2  
Maximum Fanout (Rec. SL):  
- NID8: 224  
- NID12: 336  
- NID16: 456

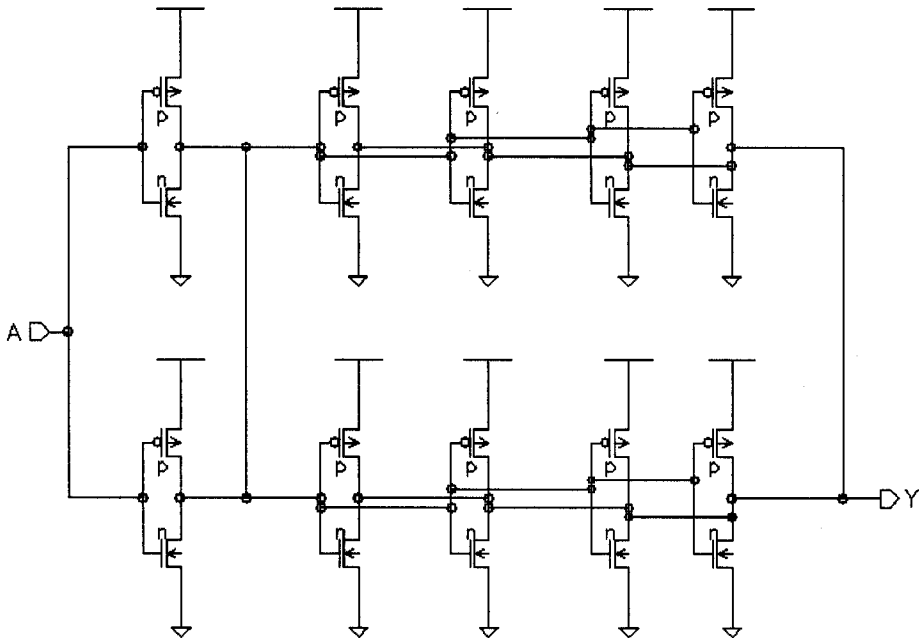
Gate Count:  
- NID8: 5  
- NID12: 7  
- NID16: 9



Symbol

A	Y
0	0
1	1

Truth Table



Schematic

**NID8 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.25	$0.24 + 0.006 * SL$	$0.24 + 0.005 * SL$	$0.24 + 0.005 * SL$
	tPHL	0.42	$0.41 + 0.005 * SL$	$0.41 + 0.004 * SL$	$0.43 + 0.003 * SL$
	tR	0.16	$0.14 + 0.010 * SL$	$0.14 + 0.011 * SL$	$0.13 + 0.011 * SL$
	tF	0.18	$0.16 + 0.007 * SL$	$0.17 + 0.004 * SL$	$0.16 + 0.005 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**NID12 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.31	$0.30 + 0.004 * SL$	$0.30 + 0.004 * SL$	$0.31 + 0.004 * SL$
	tPHL	0.50	$0.49 + 0.004 * SL$	$0.49 + 0.003 * SL$	$0.50 + 0.003 * SL$
	tR	0.18	$0.16 + 0.006 * SL$	$0.16 + 0.008 * SL$	$0.15 + 0.008 * SL$
	tF	0.22	$0.21 + 0.002 * SL$	$0.21 + 0.003 * SL$	$0.21 + 0.003 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**NID16 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.37	$0.36 + 0.003 * SL$	$0.36 + 0.003 * SL$	$0.37 + 0.003 * SL$
	tPHL	0.56	$0.56 + 0.004 * SL$	$0.56 + 0.003 * SL$	$0.57 + 0.002 * SL$
	tR	0.19	$0.18 + 0.006 * SL$	$0.18 + 0.005 * SL$	$0.17 + 0.006 * SL$
	tF	0.26	$0.25 + 0.006 * SL$	$0.26 + 0.002 * SL$	$0.26 + 0.002 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# NIT/NITD2/NITD5/NITD9

Non-Inverting 3-State Buffer, Enable High, with 1X Drive, 2X Drive, 5X Drive or 9X Drive

Inputs: A, E

Output: Y

Input Loading (SL):

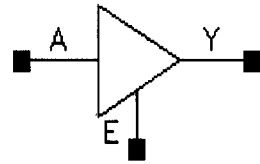
- NIT: A : 1, E : 1.5
- NITD2: A : 1, E : 2
- NITD5: A : 2, E : 2
- NITD9: A : 2, E : 2

Maximum Fanout (Rec. SL):

- NIT: 28
- NITD2: 56
- NITD5: 112
- NITD9: 252

Gate Count:

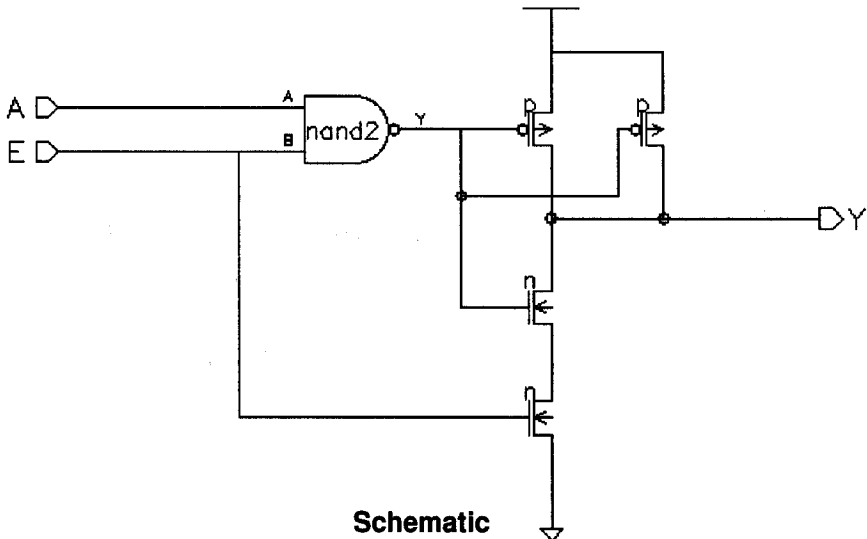
- NIT: 2
- NITD2: 3
- NITD5: 5
- NITD9: 7



Symbol

A	E	Y
x	0	hi-z
1	1	1
0	1	0

Truth Table



Schematic

**NIT Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_r$  and  $t_f = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.24	$0.19 + 0.024 \cdot \text{SL}$	$0.21 + 0.021 \cdot \text{SL}$	$0.22 + 0.020 \cdot \text{SL}$
	tPHL	0.44	$0.37 + 0.033 \cdot \text{SL}$	$0.38 + 0.030 \cdot \text{SL}$	$0.38 + 0.029 \cdot \text{SL}$
	tR	0.22	$0.14 + 0.040 \cdot \text{SL}$	$0.12 + 0.045 \cdot \text{SL}$	$0.09 + 0.046 \cdot \text{SL}$
	tF	0.27	$0.15 + 0.059 \cdot \text{SL}$	$0.14 + 0.062 \cdot \text{SL}$	$0.11 + 0.064 \cdot \text{SL}$
E to Y	tPLH	0.21	$0.16 + 0.025 \cdot \text{SL}$	$0.17 + 0.021 \cdot \text{SL}$	$0.19 + 0.020 \cdot \text{SL}$
	tPHL	0.05	$-0.04 + 0.048 \cdot \text{SL}$	$0.00 + 0.032 \cdot \text{SL}$	$0.06 + 0.030 \cdot \text{SL}$
	tR	0.22	$0.14 + 0.041 \cdot \text{SL}$	$0.13 + 0.045 \cdot \text{SL}$	$0.09 + 0.046 \cdot \text{SL}$
	tF	0.36	$0.24 + 0.060 \cdot \text{SL}$	$0.24 + 0.059 \cdot \text{SL}$	$0.17 + 0.063 \cdot \text{SL}$
	tPLZ	0.40	$0.40 + -0.000 \cdot \text{SL}$	$0.40 + -0.000 \cdot \text{SL}$	$0.40 + -0.000 \cdot \text{SL}$
	tPHZ	0.52	$0.52 + -0.000 \cdot \text{SL}$	$0.52 + -0.000 \cdot \text{SL}$	$0.52 + -0.000 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **NITD2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_r$  and  $t_f = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.28	$0.25 + 0.014 \cdot \text{SL}$	$0.26 + 0.011 \cdot \text{SL}$	$0.28 + 0.010 \cdot \text{SL}$
	tPHL	0.48	$0.44 + 0.018 \cdot \text{SL}$	$0.45 + 0.016 \cdot \text{SL}$	$0.47 + 0.015 \cdot \text{SL}$
	tR	0.20	$0.17 + 0.018 \cdot \text{SL}$	$0.16 + 0.021 \cdot \text{SL}$	$0.13 + 0.023 \cdot \text{SL}$
	tF	0.24	$0.18 + 0.030 \cdot \text{SL}$	$0.18 + 0.031 \cdot \text{SL}$	$0.14 + 0.032 \cdot \text{SL}$
E to Y	tPLH	0.24	$0.21 + 0.015 \cdot \text{SL}$	$0.22 + 0.011 \cdot \text{SL}$	$0.24 + 0.010 \cdot \text{SL}$
	tPHL	0.00	$-0.06 + 0.029 \cdot \text{SL}$	$-0.03 + 0.019 \cdot \text{SL}$	$0.04 + 0.016 \cdot \text{SL}$
	tR	0.20	$0.17 + 0.018 \cdot \text{SL}$	$0.16 + 0.021 \cdot \text{SL}$	$0.13 + 0.023 \cdot \text{SL}$
	tF	0.29	$0.23 + 0.034 \cdot \text{SL}$	$0.24 + 0.030 \cdot \text{SL}$	$0.22 + 0.031 \cdot \text{SL}$
	tPLZ	0.40	$0.40 + -0.000 \cdot \text{SL}$	$0.40 + -0.000 \cdot \text{SL}$	$0.40 + -0.000 \cdot \text{SL}$
	tPHZ	0.61	$0.61 + -0.000 \cdot \text{SL}$	$0.61 + -0.000 \cdot \text{SL}$	$0.61 + -0.000 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

# NITD5/NITD9

Non-inverting 3-State Buffer, Enable High, with 5X Drive or 9X Drive

## NITD5 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.25	$0.23 + 0.012*SL$	$0.23 + 0.010*SL$	$0.26 + 0.009*SL$
	tPHL	0.47	$0.45 + 0.010*SL$	$0.46 + 0.008*SL$	$0.49 + 0.006*SL$
	tR	0.18	$0.14 + 0.020*SL$	$0.14 + 0.020*SL$	$0.15 + 0.020*SL$
	tF	0.15	$0.14 + 0.010*SL$	$0.14 + 0.009*SL$	$0.15 + 0.009*SL$
E to Y	tPLH	0.19	$0.16 + 0.016*SL$	$0.18 + 0.011*SL$	$0.21 + 0.009*SL$
	tPHL	0.31	$0.28 + 0.013*SL$	$0.30 + 0.008*SL$	$0.34 + 0.006*SL$
	tR	0.21	$0.17 + 0.019*SL$	$0.17 + 0.019*SL$	$0.15 + 0.020*SL$
	tF	0.15	$0.12 + 0.012*SL$	$0.13 + 0.010*SL$	$0.16 + 0.009*SL$
	tPLZ	0.40	$0.40 + -0.000*SL$	$0.40 + -0.000*SL$	$0.40 + -0.000*SL$
	tPHZ	0.67	$0.67 + 0.000*SL$	$0.67 + -0.000*SL$	$0.67 + -0.000*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

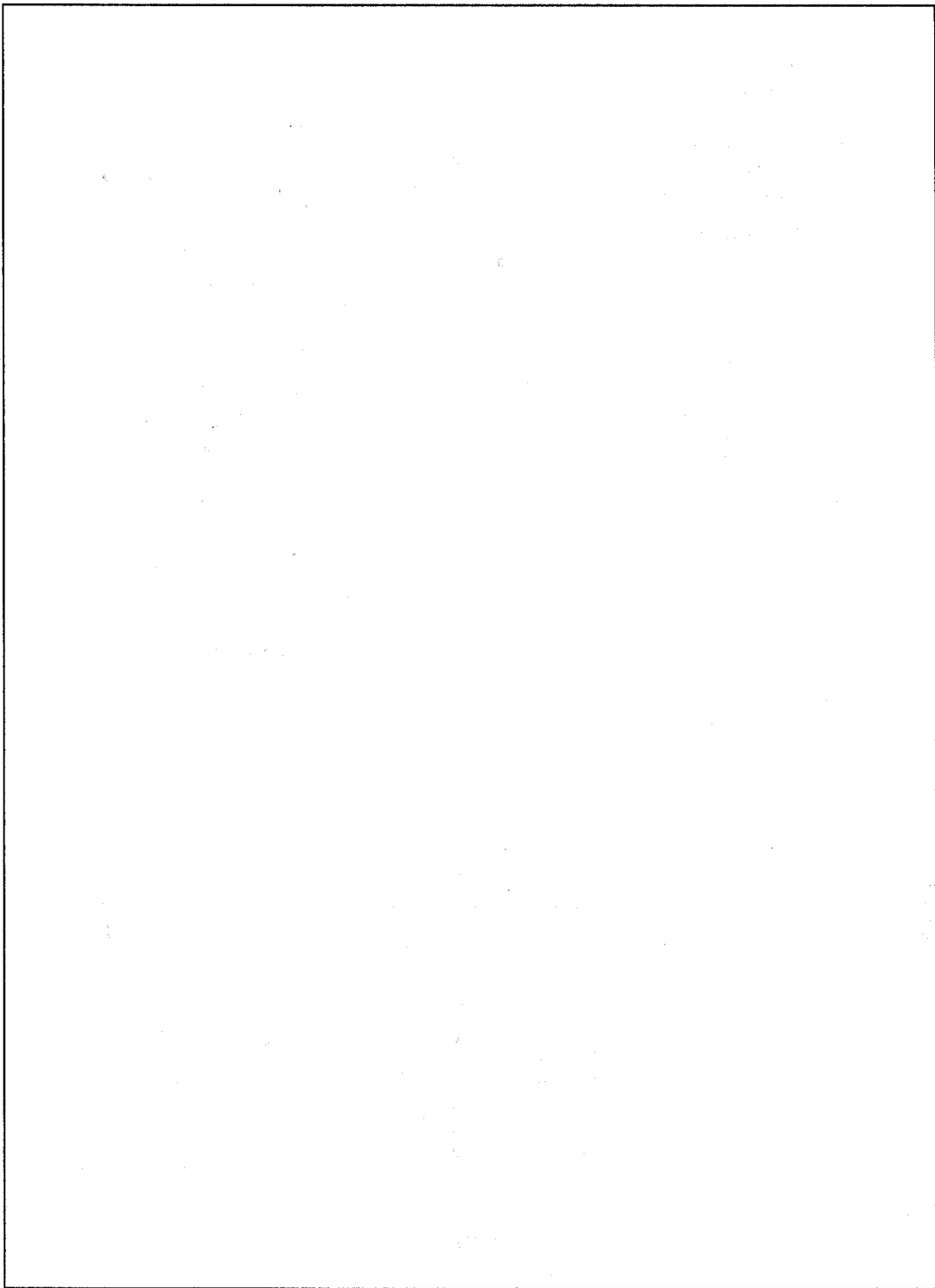
## NITD9 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.32	$0.31 + 0.007*SL$	$0.31 + 0.006*SL$	$0.32 + 0.005*SL$
	tPHL	0.55	$0.53 + 0.006*SL$	$0.54 + 0.005*SL$	$0.56 + 0.004*SL$
	tR	0.18	$0.15 + 0.013*SL$	$0.15 + 0.012*SL$	$0.16 + 0.011*SL$
	tF	0.20	$0.19 + 0.004*SL$	$0.18 + 0.005*SL$	$0.19 + 0.005*SL$
E to Y	tPLH	0.23	$0.20 + 0.010*SL$	$0.21 + 0.007*SL$	$0.25 + 0.006*SL$
	tPHL	0.36	$0.34 + 0.009*SL$	$0.35 + 0.006*SL$	$0.38 + 0.004*SL$
	tR	0.21	$0.19 + 0.011*SL$	$0.19 + 0.011*SL$	$0.19 + 0.011*SL$
	tF	0.17	$0.15 + 0.010*SL$	$0.16 + 0.007*SL$	$0.18 + 0.005*SL$
	tPLZ	0.40	$0.40 + -0.000*SL$	$0.40 + -0.000*SL$	$0.40 + -0.000*SL$
	tPHZ	0.85	$0.85 + -0.000*SL$	$0.85 + -0.000*SL$	$0.85 + -0.000*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# NR2/NR2D2/NR2D3/NR2D7

2 Input NOR with 1X Drive, 2X Drive, 3X Drive or 7X Drive

Inputs: A, B

Output: Y

Input Loading (SL):

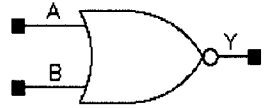
- NR2: All : 1
- NR2D2: All : 2
- NR2D3: All: 1
- NR2D7: All: 1

Maximum Fanout (Rec. SL):

- NR2: 14
- NR2D2: 28
- NR2D3: 84
- NR2D7: 196

Gate Count:

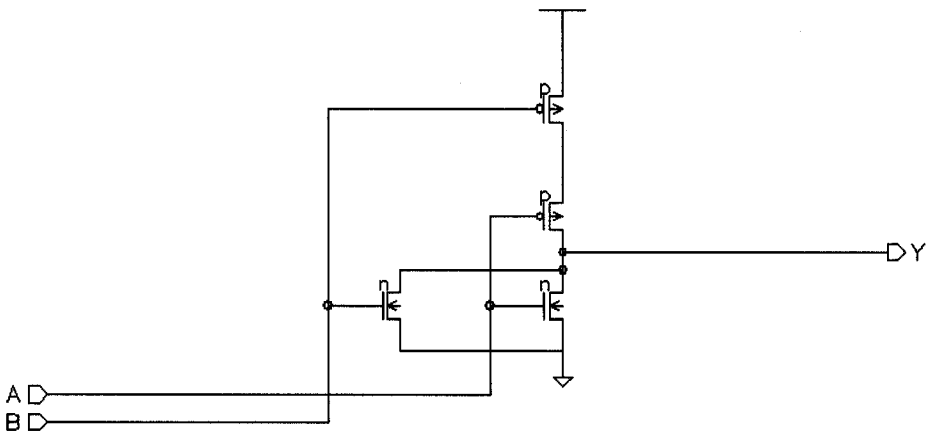
- NR2: 1
- NR2D2: 2
- NR2D3: 3
- NR2D7: 5



Symbol

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table



Schematic

**NR2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.48	$0.33 + 0.075*SL$	$0.33 + 0.075*SL$	$0.29 + 0.077*SL$
	tPHL	0.07	$-0.02 + 0.044*SL$	$0.03 + 0.025*SL$	$0.13 + 0.020*SL$
	tR	0.71	$0.35 + 0.178*SL$	$0.33 + 0.187*SL$	$0.27 + 0.190*SL$
	tF	0.33	$0.24 + 0.043*SL$	$0.26 + 0.036*SL$	$0.22 + 0.039*SL$
B to Y	tPLH	0.46	$0.31 + 0.073*SL$	$0.30 + 0.076*SL$	$0.26 + 0.078*SL$
	tPHL	0.09	$0.01 + 0.042*SL$	$0.06 + 0.025*SL$	$0.15 + 0.020*SL$
	tR	0.72	$0.37 + 0.174*SL$	$0.34 + 0.187*SL$	$0.27 + 0.190*SL$
	tF	0.38	$0.31 + 0.038*SL$	$0.32 + 0.035*SL$	$0.26 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**NR2D2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.41	$0.33 + 0.039*SL$	$0.34 + 0.037*SL$	$0.32 + 0.038*SL$
	tPHL	0.02	$-0.04 + 0.026*SL$	$-0.01 + 0.016*SL$	$0.09 + 0.011*SL$
	tR	0.52	$0.35 + 0.086*SL$	$0.34 + 0.090*SL$	$0.29 + 0.093*SL$
	tF	0.28	$0.23 + 0.023*SL$	$0.25 + 0.018*SL$	$0.26 + 0.017*SL$
B to Y	tPLH	0.38	$0.30 + 0.037*SL$	$0.31 + 0.036*SL$	$0.28 + 0.038*SL$
	tPHL	0.05	$-0.00 + 0.025*SL$	$0.02 + 0.015*SL$	$0.12 + 0.011*SL$
	tR	0.54	$0.38 + 0.081*SL$	$0.35 + 0.090*SL$	$0.29 + 0.093*SL$
	tF	0.34	$0.30 + 0.022*SL$	$0.31 + 0.017*SL$	$0.31 + 0.017*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# NR2D3/NR2D7

2 Input NOR with 3X Drive or 7X Drive

## NR2D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.63	$0.59 + 0.015 \cdot \text{SL}$	$0.60 + 0.014 \cdot \text{SL}$	$0.60 + 0.014 \cdot \text{SL}$
	tPHL	0.27	$0.24 + 0.012 \cdot \text{SL}$	$0.25 + 0.009 \cdot \text{SL}$	$0.28 + 0.007 \cdot \text{SL}$
	tR	0.18	$0.12 + 0.032 \cdot \text{SL}$	$0.11 + 0.034 \cdot \text{SL}$	$0.10 + 0.034 \cdot \text{SL}$
	tF	0.15	$0.13 + 0.012 \cdot \text{SL}$	$0.13 + 0.013 \cdot \text{SL}$	$0.12 + 0.013 \cdot \text{SL}$
B to Y	tPLH	0.60	$0.57 + 0.014 \cdot \text{SL}$	$0.57 + 0.014 \cdot \text{SL}$	$0.57 + 0.014 \cdot \text{SL}$
	tPHL	0.31	$0.29 + 0.012 \cdot \text{SL}$	$0.30 + 0.009 \cdot \text{SL}$	$0.33 + 0.007 \cdot \text{SL}$
	tR	0.18	$0.12 + 0.030 \cdot \text{SL}$	$0.11 + 0.034 \cdot \text{SL}$	$0.10 + 0.034 \cdot \text{SL}$
	tF	0.15	$0.13 + 0.011 \cdot \text{SL}$	$0.12 + 0.013 \cdot \text{SL}$	$0.12 + 0.013 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

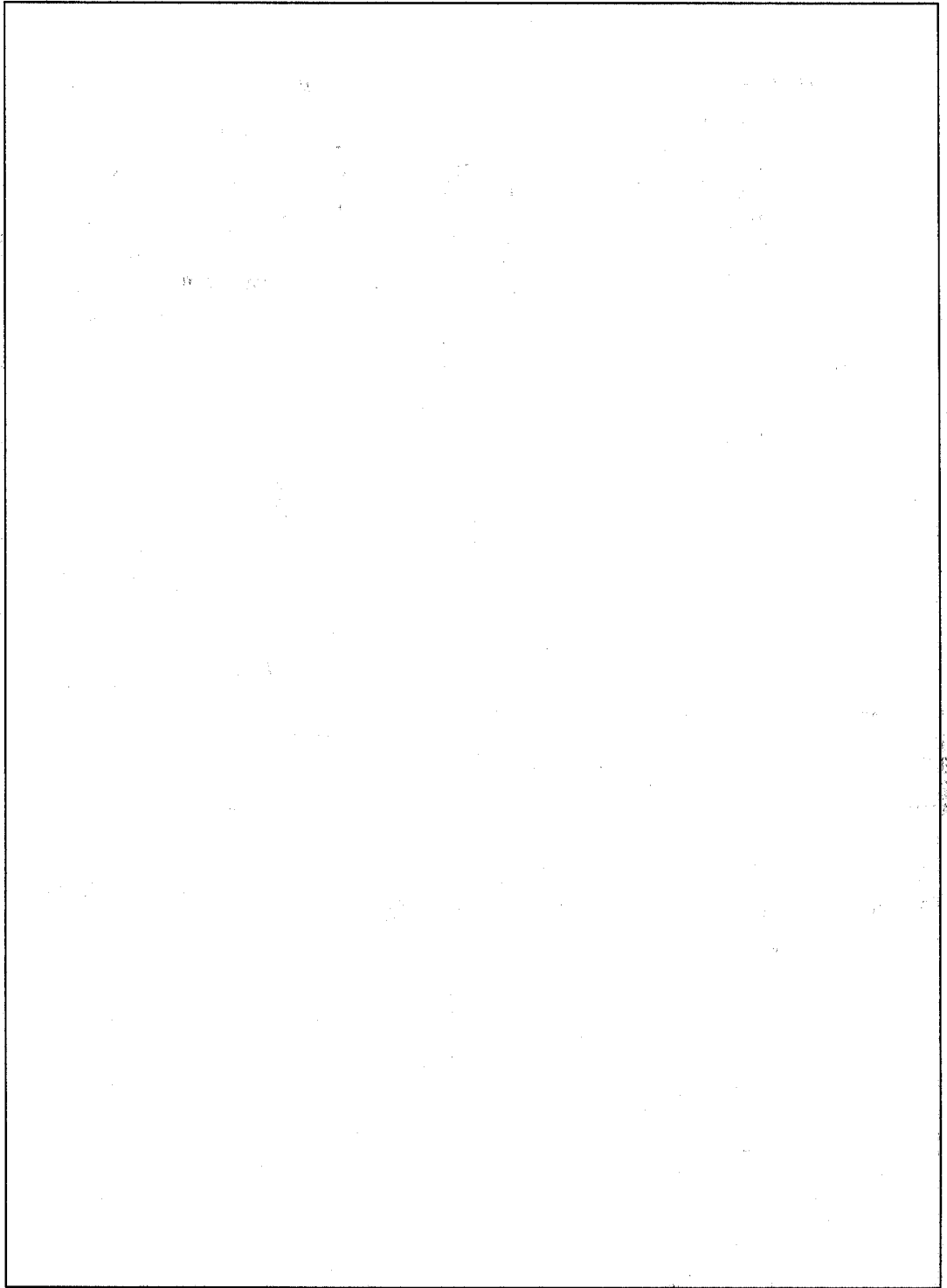
## NR2D7 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.73	$0.71 + 0.007 \cdot \text{SL}$	$0.72 + 0.006 \cdot \text{SL}$	$0.72 + 0.006 \cdot \text{SL}$
	tPHL	0.39	$0.38 + 0.006 \cdot \text{SL}$	$0.38 + 0.005 \cdot \text{SL}$	$0.41 + 0.004 \cdot \text{SL}$
	tR	0.19	$0.16 + 0.012 \cdot \text{SL}$	$0.16 + 0.014 \cdot \text{SL}$	$0.14 + 0.014 \cdot \text{SL}$
	tF	0.23	$0.21 + 0.007 \cdot \text{SL}$	$0.22 + 0.006 \cdot \text{SL}$	$0.22 + 0.005 \cdot \text{SL}$
B to Y	tPLH	0.71	$0.69 + 0.007 \cdot \text{SL}$	$0.69 + 0.006 \cdot \text{SL}$	$0.70 + 0.006 \cdot \text{SL}$
	tPHL	0.44	$0.42 + 0.006 \cdot \text{SL}$	$0.43 + 0.005 \cdot \text{SL}$	$0.45 + 0.004 \cdot \text{SL}$
	tR	0.19	$0.16 + 0.013 \cdot \text{SL}$	$0.16 + 0.014 \cdot \text{SL}$	$0.14 + 0.014 \cdot \text{SL}$
	tF	0.23	$0.23 + 0.001 \cdot \text{SL}$	$0.22 + 0.006 \cdot \text{SL}$	$0.23 + 0.005 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$



# NR3/NR3D2/NR3D3//NR3D7

3 Input NOR with 1X Drive, 2X Drive, 3X Drive or 7X Drive

Inputs: A, B, C

Output: Y

Input Loading (SL):

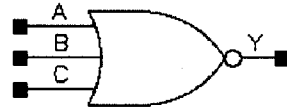
- NR3: All : 1
- NR3D2: All : 2
- NR3D3: All: 1
- NR3D7: All: 1

Maximum Fanout (Rec. SL):

- NR3: 9
- NR3D2: 19
- NR3D3: 84
- NR3D7: 196

Gate Count:

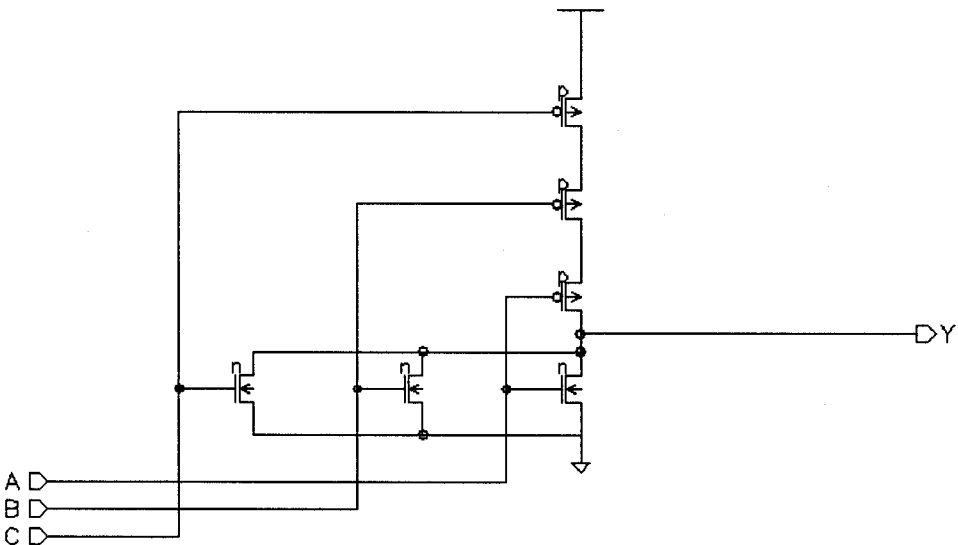
- NR3: 3
- NR3D2: 4
- NR3D3: 4
- NR3D7: 6



Symbol

A	B	C	Y
0	0	0	1
1	x	x	0
x	1	x	0
x	x	1	0

Truth Table



Schematic

**NR3 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.64	$0.42 + 0.110 * SL$	$0.41 + 0.114 * SL$	$0.36 + 0.117 * SL$
	tPHL	0.08	$-0.01 + 0.043 * SL$	$0.04 + 0.025 * SL$	$0.14 + 0.020 * SL$
	tR	1.17	$0.61 + 0.279 * SL$	$0.59 + 0.286 * SL$	$0.57 + 0.287 * SL$
	tF	0.34	$0.25 + 0.045 * SL$	$0.27 + 0.036 * SL$	$0.23 + 0.039 * SL$
B to Y	tPLH	0.66	$0.44 + 0.112 * SL$	$0.43 + 0.115 * SL$	$0.39 + 0.117 * SL$
	tPHL	0.10	$0.02 + 0.041 * SL$	$0.07 + 0.025 * SL$	$0.16 + 0.020 * SL$
	tR	1.19	$0.64 + 0.276 * SL$	$0.61 + 0.285 * SL$	$0.57 + 0.287 * SL$
	tF	0.39	$0.30 + 0.041 * SL$	$0.32 + 0.036 * SL$	$0.26 + 0.039 * SL$
C to Y	tPLH	0.66	$0.43 + 0.112 * SL$	$0.42 + 0.116 * SL$	$0.39 + 0.117 * SL$
	tPHL	0.10	$0.01 + 0.042 * SL$	$0.06 + 0.025 * SL$	$0.16 + 0.020 * SL$
	tR	1.18	$0.63 + 0.277 * SL$	$0.61 + 0.285 * SL$	$0.57 + 0.287 * SL$
	tF	0.41	$0.33 + 0.039 * SL$	$0.35 + 0.034 * SL$	$0.30 + 0.036 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **NR3D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.53	$0.42 + 0.055 * SL$	$0.42 + 0.055 * SL$	$0.39 + 0.057 * SL$
	tPHL	0.03	$-0.02 + 0.025 * SL$	$0.00 + 0.016 * SL$	$0.10 + 0.011 * SL$
	tR	0.87	$0.59 + 0.137 * SL$	$0.58 + 0.141 * SL$	$0.55 + 0.142 * SL$
	tF	0.29	$0.24 + 0.023 * SL$	$0.26 + 0.018 * SL$	$0.27 + 0.017 * SL$
B to Y	tPLH	0.54	$0.43 + 0.055 * SL$	$0.43 + 0.056 * SL$	$0.41 + 0.057 * SL$
	tPHL	0.05	$0.01 + 0.024 * SL$	$0.03 + 0.015 * SL$	$0.12 + 0.011 * SL$
	tR	0.89	$0.62 + 0.135 * SL$	$0.61 + 0.140 * SL$	$0.57 + 0.142 * SL$
	tF	0.34	$0.30 + 0.021 * SL$	$0.31 + 0.017 * SL$	$0.31 + 0.017 * SL$
C to Y	tPLH	0.54	$0.43 + 0.055 * SL$	$0.42 + 0.056 * SL$	$0.40 + 0.057 * SL$
	tPHL	0.05	$0.00 + 0.025 * SL$	$0.03 + 0.016 * SL$	$0.12 + 0.011 * SL$
	tR	0.89	$0.62 + 0.134 * SL$	$0.60 + 0.140 * SL$	$0.56 + 0.142 * SL$
	tF	0.37	$0.33 + 0.022 * SL$	$0.34 + 0.017 * SL$	$0.34 + 0.017 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# NR3D3/NR3D7

3 Input NOR with 3X Drive or 7X Drive

## NR3D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t <sub>PLH</sub>	0.56	$0.53 + 0.016 * SL$	$0.53 + 0.015 * SL$	$0.54 + 0.014 * SL$
	t <sub>PHL</sub>	0.28	$0.26 + 0.013 * SL$	$0.27 + 0.009 * SL$	$0.30 + 0.007 * SL$
	t <sub>R</sub>	0.21	$0.14 + 0.033 * SL$	$0.14 + 0.033 * SL$	$0.12 + 0.034 * SL$
	t <sub>F</sub>	0.16	$0.14 + 0.012 * SL$	$0.13 + 0.013 * SL$	$0.13 + 0.013 * SL$
B to Y	t <sub>PLH</sub>	0.71	$0.68 + 0.017 * SL$	$0.68 + 0.015 * SL$	$0.69 + 0.014 * SL$
	t <sub>PHL</sub>	0.32	$0.29 + 0.014 * SL$	$0.31 + 0.010 * SL$	$0.35 + 0.007 * SL$
	t <sub>R</sub>	0.21	$0.15 + 0.031 * SL$	$0.14 + 0.033 * SL$	$0.12 + 0.034 * SL$
	t <sub>F</sub>	0.18	$0.15 + 0.014 * SL$	$0.16 + 0.013 * SL$	$0.16 + 0.013 * SL$
C to Y	t <sub>PLH</sub>	0.69	$0.65 + 0.017 * SL$	$0.66 + 0.015 * SL$	$0.67 + 0.014 * SL$
	t <sub>PHL</sub>	0.36	$0.33 + 0.014 * SL$	$0.35 + 0.010 * SL$	$0.39 + 0.007 * SL$
	t <sub>R</sub>	0.21	$0.15 + 0.031 * SL$	$0.14 + 0.033 * SL$	$0.12 + 0.034 * SL$
	t <sub>F</sub>	0.18	$0.16 + 0.014 * SL$	$0.16 + 0.013 * SL$	$0.16 + 0.013 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

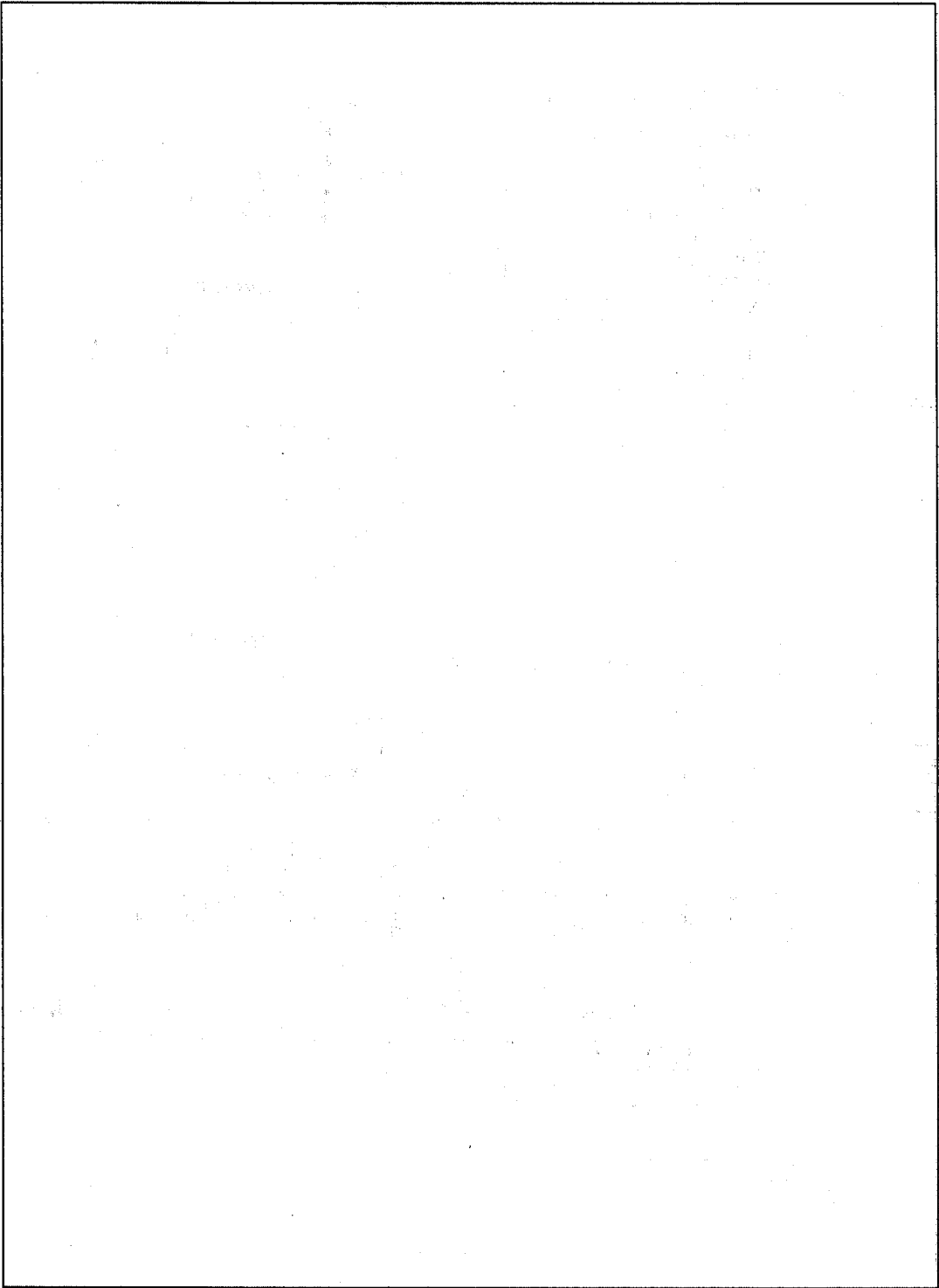
## NR3D7 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	t <sub>PLH</sub>	0.70	$0.68 + 0.008 * SL$	$0.69 + 0.007 * SL$	$0.70 + 0.006 * SL$
	t <sub>PHL</sub>	0.41	$0.40 + 0.007 * SL$	$0.40 + 0.005 * SL$	$0.43 + 0.004 * SL$
	t <sub>R</sub>	0.25	$0.23 + 0.010 * SL$	$0.22 + 0.013 * SL$	$0.20 + 0.014 * SL$
	t <sub>F</sub>	0.23	$0.22 + 0.006 * SL$	$0.22 + 0.006 * SL$	$0.23 + 0.005 * SL$
B to Y	t <sub>PLH</sub>	0.85	$0.83 + 0.009 * SL$	$0.84 + 0.007 * SL$	$0.85 + 0.006 * SL$
	t <sub>PHL</sub>	0.44	$0.43 + 0.007 * SL$	$0.43 + 0.006 * SL$	$0.46 + 0.004 * SL$
	t <sub>R</sub>	0.26	$0.24 + 0.010 * SL$	$0.23 + 0.013 * SL$	$0.20 + 0.014 * SL$
	t <sub>F</sub>	0.25	$0.24 + 0.006 * SL$	$0.24 + 0.006 * SL$	$0.25 + 0.005 * SL$
C to Y	t <sub>PLH</sub>	0.83	$0.81 + 0.009 * SL$	$0.82 + 0.007 * SL$	$0.83 + 0.006 * SL$
	t <sub>PHL</sub>	0.48	$0.47 + 0.007 * SL$	$0.47 + 0.006 * SL$	$0.50 + 0.004 * SL$
	t <sub>R</sub>	0.26	$0.24 + 0.010 * SL$	$0.23 + 0.013 * SL$	$0.20 + 0.014 * SL$
	t <sub>F</sub>	0.25	$0.24 + 0.007 * SL$	$0.24 + 0.006 * SL$	$0.25 + 0.005 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# NR4/NR4D2/NR4D4/NR4D6

4 Input NOR with 1X Drive, 2X Drive, 4X Drive or 6X Drive

Inputs: A, B, C, D

Output: Y

Input Loading (SL):

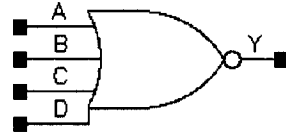
- NR4: All : 1
- NR4D2: All: 1
- NR4D4: All: 1
- NR4D6: All: 1

Maximum Fanout (Rec. SL):

- NR4: 7
- NR4D2: 56
- NR4D4: 112
- NR4D6: 168

Gate Count:

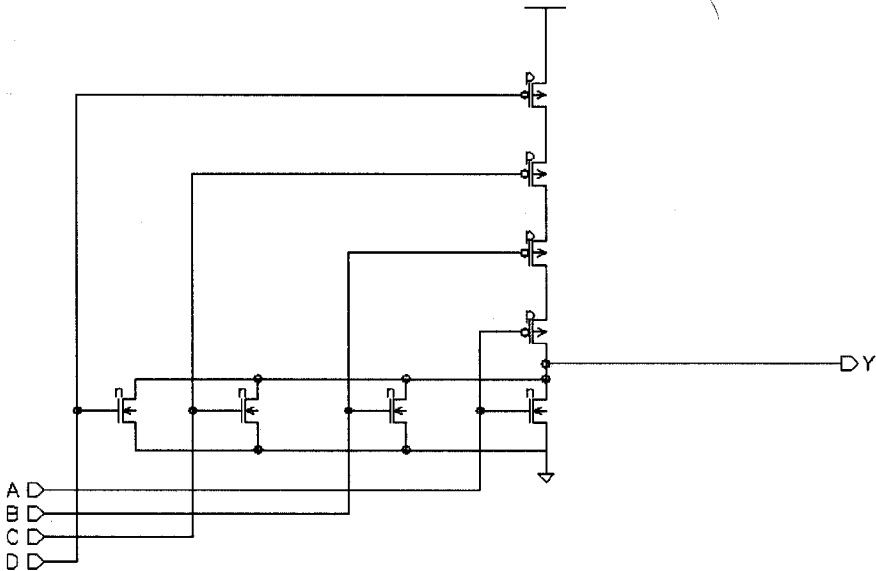
- NR4: 2
- NR4D2: 4
- NR4D4: 5
- NR4D6: 6



**Symbol**

A	B	C	D	Y
0	0	0	0	1
1	x	x	x	0
x	1	x	x	0
x	x	1	x	0
x	x	x	1	0

**Truth Table**



**Schematic**

**NR4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.79	$0.50 + 0.145^*SL$	$0.49 + 0.150^*SL$	$0.43 + 0.153^*SL$
	tPHL	0.09	$0.01 + 0.041^*SL$	$0.05 + 0.025^*SL$	$0.15 + 0.020^*SL$
	tR	1.71	$0.97 + 0.370^*SL$	$0.95 + 0.376^*SL$	$0.97 + 0.375^*SL$
	tF	0.35	$0.27 + 0.042^*SL$	$0.28 + 0.037^*SL$	$0.24 + 0.039^*SL$
B to Y	tPLH	0.86	$0.56 + 0.148^*SL$	$0.55 + 0.152^*SL$	$0.52 + 0.153^*SL$
	tPHL	0.11	$0.03 + 0.040^*SL$	$0.08 + 0.025^*SL$	$0.17 + 0.020^*SL$
	tR	1.75	$1.02 + 0.367^*SL$	$1.00 + 0.374^*SL$	$0.97 + 0.375^*SL$
	tF	0.39	$0.32 + 0.040^*SL$	$0.33 + 0.036^*SL$	$0.27 + 0.039^*SL$
C to Y	tPLH	0.90	$0.60 + 0.151^*SL$	$0.59 + 0.153^*SL$	$0.57 + 0.154^*SL$
	tPHL	0.12	$0.04 + 0.041^*SL$	$0.08 + 0.025^*SL$	$0.18 + 0.020^*SL$
	tR	1.76	$1.03 + 0.366^*SL$	$1.00 + 0.373^*SL$	$0.97 + 0.375^*SL$
	tF	0.43	$0.35 + 0.040^*SL$	$0.36 + 0.036^*SL$	$0.31 + 0.039^*SL$
D to Y	tPLH	0.91	$0.61 + 0.152^*SL$	$0.60 + 0.153^*SL$	$0.59 + 0.154^*SL$
	tPHL	0.12	$0.03 + 0.041^*SL$	$0.08 + 0.026^*SL$	$0.18 + 0.021^*SL$
	tR	1.75	$1.02 + 0.366^*SL$	$1.00 + 0.374^*SL$	$0.97 + 0.375^*SL$
	tF	0.45	$0.36 + 0.042^*SL$	$0.38 + 0.037^*SL$	$0.34 + 0.039^*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **NR4D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.67	$0.62 + 0.022^*SL$	$0.63 + 0.020^*SL$	$0.63 + 0.020^*SL$
	tPHL	0.25	$0.22 + 0.016^*SL$	$0.23 + 0.011^*SL$	$0.26 + 0.010^*SL$
	tR	0.22	$0.12 + 0.045^*SL$	$0.12 + 0.045^*SL$	$0.10 + 0.047^*SL$
	tF	0.14	$0.10 + 0.017^*SL$	$0.10 + 0.019^*SL$	$0.09 + 0.019^*SL$
B to Y	tPLH	0.64	$0.60 + 0.022^*SL$	$0.61 + 0.020^*SL$	$0.61 + 0.020^*SL$
	tPHL	0.29	$0.26 + 0.017^*SL$	$0.27 + 0.011^*SL$	$0.30 + 0.010^*SL$
	tR	0.21	$0.12 + 0.045^*SL$	$0.12 + 0.046^*SL$	$0.10 + 0.047^*SL$
	tF	0.14	$0.10 + 0.019^*SL$	$0.10 + 0.018^*SL$	$0.09 + 0.019^*SL$
C to Y	tPLH	0.66	$0.62 + 0.022^*SL$	$0.62 + 0.020^*SL$	$0.63 + 0.020^*SL$
	tPHL	0.28	$0.25 + 0.018^*SL$	$0.27 + 0.012^*SL$	$0.30 + 0.010^*SL$
	tR	0.21	$0.13 + 0.043^*SL$	$0.12 + 0.046^*SL$	$0.10 + 0.047^*SL$
	tF	0.16	$0.12 + 0.018^*SL$	$0.12 + 0.018^*SL$	$0.11 + 0.019^*SL$
D to Y	tPLH	0.64	$0.59 + 0.022^*SL$	$0.60 + 0.020^*SL$	$0.60 + 0.020^*SL$
	tPHL	0.33	$0.29 + 0.018^*SL$	$0.31 + 0.012^*SL$	$0.35 + 0.010^*SL$
	tR	0.22	$0.13 + 0.045^*SL$	$0.13 + 0.045^*SL$	$0.10 + 0.047^*SL$
	tF	0.16	$0.12 + 0.019^*SL$	$0.13 + 0.018^*SL$	$0.11 + 0.019^*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# NR4D4/NR4D6

4 Input NOR with 4X Drive or 6X Drive

## NR4D4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.75	$0.73 + 0.013*SL$	$0.73 + 0.011*SL$	$0.74 + 0.011*SL$
	tPHL	0.31	$0.29 + 0.011*SL$	$0.30 + 0.007*SL$	$0.33 + 0.006*SL$
	tR	0.21	$0.17 + 0.022*SL$	$0.16 + 0.025*SL$	$0.14 + 0.025*SL$
	tF	0.17	$0.15 + 0.010*SL$	$0.16 + 0.010*SL$	$0.15 + 0.010*SL$
B to Y	tPLH	0.73	$0.71 + 0.013*SL$	$0.71 + 0.011*SL$	$0.72 + 0.011*SL$
	tPHL	0.35	$0.33 + 0.011*SL$	$0.34 + 0.008*SL$	$0.37 + 0.006*SL$
	tR	0.21	$0.17 + 0.023*SL$	$0.16 + 0.025*SL$	$0.15 + 0.025*SL$
	tF	0.18	$0.16 + 0.011*SL$	$0.16 + 0.010*SL$	$0.16 + 0.010*SL$
C to Y	tPLH	0.74	$0.72 + 0.013*SL$	$0.72 + 0.011*SL$	$0.73 + 0.011*SL$
	tPHL	0.35	$0.33 + 0.011*SL$	$0.33 + 0.008*SL$	$0.37 + 0.006*SL$
	tR	0.21	$0.17 + 0.022*SL$	$0.16 + 0.025*SL$	$0.14 + 0.025*SL$
	tF	0.20	$0.18 + 0.011*SL$	$0.18 + 0.010*SL$	$0.18 + 0.010*SL$
D to Y	tPLH	0.72	$0.69 + 0.013*SL$	$0.70 + 0.011*SL$	$0.71 + 0.011*SL$
	tPHL	0.39	$0.37 + 0.011*SL$	$0.38 + 0.008*SL$	$0.41 + 0.006*SL$
	tR	0.22	$0.17 + 0.022*SL$	$0.16 + 0.025*SL$	$0.15 + 0.025*SL$
	tF	0.20	$0.18 + 0.010*SL$	$0.18 + 0.010*SL$	$0.18 + 0.010*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## NR4D6 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.83	$0.81 + 0.010*SL$	$0.82 + 0.008*SL$	$0.83 + 0.007*SL$
	tPHL	0.38	$0.36 + 0.008*SL$	$0.37 + 0.006*SL$	$0.39 + 0.005*SL$
	tR	0.24	$0.21 + 0.013*SL$	$0.21 + 0.015*SL$	$0.18 + 0.017*SL$
	tF	0.21	$0.20 + 0.007*SL$	$0.20 + 0.007*SL$	$0.21 + 0.006*SL$
B to Y	tPLH	0.81	$0.79 + 0.010*SL$	$0.79 + 0.008*SL$	$0.80 + 0.007*SL$
	tPHL	0.42	$0.40 + 0.008*SL$	$0.41 + 0.006*SL$	$0.43 + 0.005*SL$
	tR	0.24	$0.21 + 0.013*SL$	$0.21 + 0.015*SL$	$0.18 + 0.017*SL$
	tF	0.21	$0.20 + 0.007*SL$	$0.20 + 0.007*SL$	$0.21 + 0.006*SL$
C to Y	tPLH	0.81	$0.79 + 0.009*SL$	$0.80 + 0.008*SL$	$0.81 + 0.007*SL$
	tPHL	0.41	$0.39 + 0.009*SL$	$0.40 + 0.006*SL$	$0.43 + 0.005*SL$
	tR	0.24	$0.22 + 0.012*SL$	$0.20 + 0.015*SL$	$0.18 + 0.017*SL$
	tF	0.23	$0.22 + 0.006*SL$	$0.22 + 0.007*SL$	$0.23 + 0.006*SL$
D to Y	tPLH	0.79	$0.77 + 0.009*SL$	$0.78 + 0.008*SL$	$0.79 + 0.007*SL$
	tPHL	0.45	$0.43 + 0.008*SL$	$0.44 + 0.006*SL$	$0.47 + 0.005*SL$
	tR	0.24	$0.22 + 0.011*SL$	$0.20 + 0.016*SL$	$0.18 + 0.017*SL$
	tF	0.23	$0.22 + 0.006*SL$	$0.22 + 0.007*SL$	$0.23 + 0.006*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

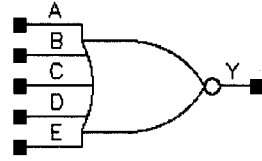


# NR5/NR5D2/NR5D4/NR5D6

5 Input NOR with 1X Drive, 2X Drive, 4X Drive or 6X Drive

Inputs: A, B, C, D, E  
 Output: Y  
 Input Loading (SL): All: 1  
 Maximum Fanout (Rec. SL):  
 - NR5: 2  
 - NR5D2: 56  
 - NR5D4: 112  
 - NR5D6: 168

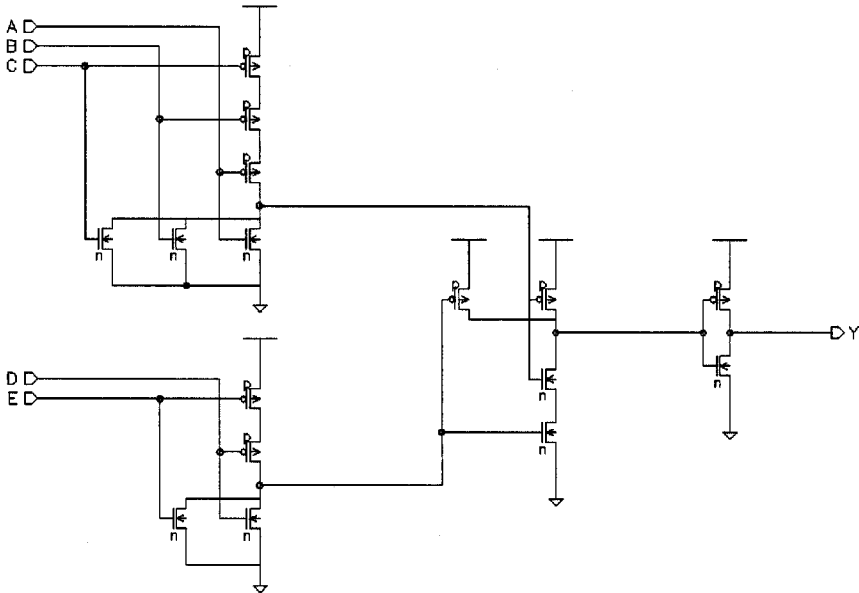
Gate Count  
 NR5: 4  
 NR5D2: 5  
 NR5D4: 6  
 NR5D6: 7



Symbol

A	B	C	D	E	Y
0	0	0	0	0	1
1	x	x	x	x	0
x	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0

Truth Table



Schematic

**NR5 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.81	$0.73 + 0.042*SL$	$0.73 + 0.040*SL$	$0.73 + 0.040*SL$
	tPHL	0.25	$0.19 + 0.026*SL$	$0.21 + 0.020*SL$	$0.22 + 0.020*SL$
	tR	0.30	$0.12 + 0.089*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.16	$0.08 + 0.036*SL$	$0.08 + 0.038*SL$	$0.05 + 0.039*SL$
B to Y	tPLH	0.83	$0.74 + 0.042*SL$	$0.75 + 0.040*SL$	$0.75 + 0.040*SL$
	tPHL	0.28	$0.23 + 0.025*SL$	$0.25 + 0.020*SL$	$0.26 + 0.020*SL$
	tR	0.30	$0.12 + 0.089*SL$	$0.12 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.16	$0.08 + 0.037*SL$	$0.08 + 0.038*SL$	$0.05 + 0.039*SL$
C to Y	tPLH	0.82	$0.73 + 0.042*SL$	$0.74 + 0.040*SL$	$0.74 + 0.040*SL$
	tPHL	0.29	$0.24 + 0.025*SL$	$0.26 + 0.020*SL$	$0.27 + 0.020*SL$
	tR	0.30	$0.12 + 0.089*SL$	$0.12 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.16	$0.09 + 0.035*SL$	$0.08 + 0.038*SL$	$0.06 + 0.039*SL$
D to Y	tPLH	0.66	$0.57 + 0.042*SL$	$0.58 + 0.040*SL$	$0.58 + 0.040*SL$
	tPHL	0.28	$0.22 + 0.028*SL$	$0.24 + 0.021*SL$	$0.26 + 0.020*SL$
	tR	0.29	$0.11 + 0.089*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.18	$0.10 + 0.036*SL$	$0.10 + 0.037*SL$	$0.07 + 0.039*SL$
E to Y	tPLH	0.63	$0.55 + 0.042*SL$	$0.55 + 0.040*SL$	$0.56 + 0.040*SL$
	tPHL	0.32	$0.27 + 0.028*SL$	$0.29 + 0.021*SL$	$0.31 + 0.020*SL$
	tR	0.29	$0.12 + 0.088*SL$	$0.10 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.18	$0.11 + 0.036*SL$	$0.10 + 0.037*SL$	$0.06 + 0.039*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **NR5D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.74	$0.70 + 0.024*SL$	$0.70 + 0.021*SL$	$0.72 + 0.020*SL$
	tPHL	0.26	$0.23 + 0.016*SL$	$0.24 + 0.012*SL$	$0.27 + 0.010*SL$
	tR	0.24	$0.15 + 0.045*SL$	$0.15 + 0.045*SL$	$0.13 + 0.046*SL$
	tF	0.14	$0.11 + 0.017*SL$	$0.11 + 0.018*SL$	$0.09 + 0.019*SL$
B to Y	tPLH	0.72	$0.67 + 0.023*SL$	$0.68 + 0.021*SL$	$0.70 + 0.020*SL$
	tPHL	0.31	$0.27 + 0.016*SL$	$0.29 + 0.012*SL$	$0.32 + 0.010*SL$
	tR	0.24	$0.15 + 0.045*SL$	$0.15 + 0.045*SL$	$0.13 + 0.046*SL$
	tF	0.15	$0.11 + 0.017*SL$	$0.11 + 0.018*SL$	$0.10 + 0.019*SL$
C to Y	tPLH	0.76	$0.72 + 0.023*SL$	$0.73 + 0.021*SL$	$0.74 + 0.020*SL$
	tPHL	0.29	$0.25 + 0.018*SL$	$0.27 + 0.012*SL$	$0.31 + 0.010*SL$
	tR	0.25	$0.16 + 0.045*SL$	$0.15 + 0.045*SL$	$0.13 + 0.046*SL$
	tF	0.17	$0.13 + 0.018*SL$	$0.13 + 0.018*SL$	$0.12 + 0.018*SL$
D to Y	tPLH	0.74	$0.69 + 0.024*SL$	$0.70 + 0.021*SL$	$0.72 + 0.020*SL$
	tPHL	0.33	$0.30 + 0.018*SL$	$0.31 + 0.012*SL$	$0.35 + 0.010*SL$
	tR	0.24	$0.16 + 0.042*SL$	$0.15 + 0.045*SL$	$0.13 + 0.046*SL$
	tF	0.17	$0.13 + 0.019*SL$	$0.13 + 0.018*SL$	$0.12 + 0.018*SL$
E to Y	tPLH	0.63	$0.58 + 0.024*SL$	$0.59 + 0.021*SL$	$0.60 + 0.020*SL$
	tPHL	0.32	$0.28 + 0.019*SL$	$0.30 + 0.013*SL$	$0.35 + 0.010*SL$
	tR	0.24	$0.16 + 0.042*SL$	$0.15 + 0.045*SL$	$0.12 + 0.046*SL$
	tF	0.18	$0.14 + 0.021*SL$	$0.15 + 0.018*SL$	$0.14 + 0.018*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# NR5D4

## 5 Input NOR with 4X Drive

### NR5D4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{rq}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.75	$0.73 + 0.013*SL$	$0.73 + 0.011*SL$	$0.74 + 0.011*SL$
	tPHL	0.31	$0.29 + 0.011*SL$	$0.30 + 0.007*SL$	$0.33 + 0.006*SL$
	tR	0.21	$0.17 + 0.022*SL$	$0.16 + 0.025*SL$	$0.14 + 0.025*SL$
	tF	0.17	$0.15 + 0.010*SL$	$0.16 + 0.010*SL$	$0.15 + 0.010*SL$
B to Y	tPLH	0.73	$0.71 + 0.013*SL$	$0.71 + 0.011*SL$	$0.72 + 0.011*SL$
	tPHL	0.35	$0.33 + 0.011*SL$	$0.34 + 0.008*SL$	$0.37 + 0.006*SL$
	tR	0.21	$0.17 + 0.023*SL$	$0.16 + 0.025*SL$	$0.15 + 0.025*SL$
	tF	0.18	$0.16 + 0.011*SL$	$0.16 + 0.010*SL$	$0.16 + 0.010*SL$
C to Y	tPLH	0.96	$0.93 + 0.013*SL$	$0.94 + 0.011*SL$	$0.95 + 0.011*SL$
	tPHL	0.40	$0.38 + 0.011*SL$	$0.39 + 0.008*SL$	$0.43 + 0.006*SL$
	tR	0.23	$0.19 + 0.021*SL$	$0.18 + 0.024*SL$	$0.16 + 0.025*SL$
	tF	0.20	$0.18 + 0.009*SL$	$0.18 + 0.010*SL$	$0.18 + 0.010*SL$
D to Y	tPLH	0.98	$0.95 + 0.013*SL$	$0.95 + 0.011*SL$	$0.97 + 0.011*SL$
	tPHL	0.44	$0.42 + 0.011*SL$	$0.42 + 0.008*SL$	$0.46 + 0.006*SL$
	tR	0.23	$0.19 + 0.021*SL$	$0.18 + 0.024*SL$	$0.16 + 0.025*SL$
	tF	0.20	$0.18 + 0.010*SL$	$0.18 + 0.010*SL$	$0.18 + 0.010*SL$
E to Y	tPLH	0.97	$0.95 + 0.013*SL$	$0.95 + 0.011*SL$	$0.96 + 0.011*SL$
	tPHL	0.45	$0.43 + 0.011*SL$	$0.44 + 0.008*SL$	$0.48 + 0.006*SL$
	tR	0.23	$0.18 + 0.023*SL$	$0.18 + 0.024*SL$	$0.16 + 0.025*SL$
	tF	0.20	$0.19 + 0.009*SL$	$0.18 + 0.010*SL$	$0.18 + 0.010*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**NR5D6 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

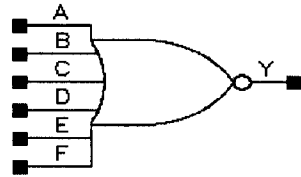
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.83	$0.81 + 0.010*SL$	$0.82 + 0.008*SL$	$0.83 + 0.007*SL$
	tPHL	0.38	$0.36 + 0.008*SL$	$0.37 + 0.006*SL$	$0.39 + 0.005*SL$
	tR	0.24	$0.21 + 0.013*SL$	$0.21 + 0.015*SL$	$0.18 + 0.017*SL$
	tF	0.21	$0.20 + 0.007*SL$	$0.20 + 0.007*SL$	$0.21 + 0.006*SL$
B to Y	tPLH	0.81	$0.79 + 0.010*SL$	$0.79 + 0.008*SL$	$0.80 + 0.007*SL$
	tPHL	0.42	$0.40 + 0.008*SL$	$0.41 + 0.006*SL$	$0.43 + 0.005*SL$
	tR	0.24	$0.21 + 0.013*SL$	$0.21 + 0.015*SL$	$0.18 + 0.017*SL$
	tF	0.21	$0.20 + 0.007*SL$	$0.20 + 0.007*SL$	$0.21 + 0.006*SL$
C to Y	tPLH	1.03	$1.02 + 0.010*SL$	$1.02 + 0.008*SL$	$1.03 + 0.007*SL$
	tPHL	0.46	$0.45 + 0.009*SL$	$0.45 + 0.006*SL$	$0.48 + 0.005*SL$
	tR	0.25	$0.23 + 0.012*SL$	$0.22 + 0.015*SL$	$0.19 + 0.016*SL$
	tF	0.24	$0.22 + 0.006*SL$	$0.22 + 0.007*SL$	$0.23 + 0.006*SL$
D to Y	tPLH	1.05	$1.03 + 0.010*SL$	$1.04 + 0.008*SL$	$1.05 + 0.007*SL$
	tPHL	0.50	$0.48 + 0.009*SL$	$0.49 + 0.006*SL$	$0.52 + 0.005*SL$
	tR	0.25	$0.23 + 0.011*SL$	$0.22 + 0.015*SL$	$0.19 + 0.017*SL$
	tF	0.23	$0.22 + 0.006*SL$	$0.22 + 0.007*SL$	$0.23 + 0.006*SL$
E to Y	tPLH	1.05	$1.03 + 0.009*SL$	$1.03 + 0.008*SL$	$1.04 + 0.007*SL$
	tPHL	0.51	$0.50 + 0.008*SL$	$0.50 + 0.006*SL$	$0.53 + 0.005*SL$
	tR	0.25	$0.23 + 0.011*SL$	$0.22 + 0.015*SL$	$0.19 + 0.016*SL$
	tF	0.24	$0.23 + 0.004*SL$	$0.22 + 0.007*SL$	$0.23 + 0.006*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# NR6/NR6D2

## 6 Input NOR with 1X Drive or 2X Drive

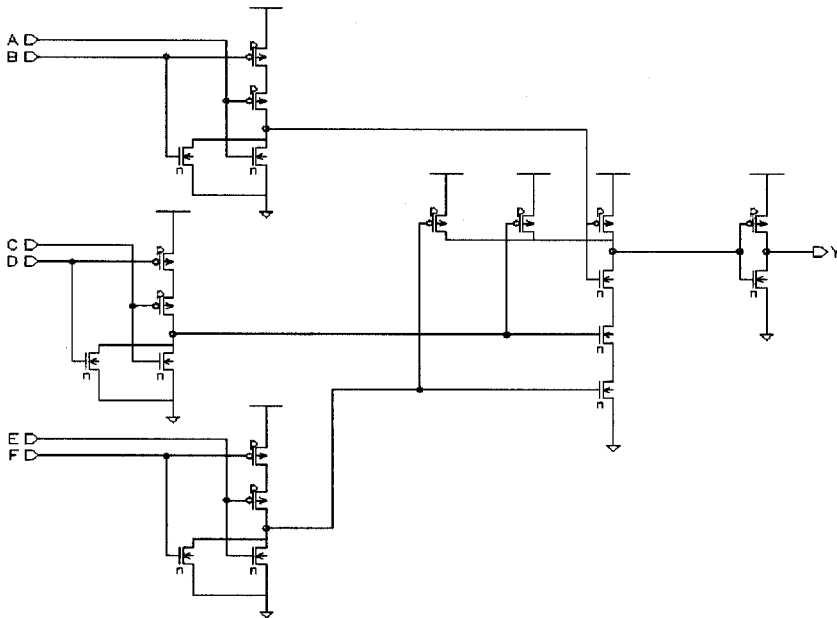
Inputs: A, B, C, D, E, F  
Output: Y  
Input Loading (SL): All : 1  
Maximum Fanout (Rec. SL):  
NR6: 28  
NR6D2: 56  
Gate Count:  
NR6: 5  
NR6D2 : 6



**Symbol**

A	B	C	D	E	F	Y
0	0	0	0	0	0	1
1	x	x	x	x	x	0
x	1	x	x	x	x	0
x	x	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0

**Truth Table**



**Schematic**

**NR6 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{p}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.74	$0.65 + 0.043*SL$	$0.66 + 0.040*SL$	$0.67 + 0.040*SL$
	tPHL	0.25	$0.20 + 0.026*SL$	$0.21 + 0.021*SL$	$0.23 + 0.020*SL$
	tR	0.32	$0.14 + 0.089*SL$	$0.13 + 0.091*SL$	$0.10 + 0.093*SL$
	tF	0.16	$0.09 + 0.035*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
B to Y	tPLH	0.72	$0.63 + 0.043*SL$	$0.64 + 0.040*SL$	$0.65 + 0.040*SL$
	tPHL	0.29	$0.24 + 0.026*SL$	$0.26 + 0.021*SL$	$0.27 + 0.020*SL$
	tR	0.32	$0.14 + 0.088*SL$	$0.13 + 0.091*SL$	$0.10 + 0.093*SL$
	tF	0.16	$0.09 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
C to Y	tPLH	0.77	$0.68 + 0.043*SL$	$0.69 + 0.040*SL$	$0.69 + 0.040*SL$
	tPHL	0.29	$0.23 + 0.029*SL$	$0.26 + 0.021*SL$	$0.28 + 0.020*SL$
	tR	0.32	$0.14 + 0.088*SL$	$0.13 + 0.091*SL$	$0.10 + 0.093*SL$
	tF	0.18	$0.11 + 0.036*SL$	$0.11 + 0.036*SL$	$0.07 + 0.038*SL$
D to Y	tPLH	0.74	$0.65 + 0.044*SL$	$0.67 + 0.040*SL$	$0.67 + 0.040*SL$
	tPHL	0.33	$0.28 + 0.028*SL$	$0.30 + 0.021*SL$	$0.32 + 0.020*SL$
	tR	0.32	$0.14 + 0.088*SL$	$0.13 + 0.091*SL$	$0.10 + 0.093*SL$
	tF	0.18	$0.11 + 0.036*SL$	$0.11 + 0.036*SL$	$0.07 + 0.038*SL$
E to Y	tPLH	0.76	$0.68 + 0.044*SL$	$0.69 + 0.040*SL$	$0.69 + 0.040*SL$
	tPHL	0.32	$0.26 + 0.031*SL$	$0.28 + 0.021*SL$	$0.32 + 0.020*SL$
	tR	0.32	$0.14 + 0.088*SL$	$0.13 + 0.091*SL$	$0.10 + 0.093*SL$
	tF	0.20	$0.13 + 0.035*SL$	$0.13 + 0.036*SL$	$0.09 + 0.038*SL$
F to Y	tPLH	0.74	$0.66 + 0.043*SL$	$0.67 + 0.040*SL$	$0.67 + 0.040*SL$
	tPHL	0.35	$0.29 + 0.031*SL$	$0.32 + 0.021*SL$	$0.35 + 0.020*SL$
	tR	0.32	$0.14 + 0.088*SL$	$0.13 + 0.091*SL$	$0.10 + 0.093*SL$
	tF	0.20	$0.13 + 0.038*SL$	$0.14 + 0.036*SL$	$0.09 + 0.038*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# NR6D2

## 6 Input NOR with 2X Drive

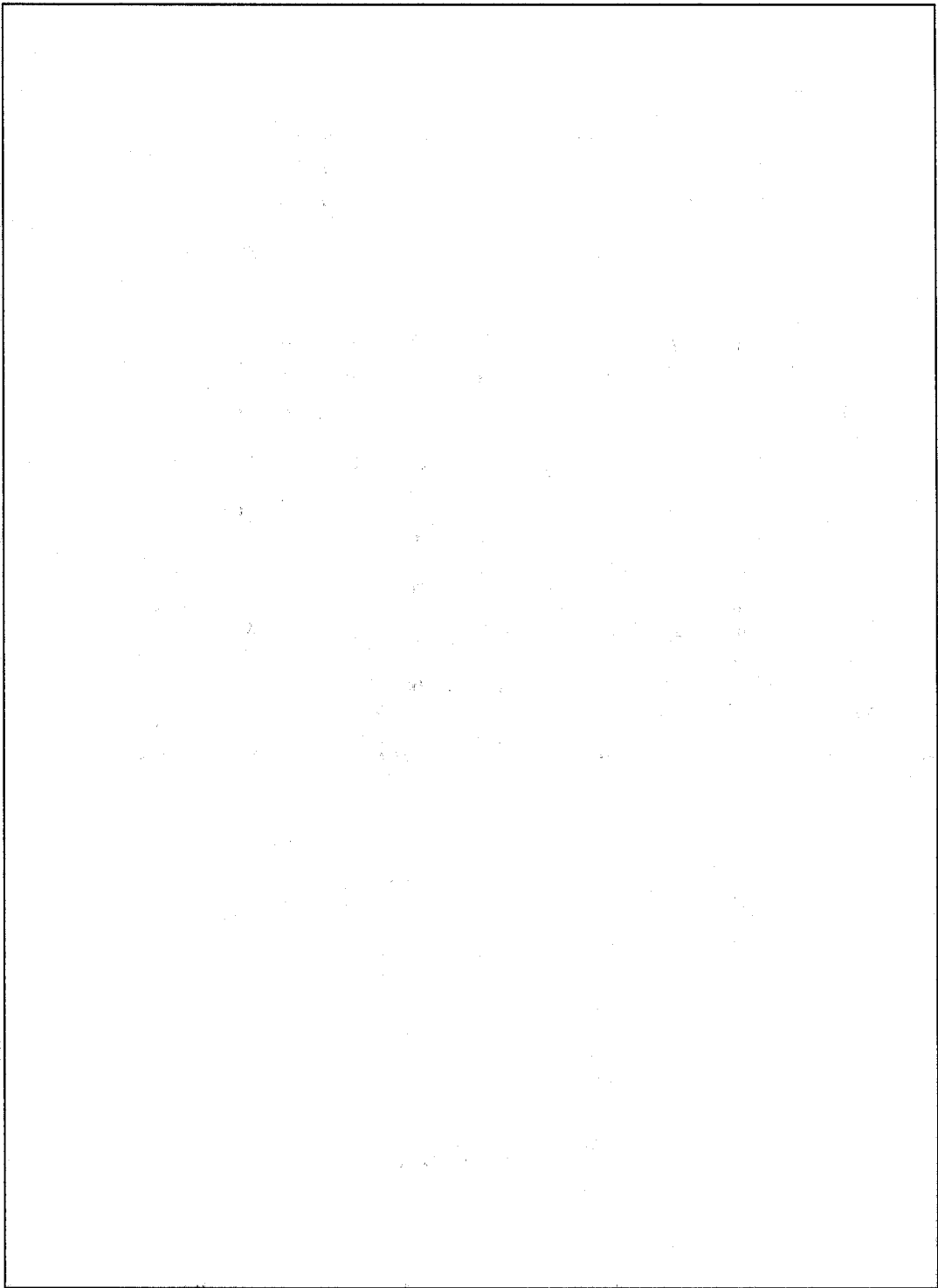
### NR6D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.74	$0.70 + 0.018*SL$	$0.71 + 0.015*SL$	$0.74 + 0.014*SL$
	tPHL	0.30	$0.27 + 0.016*SL$	$0.28 + 0.011*SL$	$0.31 + 0.010*SL$
	tR	0.23	$0.17 + 0.027*SL$	$0.16 + 0.029*SL$	$0.14 + 0.030*SL$
	tF	0.16	$0.13 + 0.017*SL$	$0.13 + 0.018*SL$	$0.11 + 0.019*SL$
B to Y	tPLH	0.72	$0.68 + 0.018*SL$	$0.69 + 0.015*SL$	$0.71 + 0.014*SL$
	tPHL	0.34	$0.31 + 0.015*SL$	$0.32 + 0.011*SL$	$0.35 + 0.010*SL$
	tR	0.23	$0.17 + 0.025*SL$	$0.16 + 0.029*SL$	$0.14 + 0.030*SL$
	tF	0.16	$0.13 + 0.017*SL$	$0.13 + 0.018*SL$	$0.11 + 0.019*SL$
C to Y	tPLH	0.75	$0.72 + 0.018*SL$	$0.73 + 0.015*SL$	$0.75 + 0.014*SL$
	tPHL	0.33	$0.30 + 0.017*SL$	$0.31 + 0.012*SL$	$0.35 + 0.010*SL$
	tR	0.23	$0.18 + 0.026*SL$	$0.17 + 0.029*SL$	$0.15 + 0.030*SL$
	tF	0.18	$0.15 + 0.019*SL$	$0.15 + 0.018*SL$	$0.13 + 0.018*SL$
D to Y	tPLH	0.73	$0.69 + 0.018*SL$	$0.71 + 0.015*SL$	$0.73 + 0.014*SL$
	tPHL	0.37	$0.34 + 0.017*SL$	$0.36 + 0.012*SL$	$0.39 + 0.010*SL$
	tR	0.23	$0.18 + 0.026*SL$	$0.17 + 0.029*SL$	$0.15 + 0.030*SL$
	tF	0.19	$0.16 + 0.015*SL$	$0.15 + 0.018*SL$	$0.14 + 0.018*SL$
E to Y	tPLH	0.76	$0.72 + 0.018*SL$	$0.74 + 0.015*SL$	$0.76 + 0.014*SL$
	tPHL	0.37	$0.33 + 0.018*SL$	$0.35 + 0.012*SL$	$0.39 + 0.010*SL$
	tR	0.23	$0.18 + 0.026*SL$	$0.17 + 0.029*SL$	$0.15 + 0.030*SL$
	tF	0.21	$0.17 + 0.018*SL$	$0.17 + 0.017*SL$	$0.16 + 0.018*SL$
F to Y	tPLH	0.74	$0.70 + 0.018*SL$	$0.71 + 0.015*SL$	$0.74 + 0.014*SL$
	tPHL	0.41	$0.37 + 0.017*SL$	$0.39 + 0.012*SL$	$0.43 + 0.010*SL$
	tR	0.23	$0.18 + 0.026*SL$	$0.17 + 0.029*SL$	$0.15 + 0.030*SL$
	tF	0.21	$0.18 + 0.016*SL$	$0.17 + 0.017*SL$	$0.16 + 0.018*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# NR8/NR8D2

## 8 Input NOR with 1X Drive and 2X Drive

Inputs: A, B, C, D, E, F, G, H

Output: Y

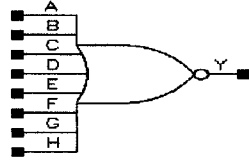
Input Loading (SL): All : 1

Maximum Fanout (Rec. SL): 56

Gate Count:

NR8: 6

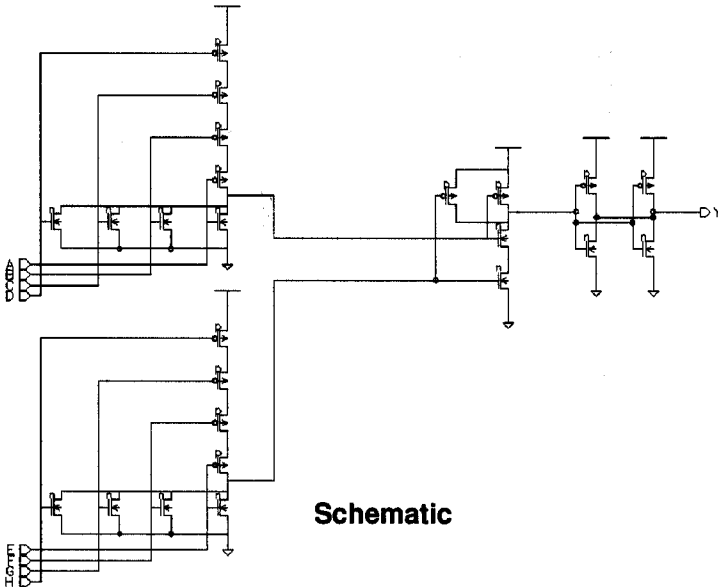
NR8D2: 7



Symbol

A	B	C	D	E	F	G	H	Y
0	0	0	0	0	0	0	0	1
1	x	x	x	x	x	x	x	0
x	1	x	x	x	x	x	x	0
x	x	1	x	x	x	x	x	0
x	x	x	1	x	x	x	x	0
x	x	x	x	1	x	x	x	0
x	x	x	x	x	1	x	x	0
x	x	x	x	x	x	1	x	0
x	x	x	x	x	x	x	1	0

Truth Table



Schematic

**NR8 Switching Characteristics**

Delays for typical process, 25.00°C, 5.00V, when  $t_q$  and  $t_f = 0.80ns$

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.92	$0.88 + 0.022*SL$	$0.89 + 0.020*SL$	$0.89 + 0.020*SL$
	tPHL	0.28	$0.25 + 0.017*SL$	$0.26 + 0.011*SL$	$0.29 + 0.010*SL$
	tR	0.23	$0.14 + 0.044*SL$	$0.14 + 0.045*SL$	$0.11 + 0.047*SL$
	tF	0.14	$0.10 + 0.017*SL$	$0.10 + 0.018*SL$	$0.09 + 0.019*SL$
B to Y	tPLH	0.98	$0.94 + 0.022*SL$	$0.94 + 0.020*SL$	$0.94 + 0.020*SL$
	tPHL	0.32	$0.29 + 0.016*SL$	$0.30 + 0.011*SL$	$0.33 + 0.010*SL$
	tR	0.23	$0.14 + 0.044*SL$	$0.13 + 0.045*SL$	$0.11 + 0.047*SL$
	tF	0.14	$0.10 + 0.021*SL$	$0.11 + 0.018*SL$	$0.09 + 0.019*SL$
C to Y	tPLH	1.01	$0.97 + 0.022*SL$	$0.97 + 0.020*SL$	$0.98 + 0.020*SL$
	tPHL	0.33	$0.30 + 0.016*SL$	$0.31 + 0.011*SL$	$0.34 + 0.010*SL$
	tR	0.23	$0.14 + 0.043*SL$	$0.13 + 0.045*SL$	$0.11 + 0.047*SL$
	tF	0.14	$0.11 + 0.018*SL$	$0.11 + 0.018*SL$	$0.09 + 0.019*SL$
D to Y	tPLH	1.02	$0.98 + 0.022*SL$	$0.98 + 0.020*SL$	$0.99 + 0.020*SL$
	tPHL	0.33	$0.30 + 0.016*SL$	$0.31 + 0.011*SL$	$0.34 + 0.010*SL$
	tR	0.23	$0.14 + 0.043*SL$	$0.13 + 0.045*SL$	$0.11 + 0.047*SL$
	tF	0.14	$0.11 + 0.018*SL$	$0.11 + 0.018*SL$	$0.09 + 0.019*SL$
E to Y	tPLH	0.89	$0.85 + 0.022*SL$	$0.85 + 0.020*SL$	$0.86 + 0.020*SL$
	tPHL	0.32	$0.28 + 0.017*SL$	$0.30 + 0.012*SL$	$0.33 + 0.010*SL$
	tR	0.23	$0.14 + 0.042*SL$	$0.14 + 0.045*SL$	$0.11 + 0.047*SL$
	tF	0.16	$0.12 + 0.020*SL$	$0.13 + 0.018*SL$	$0.11 + 0.018*SL$
F to Y	tPLH	0.94	$0.90 + 0.022*SL$	$0.90 + 0.020*SL$	$0.91 + 0.020*SL$
	tPHL	0.35	$0.32 + 0.017*SL$	$0.33 + 0.012*SL$	$0.37 + 0.010*SL$
	tR	0.23	$0.15 + 0.042*SL$	$0.14 + 0.045*SL$	$0.11 + 0.047*SL$
	tF	0.16	$0.12 + 0.021*SL$	$0.13 + 0.018*SL$	$0.11 + 0.019*SL$
G to Y	tPLH	0.97	$0.93 + 0.022*SL$	$0.93 + 0.020*SL$	$0.94 + 0.020*SL$
	tPHL	0.37	$0.33 + 0.017*SL$	$0.35 + 0.012*SL$	$0.39 + 0.010*SL$
	tR	0.23	$0.15 + 0.043*SL$	$0.14 + 0.045*SL$	$0.11 + 0.047*SL$
	tF	0.16	$0.13 + 0.019*SL$	$0.13 + 0.018*SL$	$0.11 + 0.019*SL$
H to Y	tPLH	0.98	$0.94 + 0.022*SL$	$0.94 + 0.020*SL$	$0.95 + 0.020*SL$
	tPHL	0.37	$0.34 + 0.017*SL$	$0.35 + 0.012*SL$	$0.39 + 0.010*SL$
	tR	0.23	$0.14 + 0.044*SL$	$0.14 + 0.045*SL$	$0.11 + 0.047*SL$
	tF	0.17	$0.13 + 0.017*SL$	$0.13 + 0.018*SL$	$0.11 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# NR8D2

## 8 Input NOR with 2X Drive

### NR8D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.84	$0.79 + 0.027 \cdot SL$	$0.80 + 0.023 \cdot SL$	$0.82 + 0.022 \cdot SL$
	tPHL	0.28	$0.24 + 0.018 \cdot SL$	$0.26 + 0.012 \cdot SL$	$0.30 + 0.010 \cdot SL$
	tR	0.29	$0.20 + 0.046 \cdot SL$	$0.19 + 0.050 \cdot SL$	$0.16 + 0.051 \cdot SL$
	tF	0.16	$0.12 + 0.019 \cdot SL$	$0.12 + 0.018 \cdot SL$	$0.11 + 0.019 \cdot SL$
B to Y	tPLH	0.82	$0.77 + 0.027 \cdot SL$	$0.78 + 0.023 \cdot SL$	$0.80 + 0.022 \cdot SL$
	tPHL	0.32	$0.29 + 0.017 \cdot SL$	$0.30 + 0.012 \cdot SL$	$0.34 + 0.010 \cdot SL$
	tR	0.29	$0.20 + 0.046 \cdot SL$	$0.19 + 0.050 \cdot SL$	$0.16 + 0.051 \cdot SL$
	tF	0.16	$0.12 + 0.019 \cdot SL$	$0.12 + 0.018 \cdot SL$	$0.11 + 0.019 \cdot SL$
C to Y	tPLH	0.86	$0.81 + 0.027 \cdot SL$	$0.82 + 0.023 \cdot SL$	$0.84 + 0.022 \cdot SL$
	tPHL	0.33	$0.29 + 0.019 \cdot SL$	$0.31 + 0.013 \cdot SL$	$0.35 + 0.010 \cdot SL$
	tR	0.30	$0.20 + 0.046 \cdot SL$	$0.19 + 0.050 \cdot SL$	$0.17 + 0.051 \cdot SL$
	tF	0.18	$0.14 + 0.020 \cdot SL$	$0.14 + 0.018 \cdot SL$	$0.14 + 0.018 \cdot SL$
D to Y	tPLH	0.84	$0.79 + 0.027 \cdot SL$	$0.80 + 0.023 \cdot SL$	$0.82 + 0.022 \cdot SL$
	tPHL	0.37	$0.33 + 0.019 \cdot SL$	$0.35 + 0.013 \cdot SL$	$0.40 + 0.010 \cdot SL$
	tR	0.30	$0.21 + 0.045 \cdot SL$	$0.19 + 0.050 \cdot SL$	$0.16 + 0.051 \cdot SL$
	tF	0.18	$0.15 + 0.017 \cdot SL$	$0.14 + 0.018 \cdot SL$	$0.14 + 0.018 \cdot SL$
E to Y	tPLH	0.88	$0.83 + 0.027 \cdot SL$	$0.84 + 0.023 \cdot SL$	$0.86 + 0.022 \cdot SL$
	tPHL	0.36	$0.31 + 0.020 \cdot SL$	$0.34 + 0.013 \cdot SL$	$0.39 + 0.011 \cdot SL$
	tR	0.30	$0.20 + 0.046 \cdot SL$	$0.19 + 0.050 \cdot SL$	$0.16 + 0.051 \cdot SL$
	tF	0.20	$0.17 + 0.016 \cdot SL$	$0.17 + 0.018 \cdot SL$	$0.16 + 0.018 \cdot SL$
F to Y	tPLH	0.86	$0.80 + 0.027 \cdot SL$	$0.81 + 0.023 \cdot SL$	$0.84 + 0.022 \cdot SL$
	tPHL	0.40	$0.36 + 0.020 \cdot SL$	$0.38 + 0.013 \cdot SL$	$0.44 + 0.011 \cdot SL$
	tR	0.30	$0.21 + 0.045 \cdot SL$	$0.19 + 0.050 \cdot SL$	$0.17 + 0.051 \cdot SL$
	tF	0.20	$0.16 + 0.019 \cdot SL$	$0.17 + 0.018 \cdot SL$	$0.16 + 0.018 \cdot SL$
G to Y	tPLH	0.90	$0.85 + 0.027 \cdot SL$	$0.86 + 0.023 \cdot SL$	$0.88 + 0.022 \cdot SL$
	tPHL	0.37	$0.33 + 0.021 \cdot SL$	$0.35 + 0.014 \cdot SL$	$0.42 + 0.011 \cdot SL$
	tR	0.30	$0.21 + 0.045 \cdot SL$	$0.19 + 0.050 \cdot SL$	$0.16 + 0.051 \cdot SL$
	tF	0.22	$0.18 + 0.022 \cdot SL$	$0.19 + 0.018 \cdot SL$	$0.19 + 0.018 \cdot SL$
H to Y	tPLH	0.88	$0.82 + 0.027 \cdot SL$	$0.84 + 0.023 \cdot SL$	$0.86 + 0.022 \cdot SL$
	tPHL	0.41	$0.37 + 0.022 \cdot SL$	$0.39 + 0.014 \cdot SL$	$0.46 + 0.011 \cdot SL$
	tR	0.29	$0.20 + 0.046 \cdot SL$	$0.19 + 0.050 \cdot SL$	$0.17 + 0.051 \cdot SL$
	tF	0.22	$0.18 + 0.022 \cdot SL$	$0.19 + 0.018 \cdot SL$	$0.19 + 0.018 \cdot SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# OA21/OA21D2/OA21D4/OA21D6

2-OR into 2-NAND with 1X Drive, 2X Drive, 4X Drive or 6X Drive

Inputs: A, B, C

Output: Y

Input Loading (SL):

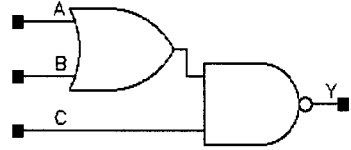
- OA21: All : 1
- OA21D2: All : 2
- OA21D4: All: 1
- OA21D6: All: 1

Maximum Fanout (Rec. SL):

- OA21: 14
- OA21D2: 28
- OA21D4: 112
- OA21D6: 168

Gate Count:

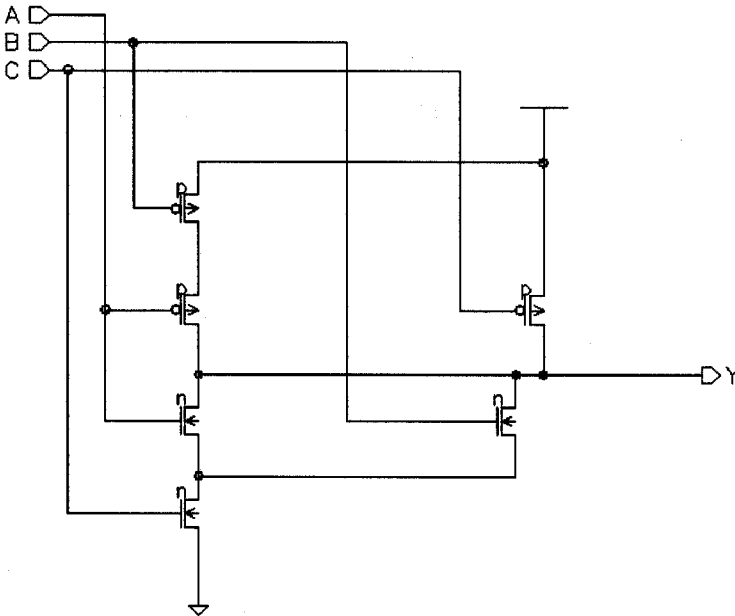
- OA21: 2
- OA21D2: 3
- OA21D4: 4
- OA21D6: 5



Symbol

A	B	C	Y
1	x	1	0
x	1	1	0
0	0	x	1
x	x	0	1

Truth Table



Schematic

**OA21 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_r$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.49	$0.33 + 0.076 * SL$	$0.33 + 0.076 * SL$	$0.30 + 0.078 * SL$
	tPHL	0.17	$0.07 + 0.051 * SL$	$0.12 + 0.034 * SL$	$0.17 + 0.032 * SL$
	tR	0.80	$0.45 + 0.174 * SL$	$0.41 + 0.186 * SL$	$0.34 + 0.190 * SL$
	tF	0.46	$0.33 + 0.065 * SL$	$0.33 + 0.065 * SL$	$0.24 + 0.070 * SL$
B to Y	tPLH	0.46	$0.31 + 0.075 * SL$	$0.30 + 0.076 * SL$	$0.28 + 0.078 * SL$
	tPHL	0.21	$0.11 + 0.048 * SL$	$0.16 + 0.034 * SL$	$0.20 + 0.032 * SL$
	tR	0.80	$0.46 + 0.171 * SL$	$0.42 + 0.186 * SL$	$0.34 + 0.190 * SL$
	tF	0.53	$0.42 + 0.059 * SL$	$0.40 + 0.064 * SL$	$0.30 + 0.069 * SL$
C to Y	tPLH	0.42	$0.34 + 0.043 * SL$	$0.34 + 0.042 * SL$	$0.33 + 0.042 * SL$
	tPHL	0.19	$0.11 + 0.038 * SL$	$0.13 + 0.032 * SL$	$0.15 + 0.032 * SL$
	tR	0.73	$0.57 + 0.083 * SL$	$0.53 + 0.095 * SL$	$0.41 + 0.101 * SL$
	tF	0.47	$0.36 + 0.057 * SL$	$0.33 + 0.066 * SL$	$0.25 + 0.070 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**OA21D2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_r$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.40	$0.33 + 0.039 * SL$	$0.33 + 0.036 * SL$	$0.32 + 0.037 * SL$
	tPHL	0.11	$0.05 + 0.029 * SL$	$0.08 + 0.019 * SL$	$0.15 + 0.016 * SL$
	tR	0.61	$0.45 + 0.082 * SL$	$0.43 + 0.087 * SL$	$0.36 + 0.091 * SL$
	tF	0.38	$0.32 + 0.033 * SL$	$0.33 + 0.030 * SL$	$0.29 + 0.032 * SL$
B to Y	tPLH	0.38	$0.30 + 0.037 * SL$	$0.31 + 0.036 * SL$	$0.29 + 0.037 * SL$
	tPHL	0.15	$0.10 + 0.026 * SL$	$0.12 + 0.018 * SL$	$0.18 + 0.015 * SL$
	tR	0.61	$0.45 + 0.080 * SL$	$0.43 + 0.087 * SL$	$0.36 + 0.091 * SL$
	tF	0.46	$0.40 + 0.029 * SL$	$0.40 + 0.029 * SL$	$0.36 + 0.031 * SL$
C to Y	tPLH	0.37	$0.33 + 0.022 * SL$	$0.33 + 0.020 * SL$	$0.33 + 0.020 * SL$
	tPHL	0.15	$0.11 + 0.020 * SL$	$0.12 + 0.016 * SL$	$0.14 + 0.015 * SL$
	tR	0.62	$0.55 + 0.038 * SL$	$0.54 + 0.042 * SL$	$0.46 + 0.045 * SL$
	tF	0.40	$0.35 + 0.027 * SL$	$0.34 + 0.029 * SL$	$0.29 + 0.032 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# OA21D4/OA21D6

2-OR into 2-NAND with 4X Drive or 6X Drive

## OA21D4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{q}$  and  $t_{f} = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.66	$0.63 + 0.012 * SL$	$0.64 + 0.011 * SL$	$0.64 + 0.011 * SL$
	tPHL	0.41	$0.39 + 0.010 * SL$	$0.40 + 0.007 * SL$	$0.43 + 0.006 * SL$
	tR	0.18	$0.14 + 0.022 * SL$	$0.13 + 0.025 * SL$	$0.11 + 0.026 * SL$
	tF	0.17	$0.16 + 0.009 * SL$	$0.16 + 0.009 * SL$	$0.15 + 0.010 * SL$
B to Y	tPLH	0.63	$0.61 + 0.012 * SL$	$0.61 + 0.011 * SL$	$0.61 + 0.011 * SL$
	tPHL	0.47	$0.45 + 0.010 * SL$	$0.46 + 0.007 * SL$	$0.49 + 0.006 * SL$
	tR	0.18	$0.13 + 0.024 * SL$	$0.13 + 0.025 * SL$	$0.11 + 0.026 * SL$
	tF	0.18	$0.16 + 0.010 * SL$	$0.16 + 0.009 * SL$	$0.15 + 0.010 * SL$
C to Y	tPLH	0.63	$0.60 + 0.011 * SL$	$0.61 + 0.011 * SL$	$0.61 + 0.011 * SL$
	tPHL	0.46	$0.44 + 0.010 * SL$	$0.45 + 0.007 * SL$	$0.48 + 0.006 * SL$
	tR	0.17	$0.13 + 0.022 * SL$	$0.12 + 0.025 * SL$	$0.11 + 0.026 * SL$
	tF	0.17	$0.16 + 0.007 * SL$	$0.15 + 0.009 * SL$	$0.15 + 0.010 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

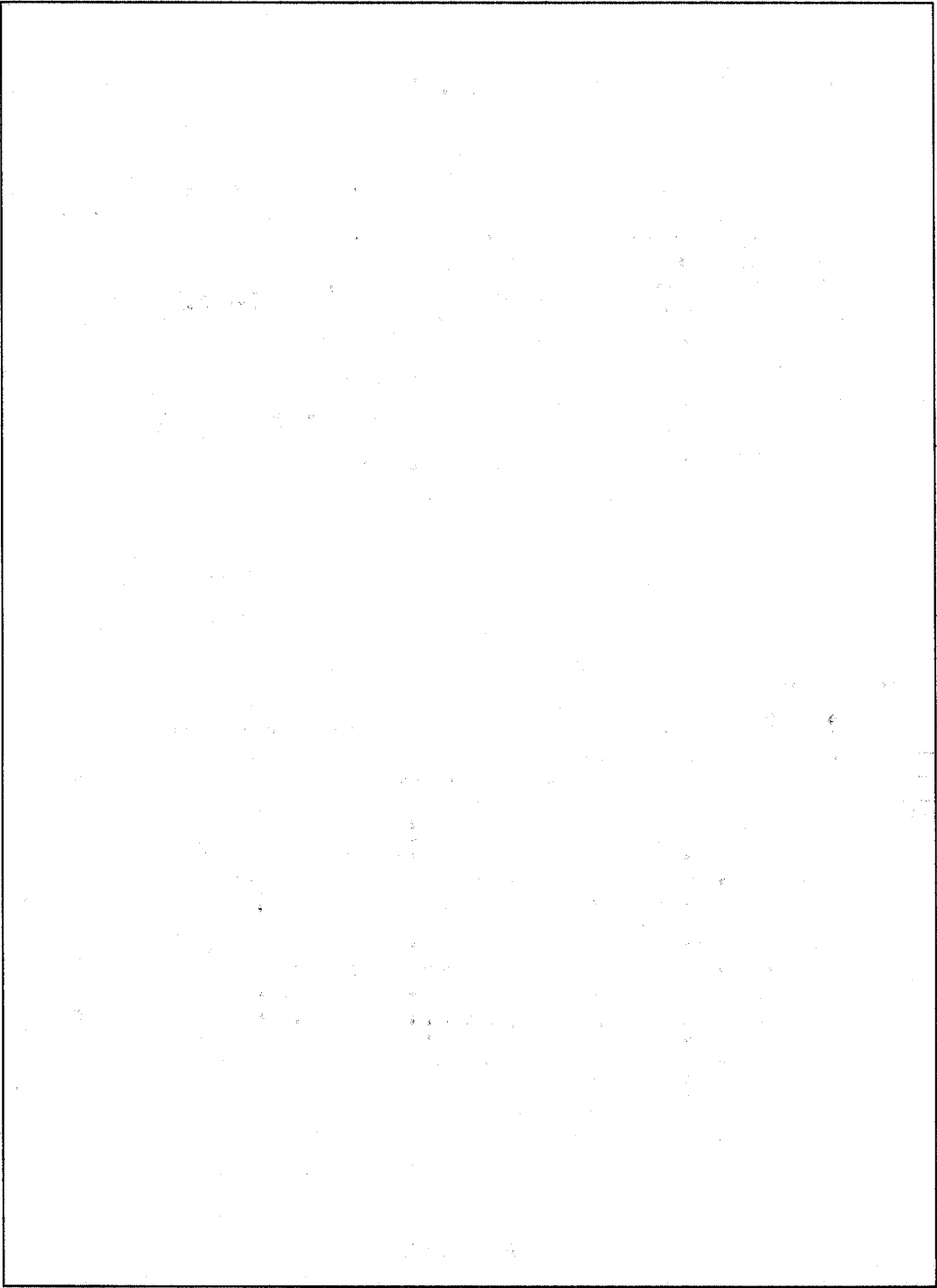
## OA21D6 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{q}$  and  $t_{f} = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.71	$0.69 + 0.008 * SL$	$0.70 + 0.007 * SL$	$0.70 + 0.007 * SL$
	tPHL	0.48	$0.46 + 0.008 * SL$	$0.47 + 0.006 * SL$	$0.49 + 0.005 * SL$
	tR	0.18	$0.15 + 0.015 * SL$	$0.15 + 0.016 * SL$	$0.13 + 0.017 * SL$
	tF	0.21	$0.20 + 0.005 * SL$	$0.20 + 0.006 * SL$	$0.20 + 0.006 * SL$
B to Y	tPLH	0.68	$0.67 + 0.008 * SL$	$0.67 + 0.007 * SL$	$0.68 + 0.007 * SL$
	tPHL	0.54	$0.52 + 0.007 * SL$	$0.53 + 0.006 * SL$	$0.55 + 0.005 * SL$
	tR	0.18	$0.15 + 0.015 * SL$	$0.15 + 0.016 * SL$	$0.13 + 0.017 * SL$
	tF	0.21	$0.21 + 0.004 * SL$	$0.20 + 0.007 * SL$	$0.20 + 0.006 * SL$
C to Y	tPLH	0.68	$0.66 + 0.008 * SL$	$0.66 + 0.007 * SL$	$0.67 + 0.007 * SL$
	tPHL	0.53	$0.51 + 0.008 * SL$	$0.52 + 0.006 * SL$	$0.54 + 0.005 * SL$
	tR	0.18	$0.15 + 0.015 * SL$	$0.15 + 0.016 * SL$	$0.13 + 0.017 * SL$
	tF	0.21	$0.20 + 0.004 * SL$	$0.20 + 0.006 * SL$	$0.20 + 0.006 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# OA21I/OA21ID3/OA21ID5/OA21ID8

2-OR into 2-AND with 1X Drive, 3X Drive, 5X Drive or 8X Drive

Inputs: A, B, C

Output: Y

Input Loading (SL):

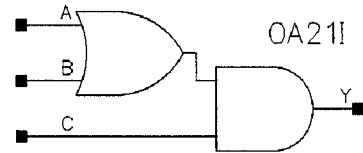
- OA21I: All: 1
- OA21ID3: All: 1
- OA21ID5: All: 1
- OA21ID8: All: 2

Maximum Fanout (Rec. SL):

- OA21I: 28
- OA21ID3: 84
- OA21ID5: 140
- OA21ID8: 224

Gate Count:

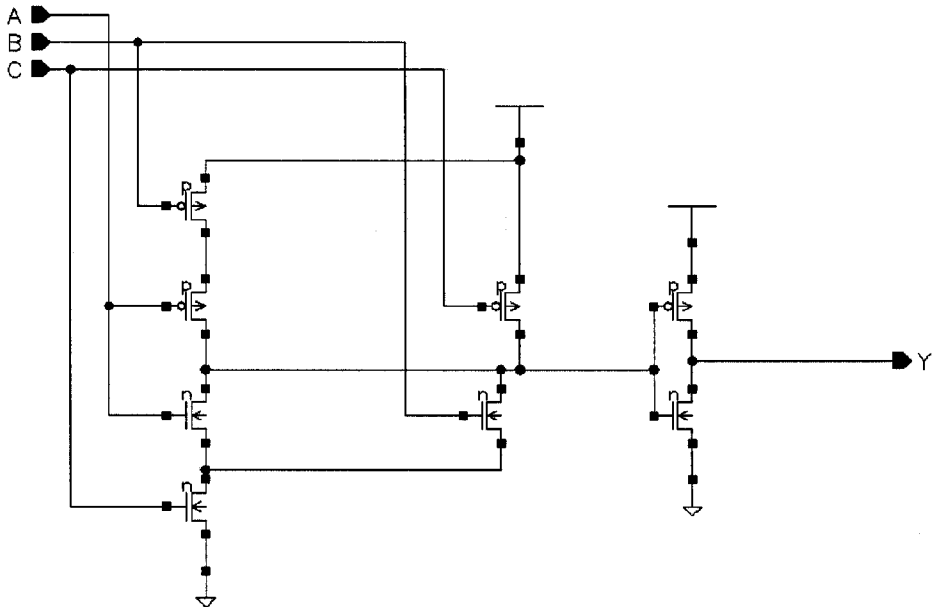
- OA21I: 2
- OA21ID3: 3
- OA21ID5: 5
- OA21ID8: 8



Symbol

A	B	C	Y
1	x	1	0
x	1	1	0
0	0	1	0
x	x	0	1

Truth Table



Schematic

**OA211 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.30	$0.21 + 0.044*SL$	$0.22 + 0.042*SL$	$0.21 + 0.043*SL$
	tPHL	0.49	$0.43 + 0.033*SL$	$0.46 + 0.023*SL$	$0.51 + 0.020*SL$
	tR	0.33	$0.13 + 0.098*SL$	$0.12 + 0.101*SL$	$0.10 + 0.102*SL$
	tF	0.23	$0.15 + 0.037*SL$	$0.16 + 0.036*SL$	$0.13 + 0.037*SL$
B to Y	tPLH	0.36	$0.27 + 0.045*SL$	$0.28 + 0.042*SL$	$0.27 + 0.042*SL$
	tPHL	0.47	$0.40 + 0.033*SL$	$0.43 + 0.023*SL$	$0.49 + 0.020*SL$
	tR	0.34	$0.15 + 0.095*SL$	$0.13 + 0.100*SL$	$0.10 + 0.102*SL$
	tF	0.23	$0.16 + 0.036*SL$	$0.16 + 0.036*SL$	$0.14 + 0.037*SL$
C to Y	tPLH	0.35	$0.26 + 0.044*SL$	$0.27 + 0.042*SL$	$0.26 + 0.043*SL$
	tPHL	0.46	$0.39 + 0.034*SL$	$0.43 + 0.022*SL$	$0.48 + 0.020*SL$
	tR	0.33	$0.14 + 0.095*SL$	$0.13 + 0.100*SL$	$0.10 + 0.102*SL$
	tF	0.24	$0.17 + 0.037*SL$	$0.18 + 0.035*SL$	$0.13 + 0.037*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**OA211D3 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.35	$0.32 + 0.017*SL$	$0.32 + 0.015*SL$	$0.33 + 0.014*SL$
	tPHL	0.57	$0.54 + 0.016*SL$	$0.55 + 0.011*SL$	$0.61 + 0.008*SL$
	tR	0.22	$0.16 + 0.031*SL$	$0.16 + 0.033*SL$	$0.13 + 0.034*SL$
	tF	0.25	$0.22 + 0.015*SL$	$0.23 + 0.012*SL$	$0.24 + 0.012*SL$
B to Y	tPLH	0.40	$0.37 + 0.017*SL$	$0.37 + 0.015*SL$	$0.38 + 0.014*SL$
	tPHL	0.54	$0.51 + 0.016*SL$	$0.52 + 0.011*SL$	$0.58 + 0.008*SL$
	tR	0.23	$0.17 + 0.030*SL$	$0.17 + 0.033*SL$	$0.14 + 0.034*SL$
	tF	0.25	$0.22 + 0.015*SL$	$0.23 + 0.012*SL$	$0.24 + 0.012*SL$
C to Y	tPLH	0.37	$0.34 + 0.016*SL$	$0.34 + 0.015*SL$	$0.35 + 0.014*SL$
	tPHL	0.50	$0.47 + 0.015*SL$	$0.48 + 0.010*SL$	$0.53 + 0.007*SL$
	tR	0.23	$0.17 + 0.031*SL$	$0.17 + 0.033*SL$	$0.14 + 0.034*SL$
	tF	0.22	$0.19 + 0.015*SL$	$0.20 + 0.011*SL$	$0.19 + 0.012*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# OA2ID5/OA21ID8

2-OR into 2-AND with 5X Drive or 8X Drive

## OA21ID5 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.44	$0.42 + 0.011*SL$	$0.42 + 0.009*SL$	$0.44 + 0.009*SL$
	tPHL	0.68	$0.66 + 0.011*SL$	$0.67 + 0.008*SL$	$0.71 + 0.006*SL$
	tR	0.24	$0.21 + 0.016*SL$	$0.20 + 0.019*SL$	$0.18 + 0.020*SL$
	tF	0.32	$0.30 + 0.010*SL$	$0.31 + 0.009*SL$	$0.32 + 0.008*SL$
B to Y	tPLH	0.49	$0.47 + 0.011*SL$	$0.47 + 0.009*SL$	$0.49 + 0.009*SL$
	tPHL	0.65	$0.63 + 0.011*SL$	$0.64 + 0.008*SL$	$0.68 + 0.006*SL$
	tR	0.25	$0.22 + 0.016*SL$	$0.21 + 0.019*SL$	$0.19 + 0.020*SL$
	tF	0.32	$0.30 + 0.010*SL$	$0.31 + 0.008*SL$	$0.32 + 0.008*SL$
C to Y	tPLH	0.45	$0.43 + 0.012*SL$	$0.44 + 0.009*SL$	$0.45 + 0.009*SL$
	tPHL	0.56	$0.54 + 0.010*SL$	$0.54 + 0.007*SL$	$0.58 + 0.006*SL$
	tR	0.25	$0.22 + 0.015*SL$	$0.21 + 0.019*SL$	$0.19 + 0.020*SL$
	tF	0.25	$0.23 + 0.008*SL$	$0.23 + 0.008*SL$	$0.24 + 0.007*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

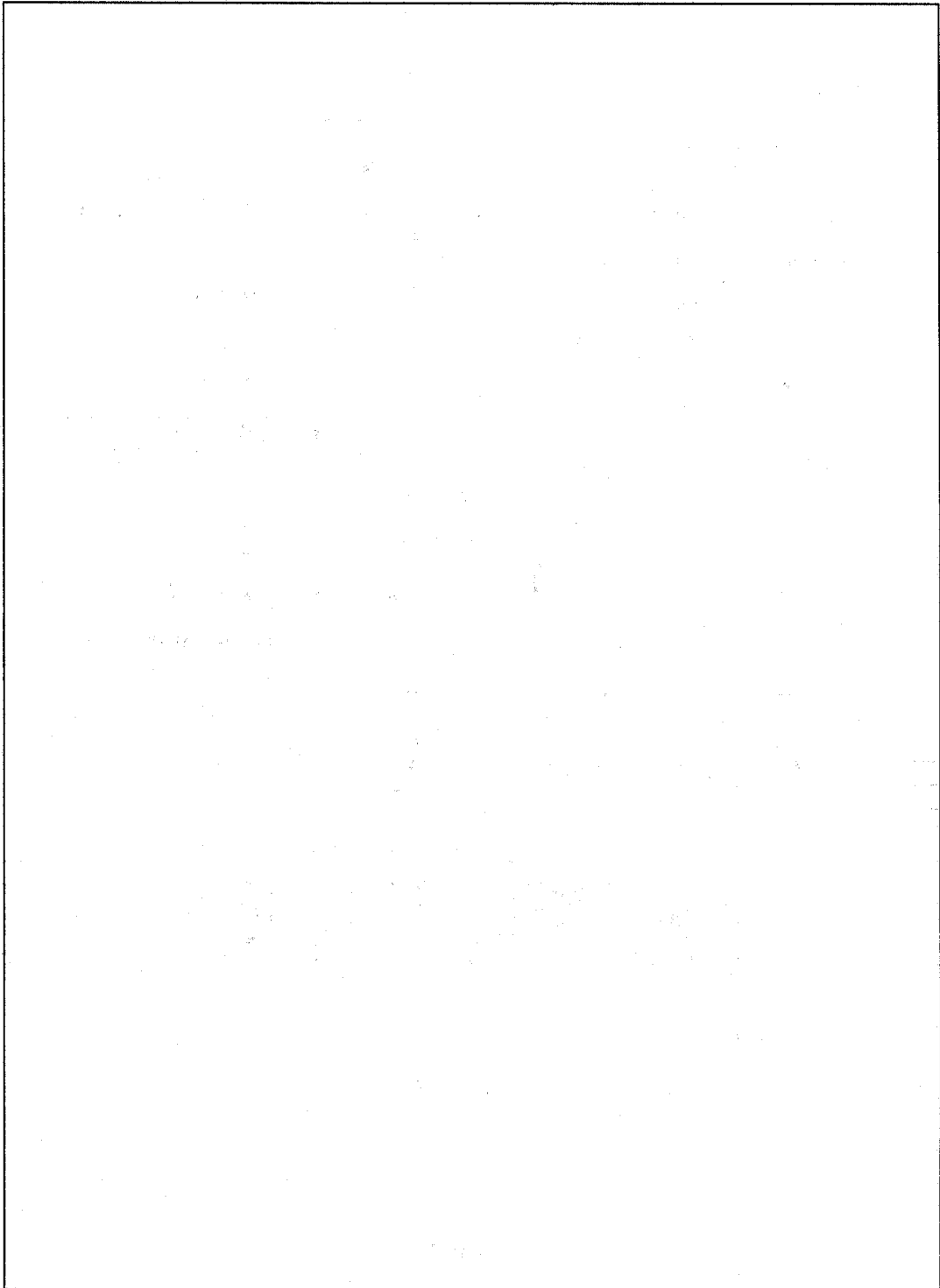
## OA21ID8 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.39	$0.38 + 0.007*SL$	$0.38 + 0.006*SL$	$0.39 + 0.006*SL$
	tPHL	0.64	$0.62 + 0.007*SL$	$0.63 + 0.006*SL$	$0.65 + 0.004*SL$
	tR	0.21	$0.20 + 0.010*SL$	$0.19 + 0.012*SL$	$0.18 + 0.012*SL$
	tF	0.29	$0.28 + 0.005*SL$	$0.28 + 0.006*SL$	$0.29 + 0.005*SL$
B to Y	tPLH	0.44	$0.43 + 0.007*SL$	$0.43 + 0.006*SL$	$0.44 + 0.006*SL$
	tPHL	0.61	$0.59 + 0.007*SL$	$0.60 + 0.006*SL$	$0.62 + 0.004*SL$
	tR	0.23	$0.21 + 0.010*SL$	$0.20 + 0.012*SL$	$0.19 + 0.012*SL$
	tF	0.29	$0.29 + 0.004*SL$	$0.28 + 0.006*SL$	$0.30 + 0.005*SL$
C to Y	tPLH	0.41	$0.40 + 0.008*SL$	$0.40 + 0.006*SL$	$0.41 + 0.006*SL$
	tPHL	0.52	$0.50 + 0.007*SL$	$0.51 + 0.005*SL$	$0.53 + 0.004*SL$
	tR	0.23	$0.21 + 0.010*SL$	$0.20 + 0.011*SL$	$0.19 + 0.012*SL$
	tF	0.23	$0.21 + 0.008*SL$	$0.22 + 0.005*SL$	$0.22 + 0.005*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$





**OA211 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.50	$0.34 + 0.077*SL$	$0.34 + 0.077*SL$	$0.32 + 0.078*SL$
	tPHL	0.25	$0.14 + 0.056*SL$	$0.17 + 0.044*SL$	$0.19 + 0.043*SL$
	tR	0.87	$0.52 + 0.173*SL$	$0.49 + 0.186*SL$	$0.41 + 0.190*SL$
	tF	0.60	$0.42 + 0.089*SL$	$0.41 + 0.094*SL$	$0.30 + 0.099*SL$
B to Y	tPLH	0.47	$0.32 + 0.076*SL$	$0.32 + 0.077*SL$	$0.30 + 0.078*SL$
	tPHL	0.29	$0.19 + 0.053*SL$	$0.22 + 0.043*SL$	$0.23 + 0.043*SL$
	tR	0.87	$0.52 + 0.173*SL$	$0.48 + 0.186*SL$	$0.41 + 0.190*SL$
	tF	0.69	$0.52 + 0.085*SL$	$0.50 + 0.093*SL$	$0.38 + 0.099*SL$
C to Y	tPLH	0.42	$0.33 + 0.044*SL$	$0.34 + 0.042*SL$	$0.34 + 0.042*SL$
	tPHL	0.30	$0.21 + 0.047*SL$	$0.22 + 0.043*SL$	$0.22 + 0.043*SL$
	tR	0.77	$0.60 + 0.082*SL$	$0.56 + 0.095*SL$	$0.44 + 0.101*SL$
	tF	0.64	$0.47 + 0.086*SL$	$0.44 + 0.095*SL$	$0.36 + 0.099*SL$
D to Y	tPLH	0.47	$0.38 + 0.043*SL$	$0.38 + 0.042*SL$	$0.38 + 0.042*SL$
	tPHL	0.27	$0.18 + 0.046*SL$	$0.19 + 0.043*SL$	$0.19 + 0.043*SL$
	tR	0.85	$0.69 + 0.082*SL$	$0.65 + 0.094*SL$	$0.52 + 0.101*SL$
	tF	0.62	$0.44 + 0.086*SL$	$0.41 + 0.096*SL$	$0.35 + 0.100*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**OA211D2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.43	$0.35 + 0.041*SL$	$0.35 + 0.039*SL$	$0.34 + 0.040*SL$
	tPHL	0.19	$0.13 + 0.031*SL$	$0.15 + 0.024*SL$	$0.20 + 0.021*SL$
	tR	0.72	$0.54 + 0.087*SL$	$0.53 + 0.093*SL$	$0.45 + 0.097*SL$
	tF	0.52	$0.43 + 0.044*SL$	$0.42 + 0.046*SL$	$0.37 + 0.049*SL$
B to Y	tPLH	0.40	$0.32 + 0.040*SL$	$0.32 + 0.039*SL$	$0.31 + 0.040*SL$
	tPHL	0.24	$0.19 + 0.029*SL$	$0.20 + 0.023*SL$	$0.24 + 0.021*SL$
	tR	0.72	$0.55 + 0.085*SL$	$0.52 + 0.094*SL$	$0.46 + 0.097*SL$
	tF	0.62	$0.53 + 0.042*SL$	$0.52 + 0.045*SL$	$0.46 + 0.048*SL$
C to Y	tPLH	0.37	$0.32 + 0.023*SL$	$0.33 + 0.020*SL$	$0.33 + 0.020*SL$
	tPHL	0.26	$0.21 + 0.024*SL$	$0.22 + 0.022*SL$	$0.23 + 0.021*SL$
	tR	0.67	$0.59 + 0.037*SL$	$0.58 + 0.042*SL$	$0.50 + 0.045*SL$
	tF	0.56	$0.48 + 0.042*SL$	$0.47 + 0.046*SL$	$0.41 + 0.049*SL$
D to Y	tPLH	0.41	$0.36 + 0.021*SL$	$0.37 + 0.020*SL$	$0.37 + 0.020*SL$
	tPHL	0.23	$0.18 + 0.023*SL$	$0.18 + 0.022*SL$	$0.19 + 0.021*SL$
	tR	0.75	$0.68 + 0.035*SL$	$0.66 + 0.040*SL$	$0.58 + 0.044*SL$
	tF	0.54	$0.45 + 0.042*SL$	$0.44 + 0.047*SL$	$0.38 + 0.050*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# OA211D3/OA211D7

2-OR into 3-NAND with 3X Drive or 7X Drive

## OA211D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.64	$0.61 + 0.015 \cdot \text{SL}$	$0.62 + 0.014 \cdot \text{SL}$	$0.62 + 0.014 \cdot \text{SL}$
	tPHL	0.48	$0.46 + 0.013 \cdot \text{SL}$	$0.47 + 0.009 \cdot \text{SL}$	$0.50 + 0.007 \cdot \text{SL}$
	tR	0.19	$0.12 + 0.031 \cdot \text{SL}$	$0.12 + 0.033 \cdot \text{SL}$	$0.10 + 0.034 \cdot \text{SL}$
	tF	0.16	$0.14 + 0.012 \cdot \text{SL}$	$0.14 + 0.013 \cdot \text{SL}$	$0.13 + 0.013 \cdot \text{SL}$
B to Y	tPLH	0.62	$0.59 + 0.015 \cdot \text{SL}$	$0.59 + 0.014 \cdot \text{SL}$	$0.59 + 0.014 \cdot \text{SL}$
	tPHL	0.56	$0.53 + 0.012 \cdot \text{SL}$	$0.54 + 0.009 \cdot \text{SL}$	$0.57 + 0.007 \cdot \text{SL}$
	tR	0.19	$0.12 + 0.032 \cdot \text{SL}$	$0.12 + 0.033 \cdot \text{SL}$	$0.10 + 0.034 \cdot \text{SL}$
	tF	0.17	$0.14 + 0.011 \cdot \text{SL}$	$0.14 + 0.012 \cdot \text{SL}$	$0.13 + 0.013 \cdot \text{SL}$
C to Y	tPLH	0.61	$0.58 + 0.015 \cdot \text{SL}$	$0.58 + 0.014 \cdot \text{SL}$	$0.58 + 0.014 \cdot \text{SL}$
	tPHL	0.57	$0.55 + 0.012 \cdot \text{SL}$	$0.56 + 0.009 \cdot \text{SL}$	$0.59 + 0.007 \cdot \text{SL}$
	tR	0.18	$0.12 + 0.031 \cdot \text{SL}$	$0.11 + 0.034 \cdot \text{SL}$	$0.10 + 0.034 \cdot \text{SL}$
	tF	0.17	$0.14 + 0.012 \cdot \text{SL}$	$0.14 + 0.013 \cdot \text{SL}$	$0.13 + 0.013 \cdot \text{SL}$
D to Y	tPLH	0.66	$0.63 + 0.015 \cdot \text{SL}$	$0.63 + 0.014 \cdot \text{SL}$	$0.63 + 0.014 \cdot \text{SL}$
	tPHL	0.54	$0.52 + 0.012 \cdot \text{SL}$	$0.53 + 0.009 \cdot \text{SL}$	$0.56 + 0.007 \cdot \text{SL}$
	tR	0.19	$0.12 + 0.032 \cdot \text{SL}$	$0.12 + 0.033 \cdot \text{SL}$	$0.10 + 0.034 \cdot \text{SL}$
	tF	0.17	$0.14 + 0.014 \cdot \text{SL}$	$0.14 + 0.012 \cdot \text{SL}$	$0.13 + 0.013 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

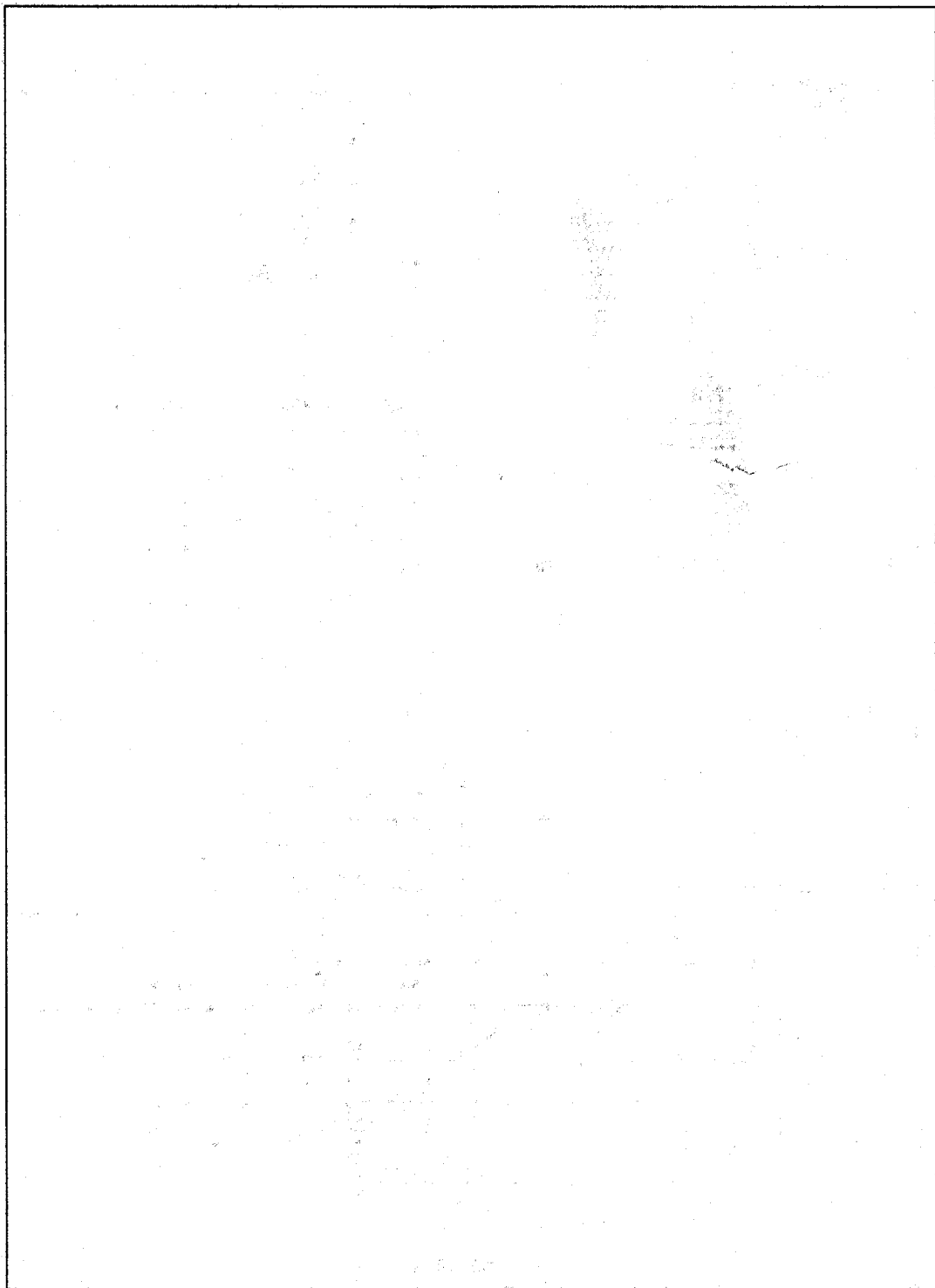
## OA211D7 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.74	$0.73 + 0.007 \cdot \text{SL}$	$0.73 + 0.006 \cdot \text{SL}$	$0.74 + 0.006 \cdot \text{SL}$
	tPHL	0.62	$0.60 + 0.007 \cdot \text{SL}$	$0.61 + 0.005 \cdot \text{SL}$	$0.63 + 0.004 \cdot \text{SL}$
	tR	0.18	$0.16 + 0.012 \cdot \text{SL}$	$0.16 + 0.013 \cdot \text{SL}$	$0.14 + 0.014 \cdot \text{SL}$
	tF	0.24	$0.23 + 0.006 \cdot \text{SL}$	$0.23 + 0.006 \cdot \text{SL}$	$0.23 + 0.005 \cdot \text{SL}$
B to Y	tPLH	0.72	$0.70 + 0.007 \cdot \text{SL}$	$0.71 + 0.006 \cdot \text{SL}$	$0.71 + 0.006 \cdot \text{SL}$
	tPHL	0.69	$0.68 + 0.006 \cdot \text{SL}$	$0.68 + 0.005 \cdot \text{SL}$	$0.70 + 0.004 \cdot \text{SL}$
	tR	0.18	$0.16 + 0.011 \cdot \text{SL}$	$0.15 + 0.014 \cdot \text{SL}$	$0.14 + 0.014 \cdot \text{SL}$
	tF	0.24	$0.23 + 0.007 \cdot \text{SL}$	$0.23 + 0.006 \cdot \text{SL}$	$0.24 + 0.005 \cdot \text{SL}$
C to Y	tPLH	0.70	$0.69 + 0.008 \cdot \text{SL}$	$0.69 + 0.006 \cdot \text{SL}$	$0.69 + 0.006 \cdot \text{SL}$
	tPHL	0.71	$0.69 + 0.008 \cdot \text{SL}$	$0.70 + 0.005 \cdot \text{SL}$	$0.72 + 0.004 \cdot \text{SL}$
	tR	0.18	$0.16 + 0.012 \cdot \text{SL}$	$0.15 + 0.014 \cdot \text{SL}$	$0.14 + 0.014 \cdot \text{SL}$
	tF	0.24	$0.24 + 0.003 \cdot \text{SL}$	$0.23 + 0.006 \cdot \text{SL}$	$0.24 + 0.005 \cdot \text{SL}$
D to Y	tPLH	0.75	$0.74 + 0.007 \cdot \text{SL}$	$0.74 + 0.006 \cdot \text{SL}$	$0.75 + 0.006 \cdot \text{SL}$
	tPHL	0.68	$0.66 + 0.006 \cdot \text{SL}$	$0.67 + 0.005 \cdot \text{SL}$	$0.69 + 0.004 \cdot \text{SL}$
	tR	0.18	$0.16 + 0.013 \cdot \text{SL}$	$0.16 + 0.014 \cdot \text{SL}$	$0.14 + 0.014 \cdot \text{SL}$
	tF	0.24	$0.22 + 0.007 \cdot \text{SL}$	$0.23 + 0.005 \cdot \text{SL}$	$0.24 + 0.005 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$



# OA22/OA22D2/OA22D3/OA22D7

2 2-OR into 2-NAND with 1X Drive, 2X Drive, 3X Drive or 7X Drive

Inputs: A, B, C, D

Outputs: Y

Input Loading (SL):

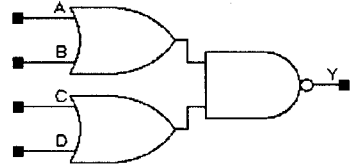
- OA22: All : 1
- OA22D2: All : 2
- OA22D3: All: 1
- OA22D7: All: 1

Maximum Fanout (Rec. SL):

- OA22: 14
- OA22D2: 28
- OA22D3: 84
- OA22D7: 196

Gate Count:

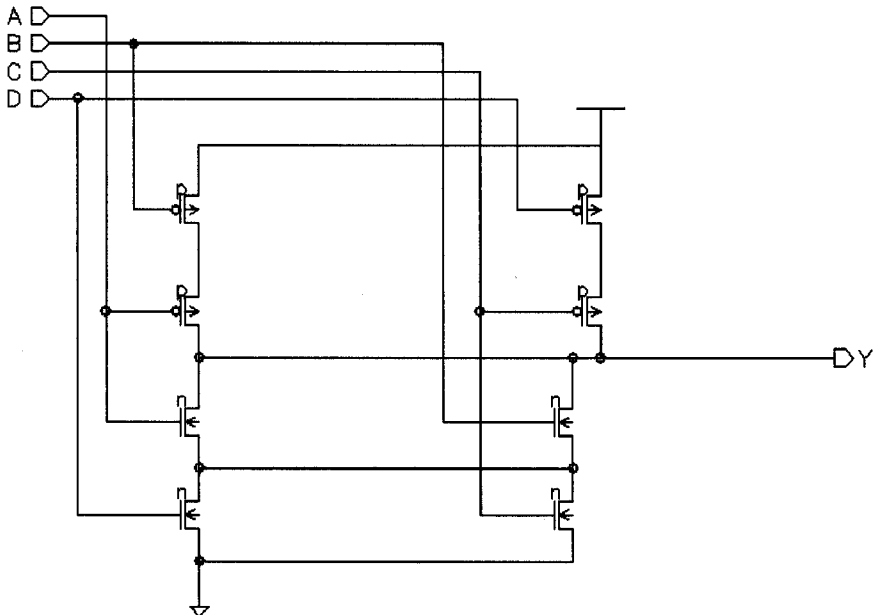
- OA22: 2
- OA22D2: 4
- OA22D3: 4
- OA22D7: 6



**Symbol**

A	B	C	D	Y
0	0	x	x	1
x	x	0	0	1
1	x	x	1	0
x	1	x	1	0
1	x	1	x	0
x	1	1	x	0

**Truth Table**



**Schematic**

**OA22 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{rj}$  and  $t_{fj}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.52	$0.37 + 0.078 \cdot SL$	$0.37 + 0.077 \cdot SL$	$0.35 + 0.078 \cdot SL$
	tPHL	0.20	$0.11 + 0.045 \cdot SL$	$0.15 + 0.032 \cdot SL$	$0.19 + 0.030 \cdot SL$
	tR	0.99	$0.64 + 0.174 \cdot SL$	$0.61 + 0.186 \cdot SL$	$0.53 + 0.190 \cdot SL$
	tF	0.48	$0.36 + 0.057 \cdot SL$	$0.36 + 0.059 \cdot SL$	$0.28 + 0.063 \cdot SL$
B to Y	tPLH	0.49	$0.34 + 0.076 \cdot SL$	$0.34 + 0.077 \cdot SL$	$0.32 + 0.078 \cdot SL$
	tPHL	0.24	$0.15 + 0.042 \cdot SL$	$0.18 + 0.032 \cdot SL$	$0.22 + 0.030 \cdot SL$
	tR	1.00	$0.65 + 0.172 \cdot SL$	$0.61 + 0.186 \cdot SL$	$0.53 + 0.190 \cdot SL$
	tF	0.54	$0.43 + 0.054 \cdot SL$	$0.42 + 0.058 \cdot SL$	$0.33 + 0.063 \cdot SL$
C to Y	tPLH	0.66	$0.51 + 0.075 \cdot SL$	$0.51 + 0.076 \cdot SL$	$0.48 + 0.078 \cdot SL$
	tPHL	0.18	$0.10 + 0.039 \cdot SL$	$0.12 + 0.031 \cdot SL$	$0.15 + 0.030 \cdot SL$
	tR	1.20	$0.86 + 0.174 \cdot SL$	$0.82 + 0.186 \cdot SL$	$0.75 + 0.190 \cdot SL$
	tF	0.44	$0.34 + 0.054 \cdot SL$	$0.32 + 0.061 \cdot SL$	$0.24 + 0.065 \cdot SL$
D to Y	tPLH	0.63	$0.48 + 0.074 \cdot SL$	$0.48 + 0.076 \cdot SL$	$0.45 + 0.078 \cdot SL$
	tPHL	0.21	$0.13 + 0.038 \cdot SL$	$0.15 + 0.031 \cdot SL$	$0.17 + 0.030 \cdot SL$
	tR	1.22	$0.87 + 0.173 \cdot SL$	$0.83 + 0.186 \cdot SL$	$0.75 + 0.190 \cdot SL$
	tF	0.50	$0.39 + 0.053 \cdot SL$	$0.37 + 0.060 \cdot SL$	$0.29 + 0.064 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**OA22D2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{rj}$  and  $t_{fj}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.43	$0.35 + 0.039 \cdot SL$	$0.36 + 0.037 \cdot SL$	$0.35 + 0.037 \cdot SL$
	tPHL	0.16	$0.11 + 0.025 \cdot SL$	$0.13 + 0.018 \cdot SL$	$0.19 + 0.016 \cdot SL$
	tR	0.80	$0.64 + 0.082 \cdot SL$	$0.63 + 0.087 \cdot SL$	$0.55 + 0.091 \cdot SL$
	tF	0.43	$0.36 + 0.032 \cdot SL$	$0.37 + 0.031 \cdot SL$	$0.34 + 0.032 \cdot SL$
B to Y	tPLH	0.41	$0.33 + 0.038 \cdot SL$	$0.33 + 0.037 \cdot SL$	$0.32 + 0.038 \cdot SL$
	tPHL	0.20	$0.15 + 0.023 \cdot SL$	$0.17 + 0.018 \cdot SL$	$0.22 + 0.015 \cdot SL$
	tR	0.81	$0.65 + 0.080 \cdot SL$	$0.63 + 0.087 \cdot SL$	$0.55 + 0.091 \cdot SL$
	tF	0.50	$0.44 + 0.028 \cdot SL$	$0.44 + 0.029 \cdot SL$	$0.40 + 0.031 \cdot SL$
C to Y	tPLH	0.58	$0.51 + 0.037 \cdot SL$	$0.51 + 0.037 \cdot SL$	$0.49 + 0.038 \cdot SL$
	tPHL	0.14	$0.10 + 0.021 \cdot SL$	$0.11 + 0.017 \cdot SL$	$0.15 + 0.015 \cdot SL$
	tR	1.02	$0.86 + 0.082 \cdot SL$	$0.84 + 0.088 \cdot SL$	$0.76 + 0.091 \cdot SL$
	tF	0.39	$0.34 + 0.028 \cdot SL$	$0.33 + 0.030 \cdot SL$	$0.29 + 0.032 \cdot SL$
D to Y	tPLH	0.55	$0.48 + 0.036 \cdot SL$	$0.47 + 0.037 \cdot SL$	$0.46 + 0.038 \cdot SL$
	tPHL	0.18	$0.13 + 0.020 \cdot SL$	$0.15 + 0.017 \cdot SL$	$0.17 + 0.015 \cdot SL$
	tR	1.03	$0.87 + 0.081 \cdot SL$	$0.85 + 0.087 \cdot SL$	$0.78 + 0.091 \cdot SL$
	tF	0.45	$0.40 + 0.026 \cdot SL$	$0.39 + 0.029 \cdot SL$	$0.34 + 0.032 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# OA22D3/OA22D7

2 2-OR into 2-NAND with 3X Drive or 7X Drive

## OA22D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.67	$0.64 + 0.015 * SL$	$0.64 + 0.014 * SL$	$0.64 + 0.014 * SL$
	tPHL	0.45	$0.42 + 0.012 * SL$	$0.43 + 0.009 * SL$	$0.46 + 0.007 * SL$
	tR	0.19	$0.13 + 0.031 * SL$	$0.12 + 0.033 * SL$	$0.10 + 0.034 * SL$
	tF	0.16	$0.14 + 0.012 * SL$	$0.13 + 0.013 * SL$	$0.13 + 0.013 * SL$
B to Y	tPLH	0.65	$0.61 + 0.015 * SL$	$0.62 + 0.014 * SL$	$0.62 + 0.014 * SL$
	tPHL	0.50	$0.48 + 0.012 * SL$	$0.49 + 0.009 * SL$	$0.52 + 0.007 * SL$
	tR	0.19	$0.13 + 0.029 * SL$	$0.12 + 0.033 * SL$	$0.10 + 0.034 * SL$
	tF	0.16	$0.14 + 0.012 * SL$	$0.13 + 0.013 * SL$	$0.13 + 0.013 * SL$
C to Y	tPLH	0.82	$0.79 + 0.015 * SL$	$0.79 + 0.014 * SL$	$0.79 + 0.014 * SL$
	tPHL	0.43	$0.41 + 0.012 * SL$	$0.42 + 0.009 * SL$	$0.45 + 0.007 * SL$
	tR	0.20	$0.14 + 0.031 * SL$	$0.13 + 0.033 * SL$	$0.11 + 0.034 * SL$
	tF	0.16	$0.13 + 0.012 * SL$	$0.13 + 0.013 * SL$	$0.12 + 0.013 * SL$
D to Y	tPLH	0.79	$0.76 + 0.015 * SL$	$0.76 + 0.014 * SL$	$0.76 + 0.014 * SL$
	tPHL	0.48	$0.46 + 0.012 * SL$	$0.47 + 0.009 * SL$	$0.50 + 0.007 * SL$
	tR	0.20	$0.14 + 0.032 * SL$	$0.13 + 0.033 * SL$	$0.11 + 0.034 * SL$
	tF	0.16	$0.14 + 0.011 * SL$	$0.13 + 0.013 * SL$	$0.13 + 0.013 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

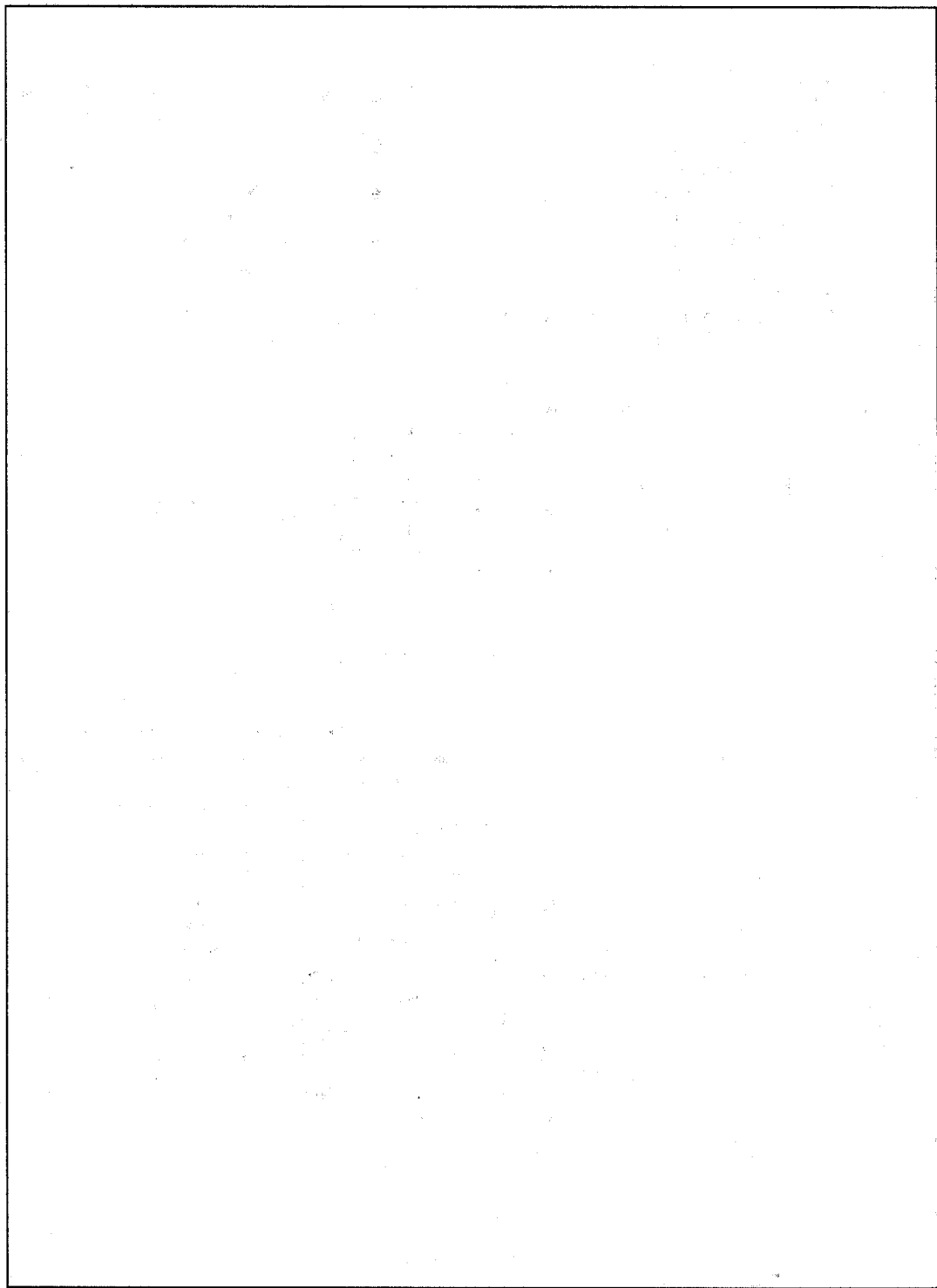
## OA22D7 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.79	$0.78 + 0.007 * SL$	$0.78 + 0.006 * SL$	$0.79 + 0.006 * SL$
	tPHL	0.58	$0.56 + 0.006 * SL$	$0.57 + 0.005 * SL$	$0.59 + 0.004 * SL$
	tR	0.19	$0.17 + 0.012 * SL$	$0.17 + 0.013 * SL$	$0.15 + 0.014 * SL$
	tF	0.23	$0.22 + 0.006 * SL$	$0.22 + 0.006 * SL$	$0.23 + 0.005 * SL$
B to Y	tPLH	0.76	$0.75 + 0.007 * SL$	$0.75 + 0.006 * SL$	$0.76 + 0.006 * SL$
	tPHL	0.63	$0.62 + 0.007 * SL$	$0.62 + 0.005 * SL$	$0.65 + 0.004 * SL$
	tR	0.19	$0.17 + 0.012 * SL$	$0.17 + 0.013 * SL$	$0.15 + 0.014 * SL$
	tF	0.23	$0.22 + 0.006 * SL$	$0.22 + 0.006 * SL$	$0.23 + 0.005 * SL$
C to Y	tPLH	0.95	$0.93 + 0.007 * SL$	$0.94 + 0.006 * SL$	$0.94 + 0.006 * SL$
	tPHL	0.56	$0.55 + 0.006 * SL$	$0.55 + 0.005 * SL$	$0.58 + 0.004 * SL$
	tR	0.20	$0.18 + 0.011 * SL$	$0.18 + 0.013 * SL$	$0.16 + 0.014 * SL$
	tF	0.24	$0.23 + 0.001 * SL$	$0.22 + 0.006 * SL$	$0.23 + 0.005 * SL$
D to Y	tPLH	0.92	$0.90 + 0.007 * SL$	$0.91 + 0.006 * SL$	$0.91 + 0.006 * SL$
	tPHL	0.61	$0.60 + 0.006 * SL$	$0.60 + 0.005 * SL$	$0.62 + 0.004 * SL$
	tR	0.20	$0.18 + 0.013 * SL$	$0.18 + 0.013 * SL$	$0.16 + 0.014 * SL$
	tF	0.24	$0.23 + 0.003 * SL$	$0.22 + 0.006 * SL$	$0.23 + 0.005 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# OA22A/OA22D2A

2-OR and 2-invert-OR into 2-NAND with 1X Drive or 2X Drive

Inputs: A, B, C, D

Output: Y

Input Loading (SL):

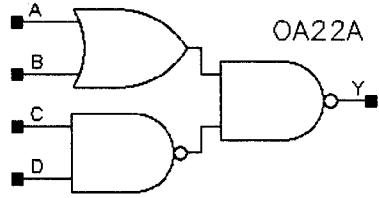
- OA22A: All : 1
- OA22D2A: A,B : 2
- C,D : 1

Maximum Fanout (Rec. SL):

- OA22A: 14
- OA22D2A: 28

Gate Count:

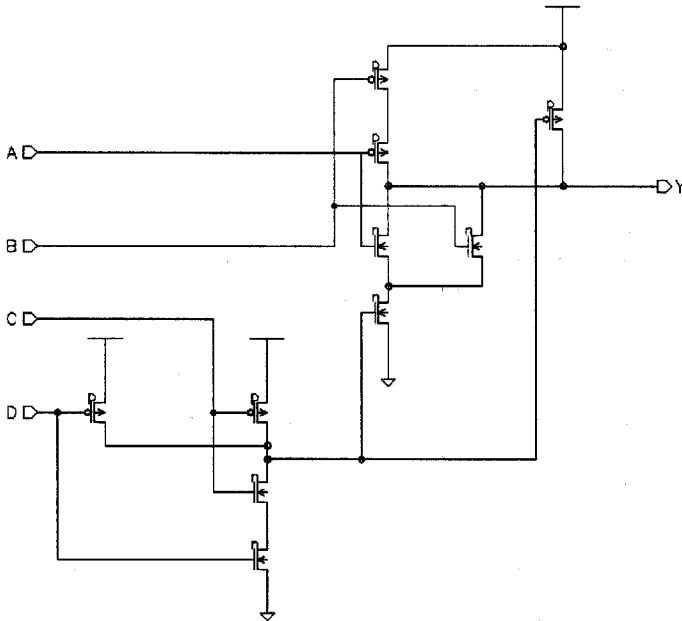
- OA22A: 3
- OA22D2A: 4



Symbol

A	B	C	D	Y
0	0	x	x	1
x	x	1	1	1
1	x	0	x	0
1	x	x	0	0
x	1	0	x	0
x	1	x	0	0

Truth Table



Schematic

**OA22A Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.49	$0.34 + 0.076*SL$	$0.34 + 0.076*SL$	$0.30 + 0.078*SL$
	tPHL	0.16	$0.06 + 0.050*SL$	$0.11 + 0.033*SL$	$0.17 + 0.031*SL$
	tR	0.80	$0.45 + 0.174*SL$	$0.41 + 0.186*SL$	$0.34 + 0.190*SL$
	tF	0.44	$0.32 + 0.063*SL$	$0.32 + 0.062*SL$	$0.24 + 0.067*SL$
B to Y	tPLH	0.46	$0.31 + 0.074*SL$	$0.30 + 0.076*SL$	$0.28 + 0.078*SL$
	tPHL	0.20	$0.11 + 0.047*SL$	$0.15 + 0.033*SL$	$0.19 + 0.031*SL$
	tR	0.80	$0.46 + 0.172*SL$	$0.42 + 0.186*SL$	$0.34 + 0.190*SL$
	tF	0.52	$0.41 + 0.056*SL$	$0.39 + 0.062*SL$	$0.29 + 0.066*SL$
C to Y	tPLH	0.40	$0.31 + 0.045*SL$	$0.31 + 0.043*SL$	$0.32 + 0.043*SL$
	tPHL	0.44	$0.38 + 0.033*SL$	$0.38 + 0.031*SL$	$0.39 + 0.031*SL$
	tR	0.60	$0.41 + 0.095*SL$	$0.39 + 0.100*SL$	$0.36 + 0.102*SL$
	tF	0.34	$0.22 + 0.062*SL$	$0.20 + 0.067*SL$	$0.18 + 0.069*SL$
D to Y	tPLH	0.37	$0.28 + 0.045*SL$	$0.29 + 0.043*SL$	$0.30 + 0.043*SL$
	tPHL	0.51	$0.45 + 0.033*SL$	$0.45 + 0.031*SL$	$0.46 + 0.031*SL$
	tR	0.60	$0.41 + 0.095*SL$	$0.40 + 0.100*SL$	$0.36 + 0.102*SL$
	tF	0.35	$0.23 + 0.061*SL$	$0.21 + 0.067*SL$	$0.18 + 0.069*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**OA22D2A Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.41	$0.33 + 0.039*SL$	$0.34 + 0.036*SL$	$0.32 + 0.037*SL$
	tPHL	0.11	$0.05 + 0.029*SL$	$0.08 + 0.019*SL$	$0.15 + 0.015*SL$
	tR	0.60	$0.44 + 0.082*SL$	$0.42 + 0.087*SL$	$0.36 + 0.091*SL$
	tF	0.38	$0.31 + 0.032*SL$	$0.32 + 0.029*SL$	$0.29 + 0.030*SL$
B to Y	tPLH	0.38	$0.30 + 0.037*SL$	$0.31 + 0.036*SL$	$0.29 + 0.037*SL$
	tPHL	0.15	$0.10 + 0.026*SL$	$0.12 + 0.018*SL$	$0.18 + 0.015*SL$
	tR	0.61	$0.45 + 0.080*SL$	$0.43 + 0.087*SL$	$0.36 + 0.091*SL$
	tF	0.45	$0.40 + 0.029*SL$	$0.40 + 0.028*SL$	$0.36 + 0.030*SL$
C to Y	tPLH	0.38	$0.34 + 0.021*SL$	$0.34 + 0.020*SL$	$0.35 + 0.020*SL$
	tPHL	0.46	$0.43 + 0.017*SL$	$0.43 + 0.015*SL$	$0.44 + 0.015*SL$
	tR	0.48	$0.40 + 0.041*SL$	$0.39 + 0.045*SL$	$0.36 + 0.047*SL$
	tF	0.29	$0.23 + 0.029*SL$	$0.22 + 0.031*SL$	$0.19 + 0.032*SL$
D to Y	tPLH	0.35	$0.31 + 0.021*SL$	$0.31 + 0.020*SL$	$0.32 + 0.020*SL$
	tPHL	0.53	$0.49 + 0.017*SL$	$0.50 + 0.015*SL$	$0.50 + 0.015*SL$
	tR	0.49	$0.40 + 0.042*SL$	$0.39 + 0.045*SL$	$0.36 + 0.047*SL$
	tF	0.30	$0.24 + 0.028*SL$	$0.24 + 0.031*SL$	$0.20 + 0.032*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# OR2D2/OR2D4/OR2D8

2 Input OR with 2X Drive, 4X Drive or 8X Drive

Inputs: A, B

Output: Y

Input Loading (SL):

OR2D2: All : 1

OR2D4 All: 1

OR2D8: All: 2

Maximum Fanout (Rec. SL):

OR2D2: 56

OR2D4: 112

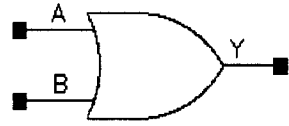
OR2D8: 224

Gate Count:

OR2D2: 2

OR2D4: 3

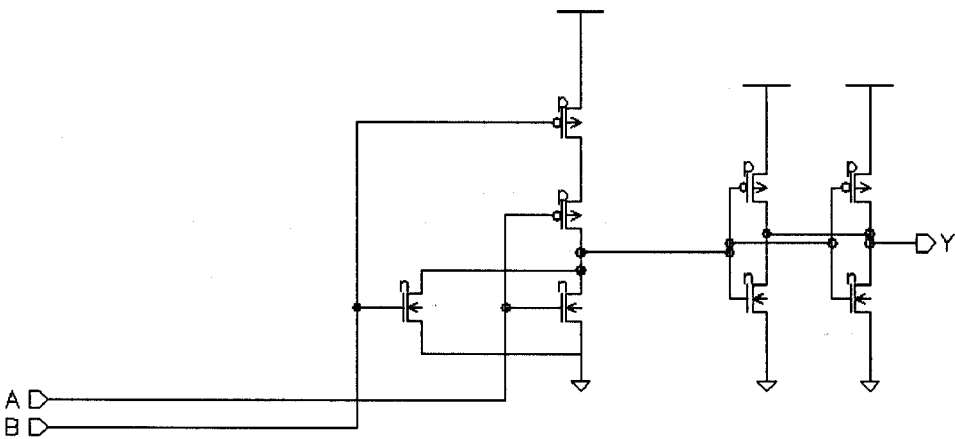
OR2D8: 6



**Symbol**

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

**Truth Table**



**Schematic**

**OR2D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.20	$0.15 + 0.023*SL$	$0.16 + 0.021*SL$	$0.15 + 0.021*SL$
	tPHL	0.53	$0.49 + 0.020*SL$	$0.51 + 0.014*SL$	$0.56 + 0.011*SL$
	tR	0.22	$0.13 + 0.048*SL$	$0.12 + 0.051*SL$	$0.09 + 0.052*SL$
	tF	0.22	$0.18 + 0.023*SL$	$0.19 + 0.019*SL$	$0.18 + 0.020*SL$
B to Y	tPLH	0.24	$0.20 + 0.022*SL$	$0.20 + 0.021*SL$	$0.19 + 0.021*SL$
	tPHL	0.50	$0.46 + 0.021*SL$	$0.48 + 0.014*SL$	$0.53 + 0.011*SL$
	tR	0.23	$0.13 + 0.049*SL$	$0.13 + 0.051*SL$	$0.10 + 0.052*SL$
	tF	0.23	$0.19 + 0.017*SL$	$0.19 + 0.020*SL$	$0.18 + 0.020*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **OR2D4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.26	$0.23 + 0.012*SL$	$0.24 + 0.011*SL$	$0.24 + 0.011*SL$
	tPHL	0.63	$0.60 + 0.013*SL$	$0.61 + 0.009*SL$	$0.66 + 0.007*SL$
	tR	0.19	$0.15 + 0.022*SL$	$0.14 + 0.025*SL$	$0.12 + 0.026*SL$
	tF	0.27	$0.25 + 0.011*SL$	$0.26 + 0.010*SL$	$0.27 + 0.010*SL$
B to Y	tPLH	0.29	$0.27 + 0.012*SL$	$0.27 + 0.011*SL$	$0.28 + 0.011*SL$
	tPHL	0.60	$0.57 + 0.013*SL$	$0.58 + 0.009*SL$	$0.63 + 0.007*SL$
	tR	0.20	$0.15 + 0.025*SL$	$0.15 + 0.024*SL$	$0.13 + 0.026*SL$
	tF	0.28	$0.26 + 0.009*SL$	$0.26 + 0.010*SL$	$0.27 + 0.010*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **OR2D8 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.24	$0.23 + 0.006*SL$	$0.23 + 0.006*SL$	$0.24 + 0.005*SL$
	tPHL	0.64	$0.63 + 0.006*SL$	$0.63 + 0.005*SL$	$0.65 + 0.004*SL$
	tR	0.17	$0.15 + 0.012*SL$	$0.15 + 0.012*SL$	$0.13 + 0.013*SL$
	tF	0.28	$0.26 + 0.006*SL$	$0.27 + 0.006*SL$	$0.28 + 0.005*SL$
B to Y	tPLH	0.28	$0.27 + 0.006*SL$	$0.27 + 0.006*SL$	$0.28 + 0.005*SL$
	tPHL	0.60	$0.59 + 0.007*SL$	$0.60 + 0.005*SL$	$0.62 + 0.004*SL$
	tR	0.18	$0.16 + 0.010*SL$	$0.15 + 0.012*SL$	$0.14 + 0.013*SL$
	tF	0.28	$0.27 + 0.006*SL$	$0.27 + 0.006*SL$	$0.28 + 0.005*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# OR3/OR3D3/OR3D6/OR3D8

3 Input OR with 1X Drive, 3X Drive, 6X Drive or 8X Drive

Inputs: A, B, C

Output: Y

Input Loading (SL):

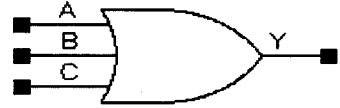
- OR3: All : 1
- OR3D2: All : 1
- OR3D6: All: 2
- OR3D8: All: 2

Maximum Fanout (Rec. SL):

- OR3: 28
- OR3D2: 84
- OR3D6: 168
- OR3D8: 224

Gate Count:

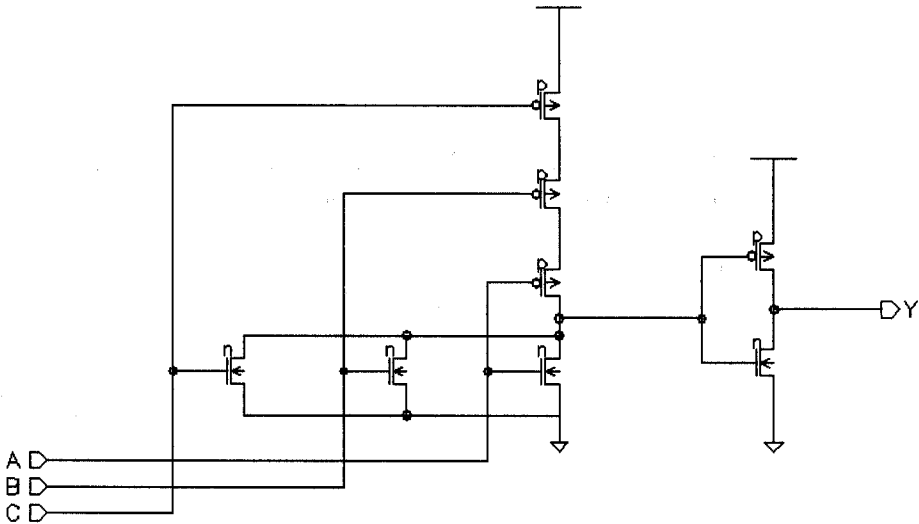
- OR3: 2
- OR3D2: 3
- OR3D6: 6
- OR3D8: 8



Symbol

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Truth Table



Schematic

**OR3 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{p}}$  and  $t_{\text{f}}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.20	$0.12 + 0.043 \cdot \text{SL}$	$0.12 + 0.043 \cdot \text{SL}$	$0.12 + 0.043 \cdot \text{SL}$
	tPHL	0.61	$0.53 + 0.038 \cdot \text{SL}$	$0.57 + 0.025 \cdot \text{SL}$	$0.66 + 0.021 \cdot \text{SL}$
	tR	0.31	$0.12 + 0.096 \cdot \text{SL}$	$0.10 + 0.101 \cdot \text{SL}$	$0.09 + 0.102 \cdot \text{SL}$
	tF	0.28	$0.19 + 0.042 \cdot \text{SL}$	$0.21 + 0.038 \cdot \text{SL}$	$0.21 + 0.038 \cdot \text{SL}$
B to Y	tPLH	0.24	$0.16 + 0.043 \cdot \text{SL}$	$0.16 + 0.042 \cdot \text{SL}$	$0.16 + 0.043 \cdot \text{SL}$
	tPHL	0.63	$0.55 + 0.039 \cdot \text{SL}$	$0.59 + 0.025 \cdot \text{SL}$	$0.68 + 0.021 \cdot \text{SL}$
	tR	0.32	$0.12 + 0.096 \cdot \text{SL}$	$0.11 + 0.101 \cdot \text{SL}$	$0.09 + 0.102 \cdot \text{SL}$
	tF	0.29	$0.21 + 0.042 \cdot \text{SL}$	$0.22 + 0.037 \cdot \text{SL}$	$0.22 + 0.037 \cdot \text{SL}$
C to Y	tPLH	0.25	$0.16 + 0.043 \cdot \text{SL}$	$0.16 + 0.042 \cdot \text{SL}$	$0.16 + 0.043 \cdot \text{SL}$
	tPHL	0.62	$0.54 + 0.039 \cdot \text{SL}$	$0.58 + 0.025 \cdot \text{SL}$	$0.67 + 0.021 \cdot \text{SL}$
	tR	0.33	$0.13 + 0.096 \cdot \text{SL}$	$0.12 + 0.101 \cdot \text{SL}$	$0.10 + 0.102 \cdot \text{SL}$
	tF	0.29	$0.20 + 0.043 \cdot \text{SL}$	$0.22 + 0.038 \cdot \text{SL}$	$0.22 + 0.037 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **OR3D3 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{p}}$  and  $t_{\text{f}}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.24	$0.21 + 0.015 \cdot \text{SL}$	$0.21 + 0.014 \cdot \text{SL}$	$0.21 + 0.014 \cdot \text{SL}$
	tPHL	0.74	$0.70 + 0.018 \cdot \text{SL}$	$0.72 + 0.013 \cdot \text{SL}$	$0.78 + 0.009 \cdot \text{SL}$
	tR	0.20	$0.14 + 0.030 \cdot \text{SL}$	$0.13 + 0.033 \cdot \text{SL}$	$0.11 + 0.034 \cdot \text{SL}$
	tF	0.34	$0.30 + 0.018 \cdot \text{SL}$	$0.32 + 0.014 \cdot \text{SL}$	$0.34 + 0.013 \cdot \text{SL}$
B to Y	tPLH	0.27	$0.24 + 0.015 \cdot \text{SL}$	$0.25 + 0.014 \cdot \text{SL}$	$0.25 + 0.014 \cdot \text{SL}$
	tPHL	0.76	$0.72 + 0.018 \cdot \text{SL}$	$0.74 + 0.013 \cdot \text{SL}$	$0.80 + 0.009 \cdot \text{SL}$
	tR	0.21	$0.14 + 0.032 \cdot \text{SL}$	$0.14 + 0.033 \cdot \text{SL}$	$0.11 + 0.034 \cdot \text{SL}$
	tF	0.35	$0.32 + 0.017 \cdot \text{SL}$	$0.32 + 0.014 \cdot \text{SL}$	$0.35 + 0.013 \cdot \text{SL}$
C to Y	tPLH	0.28	$0.24 + 0.016 \cdot \text{SL}$	$0.25 + 0.014 \cdot \text{SL}$	$0.25 + 0.014 \cdot \text{SL}$
	tPHL	0.75	$0.71 + 0.018 \cdot \text{SL}$	$0.73 + 0.013 \cdot \text{SL}$	$0.79 + 0.009 \cdot \text{SL}$
	tR	0.21	$0.15 + 0.031 \cdot \text{SL}$	$0.15 + 0.033 \cdot \text{SL}$	$0.12 + 0.034 \cdot \text{SL}$
	tF	0.35	$0.31 + 0.018 \cdot \text{SL}$	$0.32 + 0.014 \cdot \text{SL}$	$0.35 + 0.013 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

# OR3D6/OR3D8

3 Input OR with 6X Drive or 8X Drive

## OR3D6 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{p}$  and  $t_{f}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.22	$0.20 + 0.008 \cdot SL$	$0.21 + 0.007 \cdot SL$	$0.21 + 0.007 \cdot SL$
	tPHL	0.72	$0.71 + 0.010 \cdot SL$	$0.71 + 0.008 \cdot SL$	$0.75 + 0.006 \cdot SL$
	tR	0.17	$0.14 + 0.014 \cdot SL$	$0.14 + 0.016 \cdot SL$	$0.12 + 0.017 \cdot SL$
	tF	0.33	$0.31 + 0.009 \cdot SL$	$0.32 + 0.008 \cdot SL$	$0.33 + 0.007 \cdot SL$
B to Y	tPLH	0.26	$0.24 + 0.008 \cdot SL$	$0.24 + 0.007 \cdot SL$	$0.25 + 0.007 \cdot SL$
	tPHL	0.74	$0.72 + 0.010 \cdot SL$	$0.73 + 0.008 \cdot SL$	$0.76 + 0.006 \cdot SL$
	tR	0.18	$0.15 + 0.014 \cdot SL$	$0.14 + 0.016 \cdot SL$	$0.13 + 0.017 \cdot SL$
	tF	0.34	$0.32 + 0.007 \cdot SL$	$0.32 + 0.008 \cdot SL$	$0.34 + 0.007 \cdot SL$
C to Y	tPLH	0.27	$0.25 + 0.009 \cdot SL$	$0.25 + 0.007 \cdot SL$	$0.26 + 0.007 \cdot SL$
	tPHL	0.73	$0.71 + 0.010 \cdot SL$	$0.72 + 0.008 \cdot SL$	$0.76 + 0.006 \cdot SL$
	tR	0.19	$0.16 + 0.015 \cdot SL$	$0.15 + 0.016 \cdot SL$	$0.14 + 0.017 \cdot SL$
	tF	0.34	$0.32 + 0.009 \cdot SL$	$0.32 + 0.008 \cdot SL$	$0.34 + 0.007 \cdot SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

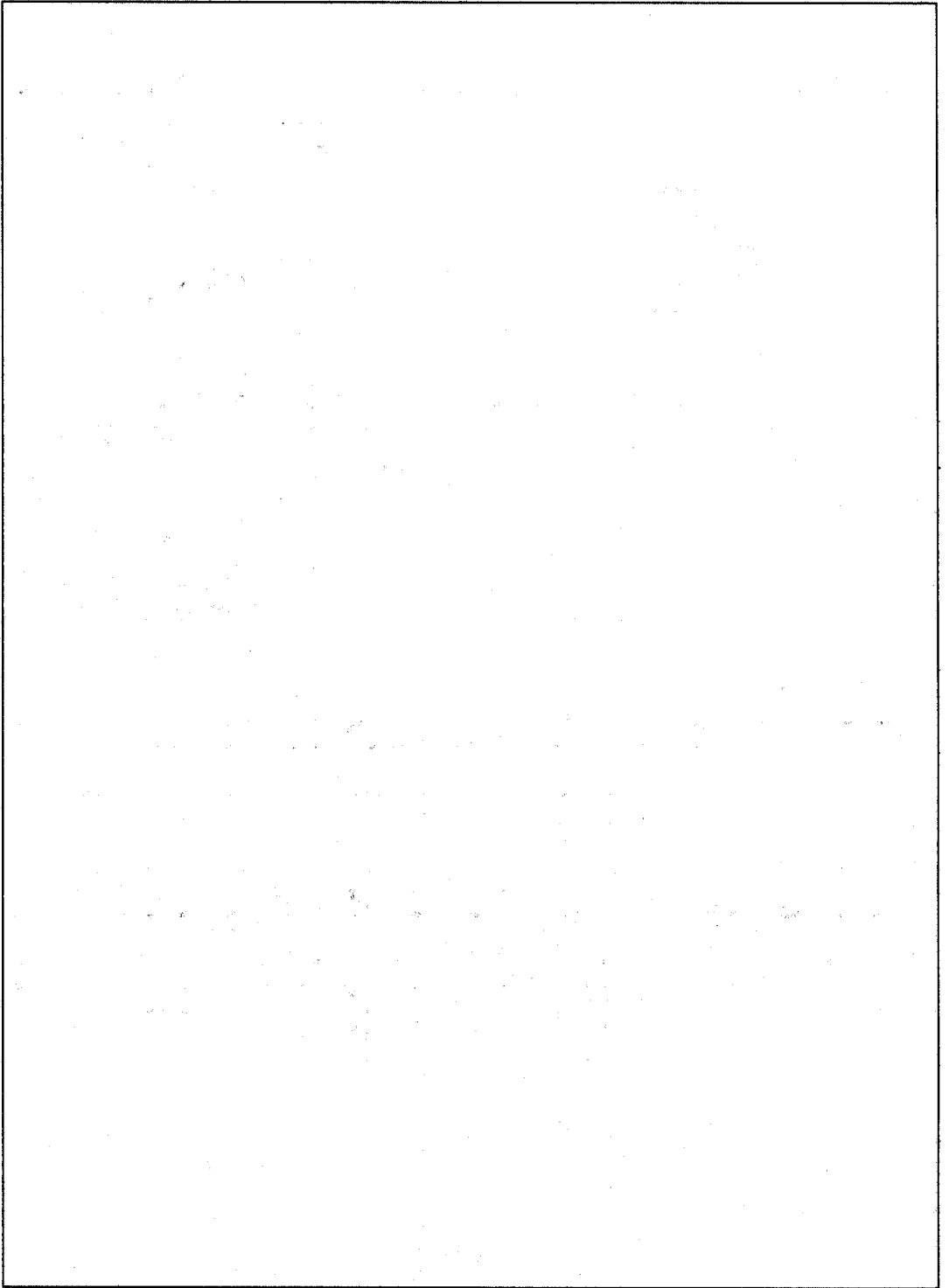
## OR3D8 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{p}$  and  $t_{f}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.25	$0.24 + 0.006 \cdot SL$	$0.24 + 0.006 \cdot SL$	$0.25 + 0.005 \cdot SL$
	tPHL	0.81	$0.79 + 0.008 \cdot SL$	$0.80 + 0.006 \cdot SL$	$0.82 + 0.005 \cdot SL$
	tR	0.17	$0.15 + 0.010 \cdot SL$	$0.15 + 0.012 \cdot SL$	$0.13 + 0.013 \cdot SL$
	tF	0.39	$0.38 + 0.006 \cdot SL$	$0.38 + 0.006 \cdot SL$	$0.39 + 0.005 \cdot SL$
B to Y	tPLH	0.29	$0.28 + 0.006 \cdot SL$	$0.28 + 0.006 \cdot SL$	$0.28 + 0.005 \cdot SL$
	tPHL	0.83	$0.81 + 0.008 \cdot SL$	$0.81 + 0.006 \cdot SL$	$0.84 + 0.005 \cdot SL$
	tR	0.18	$0.16 + 0.011 \cdot SL$	$0.15 + 0.012 \cdot SL$	$0.14 + 0.012 \cdot SL$
	tF	0.40	$0.38 + 0.007 \cdot SL$	$0.38 + 0.006 \cdot SL$	$0.40 + 0.005 \cdot SL$
C to Y	tPLH	0.30	$0.29 + 0.007 \cdot SL$	$0.29 + 0.006 \cdot SL$	$0.30 + 0.005 \cdot SL$
	tPHL	0.82	$0.80 + 0.008 \cdot SL$	$0.81 + 0.006 \cdot SL$	$0.83 + 0.005 \cdot SL$
	tR	0.19	$0.17 + 0.011 \cdot SL$	$0.16 + 0.012 \cdot SL$	$0.15 + 0.013 \cdot SL$
	tF	0.39	$0.38 + 0.005 \cdot SL$	$0.38 + 0.006 \cdot SL$	$0.40 + 0.005 \cdot SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# OR4/OR4D2/OR4D5/OR4D7

4 Input OR with 1X Drive, 2X Drive, 5X Drive or 7X Drive

Inputs: A, B, C, D

Output: YAll: 1

Input Loading (SL): All: 1

Maximum Fanout (Rec. SL):

- OR4: 28

- OR4D2: 56

- OR4D5: 140

- OR4D7: 196

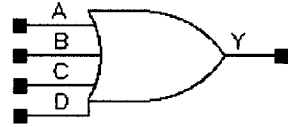
Gate Count:

- OR4: 3

- OR4D2: 4

- OR4D5: 6

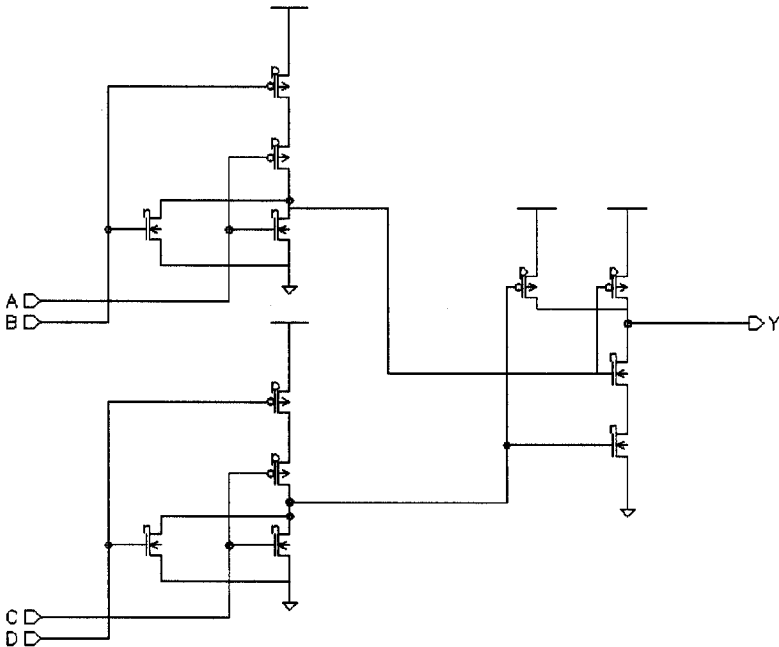
- OR4D7: 7



**Symbol**

A	B	C	D	Y
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

**Truth Table**



**Schematic**

**OR4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.20	$0.11 + 0.042*SL$	$0.12 + 0.041*SL$	$0.12 + 0.041*SL$
	tPHL	0.55	$0.48 + 0.038*SL$	$0.50 + 0.031*SL$	$0.53 + 0.030*SL$
	tR	0.32	$0.14 + 0.090*SL$	$0.13 + 0.094*SL$	$0.12 + 0.095*SL$
	tF	0.30	$0.18 + 0.060*SL$	$0.18 + 0.062*SL$	$0.14 + 0.063*SL$
B to Y	tPLH	0.24	$0.15 + 0.042*SL$	$0.16 + 0.041*SL$	$0.16 + 0.041*SL$
	tPHL	0.53	$0.45 + 0.038*SL$	$0.48 + 0.031*SL$	$0.51 + 0.030*SL$
	tR	0.33	$0.15 + 0.089*SL$	$0.14 + 0.094*SL$	$0.12 + 0.095*SL$
	tF	0.31	$0.19 + 0.060*SL$	$0.18 + 0.061*SL$	$0.15 + 0.063*SL$
C to Y	tPLH	0.24	$0.15 + 0.041*SL$	$0.15 + 0.041*SL$	$0.16 + 0.041*SL$
	tPHL	0.54	$0.47 + 0.035*SL$	$0.48 + 0.030*SL$	$0.49 + 0.030*SL$
	tR	0.40	$0.22 + 0.089*SL$	$0.21 + 0.094*SL$	$0.19 + 0.095*SL$
	tF	0.28	$0.17 + 0.058*SL$	$0.16 + 0.062*SL$	$0.12 + 0.064*SL$
D to Y	tPLH	0.28	$0.20 + 0.041*SL$	$0.20 + 0.041*SL$	$0.20 + 0.041*SL$
	tPHL	0.51	$0.44 + 0.035*SL$	$0.46 + 0.030*SL$	$0.47 + 0.030*SL$
	tR	0.41	$0.24 + 0.086*SL$	$0.22 + 0.093*SL$	$0.19 + 0.095*SL$
	tF	0.29	$0.17 + 0.057*SL$	$0.16 + 0.062*SL$	$0.12 + 0.064*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **OR4D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.20	$0.15 + 0.022*SL$	$0.16 + 0.020*SL$	$0.16 + 0.020*SL$
	tPHL	0.58	$0.53 + 0.023*SL$	$0.55 + 0.017*SL$	$0.59 + 0.015*SL$
	tR	0.24	$0.15 + 0.044*SL$	$0.14 + 0.046*SL$	$0.12 + 0.047*SL$
	tF	0.28	$0.22 + 0.029*SL$	$0.21 + 0.031*SL$	$0.20 + 0.032*SL$
B to Y	tPLH	0.23	$0.19 + 0.021*SL$	$0.19 + 0.020*SL$	$0.19 + 0.020*SL$
	tPHL	0.55	$0.51 + 0.023*SL$	$0.52 + 0.017*SL$	$0.56 + 0.015*SL$
	tR	0.25	$0.16 + 0.042*SL$	$0.15 + 0.045*SL$	$0.12 + 0.047*SL$
	tF	0.28	$0.22 + 0.028*SL$	$0.22 + 0.031*SL$	$0.20 + 0.032*SL$
C to Y	tPLH	0.23	$0.19 + 0.020*SL$	$0.19 + 0.020*SL$	$0.19 + 0.020*SL$
	tPHL	0.57	$0.53 + 0.021*SL$	$0.54 + 0.016*SL$	$0.56 + 0.015*SL$
	tR	0.32	$0.24 + 0.042*SL$	$0.23 + 0.045*SL$	$0.20 + 0.047*SL$
	tF	0.27	$0.21 + 0.027*SL$	$0.20 + 0.031*SL$	$0.17 + 0.032*SL$
D to Y	tPLH	0.27	$0.23 + 0.020*SL$	$0.23 + 0.020*SL$	$0.23 + 0.020*SL$
	tPHL	0.54	$0.50 + 0.020*SL$	$0.51 + 0.016*SL$	$0.54 + 0.015*SL$
	tR	0.33	$0.26 + 0.040*SL$	$0.24 + 0.045*SL$	$0.20 + 0.047*SL$
	tF	0.27	$0.22 + 0.026*SL$	$0.20 + 0.031*SL$	$0.17 + 0.032*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# OR4D5/OR4D7

4 Input OR with 5X Drive or 7X Drive

## OR4D5 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.46	$0.44 + 0.009*SL$	$0.44 + 0.009*SL$	$0.44 + 0.008*SL$
	tPHL	0.81	$0.79 + 0.009*SL$	$0.80 + 0.006*SL$	$0.83 + 0.005*SL$
	tR	0.17	$0.13 + 0.019*SL$	$0.13 + 0.019*SL$	$0.12 + 0.020*SL$
	tF	0.18	$0.16 + 0.010*SL$	$0.17 + 0.007*SL$	$0.16 + 0.008*SL$
B to Y	tPLH	0.50	$0.48 + 0.009*SL$	$0.48 + 0.009*SL$	$0.49 + 0.008*SL$
	tPHL	0.79	$0.77 + 0.008*SL$	$0.78 + 0.006*SL$	$0.81 + 0.005*SL$
	tR	0.17	$0.13 + 0.018*SL$	$0.13 + 0.019*SL$	$0.12 + 0.020*SL$
	tF	0.18	$0.17 + 0.007*SL$	$0.17 + 0.008*SL$	$0.16 + 0.008*SL$
C to Y	tPLH	0.41	$0.39 + 0.009*SL$	$0.39 + 0.009*SL$	$0.40 + 0.008*SL$
	tPHL	0.82	$0.80 + 0.008*SL$	$0.81 + 0.006*SL$	$0.84 + 0.005*SL$
	tR	0.17	$0.14 + 0.017*SL$	$0.13 + 0.019*SL$	$0.11 + 0.020*SL$
	tF	0.18	$0.17 + 0.004*SL$	$0.16 + 0.008*SL$	$0.16 + 0.008*SL$
D to Y	tPLH	0.45	$0.43 + 0.009*SL$	$0.43 + 0.009*SL$	$0.44 + 0.008*SL$
	tPHL	0.80	$0.78 + 0.008*SL$	$0.79 + 0.006*SL$	$0.81 + 0.005*SL$
	tR	0.17	$0.13 + 0.018*SL$	$0.13 + 0.019*SL$	$0.11 + 0.020*SL$
	tF	0.18	$0.16 + 0.010*SL$	$0.17 + 0.007*SL$	$0.16 + 0.008*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

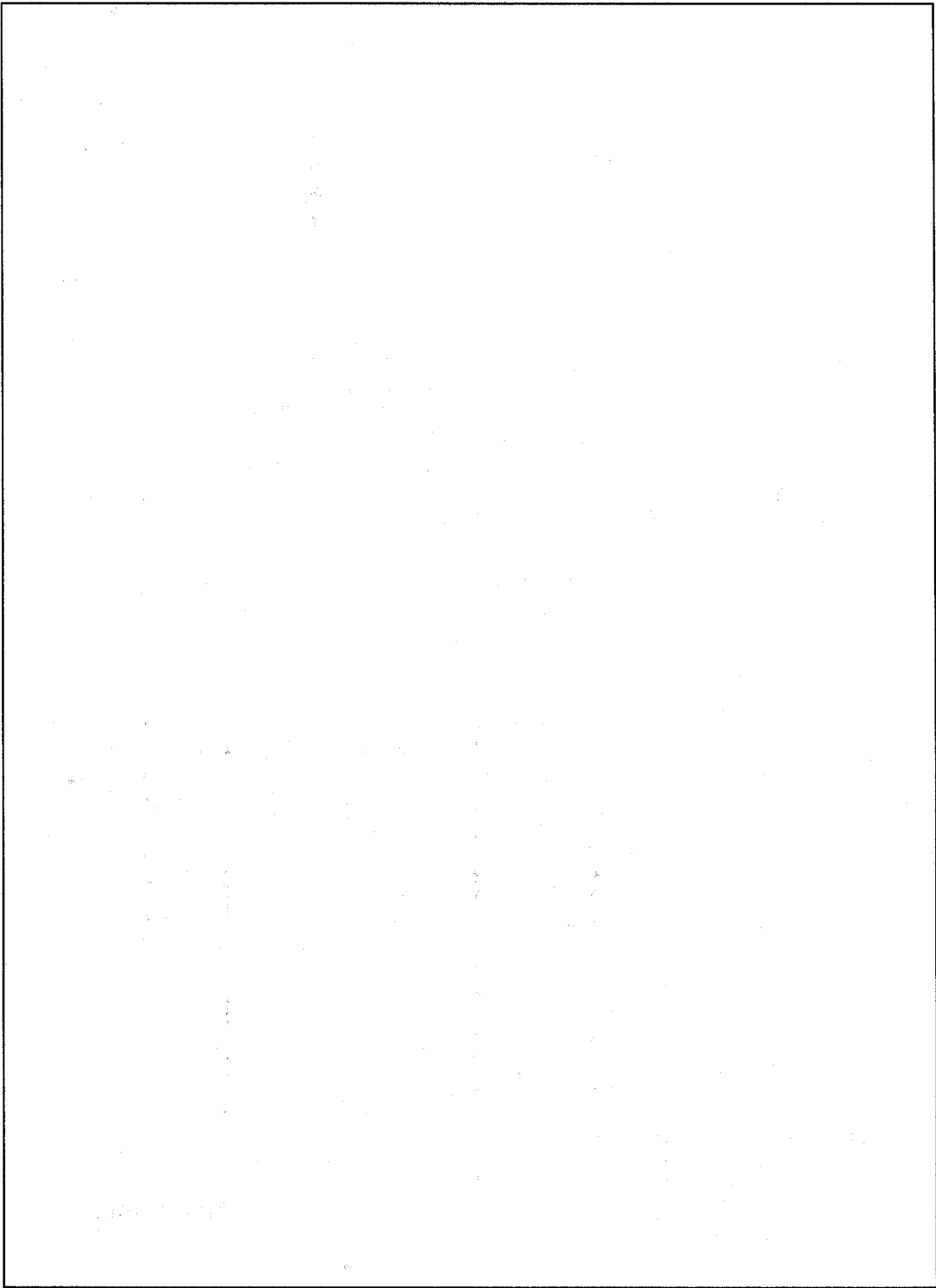
## OR4D7 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.50	$0.49 + 0.007*SL$	$0.49 + 0.006*SL$	$0.50 + 0.006*SL$
	tPHL	0.87	$0.86 + 0.007*SL$	$0.86 + 0.005*SL$	$0.89 + 0.004*SL$
	tR	0.18	$0.15 + 0.012*SL$	$0.15 + 0.014*SL$	$0.14 + 0.014*SL$
	tF	0.22	$0.22 + 0.002*SL$	$0.21 + 0.006*SL$	$0.21 + 0.005*SL$
B to Y	tPLH	0.55	$0.53 + 0.007*SL$	$0.54 + 0.006*SL$	$0.54 + 0.006*SL$
	tPHL	0.85	$0.84 + 0.007*SL$	$0.84 + 0.005*SL$	$0.86 + 0.004*SL$
	tR	0.18	$0.16 + 0.011*SL$	$0.15 + 0.014*SL$	$0.14 + 0.014*SL$
	tF	0.22	$0.21 + 0.003*SL$	$0.21 + 0.006*SL$	$0.21 + 0.005*SL$
C to Y	tPLH	0.46	$0.44 + 0.007*SL$	$0.45 + 0.006*SL$	$0.45 + 0.006*SL$
	tPHL	0.88	$0.87 + 0.007*SL$	$0.87 + 0.005*SL$	$0.90 + 0.004*SL$
	tR	0.18	$0.15 + 0.011*SL$	$0.15 + 0.014*SL$	$0.14 + 0.014*SL$
	tF	0.22	$0.21 + 0.003*SL$	$0.21 + 0.006*SL$	$0.21 + 0.005*SL$
D to Y	tPLH	0.50	$0.49 + 0.007*SL$	$0.49 + 0.006*SL$	$0.49 + 0.006*SL$
	tPHL	0.86	$0.84 + 0.007*SL$	$0.85 + 0.005*SL$	$0.87 + 0.004*SL$
	tR	0.18	$0.16 + 0.011*SL$	$0.15 + 0.014*SL$	$0.13 + 0.014*SL$
	tF	0.22	$0.21 + 0.005*SL$	$0.21 + 0.006*SL$	$0.21 + 0.005*SL$

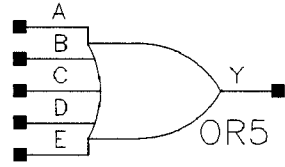
\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# OR5/OR5D2

5 Input OR with 1X Drive or 2X Drive

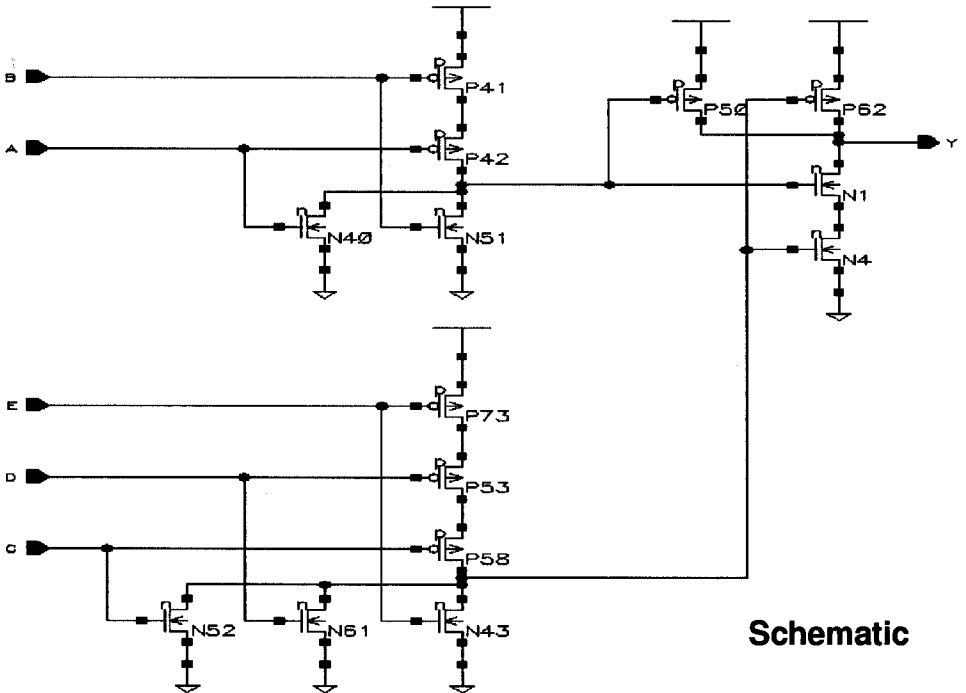
Inputs:  
 Output:  
 Input Loading (SL): All: 1  
 Maximum Fanout (Rec. SL):  
 - OR5: 28  
 - OR5D2: 56  
 Gate Count:  
 - OR5: 4  
 - OR5D2: 5



**Symbol**

A	B	C	D	E	Y
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

**Truth Table**



**Schematic**

**OR5 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.20	$0.11 + 0.044 \cdot \text{SL}$	$0.12 + 0.043 \cdot \text{SL}$	$0.12 + 0.043 \cdot \text{SL}$
	tPHL	0.55	$0.47 + 0.040 \cdot \text{SL}$	$0.49 + 0.032 \cdot \text{SL}$	$0.52 + 0.031 \cdot \text{SL}$
	tR	0.34	$0.15 + 0.097 \cdot \text{SL}$	$0.13 + 0.101 \cdot \text{SL}$	$0.12 + 0.102 \cdot \text{SL}$
	tF	0.31	$0.18 + 0.065 \cdot \text{SL}$	$0.18 + 0.067 \cdot \text{SL}$	$0.14 + 0.069 \cdot \text{SL}$
B to Y	tPLH	0.24	$0.15 + 0.044 \cdot \text{SL}$	$0.16 + 0.043 \cdot \text{SL}$	$0.16 + 0.043 \cdot \text{SL}$
	tPHL	0.53	$0.45 + 0.040 \cdot \text{SL}$	$0.47 + 0.032 \cdot \text{SL}$	$0.50 + 0.031 \cdot \text{SL}$
	tR	0.35	$0.16 + 0.096 \cdot \text{SL}$	$0.14 + 0.101 \cdot \text{SL}$	$0.12 + 0.102 \cdot \text{SL}$
	tF	0.32	$0.19 + 0.064 \cdot \text{SL}$	$0.18 + 0.067 \cdot \text{SL}$	$0.15 + 0.069 \cdot \text{SL}$
C to Y	tPLH	0.29	$0.21 + 0.043 \cdot \text{SL}$	$0.21 + 0.043 \cdot \text{SL}$	$0.21 + 0.043 \cdot \text{SL}$
	tPHL	0.73	$0.64 + 0.043 \cdot \text{SL}$	$0.67 + 0.033 \cdot \text{SL}$	$0.71 + 0.031 \cdot \text{SL}$
	tR	0.43	$0.24 + 0.093 \cdot \text{SL}$	$0.22 + 0.101 \cdot \text{SL}$	$0.19 + 0.102 \cdot \text{SL}$
	tF	0.40	$0.28 + 0.058 \cdot \text{SL}$	$0.26 + 0.065 \cdot \text{SL}$	$0.21 + 0.068 \cdot \text{SL}$
D to Y	tPLH	0.33	$0.24 + 0.043 \cdot \text{SL}$	$0.24 + 0.043 \cdot \text{SL}$	$0.24 + 0.043 \cdot \text{SL}$
	tPHL	0.74	$0.66 + 0.043 \cdot \text{SL}$	$0.69 + 0.033 \cdot \text{SL}$	$0.73 + 0.031 \cdot \text{SL}$
	tR	0.44	$0.26 + 0.092 \cdot \text{SL}$	$0.23 + 0.100 \cdot \text{SL}$	$0.20 + 0.102 \cdot \text{SL}$
	tF	0.41	$0.29 + 0.057 \cdot \text{SL}$	$0.27 + 0.065 \cdot \text{SL}$	$0.21 + 0.068 \cdot \text{SL}$
E to Y	tPLH	0.34	$0.25 + 0.043 \cdot \text{SL}$	$0.26 + 0.043 \cdot \text{SL}$	$0.26 + 0.043 \cdot \text{SL}$
	tPHL	0.74	$0.65 + 0.043 \cdot \text{SL}$	$0.68 + 0.033 \cdot \text{SL}$	$0.72 + 0.031 \cdot \text{SL}$
	tR	0.45	$0.27 + 0.091 \cdot \text{SL}$	$0.24 + 0.100 \cdot \text{SL}$	$0.20 + 0.102 \cdot \text{SL}$
	tF	0.41	$0.29 + 0.058 \cdot \text{SL}$	$0.27 + 0.065 \cdot \text{SL}$	$0.21 + 0.068 \cdot \text{SL}$

\*Range1:  $\text{SL} < 3.00$ , \*Range2:  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3:  $20.00 < \text{SL}$ **OR5D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

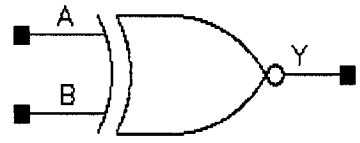
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.21	$0.16 + 0.023 \cdot \text{SL}$	$0.17 + 0.022 \cdot \text{SL}$	$0.17 + 0.022 \cdot \text{SL}$
	tPHL	0.59	$0.54 + 0.024 \cdot \text{SL}$	$0.55 + 0.019 \cdot \text{SL}$	$0.59 + 0.017 \cdot \text{SL}$
	tR	0.26	$0.16 + 0.050 \cdot \text{SL}$	$0.16 + 0.051 \cdot \text{SL}$	$0.13 + 0.052 \cdot \text{SL}$
	tF	0.30	$0.24 + 0.032 \cdot \text{SL}$	$0.23 + 0.035 \cdot \text{SL}$	$0.21 + 0.036 \cdot \text{SL}$
B to Y	tPLH	0.25	$0.20 + 0.023 \cdot \text{SL}$	$0.20 + 0.022 \cdot \text{SL}$	$0.20 + 0.021 \cdot \text{SL}$
	tPHL	0.56	$0.51 + 0.024 \cdot \text{SL}$	$0.53 + 0.019 \cdot \text{SL}$	$0.57 + 0.017 \cdot \text{SL}$
	tR	0.27	$0.18 + 0.047 \cdot \text{SL}$	$0.17 + 0.051 \cdot \text{SL}$	$0.14 + 0.052 \cdot \text{SL}$
	tF	0.30	$0.24 + 0.031 \cdot \text{SL}$	$0.23 + 0.035 \cdot \text{SL}$	$0.21 + 0.036 \cdot \text{SL}$
C to Y	tPLH	0.29	$0.25 + 0.022 \cdot \text{SL}$	$0.25 + 0.022 \cdot \text{SL}$	$0.25 + 0.022 \cdot \text{SL}$
	tPHL	0.78	$0.73 + 0.026 \cdot \text{SL}$	$0.75 + 0.019 \cdot \text{SL}$	$0.80 + 0.017 \cdot \text{SL}$
	tR	0.37	$0.28 + 0.045 \cdot \text{SL}$	$0.26 + 0.050 \cdot \text{SL}$	$0.22 + 0.052 \cdot \text{SL}$
	tF	0.42	$0.37 + 0.030 \cdot \text{SL}$	$0.36 + 0.032 \cdot \text{SL}$	$0.30 + 0.035 \cdot \text{SL}$
D to Y	tPLH	0.33	$0.29 + 0.022 \cdot \text{SL}$	$0.29 + 0.021 \cdot \text{SL}$	$0.29 + 0.022 \cdot \text{SL}$
	tPHL	0.80	$0.75 + 0.025 \cdot \text{SL}$	$0.77 + 0.019 \cdot \text{SL}$	$0.82 + 0.017 \cdot \text{SL}$
	tR	0.38	$0.29 + 0.044 \cdot \text{SL}$	$0.27 + 0.049 \cdot \text{SL}$	$0.22 + 0.052 \cdot \text{SL}$
	tF	0.43	$0.38 + 0.028 \cdot \text{SL}$	$0.36 + 0.032 \cdot \text{SL}$	$0.30 + 0.035 \cdot \text{SL}$
E to Y	tPLH	0.34	$0.30 + 0.022 \cdot \text{SL}$	$0.30 + 0.022 \cdot \text{SL}$	$0.30 + 0.022 \cdot \text{SL}$
	tPHL	0.79	$0.74 + 0.025 \cdot \text{SL}$	$0.76 + 0.019 \cdot \text{SL}$	$0.81 + 0.017 \cdot \text{SL}$
	tR	0.39	$0.30 + 0.044 \cdot \text{SL}$	$0.28 + 0.049 \cdot \text{SL}$	$0.23 + 0.052 \cdot \text{SL}$
	tF	0.43	$0.37 + 0.029 \cdot \text{SL}$	$0.36 + 0.032 \cdot \text{SL}$	$0.30 + 0.035 \cdot \text{SL}$

\*Range1:  $\text{SL} < 3.00$ , \*Range2:  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3:  $20.00 < \text{SL}$

# XN2/XN2D2/XN2D3/XN2D5

2 Input Exclusive NOR with 1X Drive, 2X Drive, 3X Drive or 5X Drive

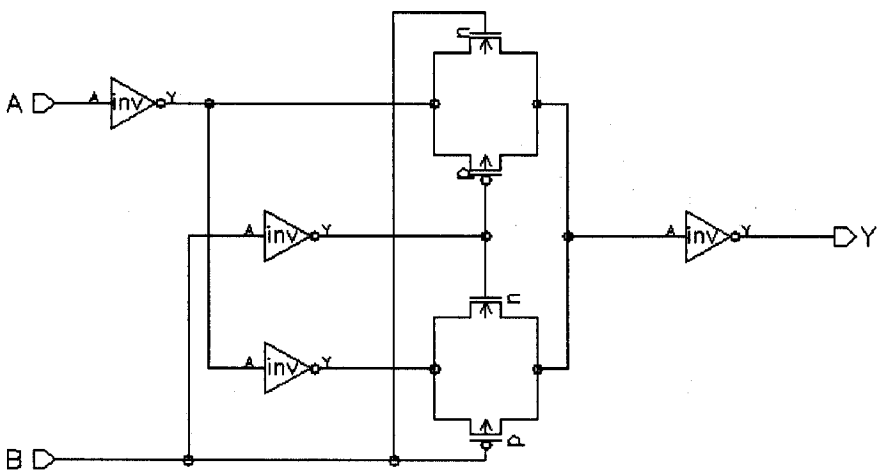
Inputs: A, B  
Output: Y  
Input Loading (SL): All: A : 1, B : 2  
Maximum Fanout (Rec. SL):  
- XN2: 28  
- XN2D2: 56  
- XN2D3: 84  
- XN2D5: 140  
Gate Count:  
- XN2: 3  
- XN2D2: 4  
- XN2D3: 4  
- XN2D5: 5



Symbol

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Truth Table



Schematic

**XN2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.64	$0.55 + 0.043*SL$	$0.56 + 0.041*SL$	$0.56 + 0.041*SL$
	tPHL	0.55	$0.48 + 0.037*SL$	$0.51 + 0.024*SL$	$0.59 + 0.020*SL$
	tR	0.31	$0.12 + 0.091*SL$	$0.11 + 0.096*SL$	$0.09 + 0.097*SL$
	tF	0.26	$0.18 + 0.041*SL$	$0.19 + 0.036*SL$	$0.18 + 0.037*SL$
B to Y	tPLH	0.52	$0.43 + 0.044*SL$	$0.44 + 0.041*SL$	$0.43 + 0.041*SL$
	tPHL	0.44	$0.37 + 0.033*SL$	$0.40 + 0.024*SL$	$0.47 + 0.020*SL$
	tR	0.31	$0.12 + 0.093*SL$	$0.11 + 0.096*SL$	$0.09 + 0.097*SL$
	tF	0.21	$0.13 + 0.043*SL$	$0.14 + 0.038*SL$	$0.15 + 0.037*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **XN2D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.63	$0.58 + 0.022*SL$	$0.59 + 0.020*SL$	$0.59 + 0.020*SL$
	tPHL	0.55	$0.51 + 0.022*SL$	$0.53 + 0.015*SL$	$0.60 + 0.011*SL$
	tR	0.22	$0.13 + 0.044*SL$	$0.13 + 0.045*SL$	$0.10 + 0.047*SL$
	tF	0.24	$0.19 + 0.023*SL$	$0.20 + 0.019*SL$	$0.22 + 0.018*SL$
B to Y	tPLH	0.50	$0.46 + 0.022*SL$	$0.46 + 0.020*SL$	$0.47 + 0.020*SL$
	tPHL	0.44	$0.40 + 0.020*SL$	$0.42 + 0.014*SL$	$0.48 + 0.011*SL$
	tR	0.22	$0.13 + 0.045*SL$	$0.13 + 0.045*SL$	$0.10 + 0.047*SL$
	tF	0.19	$0.15 + 0.022*SL$	$0.15 + 0.020*SL$	$0.18 + 0.019*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## XN2D3/XN2D5

2 Input Exclusive NOR with 3X Drive or 5X Drive

### XN2D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.65	$0.62 + 0.017*SL$	$0.63 + 0.015*SL$	$0.64 + 0.014*SL$
	tPHL	0.58	$0.55 + 0.017*SL$	$0.56 + 0.012*SL$	$0.62 + 0.009*SL$
	tR	0.22	$0.15 + 0.032*SL$	$0.15 + 0.033*SL$	$0.13 + 0.034*SL$
	tF	0.25	$0.22 + 0.016*SL$	$0.23 + 0.014*SL$	$0.25 + 0.013*SL$
B to Y	tPLH	0.53	$0.49 + 0.016*SL$	$0.50 + 0.015*SL$	$0.51 + 0.014*SL$
	tPHL	0.46	$0.43 + 0.016*SL$	$0.44 + 0.011*SL$	$0.49 + 0.009*SL$
	tR	0.22	$0.15 + 0.032*SL$	$0.15 + 0.033*SL$	$0.13 + 0.034*SL$
	tF	0.20	$0.17 + 0.015*SL$	$0.17 + 0.015*SL$	$0.20 + 0.014*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### XN2D5 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.70	$0.68 + 0.011*SL$	$0.69 + 0.009*SL$	$0.70 + 0.009*SL$
	tPHL	0.64	$0.61 + 0.011*SL$	$0.62 + 0.008*SL$	$0.66 + 0.006*SL$
	tR	0.22	$0.19 + 0.016*SL$	$0.18 + 0.019*SL$	$0.16 + 0.020*SL$
	tF	0.28	$0.26 + 0.012*SL$	$0.27 + 0.009*SL$	$0.28 + 0.008*SL$
B to Y	tPLH	0.57	$0.54 + 0.011*SL$	$0.55 + 0.009*SL$	$0.56 + 0.009*SL$
	tPHL	0.50	$0.48 + 0.011*SL$	$0.48 + 0.008*SL$	$0.52 + 0.006*SL$
	tR	0.22	$0.19 + 0.017*SL$	$0.18 + 0.019*SL$	$0.17 + 0.020*SL$
	tF	0.23	$0.22 + 0.007*SL$	$0.21 + 0.010*SL$	$0.24 + 0.009*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$





# XN3/XN3D3

3 Input Exclusive NOR with 1X Drive or 3X Drive

Inputs: A, B, C

Output: Y

Input Loading (SL):

- XN3: A, C: 2

B: 1

- XN3D2: A, C: 2

B: 1

Maximum Fanout (Rec. SL):

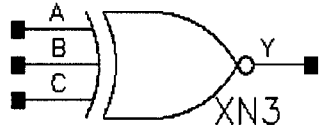
- XN3: 28

- XN3D2: 84

Gate Count:

- XN3: 5

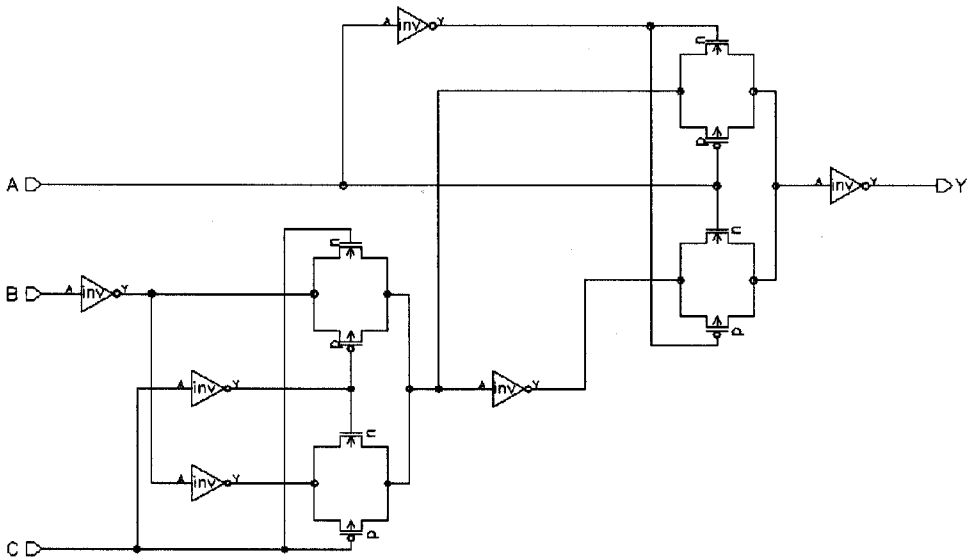
- XN3D2: 6



**Symbol**

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

**Truth Table**



**Schematic**

**XN3 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_{tf}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.55	$0.46 + 0.047*SL$	$0.47 + 0.042*SL$	$0.49 + 0.041*SL$
	tPHL	0.45	$0.38 + 0.036*SL$	$0.40 + 0.027*SL$	$0.50 + 0.022*SL$
	tR	0.33	$0.14 + 0.095*SL$	$0.14 + 0.095*SL$	$0.12 + 0.096*SL$
	tF	0.23	$0.13 + 0.049*SL$	$0.15 + 0.042*SL$	$0.22 + 0.038*SL$
B to Y	tPLH	0.87	$0.79 + 0.043*SL$	$0.79 + 0.041*SL$	$0.79 + 0.041*SL$
	tPHL	0.87	$0.80 + 0.035*SL$	$0.83 + 0.024*SL$	$0.90 + 0.020*SL$
	tR	0.32	$0.14 + 0.090*SL$	$0.12 + 0.095*SL$	$0.09 + 0.097*SL$
	tF	0.23	$0.15 + 0.040*SL$	$0.16 + 0.037*SL$	$0.15 + 0.037*SL$
C to Y	tPLH	0.74	$0.66 + 0.043*SL$	$0.66 + 0.041*SL$	$0.66 + 0.041*SL$
	tPHL	0.74	$0.67 + 0.035*SL$	$0.70 + 0.024*SL$	$0.77 + 0.020*SL$
	tR	0.31	$0.13 + 0.091*SL$	$0.12 + 0.096*SL$	$0.09 + 0.097*SL$
	tF	0.23	$0.15 + 0.040*SL$	$0.16 + 0.037*SL$	$0.15 + 0.037*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**XN3D3 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_{tf}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.57	$0.53 + 0.019*SL$	$0.54 + 0.015*SL$	$0.57 + 0.014*SL$
	tPHL	0.46	$0.43 + 0.016*SL$	$0.44 + 0.013*SL$	$0.49 + 0.010*SL$
	tR	0.26	$0.20 + 0.027*SL$	$0.19 + 0.030*SL$	$0.18 + 0.031*SL$
	tF	0.21	$0.17 + 0.021*SL$	$0.18 + 0.017*SL$	$0.23 + 0.014*SL$
B to Y	tPLH	0.87	$0.83 + 0.019*SL$	$0.84 + 0.015*SL$	$0.87 + 0.014*SL$
	tPHL	0.90	$0.87 + 0.016*SL$	$0.88 + 0.011*SL$	$0.93 + 0.008*SL$
	tR	0.28	$0.23 + 0.027*SL$	$0.22 + 0.030*SL$	$0.20 + 0.031*SL$
	tF	0.22	$0.20 + 0.013*SL$	$0.20 + 0.014*SL$	$0.22 + 0.013*SL$
C to Y	tPLH	0.73	$0.69 + 0.019*SL$	$0.70 + 0.015*SL$	$0.72 + 0.014*SL$
	tPHL	0.77	$0.74 + 0.016*SL$	$0.75 + 0.011*SL$	$0.80 + 0.008*SL$
	tR	0.28	$0.22 + 0.027*SL$	$0.22 + 0.030*SL$	$0.20 + 0.031*SL$
	tF	0.22	$0.19 + 0.017*SL$	$0.20 + 0.014*SL$	$0.22 + 0.013*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# XO2/XO2D2/XO2D3/XO2D5

2 Input Exclusive OR with 1X Drive, 2X Drive, 3X Drive or 5x Drive

Inputs: A, B

Output: Y

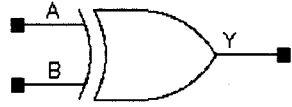
Input Loading (SL): All: A : 1, B : 2

Maximum Fanout (Rec. SL):

- XO2: 28
- XO2D2: 56
- XO2D3: 84
- XO2D5: 140

Gate Count:

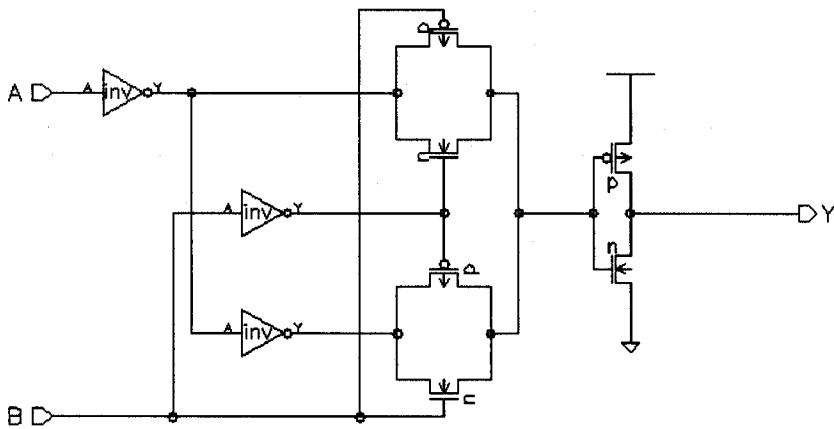
- XO2: 3
- XO2D2: 4
- XO2D3: 4
- XO2D5: 5



Symbol

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table



Schematic

**XO2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.64	$0.55 + 0.043*SL$	$0.56 + 0.041*SL$	$0.56 + 0.041*SL$
	tPHL	0.55	$0.48 + 0.036*SL$	$0.51 + 0.024*SL$	$0.59 + 0.020*SL$
	tR	0.31	$0.12 + 0.092*SL$	$0.11 + 0.096*SL$	$0.09 + 0.097*SL$
	tF	0.26	$0.18 + 0.040*SL$	$0.19 + 0.036*SL$	$0.18 + 0.037*SL$
B to Y	tPLH	0.52	$0.43 + 0.043*SL$	$0.43 + 0.041*SL$	$0.43 + 0.041*SL$
	tPHL	0.43	$0.37 + 0.032*SL$	$0.39 + 0.023*SL$	$0.45 + 0.020*SL$
	tR	0.31	$0.12 + 0.093*SL$	$0.11 + 0.096*SL$	$0.09 + 0.097*SL$
	tF	0.21	$0.13 + 0.039*SL$	$0.14 + 0.037*SL$	$0.14 + 0.037*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **XO2D2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.63	$0.58 + 0.022*SL$	$0.59 + 0.020*SL$	$0.59 + 0.020*SL$
	tPHL	0.56	$0.51 + 0.022*SL$	$0.53 + 0.015*SL$	$0.60 + 0.011*SL$
	tR	0.22	$0.13 + 0.044*SL$	$0.13 + 0.045*SL$	$0.10 + 0.047*SL$
	tF	0.24	$0.19 + 0.022*SL$	$0.20 + 0.019*SL$	$0.21 + 0.018*SL$
B to Y	tPLH	0.50	$0.45 + 0.022*SL$	$0.46 + 0.020*SL$	$0.47 + 0.020*SL$
	tPHL	0.43	$0.39 + 0.020*SL$	$0.41 + 0.014*SL$	$0.46 + 0.011*SL$
	tR	0.22	$0.13 + 0.045*SL$	$0.13 + 0.045*SL$	$0.11 + 0.047*SL$
	tF	0.19	$0.14 + 0.021*SL$	$0.15 + 0.020*SL$	$0.17 + 0.019*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# XO2D3/XO2D5

2 Input Exclusive OR with 3X Drive or 5x Drive

## XO2D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.65	$0.62 + 0.016*SL$	$0.63 + 0.015*SL$	$0.64 + 0.014*SL$
	tPHL	0.58	$0.55 + 0.017*SL$	$0.57 + 0.012*SL$	$0.62 + 0.009*SL$
	tR	0.21	$0.15 + 0.031*SL$	$0.15 + 0.032*SL$	$0.13 + 0.033*SL$
	tF	0.25	$0.22 + 0.016*SL$	$0.23 + 0.014*SL$	$0.24 + 0.013*SL$
B to Y	tPLH	0.51	$0.48 + 0.017*SL$	$0.49 + 0.015*SL$	$0.50 + 0.014*SL$
	tPHL	0.44	$0.41 + 0.015*SL$	$0.42 + 0.011*SL$	$0.47 + 0.009*SL$
	tR	0.21	$0.15 + 0.031*SL$	$0.15 + 0.032*SL$	$0.13 + 0.033*SL$
	tF	0.20	$0.17 + 0.015*SL$	$0.17 + 0.015*SL$	$0.19 + 0.014*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## XO2D5 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.71	$0.69 + 0.011*SL$	$0.69 + 0.009*SL$	$0.70 + 0.009*SL$
	tPHL	0.65	$0.62 + 0.011*SL$	$0.63 + 0.008*SL$	$0.67 + 0.006*SL$
	tR	0.23	$0.19 + 0.017*SL$	$0.19 + 0.019*SL$	$0.17 + 0.020*SL$
	tF	0.29	$0.27 + 0.010*SL$	$0.27 + 0.009*SL$	$0.29 + 0.008*SL$
B to Y	tPLH	0.56	$0.54 + 0.011*SL$	$0.55 + 0.009*SL$	$0.56 + 0.009*SL$
	tPHL	0.49	$0.46 + 0.011*SL$	$0.47 + 0.008*SL$	$0.51 + 0.006*SL$
	tR	0.23	$0.19 + 0.017*SL$	$0.19 + 0.019*SL$	$0.17 + 0.020*SL$
	tF	0.23	$0.21 + 0.010*SL$	$0.21 + 0.010*SL$	$0.23 + 0.009*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# XO3/XO3D3

## 3 Input Exclusive OR with 1X Drive or 3X Drive

Inputs: A, B, C

Output: Y

Input Loading (SL):

- XO3: A, C: 2

B: 1

- XO3D2: A, C: 2

B: 1

Maximum Fanout (Rec. SL):

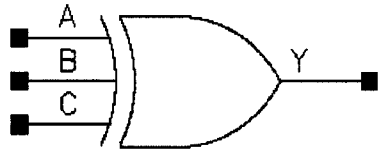
- XO3: 28

- XO3D2: 84

Gate Count:

- XO3: 5

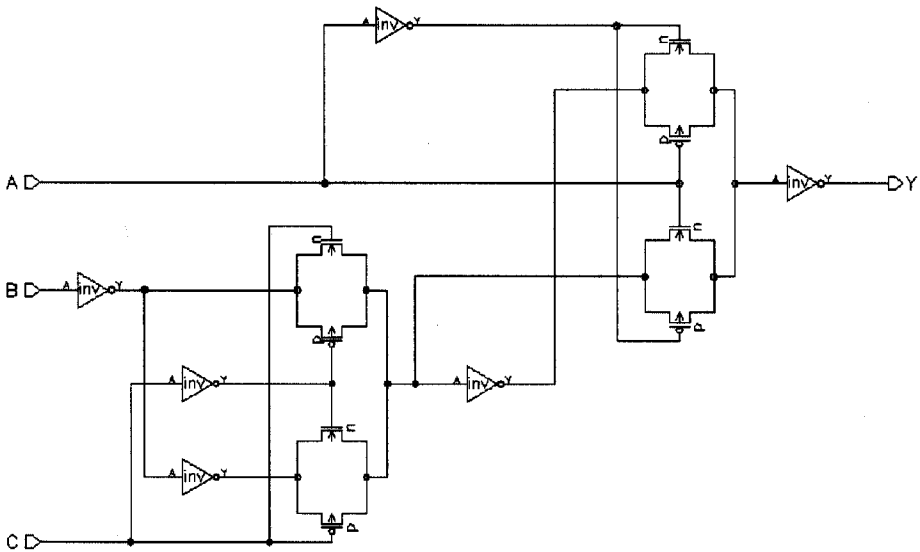
- XO3D2: 6



Symbol

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Truth Table



Schematic

**XO3 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.51	$0.43 + 0.044*SL$	$0.43 + 0.041*SL$	$0.43 + 0.041*SL$
	tPHL	0.44	$0.37 + 0.033*SL$	$0.40 + 0.024*SL$	$0.46 + 0.020*SL$
	tR	0.31	$0.12 + 0.093*SL$	$0.11 + 0.096*SL$	$0.09 + 0.097*SL$
	tF	0.22	$0.13 + 0.042*SL$	$0.14 + 0.037*SL$	$0.15 + 0.037*SL$
B to Y	tPLH	0.87	$0.78 + 0.043*SL$	$0.79 + 0.041*SL$	$0.79 + 0.041*SL$
	tPHL	0.86	$0.79 + 0.034*SL$	$0.83 + 0.024*SL$	$0.89 + 0.020*SL$
	tR	0.32	$0.14 + 0.090*SL$	$0.12 + 0.095*SL$	$0.09 + 0.097*SL$
	tF	0.23	$0.15 + 0.041*SL$	$0.16 + 0.037*SL$	$0.16 + 0.037*SL$
C to Y	tPLH	0.74	$0.65 + 0.044*SL$	$0.66 + 0.041*SL$	$0.66 + 0.041*SL$
	tPHL	0.73	$0.66 + 0.035*SL$	$0.70 + 0.024*SL$	$0.77 + 0.020*SL$
	tR	0.31	$0.13 + 0.091*SL$	$0.12 + 0.096*SL$	$0.09 + 0.097*SL$
	tF	0.23	$0.16 + 0.038*SL$	$0.16 + 0.037*SL$	$0.16 + 0.037*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **XO3D3 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.52	$0.49 + 0.016*SL$	$0.49 + 0.014*SL$	$0.50 + 0.014*SL$
	tPHL	0.45	$0.42 + 0.015*SL$	$0.44 + 0.011*SL$	$0.48 + 0.009*SL$
	tR	0.20	$0.15 + 0.030*SL$	$0.14 + 0.031*SL$	$0.13 + 0.031*SL$
	tF	0.20	$0.17 + 0.015*SL$	$0.17 + 0.014*SL$	$0.20 + 0.013*SL$
B to Y	tPLH	0.86	$0.82 + 0.019*SL$	$0.83 + 0.015*SL$	$0.86 + 0.014*SL$
	tPHL	0.89	$0.86 + 0.016*SL$	$0.88 + 0.011*SL$	$0.93 + 0.009*SL$
	tR	0.28	$0.22 + 0.026*SL$	$0.21 + 0.030*SL$	$0.19 + 0.031*SL$
	tF	0.22	$0.19 + 0.015*SL$	$0.20 + 0.014*SL$	$0.22 + 0.013*SL$
C to Y	tPLH	0.76	$0.73 + 0.016*SL$	$0.73 + 0.014*SL$	$0.74 + 0.014*SL$
	tPHL	0.76	$0.73 + 0.016*SL$	$0.75 + 0.011*SL$	$0.80 + 0.009*SL$
	tR	0.21	$0.15 + 0.030*SL$	$0.15 + 0.030*SL$	$0.13 + 0.031*SL$
	tF	0.22	$0.20 + 0.013*SL$	$0.20 + 0.014*SL$	$0.22 + 0.013*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# DC4/DC4D2/DC4D4

2>4 Non-Inverting Decoder with 1X Drive, 2X Drive or 4X Drive

Inputs: S0, S1

Outputs: Y0, Y1, Y2, Y3

Input Loading (SL):

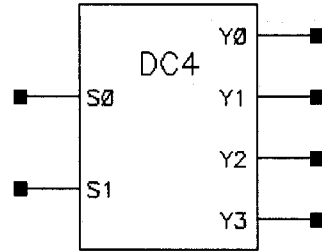
- DC4: All : 3
- DC4D2: All: 3
- DC4D4: All: 3

Maximum Fanout (Rec. SL):

- DC4: 28
- DC4D2: 56
- DC4D4: 112

Gate Count:

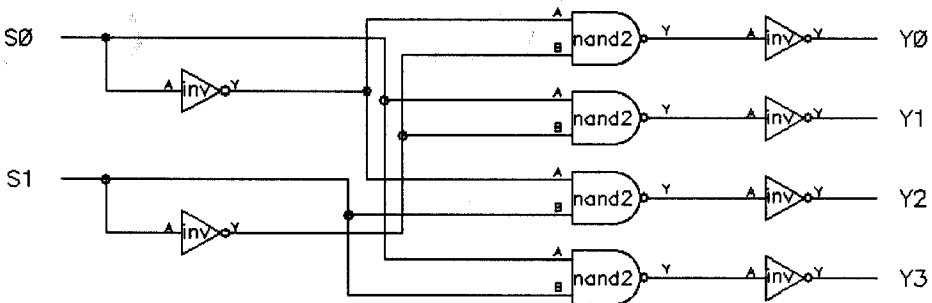
- DC4: 7
- DC4D2: 9
- DC4D4: 13



Symbol

S1	S0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Truth Table



Schematic

## DC4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{p}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to Y0	tPLH	0.59	$0.50 + 0.040 \cdot \text{SL}$	$0.51 + 0.040 \cdot \text{SL}$	$0.50 + 0.040 \cdot \text{SL}$
	tPHL	0.29	$0.24 + 0.026 \cdot \text{SL}$	$0.25 + 0.021 \cdot \text{SL}$	$0.26 + 0.020 \cdot \text{SL}$
	tR	0.29	$0.11 + 0.089 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.093 \cdot \text{SL}$
	tF	0.16	$0.09 + 0.037 \cdot \text{SL}$	$0.08 + 0.040 \cdot \text{SL}$	$0.05 + 0.041 \cdot \text{SL}$
S1 to Y0	tPLH	0.58	$0.50 + 0.042 \cdot \text{SL}$	$0.50 + 0.040 \cdot \text{SL}$	$0.50 + 0.040 \cdot \text{SL}$
	tPHL	0.34	$0.29 + 0.028 \cdot \text{SL}$	$0.31 + 0.021 \cdot \text{SL}$	$0.32 + 0.020 \cdot \text{SL}$
	tR	0.29	$0.11 + 0.090 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.093 \cdot \text{SL}$
	tF	0.18	$0.10 + 0.037 \cdot \text{SL}$	$0.10 + 0.039 \cdot \text{SL}$	$0.06 + 0.041 \cdot \text{SL}$
S0 to Y1	tPLH	0.29	$0.21 + 0.042 \cdot \text{SL}$	$0.21 + 0.040 \cdot \text{SL}$	$0.21 + 0.040 \cdot \text{SL}$
	tPHL	0.35	$0.30 + 0.027 \cdot \text{SL}$	$0.31 + 0.021 \cdot \text{SL}$	$0.33 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.13 + 0.087 \cdot \text{SL}$	$0.11 + 0.091 \cdot \text{SL}$	$0.09 + 0.093 \cdot \text{SL}$
	tF	0.19	$0.12 + 0.036 \cdot \text{SL}$	$0.11 + 0.039 \cdot \text{SL}$	$0.07 + 0.041 \cdot \text{SL}$
S1 to Y1	tPLH	0.58	$0.50 + 0.042 \cdot \text{SL}$	$0.51 + 0.040 \cdot \text{SL}$	$0.51 + 0.040 \cdot \text{SL}$
	tPHL	0.35	$0.30 + 0.028 \cdot \text{SL}$	$0.32 + 0.021 \cdot \text{SL}$	$0.34 + 0.020 \cdot \text{SL}$
	tR	0.29	$0.11 + 0.089 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.093 \cdot \text{SL}$
	tF	0.18	$0.11 + 0.038 \cdot \text{SL}$	$0.11 + 0.039 \cdot \text{SL}$	$0.07 + 0.041 \cdot \text{SL}$
S0 to Y2	tPLH	0.59	$0.50 + 0.040 \cdot \text{SL}$	$0.51 + 0.040 \cdot \text{SL}$	$0.50 + 0.040 \cdot \text{SL}$
	tPHL	0.29	$0.24 + 0.026 \cdot \text{SL}$	$0.25 + 0.021 \cdot \text{SL}$	$0.26 + 0.020 \cdot \text{SL}$
	tR	0.29	$0.11 + 0.089 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.093 \cdot \text{SL}$
	tF	0.16	$0.09 + 0.037 \cdot \text{SL}$	$0.08 + 0.040 \cdot \text{SL}$	$0.05 + 0.041 \cdot \text{SL}$
S1 to Y2	tPLH	0.27	$0.18 + 0.042 \cdot \text{SL}$	$0.19 + 0.040 \cdot \text{SL}$	$0.19 + 0.040 \cdot \text{SL}$
	tPHL	0.41	$0.35 + 0.029 \cdot \text{SL}$	$0.37 + 0.021 \cdot \text{SL}$	$0.39 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.13 + 0.087 \cdot \text{SL}$	$0.12 + 0.091 \cdot \text{SL}$	$0.09 + 0.093 \cdot \text{SL}$
	tF	0.20	$0.13 + 0.034 \cdot \text{SL}$	$0.12 + 0.038 \cdot \text{SL}$	$0.07 + 0.041 \cdot \text{SL}$
S0 to Y3	tPLH	0.29	$0.21 + 0.042 \cdot \text{SL}$	$0.21 + 0.040 \cdot \text{SL}$	$0.21 + 0.040 \cdot \text{SL}$
	tPHL	0.35	$0.30 + 0.027 \cdot \text{SL}$	$0.31 + 0.021 \cdot \text{SL}$	$0.33 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.13 + 0.087 \cdot \text{SL}$	$0.11 + 0.091 \cdot \text{SL}$	$0.09 + 0.093 \cdot \text{SL}$
	tF	0.19	$0.12 + 0.036 \cdot \text{SL}$	$0.11 + 0.039 \cdot \text{SL}$	$0.07 + 0.041 \cdot \text{SL}$
S1 to Y3	tPLH	0.27	$0.18 + 0.043 \cdot \text{SL}$	$0.19 + 0.040 \cdot \text{SL}$	$0.19 + 0.040 \cdot \text{SL}$
	tPHL	0.42	$0.36 + 0.029 \cdot \text{SL}$	$0.38 + 0.021 \cdot \text{SL}$	$0.40 + 0.020 \cdot \text{SL}$
	tR	0.31	$0.13 + 0.087 \cdot \text{SL}$	$0.12 + 0.091 \cdot \text{SL}$	$0.09 + 0.093 \cdot \text{SL}$
	tF	0.21	$0.14 + 0.034 \cdot \text{SL}$	$0.13 + 0.038 \cdot \text{SL}$	$0.08 + 0.041 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

# DC4D2

## 2>4 Non-Inverting Decoder with 2X Drive

### DC4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{q}$  and  $t_{f} = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to Y0	tPLH	0.59	$0.55 + 0.024 * SL$	$0.55 + 0.022 * SL$	$0.56 + 0.021 * SL$
	tPHL	0.30	$0.27 + 0.016 * SL$	$0.28 + 0.012 * SL$	$0.31 + 0.010 * SL$
	tR	0.23	$0.13 + 0.047 * SL$	$0.12 + 0.051 * SL$	$0.10 + 0.052 * SL$
	tF	0.15	$0.11 + 0.019 * SL$	$0.11 + 0.020 * SL$	$0.09 + 0.020 * SL$
S1 to Y0	tPLH	0.59	$0.54 + 0.023 * SL$	$0.55 + 0.022 * SL$	$0.55 + 0.022 * SL$
	tPHL	0.36	$0.32 + 0.018 * SL$	$0.34 + 0.012 * SL$	$0.38 + 0.010 * SL$
	tR	0.23	$0.13 + 0.049 * SL$	$0.12 + 0.051 * SL$	$0.10 + 0.052 * SL$
	tF	0.17	$0.13 + 0.021 * SL$	$0.13 + 0.019 * SL$	$0.12 + 0.020 * SL$
S0 to Y1	tPLH	0.31	$0.26 + 0.024 * SL$	$0.27 + 0.022 * SL$	$0.27 + 0.021 * SL$
	tPHL	0.37	$0.33 + 0.018 * SL$	$0.35 + 0.012 * SL$	$0.38 + 0.010 * SL$
	tR	0.24	$0.14 + 0.049 * SL$	$0.14 + 0.050 * SL$	$0.11 + 0.052 * SL$
	tF	0.18	$0.14 + 0.017 * SL$	$0.14 + 0.019 * SL$	$0.11 + 0.020 * SL$
S1 to Y1	tPLH	0.59	$0.54 + 0.024 * SL$	$0.54 + 0.022 * SL$	$0.55 + 0.021 * SL$
	tPHL	0.36	$0.32 + 0.018 * SL$	$0.34 + 0.012 * SL$	$0.37 + 0.010 * SL$
	tR	0.23	$0.13 + 0.050 * SL$	$0.12 + 0.051 * SL$	$0.10 + 0.052 * SL$
	tF	0.17	$0.13 + 0.020 * SL$	$0.13 + 0.019 * SL$	$0.11 + 0.020 * SL$
S0 to Y2	tPLH	0.59	$0.55 + 0.024 * SL$	$0.55 + 0.022 * SL$	$0.56 + 0.021 * SL$
	tPHL	0.30	$0.27 + 0.017 * SL$	$0.28 + 0.012 * SL$	$0.31 + 0.010 * SL$
	tR	0.23	$0.13 + 0.047 * SL$	$0.12 + 0.051 * SL$	$0.10 + 0.052 * SL$
	tF	0.15	$0.11 + 0.019 * SL$	$0.11 + 0.020 * SL$	$0.09 + 0.020 * SL$
S1 to Y2	tPLH	0.28	$0.23 + 0.024 * SL$	$0.24 + 0.022 * SL$	$0.24 + 0.021 * SL$
	tPHL	0.43	$0.39 + 0.019 * SL$	$0.41 + 0.012 * SL$	$0.45 + 0.010 * SL$
	tR	0.24	$0.15 + 0.049 * SL$	$0.14 + 0.050 * SL$	$0.11 + 0.052 * SL$
	tF	0.20	$0.17 + 0.016 * SL$	$0.16 + 0.018 * SL$	$0.13 + 0.020 * SL$
S0 to Y3	tPLH	0.31	$0.26 + 0.024 * SL$	$0.27 + 0.022 * SL$	$0.27 + 0.021 * SL$
	tPHL	0.37	$0.33 + 0.018 * SL$	$0.35 + 0.012 * SL$	$0.38 + 0.010 * SL$
	tR	0.24	$0.14 + 0.049 * SL$	$0.14 + 0.051 * SL$	$0.11 + 0.052 * SL$
	tF	0.18	$0.14 + 0.017 * SL$	$0.14 + 0.019 * SL$	$0.11 + 0.020 * SL$
S1 to Y3	tPLH	0.28	$0.23 + 0.024 * SL$	$0.23 + 0.022 * SL$	$0.24 + 0.021 * SL$
	tPHL	0.43	$0.39 + 0.019 * SL$	$0.41 + 0.012 * SL$	$0.45 + 0.010 * SL$
	tR	0.24	$0.14 + 0.049 * SL$	$0.14 + 0.050 * SL$	$0.11 + 0.052 * SL$
	tF	0.19	$0.16 + 0.018 * SL$	$0.16 + 0.018 * SL$	$0.13 + 0.020 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**DC4D4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to Y0	tPLH	0.66	$0.63 + 0.014 * SL$	$0.64 + 0.011 * SL$	$0.65 + 0.011 * SL$
	tPHL	0.36	$0.34 + 0.010 * SL$	$0.35 + 0.007 * SL$	$0.38 + 0.006 * SL$
	tR	0.21	$0.17 + 0.022 * SL$	$0.16 + 0.025 * SL$	$0.14 + 0.026 * SL$
	tF	0.18	$0.16 + 0.009 * SL$	$0.16 + 0.010 * SL$	$0.15 + 0.010 * SL$
S1 to Y0	tPLH	0.65	$0.62 + 0.013 * SL$	$0.62 + 0.011 * SL$	$0.64 + 0.011 * SL$
	tPHL	0.41	$0.39 + 0.011 * SL$	$0.40 + 0.008 * SL$	$0.44 + 0.006 * SL$
	tR	0.21	$0.17 + 0.023 * SL$	$0.16 + 0.025 * SL$	$0.14 + 0.026 * SL$
	tF	0.20	$0.18 + 0.010 * SL$	$0.18 + 0.010 * SL$	$0.18 + 0.010 * SL$
S0 to Y1	tPLH	0.38	$0.36 + 0.013 * SL$	$0.36 + 0.011 * SL$	$0.37 + 0.010 * SL$
	tPHL	0.43	$0.41 + 0.010 * SL$	$0.42 + 0.007 * SL$	$0.45 + 0.006 * SL$
	tR	0.22	$0.18 + 0.020 * SL$	$0.17 + 0.023 * SL$	$0.15 + 0.024 * SL$
	tF	0.20	$0.18 + 0.009 * SL$	$0.18 + 0.009 * SL$	$0.17 + 0.009 * SL$
S1 to Y1	tPLH	0.64	$0.61 + 0.013 * SL$	$0.62 + 0.011 * SL$	$0.63 + 0.010 * SL$
	tPHL	0.41	$0.39 + 0.011 * SL$	$0.40 + 0.008 * SL$	$0.44 + 0.006 * SL$
	tR	0.20	$0.16 + 0.022 * SL$	$0.16 + 0.023 * SL$	$0.14 + 0.024 * SL$
	tF	0.20	$0.17 + 0.011 * SL$	$0.18 + 0.009 * SL$	$0.17 + 0.010 * SL$
S0 to Y2	tPLH	0.66	$0.63 + 0.014 * SL$	$0.64 + 0.011 * SL$	$0.65 + 0.011 * SL$
	tPHL	0.36	$0.34 + 0.011 * SL$	$0.35 + 0.007 * SL$	$0.38 + 0.006 * SL$
	tR	0.21	$0.17 + 0.022 * SL$	$0.16 + 0.025 * SL$	$0.14 + 0.026 * SL$
	tF	0.18	$0.16 + 0.008 * SL$	$0.16 + 0.010 * SL$	$0.15 + 0.010 * SL$
S1 to Y2	tPLH	0.34	$0.32 + 0.013 * SL$	$0.32 + 0.011 * SL$	$0.33 + 0.011 * SL$
	tPHL	0.48	$0.46 + 0.012 * SL$	$0.47 + 0.008 * SL$	$0.51 + 0.006 * SL$
	tR	0.22	$0.18 + 0.022 * SL$	$0.17 + 0.024 * SL$	$0.15 + 0.025 * SL$
	tF	0.22	$0.20 + 0.009 * SL$	$0.20 + 0.009 * SL$	$0.20 + 0.009 * SL$
S0 to Y3	tPLH	0.38	$0.36 + 0.013 * SL$	$0.36 + 0.011 * SL$	$0.37 + 0.010 * SL$
	tPHL	0.43	$0.41 + 0.010 * SL$	$0.42 + 0.007 * SL$	$0.45 + 0.006 * SL$
	tR	0.22	$0.18 + 0.021 * SL$	$0.17 + 0.023 * SL$	$0.15 + 0.024 * SL$
	tF	0.20	$0.18 + 0.009 * SL$	$0.18 + 0.009 * SL$	$0.17 + 0.009 * SL$
S1 to Y3	tPLH	0.34	$0.31 + 0.012 * SL$	$0.32 + 0.011 * SL$	$0.33 + 0.010 * SL$
	tPHL	0.48	$0.46 + 0.011 * SL$	$0.47 + 0.008 * SL$	$0.51 + 0.006 * SL$
	tR	0.22	$0.18 + 0.020 * SL$	$0.17 + 0.023 * SL$	$0.15 + 0.024 * SL$
	tF	0.22	$0.20 + 0.009 * SL$	$0.20 + 0.009 * SL$	$0.19 + 0.009 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# DC4I/DC4ID2/DC4ID4

2>4 Inverting Decoder with 1X Drive, 2X Drive or 4X Drive

Inputs: S0, S1  
Outputs: YN0, YN1, YN2, YN3

Input Loading (SL):

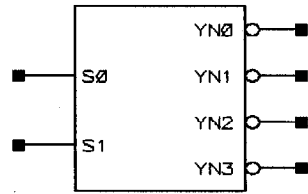
- DC4I: All : 3
- DC4ID2: All: 3
- DC4ID4: All: 3

Maximum Fanout (Rec. SL):

- DC4I: 28
- DC4ID2: 56
- DC4ID4: 112

Gate Count:

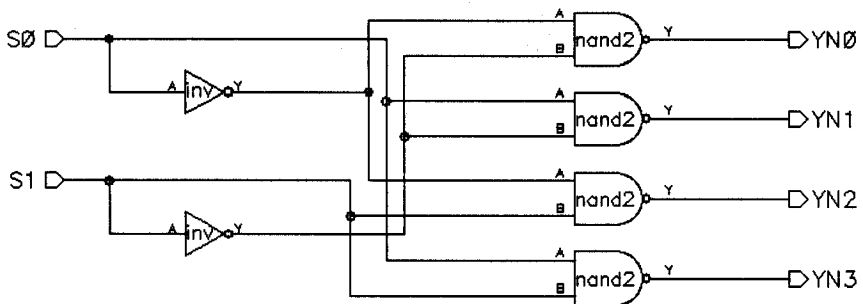
- DC4I: 5
- DC4ID2: 9
- DC4ID4: 13



Symbol

S1	S0	YN0	YN1	YN2	YN3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Truth Table



Schematic

**DC4I Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{RQ}$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN0	tPLH	0.24	$0.16 + 0.042*SL$	$0.16 + 0.041*SL$	$0.16 + 0.041*SL$
	tPHL	0.46	$0.38 + 0.036*SL$	$0.40 + 0.031*SL$	$0.41 + 0.031*SL$
	tR	0.33	$0.14 + 0.092*SL$	$0.14 + 0.094*SL$	$0.12 + 0.095*SL$
	tF	0.28	$0.16 + 0.060*SL$	$0.15 + 0.065*SL$	$0.11 + 0.067*SL$
S1 to YN0	tPLH	0.29	$0.21 + 0.041*SL$	$0.21 + 0.041*SL$	$0.21 + 0.041*SL$
	tPHL	0.45	$0.38 + 0.034*SL$	$0.39 + 0.031*SL$	$0.39 + 0.030*SL$
	tR	0.40	$0.22 + 0.087*SL$	$0.20 + 0.094*SL$	$0.18 + 0.095*SL$
	tF	0.27	$0.15 + 0.059*SL$	$0.14 + 0.065*SL$	$0.10 + 0.067*SL$
S0 to YN1	tPLH	0.32	$0.21 + 0.051*SL$	$0.24 + 0.042*SL$	$0.24 + 0.042*SL$
	tPHL	0.16	$0.07 + 0.048*SL$	$0.11 + 0.033*SL$	$0.16 + 0.031*SL$
	tR	0.49	$0.32 + 0.085*SL$	$0.29 + 0.095*SL$	$0.17 + 0.101*SL$
	tF	0.44	$0.32 + 0.060*SL$	$0.31 + 0.062*SL$	$0.21 + 0.067*SL$
S1 to YN1	tPLH	0.30	$0.22 + 0.043*SL$	$0.22 + 0.043*SL$	$0.22 + 0.043*SL$
	tPHL	0.45	$0.38 + 0.033*SL$	$0.39 + 0.031*SL$	$0.39 + 0.031*SL$
	tR	0.42	$0.23 + 0.094*SL$	$0.21 + 0.101*SL$	$0.19 + 0.102*SL$
	tF	0.28	$0.16 + 0.061*SL$	$0.14 + 0.067*SL$	$0.10 + 0.069*SL$
S0 to YN2	tPLH	0.24	$0.16 + 0.042*SL$	$0.16 + 0.041*SL$	$0.16 + 0.041*SL$
	tPHL	0.46	$0.38 + 0.036*SL$	$0.40 + 0.031*SL$	$0.41 + 0.031*SL$
	tR	0.33	$0.14 + 0.091*SL$	$0.14 + 0.094*SL$	$0.12 + 0.095*SL$
	tF	0.28	$0.16 + 0.060*SL$	$0.15 + 0.065*SL$	$0.11 + 0.067*SL$
S1 to YN2	tPLH	0.37	$0.28 + 0.044*SL$	$0.29 + 0.039*SL$	$0.28 + 0.040*SL$
	tPHL	0.13	$0.04 + 0.042*SL$	$0.07 + 0.031*SL$	$0.10 + 0.030*SL$
	tR	0.54	$0.39 + 0.077*SL$	$0.36 + 0.087*SL$	$0.23 + 0.094*SL$
	tF	0.40	$0.30 + 0.051*SL$	$0.27 + 0.060*SL$	$0.17 + 0.065*SL$
S0 to YN3	tPLH	0.32	$0.21 + 0.051*SL$	$0.24 + 0.042*SL$	$0.24 + 0.042*SL$
	tPHL	0.16	$0.07 + 0.048*SL$	$0.11 + 0.033*SL$	$0.16 + 0.031*SL$
	tR	0.49	$0.32 + 0.085*SL$	$0.29 + 0.095*SL$	$0.17 + 0.101*SL$
	tF	0.44	$0.32 + 0.060*SL$	$0.31 + 0.062*SL$	$0.21 + 0.067*SL$
S1 to YN3	tPLH	0.38	$0.29 + 0.045*SL$	$0.30 + 0.041*SL$	$0.28 + 0.042*SL$
	tPHL	0.12	$0.04 + 0.042*SL$	$0.07 + 0.032*SL$	$0.09 + 0.031*SL$
	tR	0.57	$0.40 + 0.083*SL$	$0.37 + 0.095*SL$	$0.24 + 0.101*SL$
	tF	0.41	$0.30 + 0.053*SL$	$0.27 + 0.063*SL$	$0.17 + 0.068*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# DC4ID2

## 2>4 Inverting Decoder with 2X Drive

### DC4ID2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN0	tPLH	0.20	$0.15 + 0.022 \cdot SL$	$0.15 + 0.021 \cdot SL$	$0.15 + 0.021 \cdot SL$
	tPHL	0.52	$0.48 + 0.020 \cdot SL$	$0.50 + 0.014 \cdot SL$	$0.55 + 0.011 \cdot SL$
	tR	0.22	$0.13 + 0.048 \cdot SL$	$0.12 + 0.051 \cdot SL$	$0.09 + 0.052 \cdot SL$
	tF	0.22	$0.18 + 0.021 \cdot SL$	$0.18 + 0.020 \cdot SL$	$0.17 + 0.020 \cdot SL$
S1 to YN0	tPLH	0.24	$0.19 + 0.023 \cdot SL$	$0.19 + 0.021 \cdot SL$	$0.19 + 0.021 \cdot SL$
	tPHL	0.50	$0.46 + 0.020 \cdot SL$	$0.48 + 0.014 \cdot SL$	$0.53 + 0.011 \cdot SL$
	tR	0.23	$0.14 + 0.048 \cdot SL$	$0.13 + 0.051 \cdot SL$	$0.10 + 0.052 \cdot SL$
	tF	0.22	$0.18 + 0.020 \cdot SL$	$0.18 + 0.020 \cdot SL$	$0.18 + 0.020 \cdot SL$
S0 to YN1	tPLH	0.53	$0.48 + 0.023 \cdot SL$	$0.49 + 0.022 \cdot SL$	$0.49 + 0.022 \cdot SL$
	tPHL	0.41	$0.37 + 0.020 \cdot SL$	$0.39 + 0.014 \cdot SL$	$0.45 + 0.011 \cdot SL$
	tR	0.21	$0.11 + 0.050 \cdot SL$	$0.10 + 0.051 \cdot SL$	$0.09 + 0.052 \cdot SL$
	tF	0.22	$0.18 + 0.018 \cdot SL$	$0.17 + 0.020 \cdot SL$	$0.17 + 0.020 \cdot SL$
S1 to YN1	tPLH	0.24	$0.19 + 0.023 \cdot SL$	$0.20 + 0.021 \cdot SL$	$0.19 + 0.021 \cdot SL$
	tPHL	0.50	$0.46 + 0.020 \cdot SL$	$0.48 + 0.014 \cdot SL$	$0.53 + 0.011 \cdot SL$
	tR	0.23	$0.13 + 0.048 \cdot SL$	$0.13 + 0.051 \cdot SL$	$0.10 + 0.052 \cdot SL$
	tF	0.22	$0.18 + 0.020 \cdot SL$	$0.18 + 0.020 \cdot SL$	$0.18 + 0.020 \cdot SL$
S0 to YN2	tPLH	0.19	$0.15 + 0.022 \cdot SL$	$0.15 + 0.021 \cdot SL$	$0.15 + 0.021 \cdot SL$
	tPHL	0.52	$0.48 + 0.020 \cdot SL$	$0.50 + 0.014 \cdot SL$	$0.55 + 0.011 \cdot SL$
	tR	0.22	$0.13 + 0.048 \cdot SL$	$0.12 + 0.051 \cdot SL$	$0.09 + 0.052 \cdot SL$
	tF	0.22	$0.18 + 0.021 \cdot SL$	$0.18 + 0.020 \cdot SL$	$0.17 + 0.020 \cdot SL$
S1 to YN2	tPLH	0.56	$0.51 + 0.023 \cdot SL$	$0.52 + 0.021 \cdot SL$	$0.52 + 0.021 \cdot SL$
	tPHL	0.44	$0.40 + 0.020 \cdot SL$	$0.42 + 0.014 \cdot SL$	$0.47 + 0.011 \cdot SL$
	tR	0.22	$0.12 + 0.050 \cdot SL$	$0.11 + 0.051 \cdot SL$	$0.09 + 0.052 \cdot SL$
	tF	0.21	$0.17 + 0.019 \cdot SL$	$0.17 + 0.020 \cdot SL$	$0.17 + 0.020 \cdot SL$
S0 to YN3	tPLH	0.53	$0.48 + 0.023 \cdot SL$	$0.49 + 0.022 \cdot SL$	$0.49 + 0.022 \cdot SL$
	tPHL	0.41	$0.37 + 0.020 \cdot SL$	$0.39 + 0.014 \cdot SL$	$0.45 + 0.011 \cdot SL$
	tR	0.21	$0.11 + 0.050 \cdot SL$	$0.10 + 0.051 \cdot SL$	$0.09 + 0.052 \cdot SL$
	tF	0.22	$0.18 + 0.018 \cdot SL$	$0.18 + 0.020 \cdot SL$	$0.17 + 0.020 \cdot SL$
S1 to YN3	tPLH	0.56	$0.51 + 0.023 \cdot SL$	$0.52 + 0.021 \cdot SL$	$0.52 + 0.022 \cdot SL$
	tPHL	0.44	$0.40 + 0.021 \cdot SL$	$0.42 + 0.014 \cdot SL$	$0.47 + 0.011 \cdot SL$
	tR	0.22	$0.12 + 0.050 \cdot SL$	$0.11 + 0.051 \cdot SL$	$0.09 + 0.052 \cdot SL$
	tF	0.21	$0.18 + 0.019 \cdot SL$	$0.17 + 0.020 \cdot SL$	$0.17 + 0.020 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## DC4ID4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{pr}$  and  $t_{pf}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN0	tPLH	0.26	$0.23 + 0.012 \cdot SL$	$0.23 + 0.011 \cdot SL$	$0.24 + 0.011 \cdot SL$
	tPHL	0.62	$0.60 + 0.012 \cdot SL$	$0.61 + 0.009 \cdot SL$	$0.65 + 0.007 \cdot SL$
	tR	0.19	$0.15 + 0.022 \cdot SL$	$0.14 + 0.025 \cdot SL$	$0.12 + 0.026 \cdot SL$
	tF	0.28	$0.25 + 0.011 \cdot SL$	$0.26 + 0.010 \cdot SL$	$0.27 + 0.010 \cdot SL$
S1 to YN0	tPLH	0.29	$0.27 + 0.011 \cdot SL$	$0.27 + 0.011 \cdot SL$	$0.27 + 0.011 \cdot SL$
	tPHL	0.60	$0.57 + 0.013 \cdot SL$	$0.58 + 0.009 \cdot SL$	$0.62 + 0.007 \cdot SL$
	tR	0.20	$0.15 + 0.023 \cdot SL$	$0.15 + 0.025 \cdot SL$	$0.13 + 0.026 \cdot SL$
	tF	0.28	$0.25 + 0.012 \cdot SL$	$0.26 + 0.010 \cdot SL$	$0.27 + 0.010 \cdot SL$
S0 to YN1	tPLH	0.57	$0.55 + 0.011 \cdot SL$	$0.55 + 0.011 \cdot SL$	$0.55 + 0.011 \cdot SL$
	tPHL	0.52	$0.50 + 0.012 \cdot SL$	$0.51 + 0.009 \cdot SL$	$0.55 + 0.007 \cdot SL$
	tR	0.18	$0.13 + 0.024 \cdot SL$	$0.13 + 0.025 \cdot SL$	$0.11 + 0.026 \cdot SL$
	tF	0.27	$0.25 + 0.011 \cdot SL$	$0.25 + 0.010 \cdot SL$	$0.27 + 0.010 \cdot SL$
S1 to YN1	tPLH	0.29	$0.27 + 0.012 \cdot SL$	$0.27 + 0.011 \cdot SL$	$0.28 + 0.011 \cdot SL$
	tPHL	0.60	$0.57 + 0.013 \cdot SL$	$0.59 + 0.009 \cdot SL$	$0.63 + 0.007 \cdot SL$
	tR	0.20	$0.15 + 0.024 \cdot SL$	$0.15 + 0.025 \cdot SL$	$0.13 + 0.026 \cdot SL$
	tF	0.28	$0.25 + 0.013 \cdot SL$	$0.26 + 0.010 \cdot SL$	$0.27 + 0.010 \cdot SL$
S0 to YN2	tPLH	0.25	$0.23 + 0.012 \cdot SL$	$0.23 + 0.011 \cdot SL$	$0.24 + 0.011 \cdot SL$
	tPHL	0.62	$0.60 + 0.012 \cdot SL$	$0.61 + 0.009 \cdot SL$	$0.65 + 0.007 \cdot SL$
	tR	0.19	$0.15 + 0.022 \cdot SL$	$0.14 + 0.025 \cdot SL$	$0.12 + 0.026 \cdot SL$
	tF	0.28	$0.25 + 0.011 \cdot SL$	$0.26 + 0.010 \cdot SL$	$0.27 + 0.010 \cdot SL$
S1 to YN2	tPLH	0.60	$0.57 + 0.012 \cdot SL$	$0.58 + 0.011 \cdot SL$	$0.58 + 0.011 \cdot SL$
	tPHL	0.55	$0.52 + 0.012 \cdot SL$	$0.53 + 0.009 \cdot SL$	$0.58 + 0.007 \cdot SL$
	tR	0.18	$0.13 + 0.025 \cdot SL$	$0.13 + 0.025 \cdot SL$	$0.11 + 0.026 \cdot SL$
	tF	0.27	$0.25 + 0.011 \cdot SL$	$0.25 + 0.010 \cdot SL$	$0.26 + 0.010 \cdot SL$
S0 to YN3	tPLH	0.57	$0.55 + 0.011 \cdot SL$	$0.55 + 0.011 \cdot SL$	$0.55 + 0.011 \cdot SL$
	tPHL	0.52	$0.50 + 0.012 \cdot SL$	$0.51 + 0.009 \cdot SL$	$0.55 + 0.007 \cdot SL$
	tR	0.18	$0.13 + 0.024 \cdot SL$	$0.13 + 0.025 \cdot SL$	$0.11 + 0.026 \cdot SL$
	tF	0.27	$0.25 + 0.011 \cdot SL$	$0.25 + 0.010 \cdot SL$	$0.27 + 0.010 \cdot SL$
S1 to YN3	tPLH	0.60	$0.58 + 0.012 \cdot SL$	$0.58 + 0.011 \cdot SL$	$0.58 + 0.011 \cdot SL$
	tPHL	0.55	$0.53 + 0.013 \cdot SL$	$0.54 + 0.009 \cdot SL$	$0.58 + 0.007 \cdot SL$
	tR	0.18	$0.14 + 0.024 \cdot SL$	$0.13 + 0.025 \cdot SL$	$0.11 + 0.026 \cdot SL$
	tF	0.27	$0.25 + 0.012 \cdot SL$	$0.25 + 0.010 \cdot SL$	$0.26 + 0.010 \cdot SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# MX2/MX2D3

## 2>1 Non-Inverting MUX with 1X Drive or 3X Drive

Inputs: D0, D1, S

Output: Y

Input Loading (SL):

- MX2: D0, D1:1  
S:2

- MX2D3: D0, D1:1  
S:2

Maximum Fanout (Rec. SL):

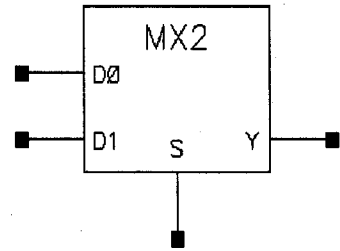
- MX2: 28

- MX2D3: 84

Gate Count:

- MX2: 3

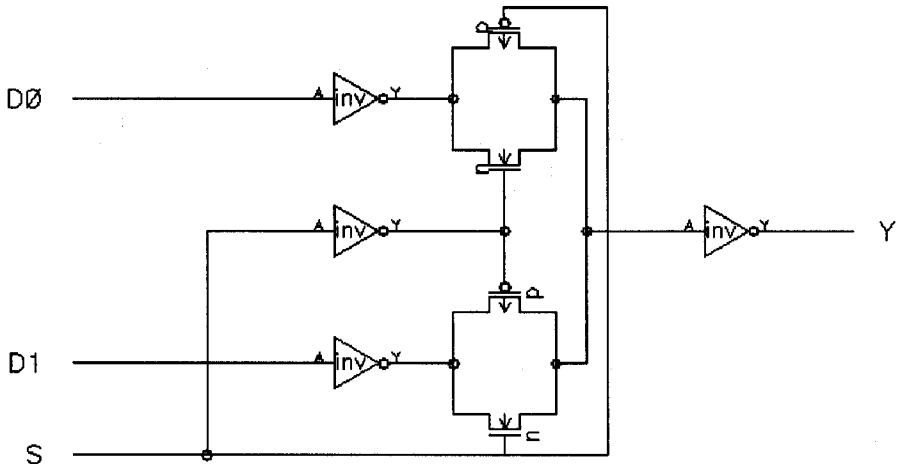
- MX2D3: 4



Symbol

D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

Truth Table



Schematic

**MX2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S to Y	tPLH	0.51	$0.43 + 0.043*SL$	$0.43 + 0.041*SL$	$0.43 + 0.041*SL$
	tPHL	0.43	$0.37 + 0.032*SL$	$0.40 + 0.023*SL$	$0.45 + 0.020*SL$
	tR	0.31	$0.12 + 0.092*SL$	$0.11 + 0.096*SL$	$0.09 + 0.097*SL$
	tF	0.21	$0.13 + 0.041*SL$	$0.14 + 0.037*SL$	$0.13 + 0.037*SL$
D0 to Y	tPLH	0.36	$0.28 + 0.043*SL$	$0.28 + 0.041*SL$	$0.28 + 0.041*SL$
	tPHL	0.51	$0.44 + 0.035*SL$	$0.47 + 0.023*SL$	$0.54 + 0.020*SL$
	tR	0.32	$0.14 + 0.091*SL$	$0.12 + 0.095*SL$	$0.09 + 0.097*SL$
	tF	0.24	$0.17 + 0.036*SL$	$0.17 + 0.036*SL$	$0.15 + 0.037*SL$
D1 to Y	tPLH	0.36	$0.27 + 0.043*SL$	$0.28 + 0.041*SL$	$0.27 + 0.041*SL$
	tPHL	0.52	$0.45 + 0.035*SL$	$0.48 + 0.024*SL$	$0.55 + 0.020*SL$
	tR	0.32	$0.13 + 0.091*SL$	$0.12 + 0.095*SL$	$0.09 + 0.097*SL$
	tF	0.24	$0.16 + 0.040*SL$	$0.17 + 0.036*SL$	$0.16 + 0.037*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**MX2D3 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S to Y	tPLH	0.52	$0.49 + 0.016*SL$	$0.49 + 0.014*SL$	$0.51 + 0.013*SL$
	tPHL	0.45	$0.42 + 0.015*SL$	$0.43 + 0.011*SL$	$0.48 + 0.008*SL$
	tR	0.21	$0.15 + 0.028*SL$	$0.14 + 0.030*SL$	$0.13 + 0.031*SL$
	tF	0.19	$0.16 + 0.016*SL$	$0.17 + 0.014*SL$	$0.19 + 0.013*SL$
D0 to Y	tPLH	0.38	$0.35 + 0.016*SL$	$0.36 + 0.014*SL$	$0.37 + 0.013*SL$
	tPHL	0.54	$0.51 + 0.015*SL$	$0.52 + 0.011*SL$	$0.57 + 0.008*SL$
	tR	0.22	$0.16 + 0.029*SL$	$0.16 + 0.030*SL$	$0.14 + 0.031*SL$
	tF	0.23	$0.21 + 0.012*SL$	$0.20 + 0.013*SL$	$0.22 + 0.012*SL$
D1 to Y	tPLH	0.38	$0.35 + 0.016*SL$	$0.35 + 0.014*SL$	$0.36 + 0.013*SL$
	tPHL	0.55	$0.52 + 0.015*SL$	$0.53 + 0.011*SL$	$0.58 + 0.009*SL$
	tR	0.22	$0.16 + 0.029*SL$	$0.16 + 0.030*SL$	$0.13 + 0.031*SL$
	tF	0.23	$0.21 + 0.013*SL$	$0.21 + 0.013*SL$	$0.22 + 0.013*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# MX2X4/MX2D2X4

4-Bit 2>1 Non-Inverting MUX, 1X Drive or 2X Drive

Inputs: D00, D10, D01, D11, D02, D12,  
D03, D13, S

Outputs: Y0, Y1, Y2, Y3

Input Loading (SL):

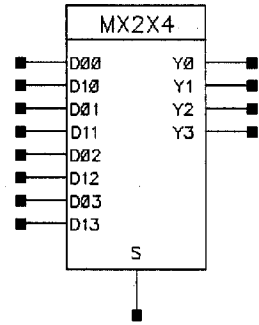
- MX2X4: All : 1
- MX2D2X4: D: 1, S: 4

Maximum Fanout (Rec. SL):

- MX2X4: All : 28
- MX2D2X4: 56

Gate Count:

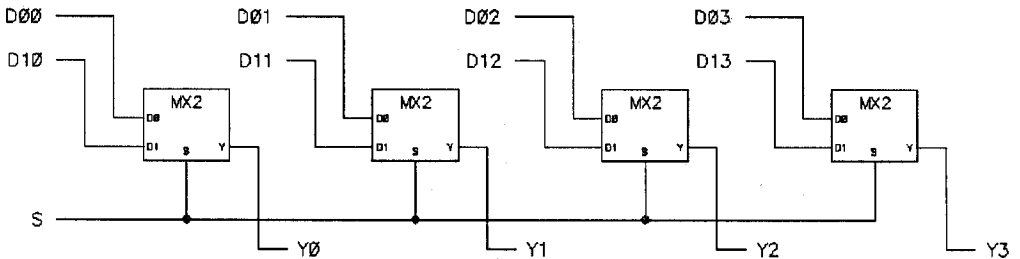
- MX2X4: 11
- MX2D2X4: 13



**Symbol**

S	Y0	Y1	Y2	Y3
0	D00	D01	D02	D03
1	D10	D11	D12	D13

**Truth Table**



**Schematic**

**MX2X4 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S to Y0	tPLH	0.68	$0.60 + 0.042 \cdot SL$	$0.60 + 0.040 \cdot SL$	$0.61 + 0.040 \cdot SL$
	tPHL	0.73	$0.66 + 0.034 \cdot SL$	$0.69 + 0.023 \cdot SL$	$0.75 + 0.020 \cdot SL$
	tR	0.30	$0.12 + 0.089 \cdot SL$	$0.11 + 0.093 \cdot SL$	$0.09 + 0.094 \cdot SL$
	tF	0.22	$0.14 + 0.041 \cdot SL$	$0.15 + 0.037 \cdot SL$	$0.13 + 0.038 \cdot SL$
D00 to Y0	tPLH	0.35	$0.27 + 0.041 \cdot SL$	$0.27 + 0.040 \cdot SL$	$0.27 + 0.040 \cdot SL$
	tPHL	0.51	$0.44 + 0.034 \cdot SL$	$0.47 + 0.023 \cdot SL$	$0.53 + 0.020 \cdot SL$
	tR	0.31	$0.14 + 0.086 \cdot SL$	$0.12 + 0.092 \cdot SL$	$0.09 + 0.094 \cdot SL$
	tF	0.24	$0.17 + 0.036 \cdot SL$	$0.16 + 0.037 \cdot SL$	$0.15 + 0.038 \cdot SL$
D10 to Y0	tPLH	0.35	$0.26 + 0.042 \cdot SL$	$0.27 + 0.040 \cdot SL$	$0.27 + 0.040 \cdot SL$
	tPHL	0.51	$0.44 + 0.035 \cdot SL$	$0.48 + 0.024 \cdot SL$	$0.54 + 0.020 \cdot SL$
	tR	0.31	$0.14 + 0.086 \cdot SL$	$0.12 + 0.092 \cdot SL$	$0.09 + 0.094 \cdot SL$
	tF	0.24	$0.16 + 0.039 \cdot SL$	$0.17 + 0.037 \cdot SL$	$0.15 + 0.038 \cdot SL$
S to Y1	tPLH	0.68	$0.60 + 0.042 \cdot SL$	$0.61 + 0.040 \cdot SL$	$0.61 + 0.040 \cdot SL$
	tPHL	0.73	$0.66 + 0.034 \cdot SL$	$0.69 + 0.023 \cdot SL$	$0.75 + 0.020 \cdot SL$
	tR	0.30	$0.12 + 0.089 \cdot SL$	$0.11 + 0.092 \cdot SL$	$0.09 + 0.094 \cdot SL$
	tF	0.22	$0.14 + 0.041 \cdot SL$	$0.15 + 0.037 \cdot SL$	$0.14 + 0.038 \cdot SL$
D01 to Y1	tPLH	0.36	$0.27 + 0.041 \cdot SL$	$0.28 + 0.040 \cdot SL$	$0.28 + 0.040 \cdot SL$
	tPHL	0.51	$0.44 + 0.034 \cdot SL$	$0.47 + 0.023 \cdot SL$	$0.53 + 0.020 \cdot SL$
	tR	0.31	$0.14 + 0.086 \cdot SL$	$0.12 + 0.092 \cdot SL$	$0.09 + 0.094 \cdot SL$
	tF	0.24	$0.17 + 0.036 \cdot SL$	$0.17 + 0.037 \cdot SL$	$0.15 + 0.038 \cdot SL$
D11 to Y1	tPLH	0.35	$0.27 + 0.041 \cdot SL$	$0.27 + 0.040 \cdot SL$	$0.27 + 0.040 \cdot SL$
	tPHL	0.51	$0.44 + 0.035 \cdot SL$	$0.48 + 0.024 \cdot SL$	$0.54 + 0.020 \cdot SL$
	tR	0.31	$0.14 + 0.086 \cdot SL$	$0.12 + 0.092 \cdot SL$	$0.09 + 0.094 \cdot SL$
	tF	0.24	$0.16 + 0.039 \cdot SL$	$0.17 + 0.037 \cdot SL$	$0.16 + 0.038 \cdot SL$
S to Y2	tPLH	0.68	$0.60 + 0.042 \cdot SL$	$0.61 + 0.040 \cdot SL$	$0.61 + 0.040 \cdot SL$
	tPHL	0.73	$0.66 + 0.034 \cdot SL$	$0.69 + 0.023 \cdot SL$	$0.75 + 0.020 \cdot SL$
	tR	0.30	$0.12 + 0.089 \cdot SL$	$0.11 + 0.092 \cdot SL$	$0.09 + 0.094 \cdot SL$
	tF	0.22	$0.14 + 0.040 \cdot SL$	$0.15 + 0.037 \cdot SL$	$0.13 + 0.038 \cdot SL$
D02 to Y2	tPLH	0.36	$0.27 + 0.041 \cdot SL$	$0.28 + 0.040 \cdot SL$	$0.28 + 0.040 \cdot SL$
	tPHL	0.51	$0.44 + 0.034 \cdot SL$	$0.47 + 0.023 \cdot SL$	$0.53 + 0.020 \cdot SL$
	tR	0.31	$0.14 + 0.086 \cdot SL$	$0.12 + 0.092 \cdot SL$	$0.09 + 0.094 \cdot SL$
	tF	0.24	$0.17 + 0.036 \cdot SL$	$0.17 + 0.037 \cdot SL$	$0.15 + 0.038 \cdot SL$
D12 to Y2	tPLH	0.36	$0.27 + 0.042 \cdot SL$	$0.28 + 0.040 \cdot SL$	$0.28 + 0.040 \cdot SL$
	tPHL	0.51	$0.44 + 0.035 \cdot SL$	$0.47 + 0.024 \cdot SL$	$0.54 + 0.020 \cdot SL$
	tR	0.31	$0.14 + 0.086 \cdot SL$	$0.12 + 0.092 \cdot SL$	$0.09 + 0.094 \cdot SL$
	tF	0.24	$0.16 + 0.039 \cdot SL$	$0.17 + 0.037 \cdot SL$	$0.16 + 0.038 \cdot SL$
S to Y3	tPLH	0.68	$0.60 + 0.042 \cdot SL$	$0.60 + 0.040 \cdot SL$	$0.61 + 0.040 \cdot SL$
	tPHL	0.73	$0.66 + 0.034 \cdot SL$	$0.69 + 0.023 \cdot SL$	$0.75 + 0.020 \cdot SL$
	tR	0.30	$0.12 + 0.089 \cdot SL$	$0.11 + 0.093 \cdot SL$	$0.09 + 0.094 \cdot SL$
	tF	0.22	$0.14 + 0.041 \cdot SL$	$0.15 + 0.037 \cdot SL$	$0.13 + 0.038 \cdot SL$

\*Range1:  $SL < 3.00$ , \*Range2:  $3.00 \leq SL \leq 20.00$ , \*Range3:  $20.00 < SL$

# MX2X4

## 4-Bit 2>1 Non-Inverting MUX

### MX2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D03 to Y3	tPLH	0.35	$0.27 + 0.041 * SL$	$0.27 + 0.040 * SL$	$0.27 + 0.040 * SL$
	tPHL	0.51	$0.44 + 0.034 * SL$	$0.47 + 0.023 * SL$	$0.53 + 0.020 * SL$
	tR	0.31	$0.14 + 0.086 * SL$	$0.12 + 0.092 * SL$	$0.09 + 0.094 * SL$
	tF	0.24	$0.17 + 0.036 * SL$	$0.16 + 0.037 * SL$	$0.15 + 0.038 * SL$
D13 to Y3	tPLH	0.35	$0.26 + 0.042 * SL$	$0.27 + 0.040 * SL$	$0.27 + 0.040 * SL$
	tPHL	0.51	$0.44 + 0.035 * SL$	$0.48 + 0.024 * SL$	$0.54 + 0.020 * SL$
	tR	0.31	$0.14 + 0.086 * SL$	$0.12 + 0.092 * SL$	$0.09 + 0.094 * SL$
	tF	0.24	$0.16 + 0.039 * SL$	$0.17 + 0.037 * SL$	$0.15 + 0.038 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**MX2D2X4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S to Y0	tPLH	0.69	$0.65 + 0.024 * SL$	$0.65 + 0.022 * SL$	$0.66 + 0.021 * SL$
	tPHL	0.73	$0.69 + 0.021 * SL$	$0.71 + 0.014 * SL$	$0.77 + 0.011 * SL$
	tR	0.23	$0.14 + 0.049 * SL$	$0.13 + 0.051 * SL$	$0.11 + 0.052 * SL$
	tF	0.21	$0.17 + 0.020 * SL$	$0.17 + 0.020 * SL$	$0.18 + 0.020 * SL$
D00 to Y0	tPLH	0.36	$0.31 + 0.024 * SL$	$0.32 + 0.022 * SL$	$0.32 + 0.021 * SL$
	tPHL	0.51	$0.47 + 0.021 * SL$	$0.49 + 0.014 * SL$	$0.55 + 0.011 * SL$
	tR	0.25	$0.15 + 0.049 * SL$	$0.14 + 0.050 * SL$	$0.11 + 0.052 * SL$
	tF	0.23	$0.19 + 0.020 * SL$	$0.19 + 0.020 * SL$	$0.19 + 0.019 * SL$
D10 to Y0	tPLH	0.35	$0.31 + 0.024 * SL$	$0.31 + 0.022 * SL$	$0.32 + 0.021 * SL$
	tPHL	0.52	$0.48 + 0.021 * SL$	$0.50 + 0.015 * SL$	$0.56 + 0.012 * SL$
	tR	0.25	$0.15 + 0.048 * SL$	$0.14 + 0.050 * SL$	$0.11 + 0.052 * SL$
	tF	0.23	$0.19 + 0.020 * SL$	$0.19 + 0.020 * SL$	$0.20 + 0.019 * SL$
S to Y1	tPLH	0.70	$0.65 + 0.024 * SL$	$0.66 + 0.022 * SL$	$0.67 + 0.021 * SL$
	tPHL	0.73	$0.68 + 0.021 * SL$	$0.70 + 0.014 * SL$	$0.77 + 0.011 * SL$
	tR	0.24	$0.15 + 0.047 * SL$	$0.13 + 0.051 * SL$	$0.11 + 0.052 * SL$
	tF	0.20	$0.16 + 0.021 * SL$	$0.17 + 0.020 * SL$	$0.18 + 0.019 * SL$
D01 to Y1	tPLH	0.37	$0.32 + 0.024 * SL$	$0.33 + 0.022 * SL$	$0.33 + 0.021 * SL$
	tPHL	0.51	$0.46 + 0.021 * SL$	$0.48 + 0.014 * SL$	$0.55 + 0.011 * SL$
	tR	0.25	$0.15 + 0.048 * SL$	$0.14 + 0.051 * SL$	$0.12 + 0.052 * SL$
	tF	0.22	$0.19 + 0.019 * SL$	$0.19 + 0.019 * SL$	$0.19 + 0.019 * SL$
D11 to Y1	tPLH	0.36	$0.32 + 0.024 * SL$	$0.32 + 0.022 * SL$	$0.33 + 0.021 * SL$
	tPHL	0.51	$0.47 + 0.021 * SL$	$0.49 + 0.015 * SL$	$0.55 + 0.011 * SL$
	tR	0.25	$0.15 + 0.049 * SL$	$0.14 + 0.050 * SL$	$0.11 + 0.052 * SL$
	tF	0.23	$0.19 + 0.020 * SL$	$0.19 + 0.019 * SL$	$0.20 + 0.019 * SL$
S to Y2	tPLH	0.70	$0.65 + 0.024 * SL$	$0.66 + 0.022 * SL$	$0.66 + 0.021 * SL$
	tPHL	0.73	$0.68 + 0.021 * SL$	$0.70 + 0.014 * SL$	$0.76 + 0.011 * SL$
	tR	0.23	$0.14 + 0.049 * SL$	$0.13 + 0.051 * SL$	$0.11 + 0.052 * SL$
	tF	0.20	$0.16 + 0.021 * SL$	$0.17 + 0.020 * SL$	$0.18 + 0.019 * SL$
D02 to Y2	tPLH	0.36	$0.32 + 0.024 * SL$	$0.32 + 0.022 * SL$	$0.33 + 0.021 * SL$
	tPHL	0.51	$0.47 + 0.021 * SL$	$0.49 + 0.014 * SL$	$0.55 + 0.011 * SL$
	tR	0.25	$0.15 + 0.049 * SL$	$0.14 + 0.050 * SL$	$0.11 + 0.052 * SL$
	tF	0.22	$0.18 + 0.019 * SL$	$0.18 + 0.019 * SL$	$0.19 + 0.019 * SL$
D12 to Y2	tPLH	0.36	$0.32 + 0.024 * SL$	$0.32 + 0.022 * SL$	$0.33 + 0.021 * SL$
	tPHL	0.51	$0.47 + 0.021 * SL$	$0.49 + 0.015 * SL$	$0.55 + 0.011 * SL$
	tR	0.25	$0.15 + 0.049 * SL$	$0.14 + 0.050 * SL$	$0.11 + 0.052 * SL$
	tF	0.23	$0.19 + 0.020 * SL$	$0.19 + 0.019 * SL$	$0.20 + 0.019 * SL$
S to Y3	tPLH	0.70	$0.65 + 0.024 * SL$	$0.65 + 0.022 * SL$	$0.66 + 0.021 * SL$
	tPHL	0.73	$0.69 + 0.021 * SL$	$0.71 + 0.014 * SL$	$0.77 + 0.011 * SL$
	tR	0.23	$0.14 + 0.048 * SL$	$0.13 + 0.051 * SL$	$0.11 + 0.052 * SL$
	tF	0.21	$0.17 + 0.020 * SL$	$0.17 + 0.020 * SL$	$0.18 + 0.020 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# MX2D2X4

## 4-Bit 2>1 Non-Inverting MUX,2X Drive

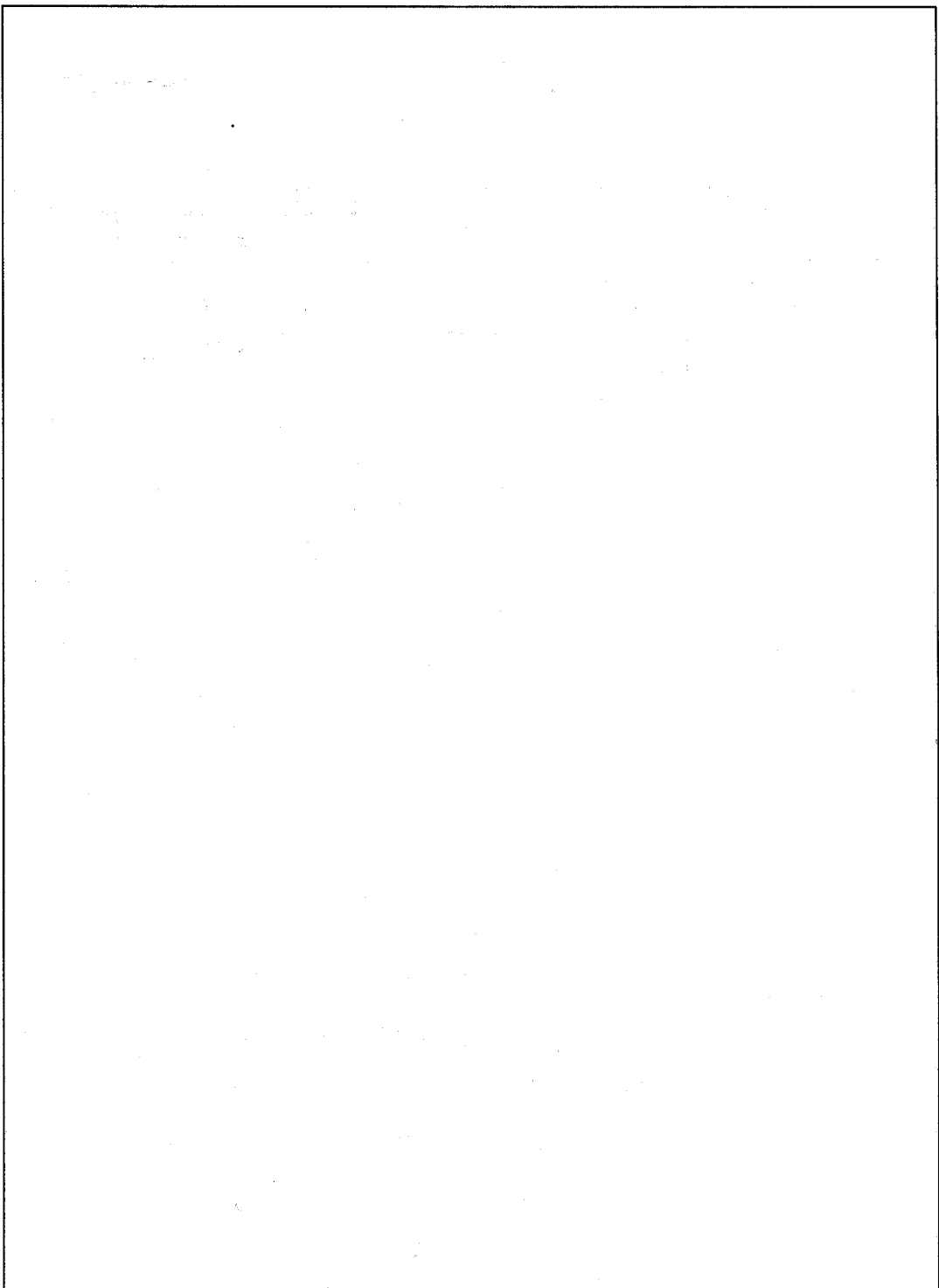
### MX2D2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D03 to Y3	tPLH	0.36	$0.31 + 0.024*SL$	$0.32 + 0.022*SL$	$0.32 + 0.021*SL$
	tPHL	0.51	$0.47 + 0.021*SL$	$0.49 + 0.014*SL$	$0.55 + 0.011*SL$
	tR	0.25	$0.15 + 0.049*SL$	$0.14 + 0.050*SL$	$0.11 + 0.052*SL$
	tF	0.23	$0.19 + 0.020*SL$	$0.19 + 0.020*SL$	$0.19 + 0.019*SL$
D13 to Y3	tPLH	0.35	$0.31 + 0.024*SL$	$0.31 + 0.022*SL$	$0.32 + 0.021*SL$
	tPHL	0.52	$0.48 + 0.021*SL$	$0.50 + 0.015*SL$	$0.56 + 0.012*SL$
	tR	0.25	$0.15 + 0.048*SL$	$0.14 + 0.050*SL$	$0.11 + 0.052*SL$
	tF	0.23	$0.19 + 0.020*SL$	$0.19 + 0.020*SL$	$0.20 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$





# MX2I/MX2ID2/MX2ID3

2>1 Inverting MUX, 1X Drive, 2X Drive or 3X Drive

Inputs: D0, D1, S

Output: YN

Input Loading (SL): S: All : 2

- MX2I: D0, D1: 3

- MX2ID2: D0, D1: 4

- MX2ID3: D0, D1: 5

Maximum Fanout (Rec. SL):

- MX2I: 28

- MX2ID2: 56

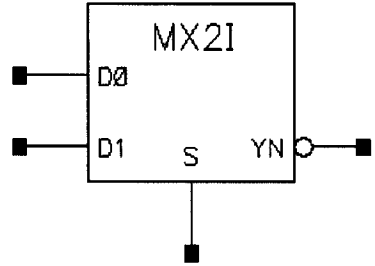
- MX2ID3: 84

Gate Count:

- MX2I: 2

- MX2ID2: 3

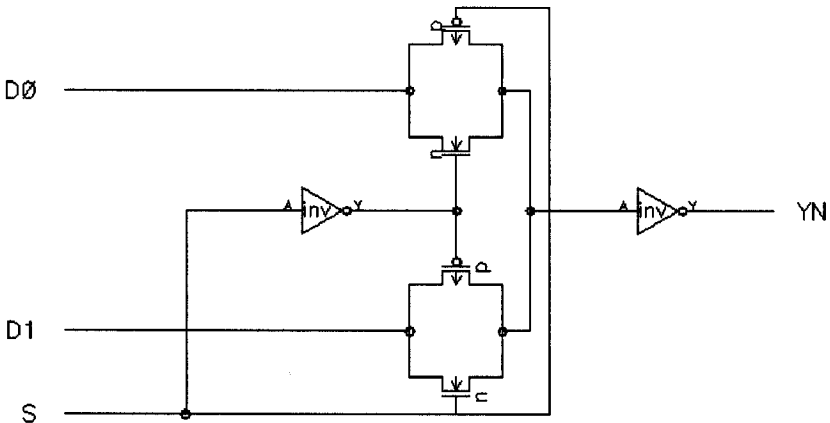
- MX2ID3: 3



Symbol

S	D0	D1	YN
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

Truth Table



Schematic

**MX2I Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	tPLH	0.37	$0.27 + 0.048*SL$	$0.29 + 0.040*SL$	$0.28 + 0.041*SL$
	tPHL	0.11	$0.03 + 0.042*SL$	$0.08 + 0.025*SL$	$0.19 + 0.020*SL$
	tR	0.41	$0.24 + 0.084*SL$	$0.22 + 0.092*SL$	$0.13 + 0.096*SL$
	tF	0.33	$0.25 + 0.039*SL$	$0.27 + 0.034*SL$	$0.24 + 0.036*SL$
D1 to YN	tPLH	0.36	$0.27 + 0.048*SL$	$0.29 + 0.040*SL$	$0.28 + 0.041*SL$
	tPHL	0.11	$0.02 + 0.043*SL$	$0.08 + 0.026*SL$	$0.19 + 0.020*SL$
	tR	0.41	$0.24 + 0.084*SL$	$0.22 + 0.092*SL$	$0.13 + 0.096*SL$
	tF	0.34	$0.26 + 0.040*SL$	$0.27 + 0.034*SL$	$0.24 + 0.035*SL$
S to YN	tPLH	0.48	$0.40 + 0.042*SL$	$0.40 + 0.041*SL$	$0.40 + 0.041*SL$
	tPHL	0.38	$0.32 + 0.027*SL$	$0.34 + 0.021*SL$	$0.36 + 0.020*SL$
	tR	0.29	$0.10 + 0.094*SL$	$0.09 + 0.096*SL$	$0.08 + 0.097*SL$
	tF	0.18	$0.11 + 0.034*SL$	$0.11 + 0.036*SL$	$0.07 + 0.038*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **MX2ID2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	tPLH	0.33	$0.27 + 0.027*SL$	$0.29 + 0.020*SL$	$0.31 + 0.019*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.06 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.32	$0.24 + 0.040*SL$	$0.23 + 0.042*SL$	$0.17 + 0.045*SL$
	tF	0.30	$0.26 + 0.021*SL$	$0.26 + 0.018*SL$	$0.28 + 0.017*SL$
D1 to YN	tPLH	0.32	$0.27 + 0.027*SL$	$0.29 + 0.020*SL$	$0.30 + 0.019*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.06 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.32	$0.24 + 0.040*SL$	$0.23 + 0.042*SL$	$0.17 + 0.045*SL$
	tF	0.30	$0.25 + 0.024*SL$	$0.27 + 0.018*SL$	$0.29 + 0.017*SL$
S to YN	tPLH	0.46	$0.41 + 0.022*SL$	$0.42 + 0.020*SL$	$0.42 + 0.020*SL$
	tPHL	0.38	$0.34 + 0.017*SL$	$0.36 + 0.012*SL$	$0.39 + 0.010*SL$
	tR	0.20	$0.11 + 0.044*SL$	$0.10 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.16	$0.12 + 0.018*SL$	$0.12 + 0.018*SL$	$0.10 + 0.019*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# MX2ID3

2>1 Inverting MUX, 3X Drive

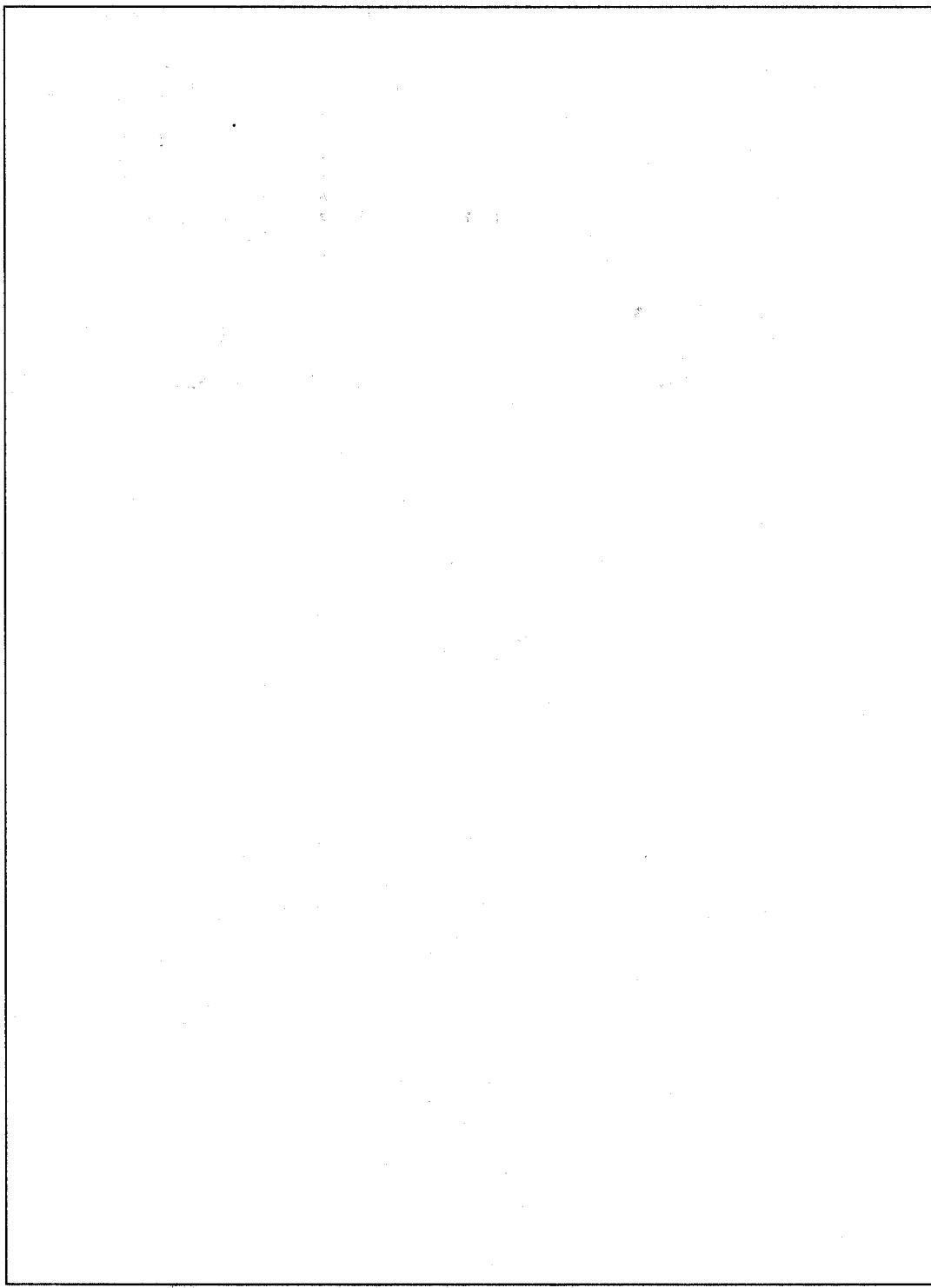
## MX2ID3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	tPLH	0.33	$0.30 + 0.019 * SL$	$0.31 + 0.015 * SL$	$0.33 + 0.014 * SL$
	tPHL	0.08	$0.05 + 0.018 * SL$	$0.06 + 0.012 * SL$	$0.14 + 0.009 * SL$
	tR	0.31	$0.25 + 0.028 * SL$	$0.24 + 0.031 * SL$	$0.20 + 0.033 * SL$
	tF	0.29	$0.27 + 0.014 * SL$	$0.27 + 0.013 * SL$	$0.30 + 0.012 * SL$
D1 to YN	tPLH	0.33	$0.29 + 0.019 * SL$	$0.30 + 0.015 * SL$	$0.32 + 0.014 * SL$
	tPHL	0.08	$0.04 + 0.018 * SL$	$0.06 + 0.012 * SL$	$0.13 + 0.009 * SL$
	tR	0.30	$0.25 + 0.028 * SL$	$0.24 + 0.031 * SL$	$0.20 + 0.033 * SL$
	tF	0.30	$0.27 + 0.014 * SL$	$0.27 + 0.013 * SL$	$0.30 + 0.012 * SL$
S to YN	tPLH	0.47	$0.44 + 0.016 * SL$	$0.45 + 0.014 * SL$	$0.45 + 0.014 * SL$
	tPHL	0.39	$0.37 + 0.013 * SL$	$0.38 + 0.009 * SL$	$0.41 + 0.007 * SL$
	tR	0.19	$0.12 + 0.032 * SL$	$0.12 + 0.033 * SL$	$0.10 + 0.034 * SL$
	tF	0.16	$0.13 + 0.015 * SL$	$0.13 + 0.013 * SL$	$0.13 + 0.013 * SL$

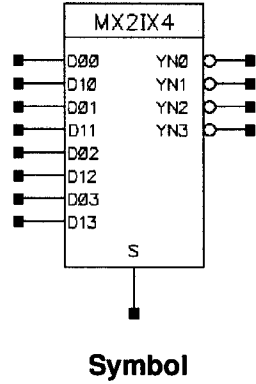
\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# MX2IX4/MX2ID2X4

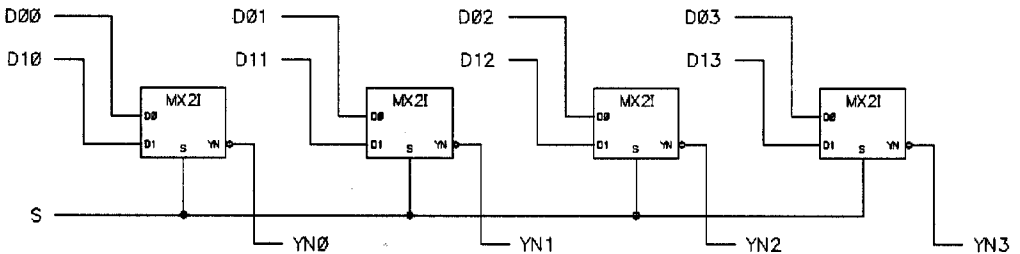
4-Bit 2>1 Inverting MUX, with 1X Drive or 2X Drive

- Inputs: D00, D10, D01, D11, D02, D12, D03, D13, S
- Outputs: YN0, YN1, YN2, YN3
- Input Loading (SL):
- MX2IX4: D00, D10, D01, D11, D12, D03, D13: 3, S: 1
  - MX2ID2X4: D00, D10, D01, D11, D02, D12, D03, D13: 4, S: 1
- Maximum Fanout (Rec. SL): All
- MX2IX4: 28
  - MX2ID2X4: 56
- Gate Count:
- MX2IX4: 7
  - MX2ID2X4: 9



S	YN0	YN1	YN2	YN3
0	D00	D01	D02	D03
1	D10	D11	D12	D13

**Truth Table**



**MX2IX4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_r = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S to YN0	tPLH	0.65	$0.57 + 0.041*SL$	$0.57 + 0.041*SL$	$0.57 + 0.041*SL$
	tPHL	0.68	$0.63 + 0.027*SL$	$0.65 + 0.021*SL$	$0.66 + 0.020*SL$
	tR	0.29	$0.11 + 0.091*SL$	$0.09 + 0.095*SL$	$0.08 + 0.096*SL$
	tF	0.17	$0.10 + 0.033*SL$	$0.09 + 0.037*SL$	$0.06 + 0.039*SL$
D00 to YN0	tPLH	0.36	$0.26 + 0.047*SL$	$0.29 + 0.039*SL$	$0.28 + 0.040*SL$
	tPHL	0.11	$0.03 + 0.042*SL$	$0.08 + 0.025*SL$	$0.19 + 0.020*SL$
	tR	0.41	$0.24 + 0.082*SL$	$0.22 + 0.090*SL$	$0.13 + 0.094*SL$
	tF	0.34	$0.26 + 0.039*SL$	$0.27 + 0.034*SL$	$0.24 + 0.036*SL$
D10 to YN0	tPLH	0.36	$0.26 + 0.047*SL$	$0.29 + 0.039*SL$	$0.28 + 0.040*SL$
	tPHL	0.11	$0.03 + 0.042*SL$	$0.08 + 0.025*SL$	$0.19 + 0.020*SL$
	tR	0.41	$0.24 + 0.082*SL$	$0.22 + 0.090*SL$	$0.13 + 0.094*SL$
	tF	0.34	$0.26 + 0.039*SL$	$0.27 + 0.034*SL$	$0.24 + 0.036*SL$
S to YN1	tPLH	0.65	$0.57 + 0.041*SL$	$0.57 + 0.041*SL$	$0.57 + 0.041*SL$
	tPHL	0.68	$0.63 + 0.027*SL$	$0.65 + 0.021*SL$	$0.66 + 0.020*SL$
	tR	0.29	$0.11 + 0.091*SL$	$0.09 + 0.095*SL$	$0.08 + 0.096*SL$
	tF	0.17	$0.10 + 0.033*SL$	$0.09 + 0.037*SL$	$0.06 + 0.039*SL$
D01 to YN1	tPLH	0.36	$0.26 + 0.047*SL$	$0.29 + 0.039*SL$	$0.28 + 0.040*SL$
	tPHL	0.11	$0.03 + 0.042*SL$	$0.08 + 0.025*SL$	$0.19 + 0.020*SL$
	tR	0.41	$0.24 + 0.082*SL$	$0.22 + 0.090*SL$	$0.13 + 0.094*SL$
	tF	0.34	$0.26 + 0.039*SL$	$0.27 + 0.034*SL$	$0.24 + 0.036*SL$
D11 to YN1	tPLH	0.36	$0.26 + 0.047*SL$	$0.29 + 0.039*SL$	$0.28 + 0.040*SL$
	tPHL	0.11	$0.03 + 0.042*SL$	$0.08 + 0.025*SL$	$0.19 + 0.020*SL$
	tR	0.41	$0.24 + 0.082*SL$	$0.22 + 0.090*SL$	$0.13 + 0.094*SL$
	tF	0.34	$0.26 + 0.039*SL$	$0.27 + 0.034*SL$	$0.24 + 0.036*SL$
S to YN2	tPLH	0.65	$0.57 + 0.041*SL$	$0.57 + 0.041*SL$	$0.57 + 0.041*SL$
	tPHL	0.68	$0.63 + 0.027*SL$	$0.65 + 0.021*SL$	$0.66 + 0.020*SL$
	tR	0.29	$0.11 + 0.091*SL$	$0.09 + 0.095*SL$	$0.08 + 0.096*SL$
	tF	0.17	$0.10 + 0.033*SL$	$0.09 + 0.037*SL$	$0.06 + 0.039*SL$
D02 to YN2	tPLH	0.36	$0.26 + 0.047*SL$	$0.29 + 0.039*SL$	$0.28 + 0.040*SL$
	tPHL	0.11	$0.03 + 0.042*SL$	$0.08 + 0.025*SL$	$0.19 + 0.020*SL$
	tR	0.41	$0.24 + 0.082*SL$	$0.22 + 0.090*SL$	$0.13 + 0.094*SL$
	tF	0.34	$0.26 + 0.039*SL$	$0.27 + 0.034*SL$	$0.24 + 0.036*SL$
D12 to YN2	tPLH	0.36	$0.26 + 0.047*SL$	$0.29 + 0.039*SL$	$0.28 + 0.040*SL$
	tPHL	0.11	$0.03 + 0.042*SL$	$0.08 + 0.025*SL$	$0.19 + 0.020*SL$
	tR	0.41	$0.24 + 0.082*SL$	$0.22 + 0.090*SL$	$0.13 + 0.094*SL$
	tF	0.34	$0.26 + 0.039*SL$	$0.27 + 0.034*SL$	$0.24 + 0.036*SL$
S to YN3	tPLH	0.65	$0.57 + 0.041*SL$	$0.57 + 0.041*SL$	$0.57 + 0.041*SL$
	tPHL	0.68	$0.63 + 0.027*SL$	$0.65 + 0.021*SL$	$0.66 + 0.020*SL$
	tR	0.29	$0.11 + 0.091*SL$	$0.09 + 0.095*SL$	$0.08 + 0.096*SL$
	tF	0.17	$0.10 + 0.033*SL$	$0.09 + 0.037*SL$	$0.06 + 0.039*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# MX2IX4

## 4-Bit 2>1 Inverting MUX

### MX2IX4 Switching Characteristics

Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D03 to YN3	tPLH	0.36	$0.26 + 0.047 \cdot \text{SL}$	$0.29 + 0.039 \cdot \text{SL}$	$0.28 + 0.040 \cdot \text{SL}$
	tPHL	0.11	$0.03 + 0.042 \cdot \text{SL}$	$0.08 + 0.025 \cdot \text{SL}$	$0.19 + 0.020 \cdot \text{SL}$
	tR	0.41	$0.24 + 0.082 \cdot \text{SL}$	$0.22 + 0.090 \cdot \text{SL}$	$0.13 + 0.094 \cdot \text{SL}$
	tF	0.34	$0.26 + 0.039 \cdot \text{SL}$	$0.27 + 0.034 \cdot \text{SL}$	$0.24 + 0.036 \cdot \text{SL}$
D13 to YN3	tPLH	0.36	$0.26 + 0.047 \cdot \text{SL}$	$0.29 + 0.039 \cdot \text{SL}$	$0.28 + 0.040 \cdot \text{SL}$
	tPHL	0.11	$0.03 + 0.042 \cdot \text{SL}$	$0.08 + 0.025 \cdot \text{SL}$	$0.19 + 0.020 \cdot \text{SL}$
	tR	0.41	$0.24 + 0.082 \cdot \text{SL}$	$0.22 + 0.090 \cdot \text{SL}$	$0.13 + 0.094 \cdot \text{SL}$
	tF	0.34	$0.26 + 0.039 \cdot \text{SL}$	$0.27 + 0.034 \cdot \text{SL}$	$0.24 + 0.036 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

**MX2ID2X4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D00 to YN0	tPLH	0.32	$0.27 + 0.027*SL$	$0.29 + 0.020*SL$	$0.30 + 0.020*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.05 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.33	$0.24 + 0.041*SL$	$0.23 + 0.044*SL$	$0.17 + 0.047*SL$
	tF	0.30	$0.25 + 0.024*SL$	$0.27 + 0.018*SL$	$0.29 + 0.017*SL$
D10 to YN0	tPLH	0.32	$0.27 + 0.027*SL$	$0.29 + 0.020*SL$	$0.30 + 0.020*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.06 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.33	$0.24 + 0.042*SL$	$0.24 + 0.044*SL$	$0.18 + 0.047*SL$
	tF	0.30	$0.26 + 0.020*SL$	$0.27 + 0.018*SL$	$0.28 + 0.017*SL$
S to YN0	tPLH	0.63	$0.59 + 0.021*SL$	$0.59 + 0.020*SL$	$0.59 + 0.020*SL$
	tPHL	0.67	$0.64 + 0.016*SL$	$0.65 + 0.012*SL$	$0.68 + 0.010*SL$
	tR	0.20	$0.11 + 0.045*SL$	$0.10 + 0.048*SL$	$0.08 + 0.049*SL$
	tF	0.15	$0.11 + 0.018*SL$	$0.11 + 0.019*SL$	$0.10 + 0.019*SL$
D01 to YN1	tPLH	0.32	$0.27 + 0.027*SL$	$0.29 + 0.020*SL$	$0.30 + 0.020*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.05 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.33	$0.24 + 0.042*SL$	$0.23 + 0.045*SL$	$0.17 + 0.048*SL$
	tF	0.30	$0.25 + 0.024*SL$	$0.27 + 0.018*SL$	$0.29 + 0.017*SL$
D11 to YN1	tPLH	0.33	$0.27 + 0.027*SL$	$0.29 + 0.020*SL$	$0.30 + 0.020*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.06 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.33	$0.24 + 0.043*SL$	$0.24 + 0.045*SL$	$0.18 + 0.048*SL$
	tF	0.30	$0.26 + 0.020*SL$	$0.27 + 0.018*SL$	$0.29 + 0.018*SL$
S to YN1	tPLH	0.63	$0.59 + 0.021*SL$	$0.59 + 0.020*SL$	$0.59 + 0.020*SL$
	tPHL	0.67	$0.64 + 0.017*SL$	$0.65 + 0.012*SL$	$0.69 + 0.010*SL$
	tR	0.20	$0.11 + 0.045*SL$	$0.10 + 0.048*SL$	$0.08 + 0.049*SL$
	tF	0.15	$0.11 + 0.018*SL$	$0.11 + 0.019*SL$	$0.10 + 0.019*SL$
D02 to YN2	tPLH	0.32	$0.27 + 0.027*SL$	$0.29 + 0.020*SL$	$0.30 + 0.020*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.05 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.33	$0.24 + 0.042*SL$	$0.23 + 0.045*SL$	$0.17 + 0.048*SL$
	tF	0.30	$0.25 + 0.024*SL$	$0.27 + 0.018*SL$	$0.29 + 0.017*SL$
D12 to YN2	tPLH	0.33	$0.27 + 0.027*SL$	$0.29 + 0.020*SL$	$0.30 + 0.020*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.06 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.33	$0.24 + 0.042*SL$	$0.24 + 0.045*SL$	$0.18 + 0.048*SL$
	tF	0.30	$0.26 + 0.020*SL$	$0.27 + 0.018*SL$	$0.28 + 0.017*SL$
S to YN2	tPLH	0.63	$0.59 + 0.022*SL$	$0.59 + 0.020*SL$	$0.59 + 0.020*SL$
	tPHL	0.67	$0.64 + 0.017*SL$	$0.65 + 0.012*SL$	$0.69 + 0.010*SL$
	tR	0.20	$0.11 + 0.045*SL$	$0.10 + 0.048*SL$	$0.08 + 0.049*SL$
	tF	0.15	$0.11 + 0.018*SL$	$0.11 + 0.019*SL$	$0.10 + 0.019*SL$
D03 to YN3	tPLH	0.32	$0.27 + 0.027*SL$	$0.29 + 0.020*SL$	$0.30 + 0.020*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.05 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.33	$0.24 + 0.041*SL$	$0.23 + 0.044*SL$	$0.17 + 0.047*SL$
	tF	0.30	$0.25 + 0.024*SL$	$0.27 + 0.018*SL$	$0.29 + 0.017*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# MX2ID2X4

## 4-Bit 2>1 Inverting MUX with 2X Drive

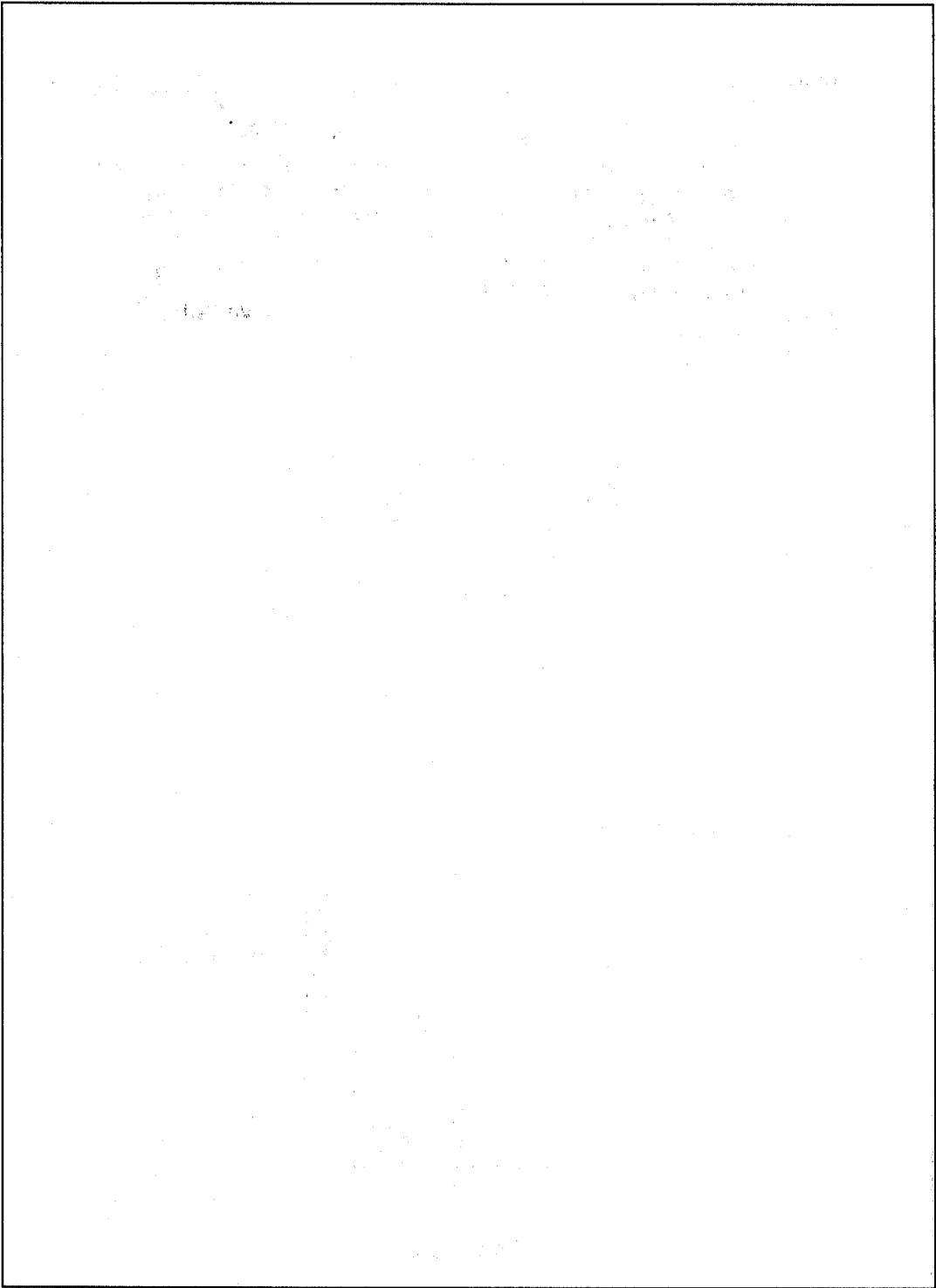
### MX2ID2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D13 to YN3	tPLH	0.32	$0.27 + 0.027*SL$	$0.29 + 0.020*SL$	$0.30 + 0.020*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.06 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.33	$0.24 + 0.042*SL$	$0.24 + 0.044*SL$	$0.18 + 0.047*SL$
	tF	0.30	$0.26 + 0.020*SL$	$0.27 + 0.018*SL$	$0.28 + 0.017*SL$
S to YN3	tPLH	0.63	$0.59 + 0.021*SL$	$0.60 + 0.020*SL$	$0.59 + 0.020*SL$
	tPHL	0.67	$0.64 + 0.016*SL$	$0.65 + 0.012*SL$	$0.68 + 0.010*SL$
	tR	0.20	$0.11 + 0.045*SL$	$0.10 + 0.048*SL$	$0.08 + 0.049*SL$
	tF	0.15	$0.11 + 0.018*SL$	$0.11 + 0.019*SL$	$0.10 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# MX2IA/MX2ID2A/MX2ID4A

2>1 Inverting MUX with separate S and SN Inputs, 1X Drive, 2X Drive or 4X Drive

Inputs: D0, D1, S, SN

Output: YN

Input Loading (SL): S, SN: All: 1

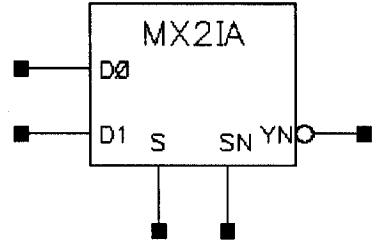
- MX2IA: D0, D1: 3
- MX2ID2A: D0, D1: 4
- MX2ID4A: D0: 3, D1: 6

Maximum Fanout (Rec. SL):

- MX2IA: 28
- MX2ID2A: 56
- MX2ID4A: 112

Gate Count:

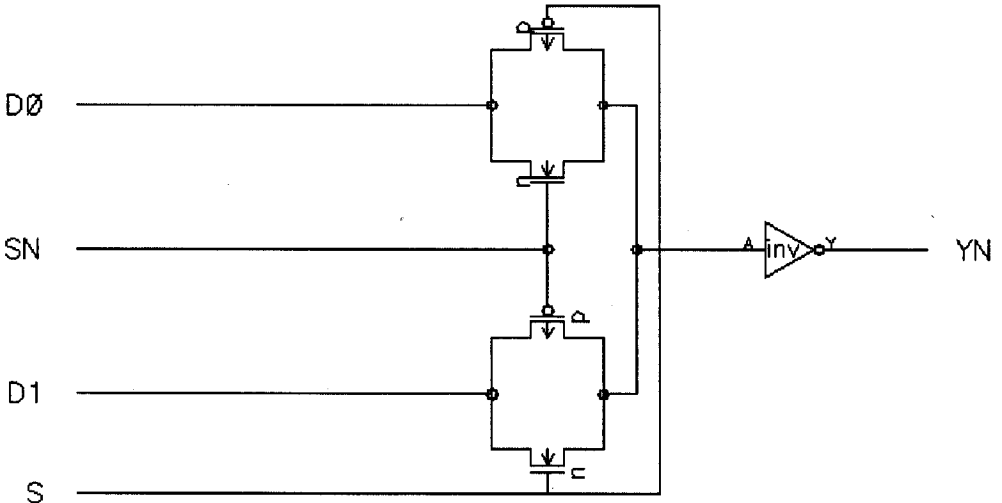
- MX2IA: 2
- MX2ID2A: 2
- MX2ID4A: 3



Symbol

S	SN	D0	D1	YN
0	1	0	x	1
0	1	1	x	0
1	0	x	0	1
1	0	x	1	0

Truth Table



Schematic

**MX2IA Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	tPLH	0.35	$0.26 + 0.046*SL$	$0.28 + 0.038*SL$	$0.27 + 0.039*SL$
	tPHL	0.11	$0.02 + 0.042*SL$	$0.08 + 0.025*SL$	$0.19 + 0.020*SL$
	tR	0.40	$0.24 + 0.078*SL$	$0.22 + 0.086*SL$	$0.13 + 0.091*SL$
	tF	0.33	$0.26 + 0.040*SL$	$0.27 + 0.034*SL$	$0.24 + 0.035*SL$
D1 to YN	tPLH	0.35	$0.26 + 0.046*SL$	$0.28 + 0.038*SL$	$0.27 + 0.039*SL$
	tPHL	0.11	$0.02 + 0.042*SL$	$0.08 + 0.025*SL$	$0.19 + 0.020*SL$
	tR	0.40	$0.24 + 0.078*SL$	$0.22 + 0.086*SL$	$0.13 + 0.091*SL$
	tF	0.33	$0.26 + 0.040*SL$	$0.27 + 0.034*SL$	$0.24 + 0.035*SL$
S to YN	tPLH	0.22	$0.14 + 0.041*SL$	$0.14 + 0.039*SL$	$0.14 + 0.040*SL$
	tPHL	0.32	$0.26 + 0.029*SL$	$0.29 + 0.021*SL$	$0.31 + 0.020*SL$
	tR	0.29	$0.11 + 0.088*SL$	$0.11 + 0.091*SL$	$0.08 + 0.092*SL$
	tF	0.21	$0.15 + 0.029*SL$	$0.13 + 0.035*SL$	$0.08 + 0.038*SL$
SN to YN	tPLH	0.22	$0.14 + 0.041*SL$	$0.14 + 0.039*SL$	$0.14 + 0.040*SL$
	tPHL	0.32	$0.26 + 0.029*SL$	$0.29 + 0.021*SL$	$0.31 + 0.020*SL$
	tR	0.29	$0.11 + 0.088*SL$	$0.11 + 0.091*SL$	$0.08 + 0.092*SL$
	tF	0.21	$0.15 + 0.029*SL$	$0.13 + 0.035*SL$	$0.08 + 0.038*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**MX2ID2A Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	tPLH	0.32	$0.26 + 0.027*SL$	$0.29 + 0.020*SL$	$0.30 + 0.019*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.06 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.32	$0.24 + 0.040*SL$	$0.23 + 0.042*SL$	$0.17 + 0.045*SL$
	tF	0.30	$0.25 + 0.024*SL$	$0.27 + 0.018*SL$	$0.29 + 0.017*SL$
D1 to YN	tPLH	0.32	$0.26 + 0.027*SL$	$0.28 + 0.020*SL$	$0.30 + 0.019*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.06 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.32	$0.24 + 0.040*SL$	$0.23 + 0.042*SL$	$0.17 + 0.045*SL$
	tF	0.30	$0.25 + 0.024*SL$	$0.27 + 0.018*SL$	$0.29 + 0.017*SL$
S to YN	tPLH	0.22	$0.18 + 0.021*SL$	$0.18 + 0.020*SL$	$0.18 + 0.020*SL$
	tPHL	0.32	$0.28 + 0.019*SL$	$0.30 + 0.012*SL$	$0.34 + 0.010*SL$
	tR	0.21	$0.12 + 0.042*SL$	$0.11 + 0.046*SL$	$0.09 + 0.047*SL$
	tF	0.20	$0.17 + 0.016*SL$	$0.16 + 0.017*SL$	$0.14 + 0.018*SL$
SN to YN	tPLH	0.22	$0.18 + 0.021*SL$	$0.18 + 0.020*SL$	$0.18 + 0.020*SL$
	tPHL	0.32	$0.28 + 0.019*SL$	$0.30 + 0.012*SL$	$0.34 + 0.010*SL$
	tR	0.21	$0.12 + 0.042*SL$	$0.11 + 0.046*SL$	$0.09 + 0.047*SL$
	tF	0.20	$0.17 + 0.016*SL$	$0.16 + 0.017*SL$	$0.14 + 0.018*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# MX2ID4A

2>1 Inverting MUX, 4X Drive with separate S and SN Inputs

## MX2ID4A Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to YN	tPLH	0.33	$0.30 + 0.015*SL$	$0.31 + 0.011*SL$	$0.33 + 0.010*SL$
	tPHL	0.09	$0.06 + 0.014*SL$	$0.07 + 0.010*SL$	$0.13 + 0.007*SL$
	tR	0.29	$0.25 + 0.021*SL$	$0.24 + 0.023*SL$	$0.21 + 0.024*SL$
	tF	0.29	$0.27 + 0.014*SL$	$0.28 + 0.011*SL$	$0.30 + 0.009*SL$
D1 to YN	tPLH	0.33	$0.30 + 0.015*SL$	$0.31 + 0.011*SL$	$0.33 + 0.010*SL$
	tPHL	0.09	$0.06 + 0.014*SL$	$0.07 + 0.010*SL$	$0.13 + 0.007*SL$
	tR	0.29	$0.25 + 0.021*SL$	$0.25 + 0.023*SL$	$0.22 + 0.024*SL$
	tF	0.29	$0.27 + 0.014*SL$	$0.27 + 0.011*SL$	$0.30 + 0.009*SL$
S to YN	tPLH	0.27	$0.25 + 0.012*SL$	$0.25 + 0.011*SL$	$0.26 + 0.011*SL$
	tPHL	0.34	$0.32 + 0.011*SL$	$0.33 + 0.008*SL$	$0.37 + 0.006*SL$
	tR	0.19	$0.15 + 0.022*SL$	$0.14 + 0.025*SL$	$0.12 + 0.026*SL$
	tF	0.21	$0.20 + 0.006*SL$	$0.19 + 0.009*SL$	$0.19 + 0.010*SL$
SN to YN	tPLH	0.27	$0.25 + 0.012*SL$	$0.25 + 0.011*SL$	$0.26 + 0.011*SL$
	tPHL	0.34	$0.32 + 0.011*SL$	$0.33 + 0.008*SL$	$0.37 + 0.006*SL$
	tR	0.19	$0.15 + 0.022*SL$	$0.14 + 0.025*SL$	$0.12 + 0.026*SL$
	tF	0.21	$0.20 + 0.006*SL$	$0.19 + 0.009*SL$	$0.19 + 0.010*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# MX3I/MX3ID2/MX3ID4

3>1 Inverting Mux with 1X Drive, 2x Drive or 4X Drive

Inputs: D0, D1, D2, S0, S1

Output: YN

Input Loading (SL):

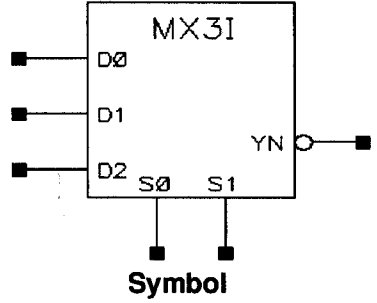
- MX3I: D0, D1: 3, D2:1, S0, S1:2
- MX3ID2: D0, D1:6, D2:4,S0,S1:2
- MX3ID4: D0, D1: 3, D2: 6, S0, S1: 2

Maximum Fanout (Rec. SL):

- MX3: 14
- MX3ID2: 56
- MX3ID: 112

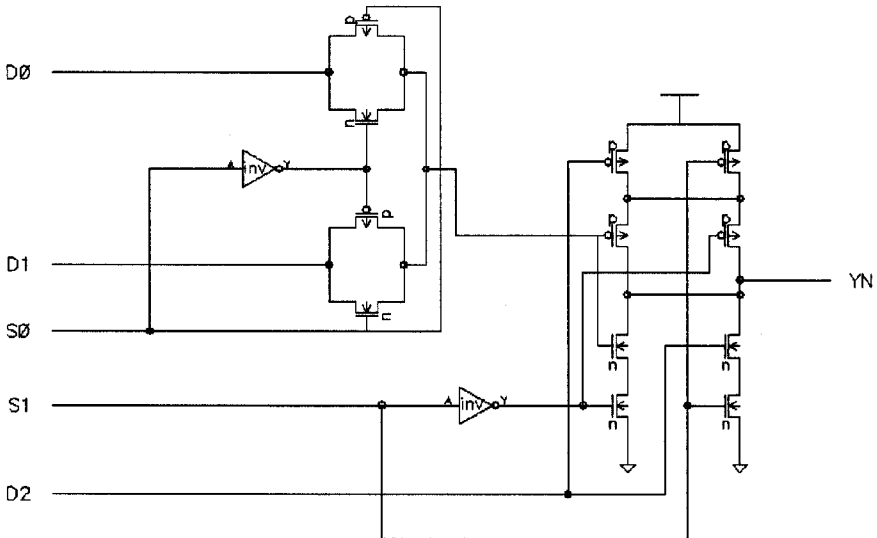
Gate Count:

- MX3I: 4
- MX3ID2: 5
- MX3ID4: 6



S0	S1	YN
0	0	$\overline{D0}$
1	0	$\overline{D1}$
x	1	$\overline{D2}$

**Truth Table**



**Schematic**

**MX3I Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN	tPLH	0.70	$0.55 + 0.077*SL$	$0.55 + 0.076*SL$	$0.56 + 0.076*SL$
	tPHL	0.46	$0.39 + 0.035*SL$	$0.41 + 0.031*SL$	$0.42 + 0.031*SL$
	tR	0.84	$0.48 + 0.181*SL$	$0.47 + 0.182*SL$	$0.48 + 0.182*SL$
	tF	0.37	$0.25 + 0.061*SL$	$0.24 + 0.065*SL$	$0.20 + 0.067*SL$
S1 to YN	tPLH	0.55	$0.41 + 0.071*SL$	$0.40 + 0.074*SL$	$0.37 + 0.075*SL$
	tPHL	0.42	$0.35 + 0.032*SL$	$0.36 + 0.031*SL$	$0.36 + 0.031*SL$
	tR	0.93	$0.60 + 0.165*SL$	$0.56 + 0.178*SL$	$0.49 + 0.181*SL$
	tF	0.28	$0.16 + 0.062*SL$	$0.14 + 0.066*SL$	$0.13 + 0.067*SL$
D0 to YN	tPLH	0.59	$0.45 + 0.073*SL$	$0.45 + 0.074*SL$	$0.42 + 0.075*SL$
	tPHL	0.24	$0.14 + 0.048*SL$	$0.18 + 0.034*SL$	$0.25 + 0.030*SL$
	tR	0.90	$0.56 + 0.170*SL$	$0.54 + 0.179*SL$	$0.48 + 0.181*SL$
	tF	0.53	$0.41 + 0.058*SL$	$0.41 + 0.061*SL$	$0.33 + 0.065*SL$
D1 to YN	tPLH	0.59	$0.44 + 0.073*SL$	$0.44 + 0.074*SL$	$0.42 + 0.075*SL$
	tPHL	0.24	$0.14 + 0.048*SL$	$0.19 + 0.034*SL$	$0.25 + 0.030*SL$
	tR	0.90	$0.56 + 0.170*SL$	$0.54 + 0.179*SL$	$0.48 + 0.181*SL$
	tF	0.54	$0.42 + 0.058*SL$	$0.41 + 0.061*SL$	$0.34 + 0.064*SL$
D2 to YN	tPLH	0.55	$0.40 + 0.073*SL$	$0.40 + 0.073*SL$	$0.39 + 0.074*SL$
	tPHL	0.25	$0.16 + 0.042*SL$	$0.19 + 0.032*SL$	$0.23 + 0.030*SL$
	tR	0.89	$0.56 + 0.164*SL$	$0.53 + 0.174*SL$	$0.47 + 0.177*SL$
	tF	0.62	$0.51 + 0.053*SL$	$0.49 + 0.060*SL$	$0.39 + 0.065*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# MX3ID2

## 3>1 Inverting MUX with 2X Drive

### MX3ID2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN	tPLH	0.75	$0.70 + 0.023*SL$	$0.71 + 0.020*SL$	$0.71 + 0.020*SL$
	tPHL	0.67	$0.63 + 0.021*SL$	$0.65 + 0.014*SL$	$0.71 + 0.011*SL$
	tR	0.22	$0.13 + 0.045*SL$	$0.12 + 0.045*SL$	$0.10 + 0.047*SL$
	tF	0.20	$0.16 + 0.022*SL$	$0.17 + 0.019*SL$	$0.18 + 0.019*SL$
S1 to YN	tPLH	0.50	$0.46 + 0.022*SL$	$0.46 + 0.020*SL$	$0.47 + 0.020*SL$
	tPHL	0.44	$0.40 + 0.020*SL$	$0.42 + 0.014*SL$	$0.48 + 0.011*SL$
	tR	0.21	$0.12 + 0.045*SL$	$0.12 + 0.046*SL$	$0.10 + 0.047*SL$
	tF	0.19	$0.15 + 0.021*SL$	$0.15 + 0.020*SL$	$0.17 + 0.019*SL$
D0 to YN	tPLH	0.63	$0.58 + 0.022*SL$	$0.59 + 0.020*SL$	$0.59 + 0.020*SL$
	tPHL	0.41	$0.37 + 0.021*SL$	$0.39 + 0.014*SL$	$0.45 + 0.011*SL$
	tR	0.22	$0.13 + 0.045*SL$	$0.13 + 0.045*SL$	$0.10 + 0.047*SL$
	tF	0.21	$0.16 + 0.021*SL$	$0.17 + 0.019*SL$	$0.18 + 0.019*SL$
D1 to YN	tPLH	0.63	$0.58 + 0.022*SL$	$0.59 + 0.020*SL$	$0.59 + 0.020*SL$
	tPHL	0.41	$0.37 + 0.021*SL$	$0.39 + 0.014*SL$	$0.45 + 0.011*SL$
	tR	0.22	$0.13 + 0.045*SL$	$0.13 + 0.045*SL$	$0.10 + 0.047*SL$
	tF	0.21	$0.16 + 0.021*SL$	$0.17 + 0.019*SL$	$0.18 + 0.019*SL$
D2 to YN	tPLH	0.32	$0.27 + 0.027*SL$	$0.28 + 0.020*SL$	$0.30 + 0.019*SL$
	tPHL	0.08	$0.03 + 0.025*SL$	$0.06 + 0.016*SL$	$0.15 + 0.011*SL$
	tR	0.32	$0.24 + 0.041*SL$	$0.23 + 0.042*SL$	$0.17 + 0.045*SL$
	tF	0.30	$0.25 + 0.024*SL$	$0.27 + 0.018*SL$	$0.29 + 0.017*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**MX3ID4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

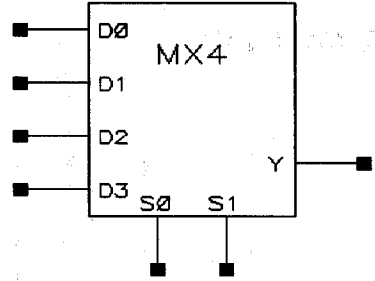
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S0 to YN	tPLH	0.79	$0.77 + 0.013*SL$	$0.77 + 0.011*SL$	$0.79 + 0.011*SL$
	tPHL	0.73	$0.70 + 0.013*SL$	$0.71 + 0.009*SL$	$0.75 + 0.007*SL$
	tR	0.21	$0.17 + 0.022*SL$	$0.16 + 0.025*SL$	$0.14 + 0.025*SL$
	tF	0.23	$0.22 + 0.010*SL$	$0.21 + 0.011*SL$	$0.23 + 0.010*SL$
S1 to YN	tPLH	0.55	$0.52 + 0.013*SL$	$0.52 + 0.011*SL$	$0.54 + 0.011*SL$
	tPHL	0.49	$0.46 + 0.013*SL$	$0.47 + 0.009*SL$	$0.51 + 0.007*SL$
	tR	0.21	$0.17 + 0.022*SL$	$0.16 + 0.025*SL$	$0.14 + 0.025*SL$
	tF	0.21	$0.18 + 0.014*SL$	$0.19 + 0.012*SL$	$0.22 + 0.010*SL$
D0 to YN	tPLH	0.68	$0.65 + 0.013*SL$	$0.66 + 0.011*SL$	$0.67 + 0.011*SL$
	tPHL	0.47	$0.44 + 0.013*SL$	$0.45 + 0.009*SL$	$0.49 + 0.007*SL$
	tR	0.21	$0.17 + 0.022*SL$	$0.16 + 0.025*SL$	$0.14 + 0.025*SL$
	tF	0.24	$0.21 + 0.011*SL$	$0.21 + 0.011*SL$	$0.23 + 0.010*SL$
D1 to YN	tPLH	0.68	$0.65 + 0.013*SL$	$0.65 + 0.011*SL$	$0.67 + 0.011*SL$
	tPHL	0.47	$0.44 + 0.013*SL$	$0.45 + 0.009*SL$	$0.50 + 0.007*SL$
	tR	0.21	$0.17 + 0.021*SL$	$0.16 + 0.025*SL$	$0.14 + 0.026*SL$
	tF	0.24	$0.21 + 0.011*SL$	$0.21 + 0.011*SL$	$0.23 + 0.010*SL$
D2 to YN	tPLH	0.33	$0.30 + 0.015*SL$	$0.31 + 0.011*SL$	$0.33 + 0.010*SL$
	tPHL	0.09	$0.06 + 0.014*SL$	$0.07 + 0.010*SL$	$0.13 + 0.007*SL$
	tR	0.29	$0.25 + 0.021*SL$	$0.24 + 0.023*SL$	$0.21 + 0.024*SL$
	tF	0.29	$0.27 + 0.014*SL$	$0.28 + 0.011*SL$	$0.30 + 0.009*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# MX4/MX4D2

4>1 Non-inverting MUX with 1X Drive or 2X Drive

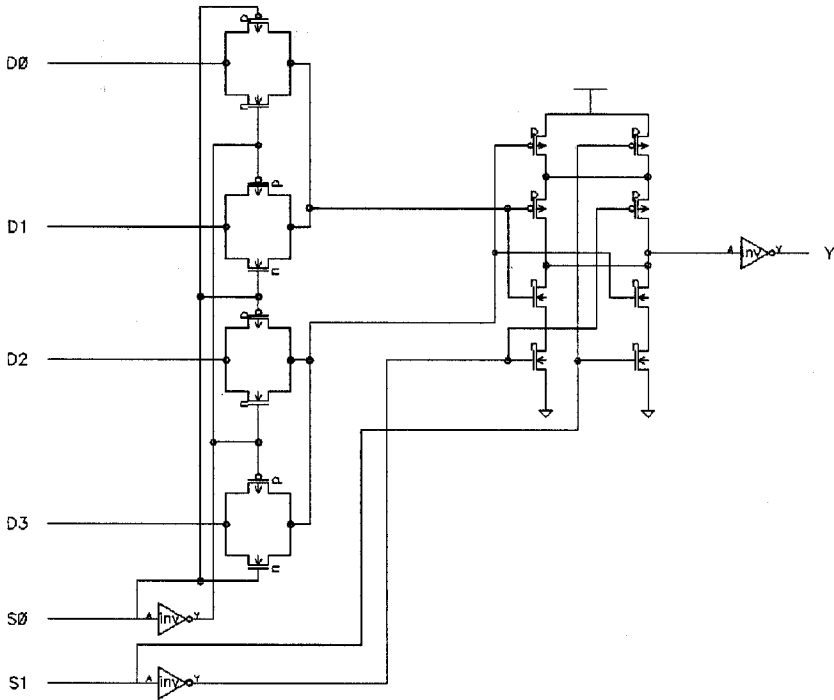
Inputs: D0, D1, D2, D3, S0, S1  
Outputs: Y  
Input Loading (SL):  
- D0, D1, D2, D3, S0: 3  
- S1: 2  
Maximum Fanout (Rec. SL):  
MX4: 28  
MX4D2: 56  
Gate Count: 6



Symbol

S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Truth Table



Schematic

**MX4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Y	tPLH	0.39	$0.30 + 0.045*SL$	$0.31 + 0.042*SL$	$0.31 + 0.043*SL$
	tPHL	0.62	$0.55 + 0.039*SL$	$0.59 + 0.025*SL$	$0.66 + 0.021*SL$
	tR	0.35	$0.15 + 0.096*SL$	$0.14 + 0.100*SL$	$0.11 + 0.102*SL$
	tF	0.28	$0.19 + 0.042*SL$	$0.20 + 0.039*SL$	$0.18 + 0.040*SL$
D1 to Y	tPLH	0.39	$0.30 + 0.045*SL$	$0.31 + 0.042*SL$	$0.31 + 0.043*SL$
	tPHL	0.62	$0.54 + 0.039*SL$	$0.58 + 0.025*SL$	$0.66 + 0.021*SL$
	tR	0.35	$0.15 + 0.096*SL$	$0.14 + 0.100*SL$	$0.11 + 0.102*SL$
	tF	0.28	$0.19 + 0.042*SL$	$0.20 + 0.039*SL$	$0.18 + 0.040*SL$
D2 to Y	tPLH	0.47	$0.38 + 0.046*SL$	$0.39 + 0.042*SL$	$0.39 + 0.042*SL$
	tPHL	0.62	$0.54 + 0.038*SL$	$0.58 + 0.025*SL$	$0.66 + 0.021*SL$
	tR	0.36	$0.17 + 0.096*SL$	$0.16 + 0.100*SL$	$0.12 + 0.102*SL$
	tF	0.28	$0.19 + 0.043*SL$	$0.21 + 0.038*SL$	$0.18 + 0.040*SL$
D3 to Y	tPLH	0.48	$0.38 + 0.046*SL$	$0.39 + 0.042*SL$	$0.39 + 0.042*SL$
	tPHL	0.62	$0.55 + 0.038*SL$	$0.59 + 0.025*SL$	$0.66 + 0.021*SL$
	tR	0.36	$0.17 + 0.095*SL$	$0.16 + 0.100*SL$	$0.12 + 0.102*SL$
	tF	0.28	$0.19 + 0.042*SL$	$0.21 + 0.038*SL$	$0.18 + 0.040*SL$
S0 to Y	tPLH	0.67	$0.58 + 0.046*SL$	$0.59 + 0.043*SL$	$0.60 + 0.043*SL$
	tPHL	0.84	$0.76 + 0.038*SL$	$0.80 + 0.025*SL$	$0.88 + 0.021*SL$
	tR	0.35	$0.16 + 0.094*SL$	$0.15 + 0.100*SL$	$0.11 + 0.102*SL$
	tF	0.27	$0.18 + 0.042*SL$	$0.19 + 0.039*SL$	$0.17 + 0.040*SL$
S1 to Y	tPLH	0.57	$0.48 + 0.044*SL$	$0.48 + 0.043*SL$	$0.48 + 0.043*SL$
	tPHL	0.58	$0.50 + 0.039*SL$	$0.54 + 0.025*SL$	$0.62 + 0.021*SL$
	tR	0.32	$0.12 + 0.097*SL$	$0.11 + 0.101*SL$	$0.09 + 0.102*SL$
	tF	0.28	$0.20 + 0.041*SL$	$0.21 + 0.039*SL$	$0.19 + 0.040*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# MX4D2

## 4>1 Non-inverting MUX with 2X Drive

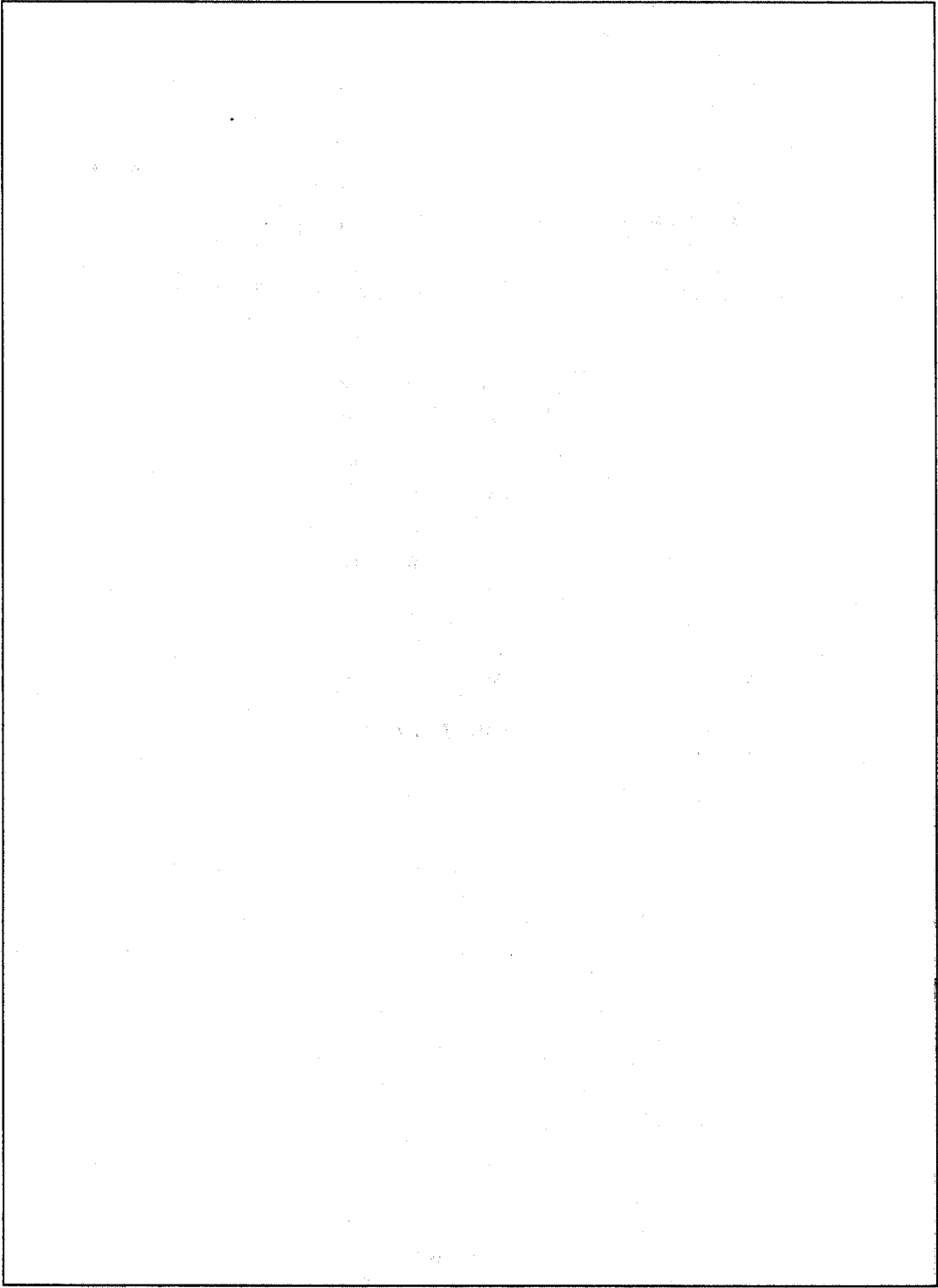
### MX4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{RQ}$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Y	tPLH	0.40	$0.35 + 0.024*SL$	$0.36 + 0.021*SL$	$0.37 + 0.021*SL$
	tPHL	0.64	$0.60 + 0.024*SL$	$0.62 + 0.015*SL$	$0.70 + 0.012*SL$
	tR	0.25	$0.16 + 0.046*SL$	$0.16 + 0.048*SL$	$0.13 + 0.050*SL$
	tF	0.27	$0.22 + 0.024*SL$	$0.24 + 0.019*SL$	$0.25 + 0.018*SL$
D1 to Y	tPLH	0.40	$0.35 + 0.024*SL$	$0.36 + 0.021*SL$	$0.37 + 0.021*SL$
	tPHL	0.64	$0.59 + 0.023*SL$	$0.62 + 0.015*SL$	$0.69 + 0.012*SL$
	tR	0.26	$0.16 + 0.046*SL$	$0.16 + 0.048*SL$	$0.13 + 0.050*SL$
	tF	0.27	$0.22 + 0.024*SL$	$0.24 + 0.019*SL$	$0.25 + 0.018*SL$
D2 to Y	tPLH	0.47	$0.42 + 0.024*SL$	$0.43 + 0.021*SL$	$0.44 + 0.021*SL$
	tPHL	0.64	$0.60 + 0.023*SL$	$0.62 + 0.015*SL$	$0.69 + 0.012*SL$
	tR	0.27	$0.18 + 0.046*SL$	$0.17 + 0.048*SL$	$0.14 + 0.050*SL$
	tF	0.27	$0.23 + 0.022*SL$	$0.24 + 0.019*SL$	$0.24 + 0.018*SL$
D3 to Y	tPLH	0.48	$0.43 + 0.025*SL$	$0.44 + 0.021*SL$	$0.45 + 0.021*SL$
	tPHL	0.64	$0.60 + 0.023*SL$	$0.62 + 0.015*SL$	$0.70 + 0.012*SL$
	tR	0.27	$0.18 + 0.046*SL$	$0.17 + 0.048*SL$	$0.14 + 0.050*SL$
	tF	0.27	$0.22 + 0.022*SL$	$0.23 + 0.019*SL$	$0.24 + 0.018*SL$
S0 to Y	tPLH	0.67	$0.62 + 0.024*SL$	$0.63 + 0.021*SL$	$0.64 + 0.021*SL$
	tPHL	0.86	$0.81 + 0.023*SL$	$0.84 + 0.015*SL$	$0.91 + 0.012*SL$
	tR	0.26	$0.17 + 0.045*SL$	$0.16 + 0.048*SL$	$0.13 + 0.050*SL$
	tF	0.26	$0.21 + 0.024*SL$	$0.23 + 0.019*SL$	$0.24 + 0.018*SL$
S1 to Y	tPLH	0.56	$0.51 + 0.023*SL$	$0.52 + 0.021*SL$	$0.52 + 0.021*SL$
	tPHL	0.60	$0.55 + 0.023*SL$	$0.58 + 0.015*SL$	$0.65 + 0.012*SL$
	tR	0.23	$0.13 + 0.047*SL$	$0.13 + 0.049*SL$	$0.10 + 0.050*SL$
	tF	0.27	$0.23 + 0.023*SL$	$0.24 + 0.019*SL$	$0.25 + 0.018*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# MX8/MX8D2

## 8>1 Non-inverting MUX

Inputs: D0, D1, D2, D3, D4, D5, D6, D7  
 S0, S1, S2

Outputs: Y

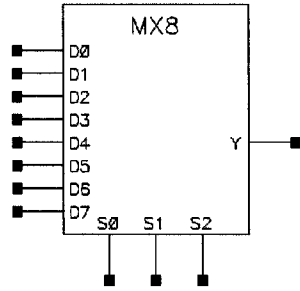
Input Loading (SL):

- S0: 1
- S2: 2
- D0, D1, D2, D3, D4, D5, D6, D7, S1: 3

Maximum Fanout (Rec. SL):

- MX8: 28
- MX8D2: 56

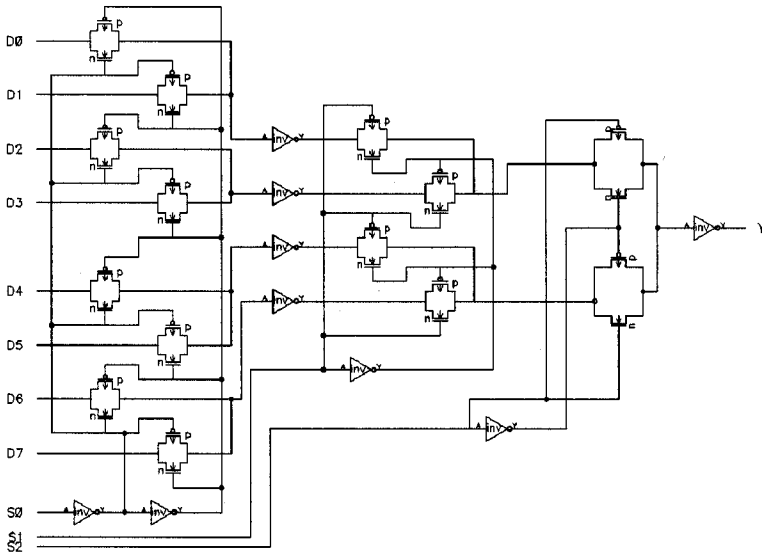
Gate Count: All : 12



**Symbol**

S2	S1	S0	Y
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

**Truth Table**



**Schematic**

**MX8 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Y	tPLH	0.61	$0.52 + 0.043 \cdot SL$	$0.53 + 0.040 \cdot SL$	$0.53 + 0.040 \cdot SL$
	tPHL	0.74	$0.66 + 0.040 \cdot SL$	$0.70 + 0.028 \cdot SL$	$0.81 + 0.022 \cdot SL$
	tR	0.40	$0.23 + 0.087 \cdot SL$	$0.22 + 0.090 \cdot SL$	$0.18 + 0.092 \cdot SL$
	tF	0.34	$0.26 + 0.045 \cdot SL$	$0.27 + 0.039 \cdot SL$	$0.31 + 0.037 \cdot SL$
D1 to Y	tPLH	0.61	$0.52 + 0.043 \cdot SL$	$0.53 + 0.040 \cdot SL$	$0.54 + 0.040 \cdot SL$
	tPHL	0.74	$0.66 + 0.039 \cdot SL$	$0.70 + 0.028 \cdot SL$	$0.81 + 0.022 \cdot SL$
	tR	0.40	$0.23 + 0.087 \cdot SL$	$0.22 + 0.090 \cdot SL$	$0.18 + 0.092 \cdot SL$
	tF	0.34	$0.26 + 0.045 \cdot SL$	$0.27 + 0.039 \cdot SL$	$0.31 + 0.037 \cdot SL$
D2 to Y	tPLH	0.61	$0.52 + 0.043 \cdot SL$	$0.53 + 0.040 \cdot SL$	$0.53 + 0.040 \cdot SL$
	tPHL	0.75	$0.67 + 0.040 \cdot SL$	$0.70 + 0.028 \cdot SL$	$0.81 + 0.022 \cdot SL$
	tR	0.40	$0.23 + 0.087 \cdot SL$	$0.22 + 0.090 \cdot SL$	$0.18 + 0.092 \cdot SL$
	tF	0.35	$0.26 + 0.045 \cdot SL$	$0.27 + 0.039 \cdot SL$	$0.31 + 0.037 \cdot SL$
D3 to Y	tPLH	0.60	$0.52 + 0.043 \cdot SL$	$0.53 + 0.040 \cdot SL$	$0.53 + 0.040 \cdot SL$
	tPHL	0.74	$0.66 + 0.040 \cdot SL$	$0.70 + 0.028 \cdot SL$	$0.81 + 0.022 \cdot SL$
	tR	0.40	$0.23 + 0.086 \cdot SL$	$0.22 + 0.090 \cdot SL$	$0.18 + 0.092 \cdot SL$
	tF	0.35	$0.26 + 0.045 \cdot SL$	$0.27 + 0.039 \cdot SL$	$0.31 + 0.037 \cdot SL$
D4 to Y	tPLH	0.60	$0.52 + 0.043 \cdot SL$	$0.53 + 0.040 \cdot SL$	$0.53 + 0.040 \cdot SL$
	tPHL	0.74	$0.66 + 0.039 \cdot SL$	$0.70 + 0.028 \cdot SL$	$0.81 + 0.022 \cdot SL$
	tR	0.40	$0.23 + 0.086 \cdot SL$	$0.22 + 0.090 \cdot SL$	$0.18 + 0.092 \cdot SL$
	tF	0.34	$0.25 + 0.045 \cdot SL$	$0.27 + 0.039 \cdot SL$	$0.31 + 0.037 \cdot SL$
D5 to Y	tPLH	0.60	$0.52 + 0.043 \cdot SL$	$0.53 + 0.040 \cdot SL$	$0.53 + 0.040 \cdot SL$
	tPHL	0.74	$0.66 + 0.039 \cdot SL$	$0.70 + 0.028 \cdot SL$	$0.81 + 0.022 \cdot SL$
	tR	0.40	$0.23 + 0.086 \cdot SL$	$0.22 + 0.090 \cdot SL$	$0.18 + 0.092 \cdot SL$
	tF	0.34	$0.25 + 0.045 \cdot SL$	$0.27 + 0.039 \cdot SL$	$0.31 + 0.037 \cdot SL$
D6 to Y	tPLH	0.60	$0.52 + 0.043 \cdot SL$	$0.53 + 0.040 \cdot SL$	$0.53 + 0.040 \cdot SL$
	tPHL	0.74	$0.67 + 0.040 \cdot SL$	$0.70 + 0.027 \cdot SL$	$0.81 + 0.022 \cdot SL$
	tR	0.40	$0.23 + 0.086 \cdot SL$	$0.22 + 0.090 \cdot SL$	$0.18 + 0.092 \cdot SL$
	tF	0.34	$0.26 + 0.045 \cdot SL$	$0.27 + 0.039 \cdot SL$	$0.31 + 0.037 \cdot SL$
D7 to Y	tPLH	0.60	$0.52 + 0.043 \cdot SL$	$0.53 + 0.040 \cdot SL$	$0.53 + 0.040 \cdot SL$
	tPHL	0.74	$0.67 + 0.040 \cdot SL$	$0.70 + 0.027 \cdot SL$	$0.81 + 0.022 \cdot SL$
	tR	0.40	$0.23 + 0.086 \cdot SL$	$0.22 + 0.090 \cdot SL$	$0.18 + 0.092 \cdot SL$
	tF	0.34	$0.26 + 0.045 \cdot SL$	$0.27 + 0.039 \cdot SL$	$0.31 + 0.037 \cdot SL$
S0 to Y	tPLH	1.14	$1.05 + 0.044 \cdot SL$	$1.06 + 0.040 \cdot SL$	$1.07 + 0.040 \cdot SL$
	tPHL	0.95	$0.87 + 0.039 \cdot SL$	$0.91 + 0.027 \cdot SL$	$1.02 + 0.022 \cdot SL$
	tR	0.39	$0.22 + 0.088 \cdot SL$	$0.21 + 0.090 \cdot SL$	$0.17 + 0.092 \cdot SL$
	tF	0.34	$0.24 + 0.046 \cdot SL$	$0.27 + 0.039 \cdot SL$	$0.30 + 0.037 \cdot SL$
S1 to Y	tPLH	0.73	$0.64 + 0.043 \cdot SL$	$0.65 + 0.040 \cdot SL$	$0.66 + 0.040 \cdot SL$
	tPHL	0.50	$0.42 + 0.039 \cdot SL$	$0.46 + 0.027 \cdot SL$	$0.57 + 0.022 \cdot SL$
	tR	0.40	$0.22 + 0.088 \cdot SL$	$0.21 + 0.090 \cdot SL$	$0.17 + 0.092 \cdot SL$
	tF	0.34	$0.24 + 0.046 \cdot SL$	$0.26 + 0.039 \cdot SL$	$0.30 + 0.037 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# MX8

## 8>1 Non-inverting MUX

### MX8 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S2 to Y	tPLH	0.56	$0.48 + 0.044 * SL$	$0.49 + 0.040 * SL$	$0.50 + 0.040 * SL$
	tPHL	0.33	$0.26 + 0.035 * SL$	$0.29 + 0.026 * SL$	$0.38 + 0.022 * SL$
	tR	0.38	$0.20 + 0.090 * SL$	$0.19 + 0.091 * SL$	$0.17 + 0.092 * SL$
	tF	0.28	$0.19 + 0.044 * SL$	$0.21 + 0.039 * SL$	$0.24 + 0.038 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## MX8D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Y	tPLH	0.59	$0.54 + 0.025*SL$	$0.56 + 0.021*SL$	$0.58 + 0.020*SL$
	tPHL	0.71	$0.66 + 0.025*SL$	$0.69 + 0.017*SL$	$0.77 + 0.013*SL$
	tR	0.28	$0.20 + 0.042*SL$	$0.19 + 0.044*SL$	$0.16 + 0.046*SL$
	tF	0.30	$0.24 + 0.026*SL$	$0.26 + 0.022*SL$	$0.30 + 0.019*SL$
D1 to Y	tPLH	0.59	$0.54 + 0.025*SL$	$0.56 + 0.021*SL$	$0.58 + 0.020*SL$
	tPHL	0.71	$0.66 + 0.025*SL$	$0.69 + 0.017*SL$	$0.77 + 0.013*SL$
	tR	0.28	$0.20 + 0.042*SL$	$0.19 + 0.044*SL$	$0.16 + 0.046*SL$
	tF	0.30	$0.24 + 0.026*SL$	$0.26 + 0.022*SL$	$0.30 + 0.019*SL$
D2 to Y	tPLH	0.59	$0.54 + 0.025*SL$	$0.56 + 0.021*SL$	$0.58 + 0.020*SL$
	tPHL	0.72	$0.67 + 0.026*SL$	$0.69 + 0.017*SL$	$0.77 + 0.013*SL$
	tR	0.28	$0.20 + 0.042*SL$	$0.19 + 0.044*SL$	$0.16 + 0.046*SL$
	tF	0.30	$0.24 + 0.026*SL$	$0.26 + 0.022*SL$	$0.30 + 0.019*SL$
D3 to Y	tPLH	0.59	$0.54 + 0.025*SL$	$0.55 + 0.021*SL$	$0.57 + 0.020*SL$
	tPHL	0.71	$0.66 + 0.025*SL$	$0.69 + 0.017*SL$	$0.77 + 0.013*SL$
	tR	0.28	$0.20 + 0.042*SL$	$0.19 + 0.044*SL$	$0.16 + 0.046*SL$
	tF	0.30	$0.24 + 0.026*SL$	$0.26 + 0.021*SL$	$0.30 + 0.019*SL$
D4 to Y	tPLH	0.59	$0.54 + 0.025*SL$	$0.55 + 0.021*SL$	$0.57 + 0.020*SL$
	tPHL	0.71	$0.66 + 0.025*SL$	$0.69 + 0.017*SL$	$0.77 + 0.013*SL$
	tR	0.28	$0.20 + 0.042*SL$	$0.19 + 0.044*SL$	$0.16 + 0.046*SL$
	tF	0.29	$0.24 + 0.026*SL$	$0.26 + 0.021*SL$	$0.30 + 0.019*SL$
D5 to Y	tPLH	0.59	$0.54 + 0.025*SL$	$0.55 + 0.021*SL$	$0.57 + 0.020*SL$
	tPHL	0.71	$0.66 + 0.025*SL$	$0.69 + 0.017*SL$	$0.77 + 0.013*SL$
	tR	0.28	$0.20 + 0.042*SL$	$0.19 + 0.044*SL$	$0.16 + 0.046*SL$
	tF	0.29	$0.24 + 0.026*SL$	$0.26 + 0.021*SL$	$0.30 + 0.019*SL$
D6 to Y	tPLH	0.59	$0.54 + 0.025*SL$	$0.55 + 0.021*SL$	$0.57 + 0.020*SL$
	tPHL	0.72	$0.66 + 0.025*SL$	$0.69 + 0.017*SL$	$0.77 + 0.013*SL$
	tR	0.28	$0.20 + 0.042*SL$	$0.19 + 0.044*SL$	$0.16 + 0.046*SL$
	tF	0.30	$0.24 + 0.026*SL$	$0.26 + 0.021*SL$	$0.30 + 0.019*SL$
D7 to Y	tPLH	0.59	$0.54 + 0.025*SL$	$0.55 + 0.021*SL$	$0.57 + 0.020*SL$
	tPHL	0.72	$0.66 + 0.025*SL$	$0.69 + 0.017*SL$	$0.77 + 0.013*SL$
	tR	0.28	$0.20 + 0.042*SL$	$0.19 + 0.044*SL$	$0.16 + 0.046*SL$
	tF	0.30	$0.24 + 0.026*SL$	$0.26 + 0.021*SL$	$0.30 + 0.019*SL$
S0 to Y	tPLH	1.13	$1.08 + 0.025*SL$	$1.09 + 0.021*SL$	$1.11 + 0.020*SL$
	tPHL	0.93	$0.88 + 0.025*SL$	$0.90 + 0.017*SL$	$0.98 + 0.013*SL$
	tR	0.27	$0.19 + 0.042*SL$	$0.18 + 0.045*SL$	$0.15 + 0.046*SL$
	tF	0.29	$0.23 + 0.027*SL$	$0.25 + 0.022*SL$	$0.29 + 0.019*SL$
S1 to Y	tPLH	0.70	$0.65 + 0.025*SL$	$0.67 + 0.021*SL$	$0.69 + 0.020*SL$
	tPHL	0.47	$0.42 + 0.026*SL$	$0.44 + 0.017*SL$	$0.53 + 0.013*SL$
	tR	0.28	$0.19 + 0.042*SL$	$0.18 + 0.045*SL$	$0.15 + 0.046*SL$
	tF	0.29	$0.23 + 0.027*SL$	$0.25 + 0.022*SL$	$0.30 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# MX8D2

## 8>1 Non-inverting MUX with 2X Drive

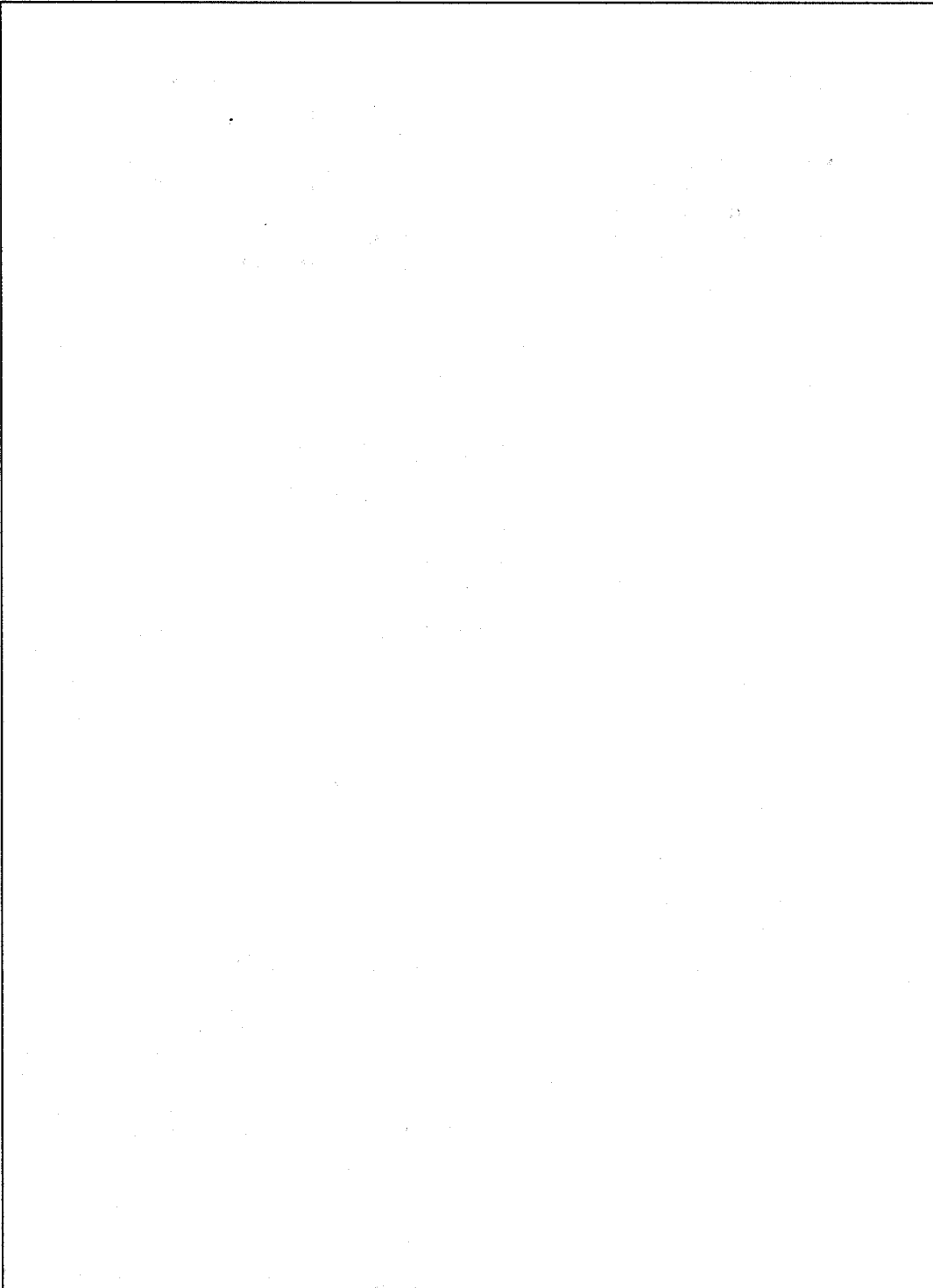
### MX8D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
S2 to Y	tPLH	0.54	$0.49 + 0.025*SL$	$0.50 + 0.021*SL$	$0.52 + 0.020*SL$
	tPHL	0.31	$0.27 + 0.023*SL$	$0.29 + 0.016*SL$	$0.36 + 0.013*SL$
	tR	0.26	$0.17 + 0.043*SL$	$0.16 + 0.045*SL$	$0.15 + 0.046*SL$
	tF	0.24	$0.19 + 0.025*SL$	$0.20 + 0.022*SL$	$0.24 + 0.020*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# LD1/LD1D2

## D-Latch Active High Gate with 1X Drive or 2X Drive

Inputs: D, G

Outputs: Q, QN

Input Loading (SL):

- D: 3

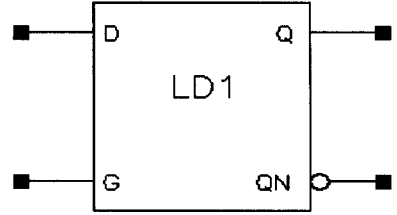
- G: 1

Maximum Fanout (Rec. SL):

LD1: 28

LD1D2: 56

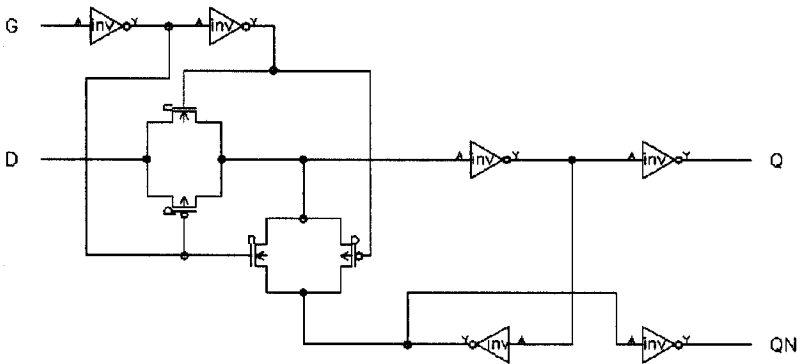
Gate Count: 5



Symbol

D	G	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	0	1
1	1	1	0
x	0	Q <sub>n</sub>	Q <sub>Nn</sub>

Truth Table



Schematic

**LD1 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.27	$0.19 + 0.040*SL$	$0.19 + 0.040*SL$	$0.19 + 0.040*SL$
	tPHL	0.44	$0.39 + 0.028*SL$	$0.41 + 0.021*SL$	$0.43 + 0.020*SL$
	tR	0.29	$0.12 + 0.088*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.19	$0.12 + 0.036*SL$	$0.12 + 0.036*SL$	$0.08 + 0.038*SL$
G to Q	tPLH	0.44	$0.36 + 0.041*SL$	$0.36 + 0.040*SL$	$0.36 + 0.040*SL$
	tPHL	0.44	$0.39 + 0.027*SL$	$0.40 + 0.021*SL$	$0.43 + 0.020*SL$
	tR	0.28	$0.10 + 0.089*SL$	$0.09 + 0.092*SL$	$0.08 + 0.093*SL$
	tF	0.17	$0.09 + 0.037*SL$	$0.09 + 0.037*SL$	$0.07 + 0.038*SL$
D to QN	tPLH	0.58	$0.51 + 0.039*SL$	$0.50 + 0.040*SL$	$0.50 + 0.040*SL$
	tPHL	0.34	$0.29 + 0.026*SL$	$0.31 + 0.021*SL$	$0.32 + 0.020*SL$
	tR	0.28	$0.10 + 0.088*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.10 + 0.035*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
G to QN	tPLH	0.58	$0.50 + 0.039*SL$	$0.50 + 0.040*SL$	$0.50 + 0.040*SL$
	tPHL	0.52	$0.46 + 0.026*SL$	$0.48 + 0.021*SL$	$0.50 + 0.020*SL$
	tR	0.28	$0.10 + 0.089*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.09 + 0.037*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**LD1 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	tPWH	0.920
Input Hold Time (D to G)	tHD	0.233
Input Setup Time (D to G)	tSU	0.123

# LD1D2

## D-Latch Active High Gate with 2X Drive

### LD1D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

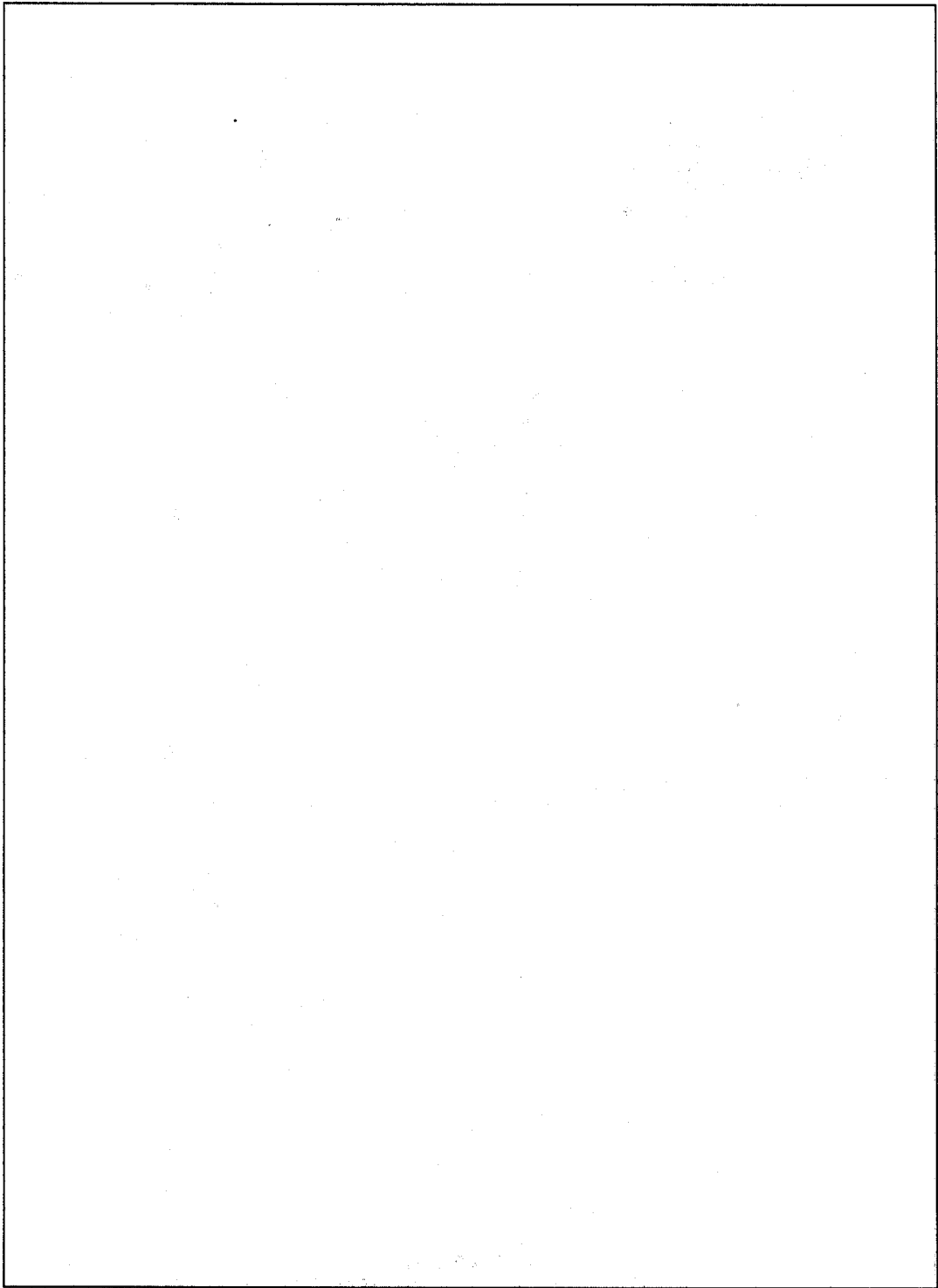
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.28	$0.23 + 0.021*SL$	$0.24 + 0.020*SL$	$0.24 + 0.020*SL$
	tPHL	0.45	$0.42 + 0.017*SL$	$0.43 + 0.012*SL$	$0.47 + 0.010*SL$
	tR	0.21	$0.13 + 0.043*SL$	$0.12 + 0.045*SL$	$0.09 + 0.047*SL$
	tF	0.18	$0.14 + 0.017*SL$	$0.14 + 0.018*SL$	$0.12 + 0.018*SL$
G to Q	tPLH	0.44	$0.39 + 0.021*SL$	$0.40 + 0.020*SL$	$0.40 + 0.020*SL$
	tPHL	0.45	$0.42 + 0.016*SL$	$0.43 + 0.012*SL$	$0.47 + 0.010*SL$
	tR	0.19	$0.11 + 0.042*SL$	$0.10 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.15	$0.11 + 0.019*SL$	$0.12 + 0.018*SL$	$0.11 + 0.019*SL$
D to QN	tPLH	0.63	$0.59 + 0.019*SL$	$0.59 + 0.020*SL$	$0.58 + 0.020*SL$
	tPHL	0.41	$0.37 + 0.015*SL$	$0.39 + 0.012*SL$	$0.42 + 0.010*SL$
	tR	0.20	$0.11 + 0.043*SL$	$0.10 + 0.047*SL$	$0.08 + 0.048*SL$
	tF	0.15	$0.12 + 0.018*SL$	$0.12 + 0.018*SL$	$0.10 + 0.019*SL$
G to QN	tPLH	0.62	$0.59 + 0.019*SL$	$0.58 + 0.020*SL$	$0.57 + 0.020*SL$
	tPHL	0.57	$0.53 + 0.016*SL$	$0.55 + 0.012*SL$	$0.58 + 0.010*SL$
	tR	0.20	$0.11 + 0.045*SL$	$0.10 + 0.047*SL$	$0.08 + 0.048*SL$
	tF	0.15	$0.12 + 0.018*SL$	$0.11 + 0.018*SL$	$0.10 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### LD1D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	tPWH	0.920
Input Hold Time (D to G)	tHD	0.178
Input Setup Time (D to G)	tSU	0.178





# LD1D2Q/LD1D4Q

D-Latch Active High Gate with Q Output Only, 2X Drive or 4X Drive

Inputs: D, G

Outputs: Q

Input Loading (SL):

- LD1D2Q: D: 3, G: 1

- LD1D4Q: D: 3, G: 1

Maximum Fanout (Rec. SL):

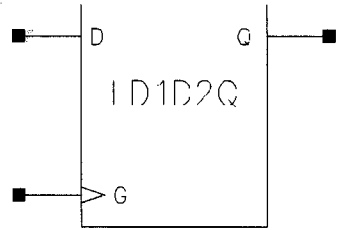
- LD1D2Q: 56

- LD1D4Q: 112

Gate Count:

- LD1D2Q: 4

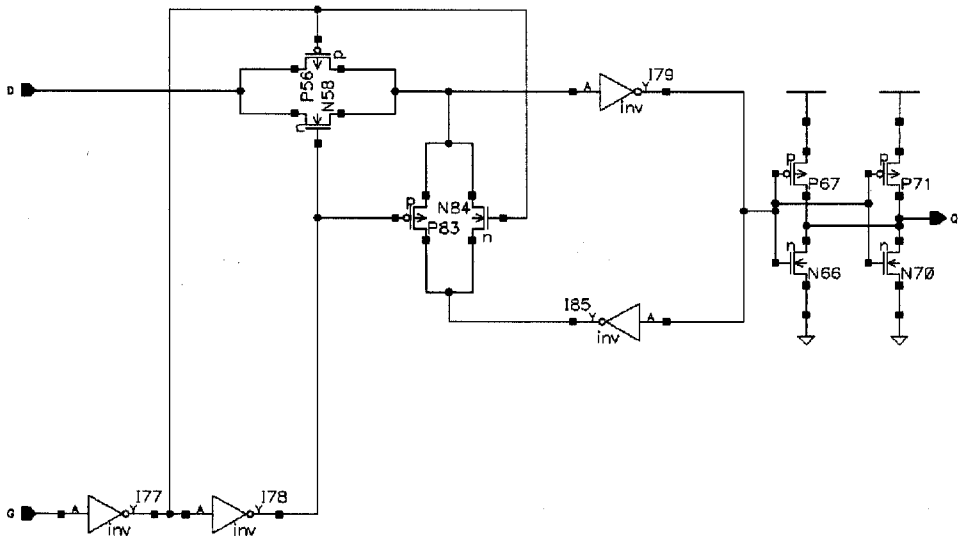
- LD1D4Q: 5



**Symbol**

D	G	Qn+1
0	1	0
1	1	1
x	0	Qn

**Truth Table**



**Schematic**

**LD1D2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.28	$0.24 + 0.021*SL$	$0.24 + 0.020*SL$	$0.24 + 0.020*SL$
	tPHL	0.46	$0.42 + 0.018*SL$	$0.44 + 0.012*SL$	$0.48 + 0.010*SL$
	tR	0.21	$0.12 + 0.044*SL$	$0.12 + 0.046*SL$	$0.10 + 0.047*SL$
	tF	0.18	$0.14 + 0.018*SL$	$0.14 + 0.018*SL$	$0.13 + 0.018*SL$
G to Q	tPLH	0.44	$0.40 + 0.022*SL$	$0.40 + 0.020*SL$	$0.40 + 0.020*SL$
	tPHL	0.45	$0.42 + 0.017*SL$	$0.44 + 0.012*SL$	$0.47 + 0.010*SL$
	tR	0.20	$0.11 + 0.042*SL$	$0.10 + 0.046*SL$	$0.09 + 0.047*SL$
	tF	0.16	$0.12 + 0.019*SL$	$0.12 + 0.018*SL$	$0.11 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD1D2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	tPWH	0.920
Input Hold Time (D to G)	tHD	0.178
Input Setup Time (D to G)	tSU	0.178

**LD1D4Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.34	$0.32 + 0.012*SL$	$0.32 + 0.011*SL$	$0.33 + 0.011*SL$
	tPHL	0.51	$0.49 + 0.011*SL$	$0.50 + 0.008*SL$	$0.54 + 0.006*SL$
	tR	0.20	$0.15 + 0.023*SL$	$0.15 + 0.025*SL$	$0.13 + 0.026*SL$
	tF	0.21	$0.20 + 0.006*SL$	$0.19 + 0.009*SL$	$0.19 + 0.010*SL$
G to Q	tPLH	0.48	$0.46 + 0.012*SL$	$0.46 + 0.011*SL$	$0.46 + 0.011*SL$
	tPHL	0.51	$0.49 + 0.012*SL$	$0.50 + 0.008*SL$	$0.53 + 0.006*SL$
	tR	0.18	$0.13 + 0.024*SL$	$0.13 + 0.025*SL$	$0.11 + 0.026*SL$
	tF	0.19	$0.16 + 0.013*SL$	$0.17 + 0.010*SL$	$0.17 + 0.010*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD1D4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	tPWH	0.920
Input Hold Time (D to G)	tHD	0.123
Input Setup Time (D to G)	tSU	0.178

# LD1A

## D-Latch Active High Gate with 3-State Output

Inputs: D, G, E

Outputs: Q

Input Loading (SL):

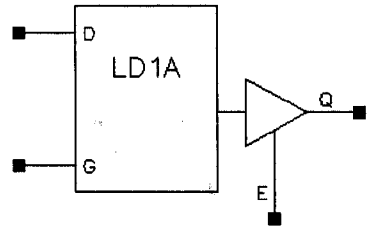
- D: 3

- G: 1

- E: 1.5

Maximum Fanout (Rec. SL): 28

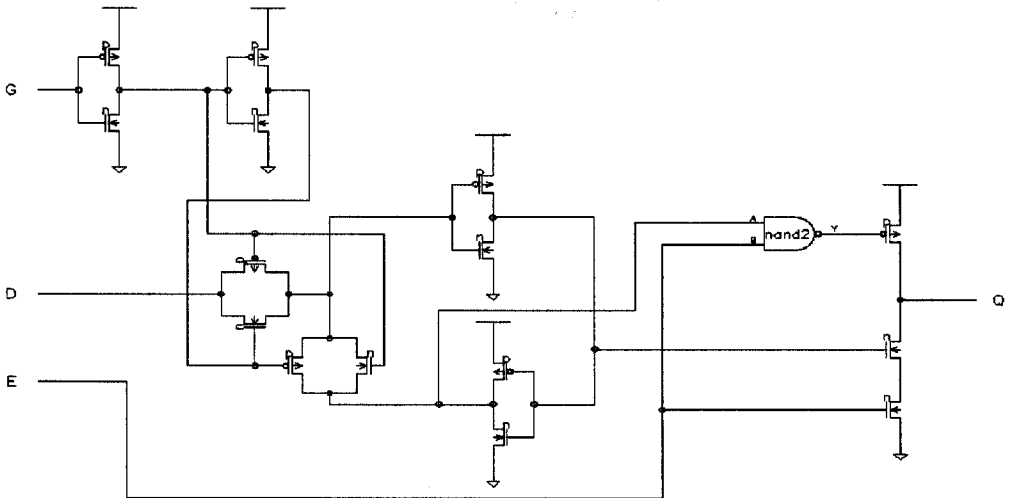
Gate Count: 5



Symbol

D	G	E	Q <sub>n+1</sub>
x	x	0	Hi-Z
0	1	1	0
1	1	1	1
x	0	1	Q <sub>n</sub>

Truth Table



Schematic

**LD1A Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
E to Q	tPLH	0.20	$0.11 + 0.048^*SL$	$0.13 + 0.040^*SL$	$0.14 + 0.040^*SL$
	tPHL	0.04	$-0.07 + 0.052^*SL$	$-0.01 + 0.034^*SL$	$0.05 + 0.031^*SL$
	tR	0.32	$0.15 + 0.084^*SL$	$0.13 + 0.090^*SL$	$0.09 + 0.092^*SL$
	tF	0.35	$0.22 + 0.063^*SL$	$0.22 + 0.062^*SL$	$0.15 + 0.065^*SL$
	tPLZ	0.40	$0.40 + -0.000^*SL$	$0.40 + -0.000^*SL$	$0.40 + -0.000^*SL$
	tPHZ	0.49	$0.49 + -0.000^*SL$	$0.49 + -0.000^*SL$	$0.49 + -0.000^*SL$
D to Q	tPLH	0.48	$0.39 + 0.045^*SL$	$0.40 + 0.040^*SL$	$0.41 + 0.040^*SL$
	tPHL	0.53	$0.47 + 0.028^*SL$	$0.47 + 0.029^*SL$	$0.44 + 0.030^*SL$
	tR	0.28	$0.11 + 0.088^*SL$	$0.10 + 0.092^*SL$	$0.08 + 0.092^*SL$
	tF	0.34	$0.24 + 0.048^*SL$	$0.20 + 0.061^*SL$	$0.10 + 0.066^*SL$
G to Q	tPLH	0.65	$0.56 + 0.045^*SL$	$0.58 + 0.040^*SL$	$0.59 + 0.040^*SL$
	tPHL	0.53	$0.47 + 0.029^*SL$	$0.47 + 0.029^*SL$	$0.44 + 0.030^*SL$
	tR	0.28	$0.10 + 0.089^*SL$	$0.10 + 0.092^*SL$	$0.08 + 0.092^*SL$
	tF	0.33	$0.23 + 0.049^*SL$	$0.19 + 0.062^*SL$	$0.10 + 0.066^*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD1A Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	tPWH	0.920
Input Hold Time (D to G)	tHD	0.233
Input Setup Time (D to G)	tSU	0.123

# LD1B

## D-Latch Active High Gate with WR, WRN Inputs

Inputs: D, WR, WRN, RD

Outputs: QN, ZN

Input Loading (SL):

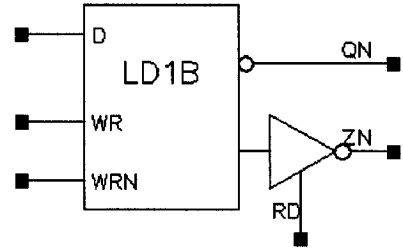
- D: 3

- WR, WRN: 1

- RD: 1.5

Maximum Fanout (Rec. SL): 14

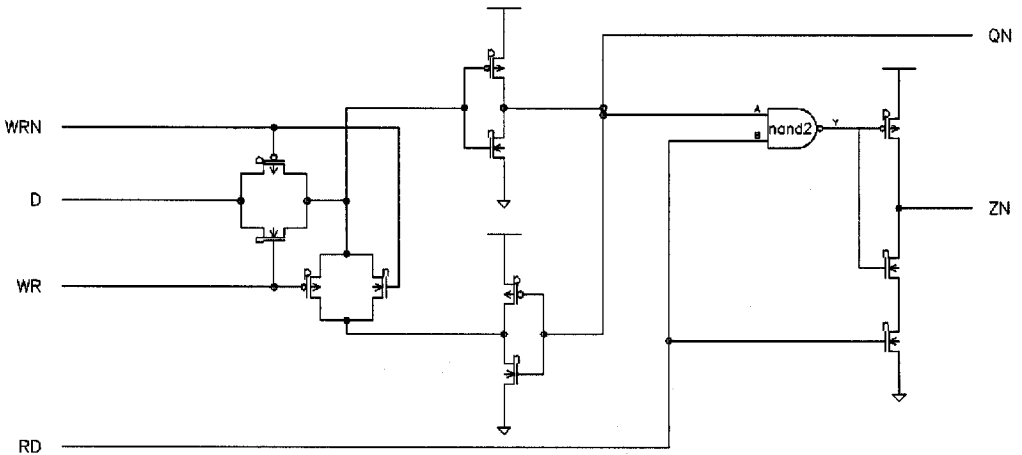
Gate Count: 4



**Symbol**

D	WR	WRN	RD	QN <sub>n+1</sub>	ZN <sub>n+1</sub>
0	1	0	0	1	Hi-Z
1	1	0	0	0	Hi-Z
0	1	0	1	1	1
1	1	0	1	0	0
x	0	1	0	QN <sub>n</sub>	Hi-Z
x	0	1	1	QN <sub>n</sub>	QN <sub>n</sub>

**Truth Table**



**Schematic**

**LD1B Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to QN	tPLH	0.45	$0.36 + 0.044*SL$	$0.36 + 0.042*SL$	$0.35 + 0.043*SL$
	tPHL	0.17	$0.10 + 0.036*SL$	$0.13 + 0.024*SL$	$0.22 + 0.020*SL$
	tR	0.61	$0.43 + 0.089*SL$	$0.41 + 0.097*SL$	$0.32 + 0.102*SL$
	tF	0.42	$0.34 + 0.039*SL$	$0.35 + 0.034*SL$	$0.32 + 0.036*SL$
WR to QN	tPLH	0.28	$0.19 + 0.044*SL$	$0.19 + 0.043*SL$	$0.20 + 0.043*SL$
	tPHL	0.34	$0.29 + 0.025*SL$	$0.30 + 0.021*SL$	$0.32 + 0.020*SL$
	tR	0.52	$0.33 + 0.097*SL$	$0.31 + 0.101*SL$	$0.29 + 0.103*SL$
	tF	0.27	$0.20 + 0.037*SL$	$0.20 + 0.036*SL$	$0.16 + 0.038*SL$
WRN to QN	tPLH	0.28	$0.19 + 0.044*SL$	$0.19 + 0.043*SL$	$0.20 + 0.043*SL$
	tPHL	0.34	$0.29 + 0.025*SL$	$0.30 + 0.021*SL$	$0.32 + 0.020*SL$
	tR	0.52	$0.33 + 0.097*SL$	$0.31 + 0.101*SL$	$0.29 + 0.103*SL$
	tF	0.27	$0.20 + 0.037*SL$	$0.20 + 0.036*SL$	$0.16 + 0.038*SL$
RD to ZN	tPLH	0.27	$0.18 + 0.043*SL$	$0.19 + 0.040*SL$	$0.19 + 0.040*SL$
	tPHL	0.03	$-0.07 + 0.051*SL$	$-0.01 + 0.033*SL$	$0.05 + 0.030*SL$
	tR	0.30	$0.14 + 0.084*SL$	$0.12 + 0.090*SL$	$0.09 + 0.092*SL$
	tF	0.34	$0.22 + 0.061*SL$	$0.22 + 0.059*SL$	$0.15 + 0.063*SL$
	tPLZ	0.40	$0.40 + -0.000*SL$	$0.40 + -0.000*SL$	$0.40 + -0.000*SL$
	tPHZ	0.49	$0.49 + -0.001*SL$	$0.49 + -0.000*SL$	$0.49 + -0.000*SL$
D to ZN	tPLH	0.73	$0.55 + 0.091*SL$	$0.57 + 0.083*SL$	$0.60 + 0.082*SL$
	tPHL	0.45	$0.29 + 0.078*SL$	$0.35 + 0.060*SL$	$0.44 + 0.055*SL$
	tR	0.29	$0.11 + 0.090*SL$	$0.10 + 0.092*SL$	$0.08 + 0.093*SL$
	tF	0.23	$0.11 + 0.061*SL$	$0.10 + 0.063*SL$	$0.08 + 0.064*SL$
WR to ZN	tPLH	0.56	$0.38 + 0.093*SL$	$0.40 + 0.084*SL$	$0.45 + 0.082*SL$
	tPHL	0.60	$0.47 + 0.067*SL$	$0.50 + 0.057*SL$	$0.53 + 0.055*SL$
	tR	0.29	$0.11 + 0.089*SL$	$0.10 + 0.092*SL$	$0.08 + 0.093*SL$
	tF	0.23	$0.11 + 0.060*SL$	$0.10 + 0.063*SL$	$0.08 + 0.064*SL$
WRN to ZN	tPLH	0.56	$0.38 + 0.093*SL$	$0.40 + 0.084*SL$	$0.45 + 0.082*SL$
	tPHL	0.60	$0.47 + 0.067*SL$	$0.50 + 0.057*SL$	$0.53 + 0.055*SL$
	tR	0.29	$0.11 + 0.089*SL$	$0.10 + 0.092*SL$	$0.08 + 0.093*SL$
	tF	0.23	$0.11 + 0.060*SL$	$0.10 + 0.063*SL$	$0.08 + 0.064*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD1B Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (WRN)	tPWL	0.920
Pulse Width High (WR)	tPWH	0.920
Input Hold Time (D to WR)	tHD	0.000
Input Hold Time (D to WRN)	tHD	0.000

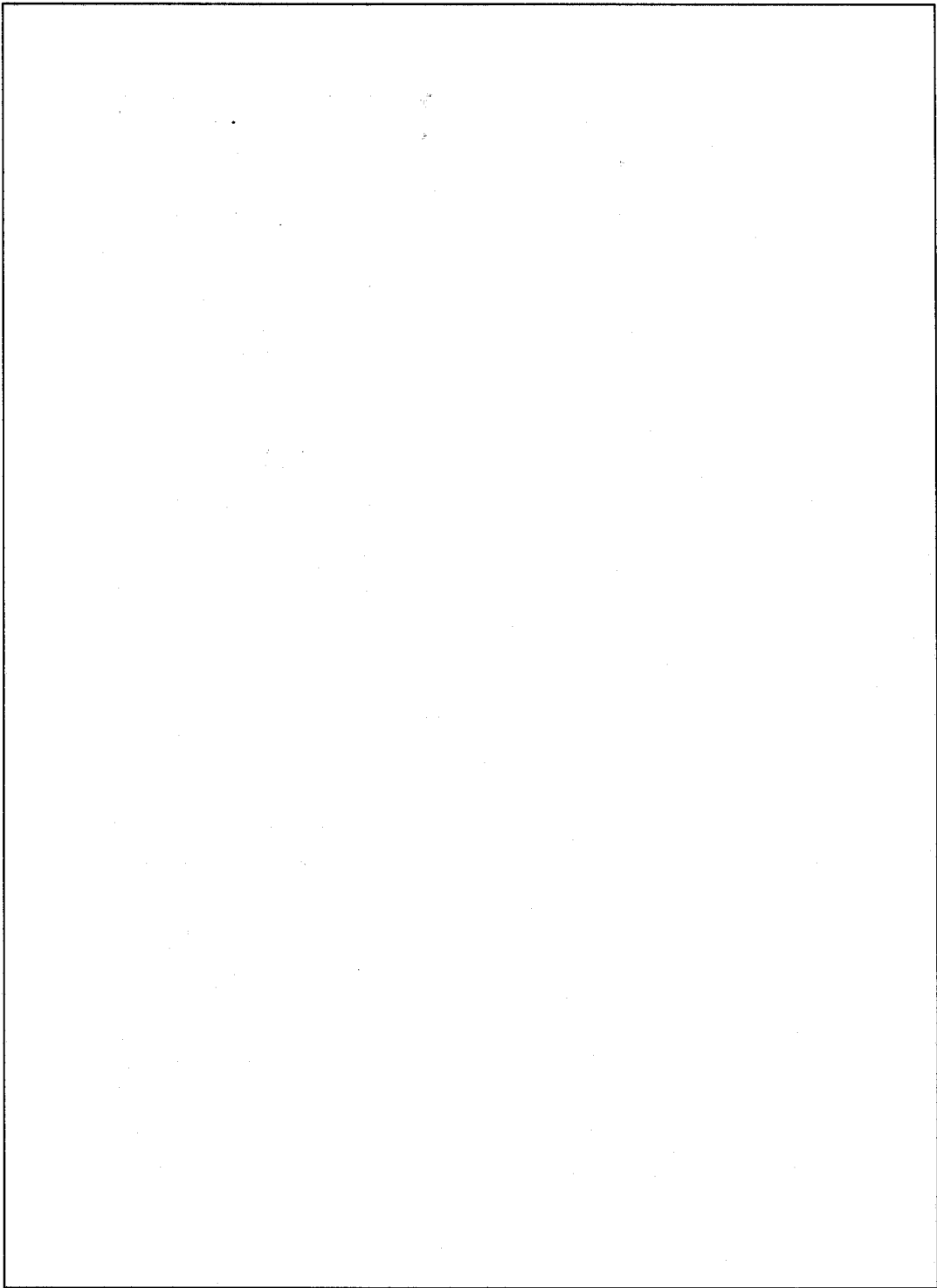
# LD1B

## D-Latch Active High Gate with WR, WRN Inputs

### LD1B Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Input Setup Time (D to WR)	tSU	0.561
Input Setup Time (D to WRN)	tSU	0.561





# LD1S/LD1SD2

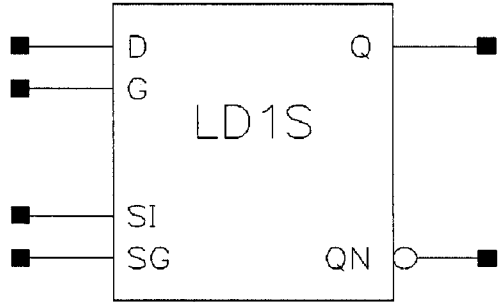
## D-Latch Active High Gate with scan

Inputs: D, G, SI, SG  
 Outputs: Q, QN

Input Loading (SL):  
 - LD1S: D, SI: All : 1  
 - LD1SD2: G, SG: All : 2

Maximum Fanout (Rec. SL):  
 - LD1S: 28  
 - LD1SD2: 56

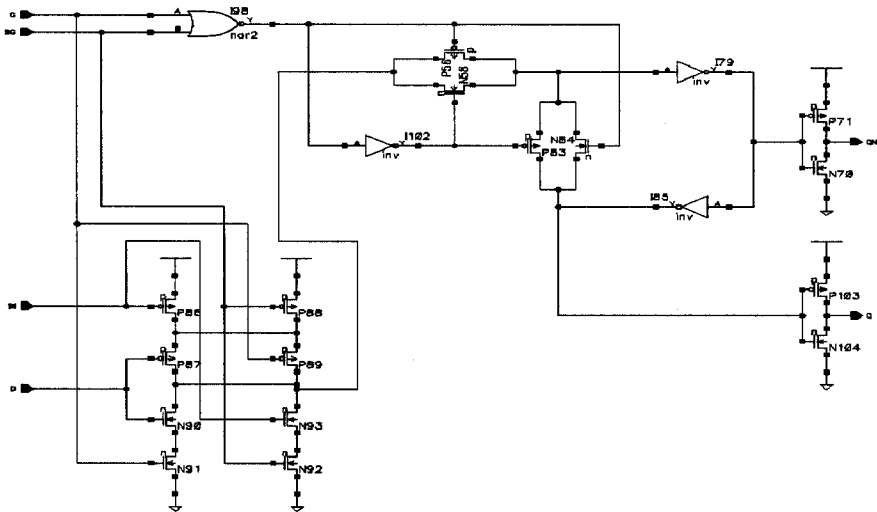
Gate Count:  
 - LD1S: 7  
 - LD1SD2: 8



**Symbol**

D	G	SI	SG	Qn+1	QNn+1
x	0	x	0	Qn	QNn
x	x	1	1	1	0
x	0	0	1	0	1
1	1	x	x	1	0
0	1	x	0	0	1
0	1	0	1	0	1

**Truth Table**



**Schematic**

**LD1S Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.77	$0.70 + 0.039*SL$	$0.69 + 0.040*SL$	$0.69 + 0.040*SL$
	tPHL	1.01	$0.95 + 0.026*SL$	$0.97 + 0.021*SL$	$0.99 + 0.020*SL$
	tR	0.28	$0.10 + 0.089*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.10 + 0.035*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
G to Q	tPLH	0.69	$0.61 + 0.039*SL$	$0.61 + 0.040*SL$	$0.60 + 0.040*SL$
	tPHL	1.01	$0.96 + 0.026*SL$	$0.97 + 0.021*SL$	$0.99 + 0.020*SL$
	tR	0.28	$0.10 + 0.088*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.10 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
SI to Q	tPLH	0.84	$0.76 + 0.039*SL$	$0.76 + 0.040*SL$	$0.75 + 0.040*SL$
	tPHL	1.02	$0.97 + 0.026*SL$	$0.98 + 0.021*SL$	$1.00 + 0.020*SL$
	tR	0.28	$0.10 + 0.088*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.10 + 0.035*SL$	$0.09 + 0.037*SL$	$0.07 + 0.038*SL$
SG to Q	tPLH	0.75	$0.67 + 0.040*SL$	$0.67 + 0.040*SL$	$0.67 + 0.040*SL$
	tPHL	1.01	$0.96 + 0.026*SL$	$0.97 + 0.021*SL$	$0.99 + 0.020*SL$
	tR	0.28	$0.10 + 0.088*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.10 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
D to QN	tPLH	0.93	$0.85 + 0.041*SL$	$0.85 + 0.040*SL$	$0.85 + 0.040*SL$
	tPHL	0.63	$0.58 + 0.027*SL$	$0.60 + 0.021*SL$	$0.62 + 0.020*SL$
	tR	0.30	$0.12 + 0.089*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.18	$0.11 + 0.037*SL$	$0.11 + 0.037*SL$	$0.08 + 0.038*SL$
G to QN	tPLH	0.93	$0.85 + 0.041*SL$	$0.86 + 0.040*SL$	$0.86 + 0.040*SL$
	tPHL	0.54	$0.49 + 0.028*SL$	$0.51 + 0.021*SL$	$0.54 + 0.020*SL$
	tR	0.30	$0.12 + 0.089*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.18	$0.11 + 0.036*SL$	$0.11 + 0.037*SL$	$0.08 + 0.038*SL$
SI to QN	tPLH	0.94	$0.86 + 0.041*SL$	$0.86 + 0.040*SL$	$0.86 + 0.040*SL$
	tPHL	0.70	$0.64 + 0.028*SL$	$0.66 + 0.021*SL$	$0.69 + 0.020*SL$
	tR	0.30	$0.12 + 0.089*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.18	$0.11 + 0.037*SL$	$0.11 + 0.036*SL$	$0.08 + 0.038*SL$
SG to QN	tPLH	0.93	$0.85 + 0.041*SL$	$0.86 + 0.040*SL$	$0.86 + 0.040*SL$
	tPHL	0.61	$0.55 + 0.028*SL$	$0.57 + 0.021*SL$	$0.60 + 0.020*SL$
	tR	0.30	$0.12 + 0.088*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.18	$0.11 + 0.037*SL$	$0.11 + 0.037*SL$	$0.08 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD1S Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	tPWH	0.920

# LD1S

D-Latch Active High Gate with scan

## LD1S Timing Requirements [Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (SG)	tPWH	0.920
Input Hold Time (D to G)	tHD	0.000
Input Hold Time (SI to SG)	tHD	0.000
Input Setup Time (D to G)	tSU	0.561
Input Setup Time (SI to SG)	tSU	0.616

**LD1SD2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	1PLH	0.82	$0.78 + 0.019 \cdot \text{SL}$	$0.78 + 0.020 \cdot \text{SL}$	$0.77 + 0.020 \cdot \text{SL}$
	1PHL	1.07	$1.04 + 0.016 \cdot \text{SL}$	$1.05 + 0.011 \cdot \text{SL}$	$1.08 + 0.010 \cdot \text{SL}$
	1R	0.20	$0.11 + 0.044 \cdot \text{SL}$	$0.10 + 0.047 \cdot \text{SL}$	$0.08 + 0.048 \cdot \text{SL}$
	1F	0.15	$0.12 + 0.016 \cdot \text{SL}$	$0.12 + 0.018 \cdot \text{SL}$	$0.10 + 0.019 \cdot \text{SL}$
G to Q	1PLH	0.73	$0.70 + 0.018 \cdot \text{SL}$	$0.69 + 0.020 \cdot \text{SL}$	$0.68 + 0.020 \cdot \text{SL}$
	1PHL	1.07	$1.04 + 0.015 \cdot \text{SL}$	$1.05 + 0.012 \cdot \text{SL}$	$1.08 + 0.010 \cdot \text{SL}$
	1R	0.20	$0.11 + 0.044 \cdot \text{SL}$	$0.10 + 0.047 \cdot \text{SL}$	$0.08 + 0.048 \cdot \text{SL}$
	1F	0.15	$0.12 + 0.017 \cdot \text{SL}$	$0.12 + 0.018 \cdot \text{SL}$	$0.10 + 0.019 \cdot \text{SL}$
SI to Q	1PLH	0.89	$0.85 + 0.018 \cdot \text{SL}$	$0.84 + 0.020 \cdot \text{SL}$	$0.83 + 0.020 \cdot \text{SL}$
	1PHL	1.08	$1.05 + 0.015 \cdot \text{SL}$	$1.06 + 0.012 \cdot \text{SL}$	$1.09 + 0.010 \cdot \text{SL}$
	1R	0.20	$0.11 + 0.044 \cdot \text{SL}$	$0.10 + 0.047 \cdot \text{SL}$	$0.08 + 0.048 \cdot \text{SL}$
	1F	0.15	$0.12 + 0.017 \cdot \text{SL}$	$0.12 + 0.018 \cdot \text{SL}$	$0.10 + 0.019 \cdot \text{SL}$
SG to Q	1PLH	0.79	$0.76 + 0.018 \cdot \text{SL}$	$0.75 + 0.020 \cdot \text{SL}$	$0.74 + 0.020 \cdot \text{SL}$
	1PHL	1.07	$1.04 + 0.015 \cdot \text{SL}$	$1.05 + 0.011 \cdot \text{SL}$	$1.08 + 0.010 \cdot \text{SL}$
	1R	0.20	$0.11 + 0.046 \cdot \text{SL}$	$0.11 + 0.047 \cdot \text{SL}$	$0.08 + 0.048 \cdot \text{SL}$
	1F	0.15	$0.12 + 0.015 \cdot \text{SL}$	$0.12 + 0.018 \cdot \text{SL}$	$0.10 + 0.019 \cdot \text{SL}$
D to QN	1PLH	0.94	$0.89 + 0.022 \cdot \text{SL}$	$0.90 + 0.020 \cdot \text{SL}$	$0.90 + 0.020 \cdot \text{SL}$
	1PHL	0.64	$0.61 + 0.017 \cdot \text{SL}$	$0.62 + 0.012 \cdot \text{SL}$	$0.66 + 0.010 \cdot \text{SL}$
	1R	0.22	$0.13 + 0.044 \cdot \text{SL}$	$0.13 + 0.045 \cdot \text{SL}$	$0.10 + 0.047 \cdot \text{SL}$
	1F	0.17	$0.13 + 0.020 \cdot \text{SL}$	$0.14 + 0.018 \cdot \text{SL}$	$0.12 + 0.019 \cdot \text{SL}$
G to QN	1PLH	0.94	$0.90 + 0.022 \cdot \text{SL}$	$0.90 + 0.020 \cdot \text{SL}$	$0.90 + 0.020 \cdot \text{SL}$
	1PHL	0.56	$0.52 + 0.017 \cdot \text{SL}$	$0.54 + 0.012 \cdot \text{SL}$	$0.58 + 0.010 \cdot \text{SL}$
	1R	0.22	$0.13 + 0.045 \cdot \text{SL}$	$0.13 + 0.045 \cdot \text{SL}$	$0.10 + 0.047 \cdot \text{SL}$
	1F	0.17	$0.13 + 0.020 \cdot \text{SL}$	$0.13 + 0.018 \cdot \text{SL}$	$0.12 + 0.019 \cdot \text{SL}$
SI to QN	1PLH	0.95	$0.91 + 0.022 \cdot \text{SL}$	$0.91 + 0.020 \cdot \text{SL}$	$0.91 + 0.020 \cdot \text{SL}$
	1PHL	0.71	$0.67 + 0.018 \cdot \text{SL}$	$0.69 + 0.012 \cdot \text{SL}$	$0.73 + 0.010 \cdot \text{SL}$
	1R	0.22	$0.13 + 0.044 \cdot \text{SL}$	$0.13 + 0.045 \cdot \text{SL}$	$0.10 + 0.047 \cdot \text{SL}$
	1F	0.17	$0.13 + 0.020 \cdot \text{SL}$	$0.14 + 0.018 \cdot \text{SL}$	$0.12 + 0.019 \cdot \text{SL}$
SG to QN	1PLH	0.94	$0.90 + 0.022 \cdot \text{SL}$	$0.90 + 0.020 \cdot \text{SL}$	$0.90 + 0.020 \cdot \text{SL}$
	1PHL	0.62	$0.59 + 0.017 \cdot \text{SL}$	$0.60 + 0.012 \cdot \text{SL}$	$0.64 + 0.010 \cdot \text{SL}$
	1R	0.22	$0.13 + 0.045 \cdot \text{SL}$	$0.13 + 0.045 \cdot \text{SL}$	$0.10 + 0.047 \cdot \text{SL}$
	1F	0.17	$0.14 + 0.018 \cdot \text{SL}$	$0.14 + 0.018 \cdot \text{SL}$	$0.12 + 0.019 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **LD1SD2 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	1PWH	0.920

# LD1SD2

D-Latch Active High Gate with scan and 2X Drive

## LD1SD2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (SG)	tPWH	0.920
Input Hold Time (D to G)	tHD	0.000
Input Hold Time (SI to SG)	tHD	0.000
Input Setup Time (D to G)	tSU	0.561
Input Setup Time (SI to SG)	tSU	0.616



# LD1X4

## 4-Bit D-Latch with Active High Gate

Inputs: D0, D1, D2, D3, G

Outputs: Q0, Q1, Q2, Q3

QN0, QN1, QN2, QN3

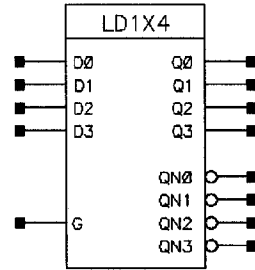
Input Loading (SL):

- D0, D1, D2, D3: 3

- G: 1

Maximum Fanout (Rec. SL): All : 28

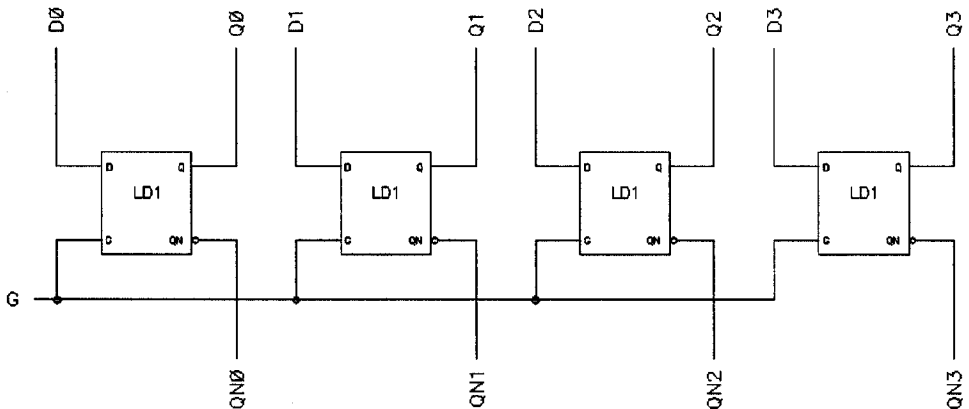
Gate Count: 13



**Symbol**

D	G	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	0	1
1	1	1	0
x	0	Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

## LD1X4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Q0	tPLH	0.28	$0.19 + 0.043 \cdot SL$	$0.20 + 0.043 \cdot SL$	$0.20 + 0.043 \cdot SL$
	tPHL	0.44	$0.39 + 0.028 \cdot SL$	$0.40 + 0.022 \cdot SL$	$0.43 + 0.020 \cdot SL$
	tR	0.32	$0.12 + 0.098 \cdot SL$	$0.11 + 0.101 \cdot SL$	$0.09 + 0.102 \cdot SL$
	tF	0.20	$0.12 + 0.039 \cdot SL$	$0.12 + 0.039 \cdot SL$	$0.08 + 0.041 \cdot SL$
G to Q0	tPLH	0.55	$0.46 + 0.044 \cdot SL$	$0.46 + 0.043 \cdot SL$	$0.46 + 0.043 \cdot SL$
	tPHL	0.62	$0.57 + 0.028 \cdot SL$	$0.58 + 0.022 \cdot SL$	$0.61 + 0.020 \cdot SL$
	tR	0.30	$0.11 + 0.099 \cdot SL$	$0.10 + 0.102 \cdot SL$	$0.09 + 0.102 \cdot SL$
	tF	0.18	$0.10 + 0.040 \cdot SL$	$0.10 + 0.040 \cdot SL$	$0.07 + 0.041 \cdot SL$
D1 to Q1	tPLH	0.27	$0.19 + 0.041 \cdot SL$	$0.19 + 0.040 \cdot SL$	$0.19 + 0.040 \cdot SL$
	tPHL	0.44	$0.39 + 0.028 \cdot SL$	$0.40 + 0.021 \cdot SL$	$0.43 + 0.020 \cdot SL$
	tR	0.29	$0.12 + 0.089 \cdot SL$	$0.11 + 0.092 \cdot SL$	$0.09 + 0.093 \cdot SL$
	tF	0.19	$0.12 + 0.037 \cdot SL$	$0.12 + 0.036 \cdot SL$	$0.08 + 0.038 \cdot SL$
G to Q1	tPLH	0.54	$0.46 + 0.041 \cdot SL$	$0.46 + 0.040 \cdot SL$	$0.46 + 0.040 \cdot SL$
	tPHL	0.62	$0.56 + 0.027 \cdot SL$	$0.58 + 0.021 \cdot SL$	$0.61 + 0.020 \cdot SL$
	tR	0.28	$0.10 + 0.089 \cdot SL$	$0.09 + 0.092 \cdot SL$	$0.08 + 0.093 \cdot SL$
	tF	0.17	$0.09 + 0.038 \cdot SL$	$0.10 + 0.037 \cdot SL$	$0.07 + 0.038 \cdot SL$
D2 to Q2	tPLH	0.28	$0.19 + 0.043 \cdot SL$	$0.20 + 0.043 \cdot SL$	$0.20 + 0.043 \cdot SL$
	tPHL	0.44	$0.39 + 0.028 \cdot SL$	$0.40 + 0.022 \cdot SL$	$0.43 + 0.020 \cdot SL$
	tR	0.32	$0.12 + 0.098 \cdot SL$	$0.11 + 0.101 \cdot SL$	$0.09 + 0.102 \cdot SL$
	tF	0.20	$0.12 + 0.039 \cdot SL$	$0.12 + 0.039 \cdot SL$	$0.08 + 0.041 \cdot SL$
G to Q2	tPLH	0.55	$0.46 + 0.044 \cdot SL$	$0.46 + 0.043 \cdot SL$	$0.46 + 0.043 \cdot SL$
	tPHL	0.62	$0.56 + 0.028 \cdot SL$	$0.58 + 0.022 \cdot SL$	$0.61 + 0.020 \cdot SL$
	tR	0.30	$0.11 + 0.099 \cdot SL$	$0.10 + 0.102 \cdot SL$	$0.09 + 0.102 \cdot SL$
	tF	0.18	$0.10 + 0.040 \cdot SL$	$0.10 + 0.040 \cdot SL$	$0.07 + 0.041 \cdot SL$
D3 to Q3	tPLH	0.27	$0.19 + 0.041 \cdot SL$	$0.20 + 0.040 \cdot SL$	$0.19 + 0.040 \cdot SL$
	tPHL	0.44	$0.38 + 0.028 \cdot SL$	$0.40 + 0.021 \cdot SL$	$0.43 + 0.020 \cdot SL$
	tR	0.29	$0.12 + 0.089 \cdot SL$	$0.11 + 0.092 \cdot SL$	$0.09 + 0.093 \cdot SL$
	tF	0.19	$0.12 + 0.037 \cdot SL$	$0.12 + 0.036 \cdot SL$	$0.08 + 0.038 \cdot SL$
G to Q3	tPLH	0.54	$0.46 + 0.041 \cdot SL$	$0.46 + 0.040 \cdot SL$	$0.46 + 0.040 \cdot SL$
	tPHL	0.62	$0.56 + 0.027 \cdot SL$	$0.58 + 0.021 \cdot SL$	$0.61 + 0.020 \cdot SL$
	tR	0.28	$0.10 + 0.089 \cdot SL$	$0.09 + 0.092 \cdot SL$	$0.08 + 0.093 \cdot SL$
	tF	0.17	$0.09 + 0.038 \cdot SL$	$0.10 + 0.037 \cdot SL$	$0.07 + 0.038 \cdot SL$
D0 to QN0	tPLH	0.59	$0.51 + 0.041 \cdot SL$	$0.51 + 0.042 \cdot SL$	$0.50 + 0.043 \cdot SL$
	tPHL	0.35	$0.30 + 0.027 \cdot SL$	$0.31 + 0.021 \cdot SL$	$0.33 + 0.020 \cdot SL$
	tR	0.30	$0.10 + 0.098 \cdot SL$	$0.09 + 0.102 \cdot SL$	$0.08 + 0.102 \cdot SL$
	tF	0.17	$0.10 + 0.040 \cdot SL$	$0.10 + 0.040 \cdot SL$	$0.06 + 0.041 \cdot SL$
G to QN0	tPLH	0.77	$0.68 + 0.042 \cdot SL$	$0.68 + 0.043 \cdot SL$	$0.68 + 0.043 \cdot SL$
	tPHL	0.61	$0.56 + 0.027 \cdot SL$	$0.57 + 0.021 \cdot SL$	$0.59 + 0.020 \cdot SL$
	tR	0.30	$0.10 + 0.100 \cdot SL$	$0.10 + 0.102 \cdot SL$	$0.08 + 0.102 \cdot SL$
	tF	0.17	$0.10 + 0.038 \cdot SL$	$0.09 + 0.040 \cdot SL$	$0.06 + 0.041 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# LD1X4

## 4-Bit D-Latch with Active High Gate

### LD1X4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_{f} = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D1 to QN1	tPLH	0.58	$0.51 + 0.039*SL$	$0.50 + 0.040*SL$	$0.50 + 0.040*SL$
	tPHL	0.35	$0.30 + 0.026*SL$	$0.31 + 0.021*SL$	$0.33 + 0.020*SL$
	tR	0.28	$0.10 + 0.087*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.09 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
G to QN1	tPLH	0.76	$0.68 + 0.040*SL$	$0.68 + 0.040*SL$	$0.67 + 0.040*SL$
	tPHL	0.61	$0.56 + 0.026*SL$	$0.58 + 0.021*SL$	$0.59 + 0.020*SL$
	tR	0.28	$0.10 + 0.088*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.09 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
D2 to QN2	tPLH	0.59	$0.51 + 0.041*SL$	$0.50 + 0.042*SL$	$0.50 + 0.043*SL$
	tPHL	0.35	$0.30 + 0.027*SL$	$0.31 + 0.021*SL$	$0.33 + 0.020*SL$
	tR	0.30	$0.10 + 0.098*SL$	$0.09 + 0.102*SL$	$0.08 + 0.102*SL$
	tF	0.17	$0.10 + 0.040*SL$	$0.10 + 0.040*SL$	$0.06 + 0.041*SL$
G to QN2	tPLH	0.77	$0.68 + 0.042*SL$	$0.68 + 0.043*SL$	$0.68 + 0.043*SL$
	tPHL	0.61	$0.56 + 0.027*SL$	$0.57 + 0.021*SL$	$0.59 + 0.020*SL$
	tR	0.30	$0.10 + 0.100*SL$	$0.10 + 0.102*SL$	$0.08 + 0.102*SL$
	tF	0.17	$0.09 + 0.040*SL$	$0.09 + 0.040*SL$	$0.06 + 0.041*SL$
D3 to QN3	tPLH	0.58	$0.51 + 0.039*SL$	$0.50 + 0.040*SL$	$0.50 + 0.040*SL$
	tPHL	0.35	$0.30 + 0.026*SL$	$0.31 + 0.021*SL$	$0.33 + 0.020*SL$
	tR	0.28	$0.10 + 0.087*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.09 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
G to QN3	tPLH	0.76	$0.68 + 0.040*SL$	$0.68 + 0.040*SL$	$0.67 + 0.040*SL$
	tPHL	0.61	$0.56 + 0.026*SL$	$0.58 + 0.021*SL$	$0.59 + 0.020*SL$
	tR	0.28	$0.10 + 0.088*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.09 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### LD1X4 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (G)	tPWH	0.920
Input Hold Time (D0 to G)	tHD	0.342
Input Hold Time (D1 to G)	tHD	0.287
Input Hold Time (D2 to G)	tHD	0.342
Input Hold Time (D3 to G)	tHD	0.342
Input Setup Time (D0 to G)	tSU	0.000
Input Setup Time (D1 to G)	tSU	0.000

**LD1X4 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Input Setup Time (D2 to G)	tSU	0.000
Input Setup Time (D3 to G)	tSU	0.000

# LD2

## D-Latch Active High Gate with Reset

Inputs: D, G, RN

Out

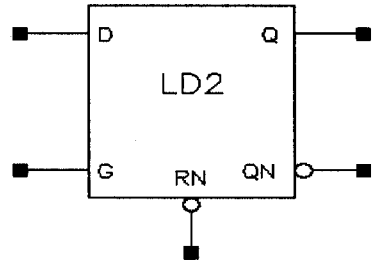
Input Loading (SL):

- D: 3

- G, RN: 1

Maximum Fanout (Rec. SL): All : 28

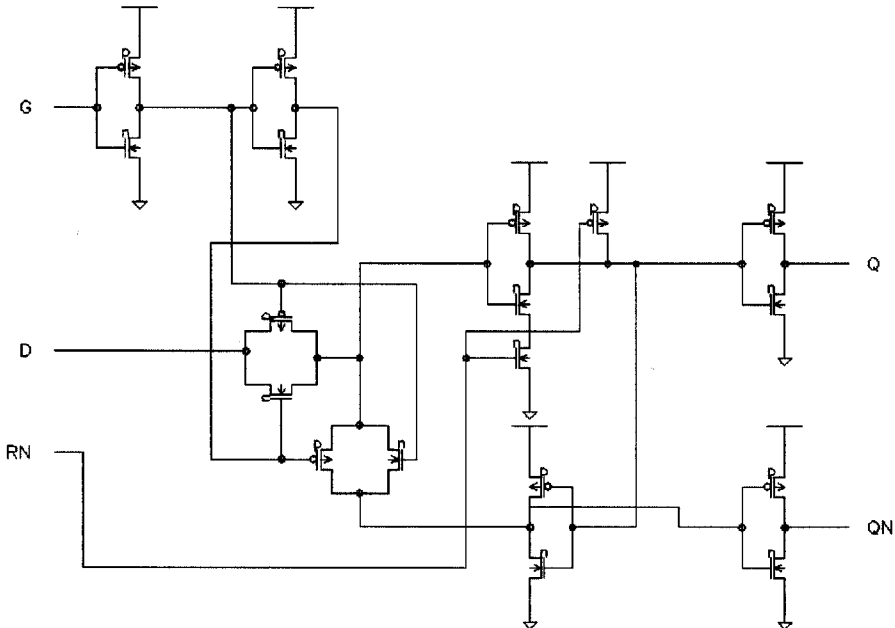
Gate Count: 5



Symbol

D	G	RN	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	1	0	1
1	1	1	1	0
x	0	1	Q <sub>n</sub>	Q <sub>Nn</sub>
x	x	0	0	1

Truth Table



Schematic

**LD2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_q$  and  $t_r = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.32	$0.23 + 0.043 \cdot SL$	$0.24 + 0.040 \cdot SL$	$0.24 + 0.040 \cdot SL$
	tPHL	0.46	$0.40 + 0.031 \cdot SL$	$0.42 + 0.022 \cdot SL$	$0.47 + 0.020 \cdot SL$
	tR	0.32	$0.14 + 0.086 \cdot SL$	$0.13 + 0.091 \cdot SL$	$0.10 + 0.092 \cdot SL$
	tF	0.22	$0.15 + 0.035 \cdot SL$	$0.15 + 0.035 \cdot SL$	$0.11 + 0.038 \cdot SL$
D to Q	tPLH	0.39	$0.31 + 0.043 \cdot SL$	$0.32 + 0.040 \cdot SL$	$0.32 + 0.040 \cdot SL$
	tPHL	0.44	$0.38 + 0.029 \cdot SL$	$0.40 + 0.021 \cdot SL$	$0.43 + 0.020 \cdot SL$
	tR	0.32	$0.14 + 0.087 \cdot SL$	$0.13 + 0.091 \cdot SL$	$0.10 + 0.092 \cdot SL$
	tF	0.20	$0.13 + 0.035 \cdot SL$	$0.13 + 0.036 \cdot SL$	$0.09 + 0.038 \cdot SL$
G to Q	tPLH	0.53	$0.44 + 0.043 \cdot SL$	$0.45 + 0.040 \cdot SL$	$0.45 + 0.040 \cdot SL$
	tPHL	0.46	$0.41 + 0.028 \cdot SL$	$0.42 + 0.021 \cdot SL$	$0.46 + 0.020 \cdot SL$
	tR	0.30	$0.12 + 0.090 \cdot SL$	$0.12 + 0.091 \cdot SL$	$0.09 + 0.093 \cdot SL$
	tF	0.18	$0.10 + 0.037 \cdot SL$	$0.10 + 0.037 \cdot SL$	$0.08 + 0.038 \cdot SL$
RN to QN	tPLH	0.61	$0.53 + 0.039 \cdot SL$	$0.53 + 0.040 \cdot SL$	$0.53 + 0.040 \cdot SL$
	tPHL	0.40	$0.34 + 0.027 \cdot SL$	$0.36 + 0.021 \cdot SL$	$0.38 + 0.020 \cdot SL$
	tR	0.28	$0.11 + 0.088 \cdot SL$	$0.10 + 0.092 \cdot SL$	$0.08 + 0.092 \cdot SL$
	tF	0.17	$0.10 + 0.034 \cdot SL$	$0.10 + 0.037 \cdot SL$	$0.07 + 0.038 \cdot SL$
D to QN	tPLH	0.59	$0.51 + 0.039 \cdot SL$	$0.51 + 0.040 \cdot SL$	$0.50 + 0.040 \cdot SL$
	tPHL	0.47	$0.42 + 0.026 \cdot SL$	$0.44 + 0.021 \cdot SL$	$0.46 + 0.020 \cdot SL$
	tR	0.28	$0.10 + 0.089 \cdot SL$	$0.09 + 0.092 \cdot SL$	$0.08 + 0.092 \cdot SL$
	tF	0.17	$0.10 + 0.035 \cdot SL$	$0.10 + 0.037 \cdot SL$	$0.07 + 0.038 \cdot SL$
G to QN	tPLH	0.61	$0.53 + 0.039 \cdot SL$	$0.53 + 0.040 \cdot SL$	$0.53 + 0.040 \cdot SL$
	tPHL	0.61	$0.55 + 0.026 \cdot SL$	$0.57 + 0.021 \cdot SL$	$0.59 + 0.020 \cdot SL$
	tR	0.28	$0.10 + 0.089 \cdot SL$	$0.09 + 0.092 \cdot SL$	$0.08 + 0.092 \cdot SL$
	tF	0.17	$0.11 + 0.033 \cdot SL$	$0.09 + 0.037 \cdot SL$	$0.07 + 0.038 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD2 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (G)	tPWH	0.920
Input Hold Time (D to G)	tHD	0.178
Input Setup Time (D to G)	tSU	0.123
Recovery Time (RN)	tRC	0.139

# LD2Q/LD2D3Q

D-Latch Active High Gate with Reset, Q Output Only, 1X Drive or 3X Drive

Inputs: D, G, RN

Output: Q

Input Loading (SL): All: D: 3, G,RN: 1

Maximum Fanout (Rec. SL):

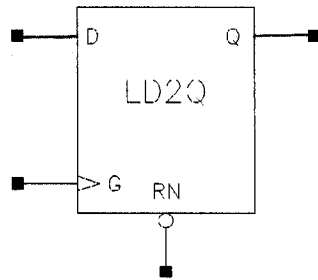
- LD2Q: 28

- LD2D3Q: 84

Gate Count:

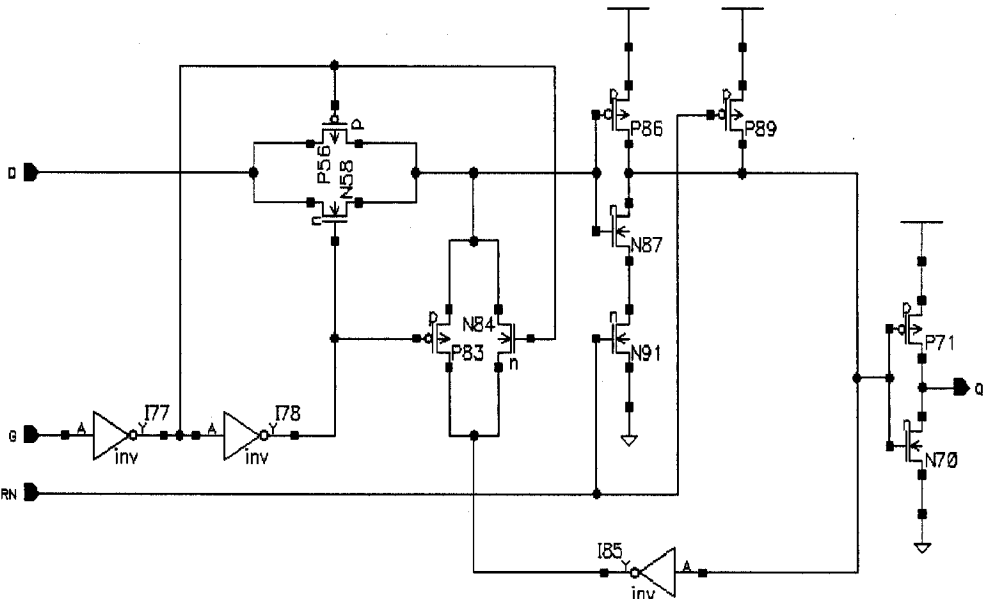
- LD2Q: 4

- LD2D3Q: 5



D	G	RN	Qn+1
0	1	1	0
1	1	1	1
x	0	1	Qn
x	x	0	0

Truth Table



Schematic

**LD2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.33	$0.24 + 0.046*SL$	$0.25 + 0.043*SL$	$0.25 + 0.043*SL$
	tPHL	0.46	$0.40 + 0.033*SL$	$0.43 + 0.022*SL$	$0.47 + 0.020*SL$
	tR	0.34	$0.15 + 0.094*SL$	$0.14 + 0.100*SL$	$0.10 + 0.102*SL$
	tF	0.23	$0.16 + 0.036*SL$	$0.16 + 0.038*SL$	$0.10 + 0.040*SL$
D to Q	tPLH	0.41	$0.31 + 0.047*SL$	$0.33 + 0.043*SL$	$0.33 + 0.043*SL$
	tPHL	0.44	$0.38 + 0.031*SL$	$0.41 + 0.022*SL$	$0.44 + 0.020*SL$
	tR	0.34	$0.15 + 0.095*SL$	$0.14 + 0.100*SL$	$0.10 + 0.102*SL$
	tF	0.21	$0.14 + 0.035*SL$	$0.13 + 0.038*SL$	$0.09 + 0.041*SL$
G to Q	tPLH	0.54	$0.44 + 0.047*SL$	$0.46 + 0.043*SL$	$0.46 + 0.043*SL$
	tPHL	0.47	$0.41 + 0.029*SL$	$0.43 + 0.022*SL$	$0.46 + 0.020*SL$
	tR	0.33	$0.13 + 0.098*SL$	$0.12 + 0.101*SL$	$0.10 + 0.102*SL$
	tF	0.19	$0.11 + 0.040*SL$	$0.11 + 0.039*SL$	$0.08 + 0.041*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (G)	tPWH	0.920
Input Hold Time (D to G)	tHD	0.123
Input Setup Time (D to G)	tSU	0.123
Recovery Time (RN)	tRC	0.139

## LD2D3Q

D-Latch Active High Gate with Reset, Q Output Only, 3X Drive

### LD2D3Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

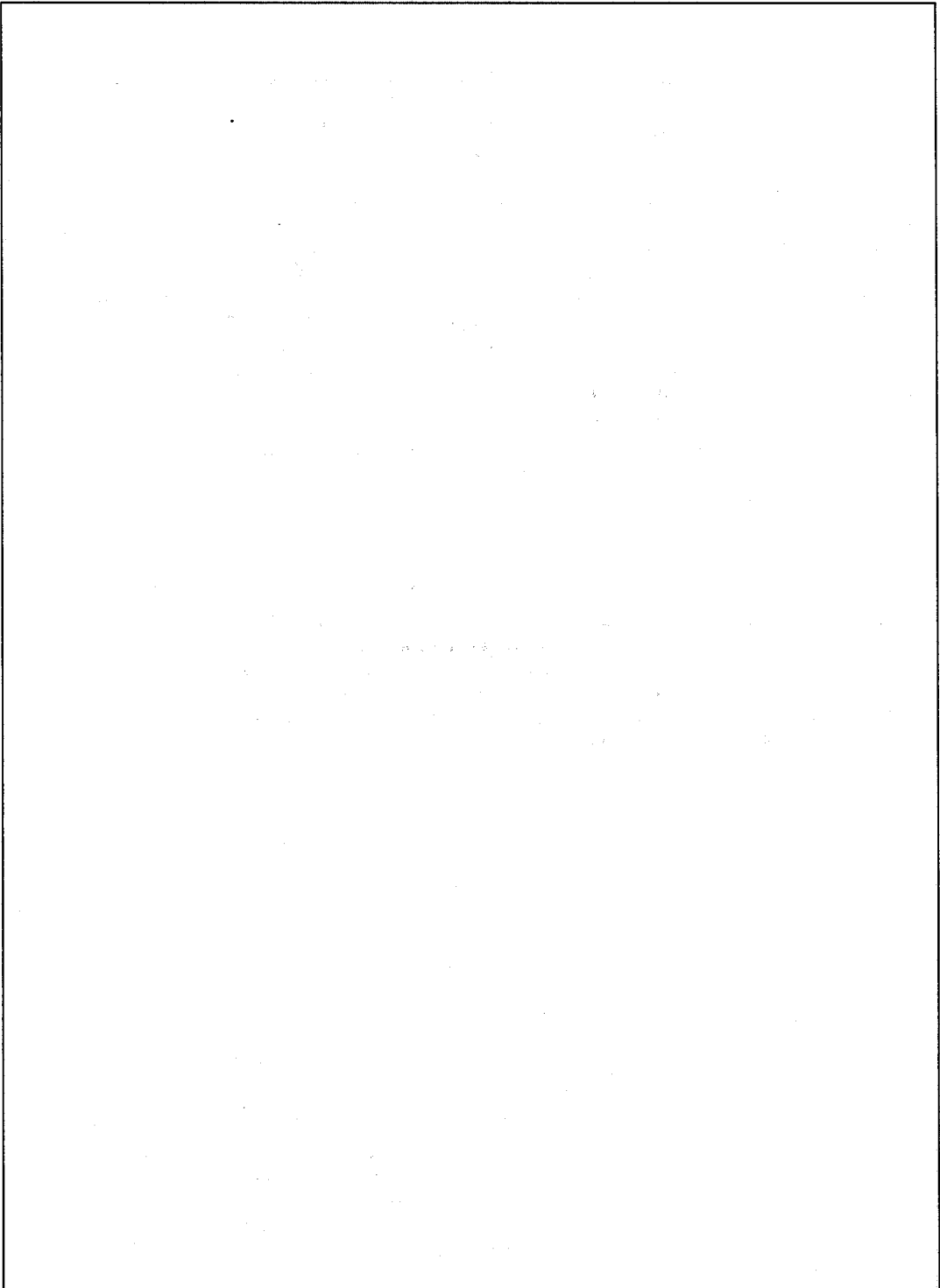
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.35	$0.32 + 0.017 \cdot SL$	$0.32 + 0.015 \cdot SL$	$0.34 + 0.014 \cdot SL$
	tPHL	0.49	$0.46 + 0.015 \cdot SL$	$0.47 + 0.010 \cdot SL$	$0.52 + 0.008 \cdot SL$
	tR	0.24	$0.18 + 0.031 \cdot SL$	$0.17 + 0.033 \cdot SL$	$0.15 + 0.034 \cdot SL$
	tF	0.22	$0.20 + 0.014 \cdot SL$	$0.20 + 0.012 \cdot SL$	$0.20 + 0.013 \cdot SL$
D to Q	tPLH	0.45	$0.41 + 0.017 \cdot SL$	$0.42 + 0.015 \cdot SL$	$0.43 + 0.014 \cdot SL$
	tPHL	0.48	$0.45 + 0.014 \cdot SL$	$0.46 + 0.010 \cdot SL$	$0.51 + 0.008 \cdot SL$
	tR	0.24	$0.18 + 0.030 \cdot SL$	$0.17 + 0.033 \cdot SL$	$0.15 + 0.034 \cdot SL$
	tF	0.21	$0.19 + 0.010 \cdot SL$	$0.18 + 0.012 \cdot SL$	$0.17 + 0.013 \cdot SL$
G to Q	tPLH	0.56	$0.52 + 0.017 \cdot SL$	$0.53 + 0.015 \cdot SL$	$0.54 + 0.014 \cdot SL$
	tPHL	0.50	$0.47 + 0.014 \cdot SL$	$0.48 + 0.010 \cdot SL$	$0.52 + 0.008 \cdot SL$
	tR	0.22	$0.16 + 0.031 \cdot SL$	$0.16 + 0.033 \cdot SL$	$0.14 + 0.034 \cdot SL$
	tF	0.18	$0.15 + 0.013 \cdot SL$	$0.15 + 0.013 \cdot SL$	$0.15 + 0.013 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### LD2D3Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (G)	tPWH	0.920
Input Hold Time (D to G)	tHD	0.178
Input Setup Time (D to G)	tSU	0.178
Recovery Time (RN)	tRC	0.139

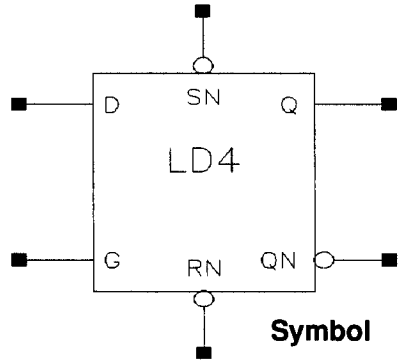




# LD4

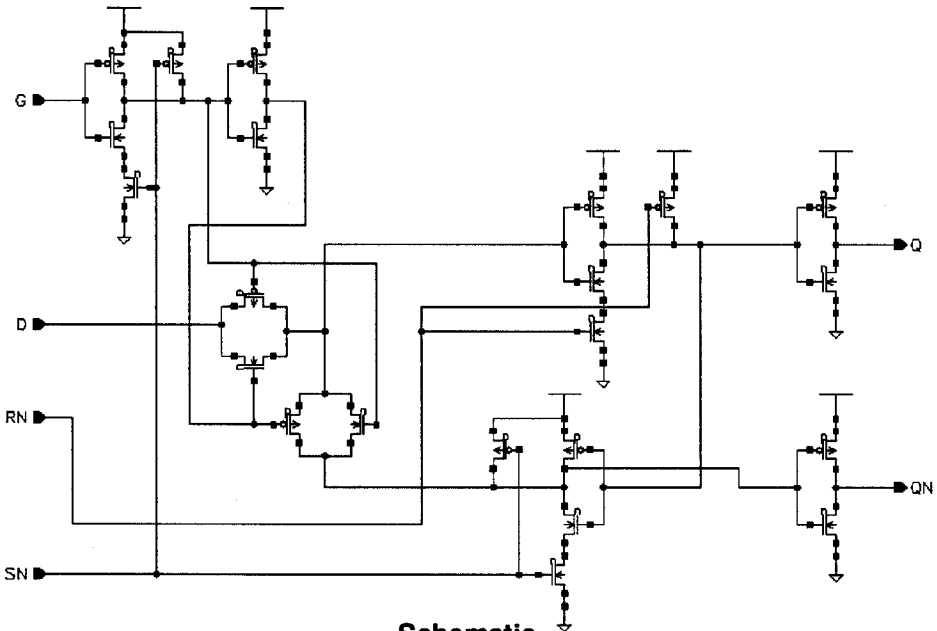
## D-Latch Active High Gate with Set, Reset, 1X Drive

Inputs: D, G, RN, SN  
 OutPUT: Q, QN  
 Input Loading (SL): D: 3, G, RN : 1  
                                   SN : 2  
 Maximum Fanout (Rec. SL): 28  
 Gate Count: 6



D	G	RN	SN	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	1	1	0	1
1	1	1	1	1	0
x	x	0	0	0	1
x	x	0	1	0	1
x	x	1	0	1	0
x	0	1	1	Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**LD4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.32	$0.23 + 0.043 \cdot \text{SL}$	$0.24 + 0.040 \cdot \text{SL}$	$0.24 + 0.040 \cdot \text{SL}$
	tPHL	0.46	$0.39 + 0.031 \cdot \text{SL}$	$0.42 + 0.022 \cdot \text{SL}$	$0.46 + 0.020 \cdot \text{SL}$
	tR	0.32	$0.14 + 0.087 \cdot \text{SL}$	$0.13 + 0.091 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$
	tF	0.22	$0.15 + 0.034 \cdot \text{SL}$	$0.15 + 0.036 \cdot \text{SL}$	$0.11 + 0.038 \cdot \text{SL}$
SN to Q	tPLH	0.94	$0.86 + 0.040 \cdot \text{SL}$	$0.86 + 0.039 \cdot \text{SL}$	$0.85 + 0.040 \cdot \text{SL}$
	tPHL	0.53	$0.48 + 0.027 \cdot \text{SL}$	$0.50 + 0.021 \cdot \text{SL}$	$0.53 + 0.020 \cdot \text{SL}$
	tR	0.31	$0.13 + 0.088 \cdot \text{SL}$	$0.12 + 0.091 \cdot \text{SL}$	$0.09 + 0.093 \cdot \text{SL}$
	tF	0.17	$0.10 + 0.036 \cdot \text{SL}$	$0.10 + 0.037 \cdot \text{SL}$	$0.08 + 0.038 \cdot \text{SL}$
D to Q	tPLH	0.40	$0.31 + 0.043 \cdot \text{SL}$	$0.32 + 0.040 \cdot \text{SL}$	$0.32 + 0.040 \cdot \text{SL}$
	tPHL	0.43	$0.37 + 0.029 \cdot \text{SL}$	$0.40 + 0.022 \cdot \text{SL}$	$0.43 + 0.020 \cdot \text{SL}$
	tR	0.32	$0.14 + 0.088 \cdot \text{SL}$	$0.13 + 0.091 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$
	tF	0.20	$0.13 + 0.034 \cdot \text{SL}$	$0.13 + 0.036 \cdot \text{SL}$	$0.09 + 0.038 \cdot \text{SL}$
G to Q	tPLH	0.63	$0.55 + 0.042 \cdot \text{SL}$	$0.55 + 0.040 \cdot \text{SL}$	$0.56 + 0.040 \cdot \text{SL}$
	tPHL	0.56	$0.51 + 0.028 \cdot \text{SL}$	$0.53 + 0.021 \cdot \text{SL}$	$0.56 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.12 + 0.090 \cdot \text{SL}$	$0.12 + 0.091 \cdot \text{SL}$	$0.09 + 0.093 \cdot \text{SL}$
	tF	0.18	$0.10 + 0.036 \cdot \text{SL}$	$0.10 + 0.037 \cdot \text{SL}$	$0.08 + 0.038 \cdot \text{SL}$
RN to QN	tPLH	0.69	$0.62 + 0.040 \cdot \text{SL}$	$0.62 + 0.039 \cdot \text{SL}$	$0.61 + 0.040 \cdot \text{SL}$
	tPHL	0.41	$0.35 + 0.027 \cdot \text{SL}$	$0.37 + 0.021 \cdot \text{SL}$	$0.39 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.12 + 0.088 \cdot \text{SL}$	$0.12 + 0.091 \cdot \text{SL}$	$0.09 + 0.092 \cdot \text{SL}$
	tF	0.18	$0.10 + 0.037 \cdot \text{SL}$	$0.11 + 0.037 \cdot \text{SL}$	$0.07 + 0.038 \cdot \text{SL}$
SN to QN	tPLH	0.39	$0.31 + 0.042 \cdot \text{SL}$	$0.31 + 0.039 \cdot \text{SL}$	$0.31 + 0.040 \cdot \text{SL}$
	tPHL	0.44	$0.38 + 0.028 \cdot \text{SL}$	$0.40 + 0.022 \cdot \text{SL}$	$0.43 + 0.020 \cdot \text{SL}$
	tR	0.31	$0.13 + 0.087 \cdot \text{SL}$	$0.12 + 0.091 \cdot \text{SL}$	$0.09 + 0.092 \cdot \text{SL}$
	tF	0.20	$0.14 + 0.032 \cdot \text{SL}$	$0.13 + 0.036 \cdot \text{SL}$	$0.09 + 0.038 \cdot \text{SL}$
D to QN	tPLH	0.67	$0.59 + 0.039 \cdot \text{SL}$	$0.59 + 0.039 \cdot \text{SL}$	$0.58 + 0.040 \cdot \text{SL}$
	tPHL	0.48	$0.43 + 0.027 \cdot \text{SL}$	$0.45 + 0.021 \cdot \text{SL}$	$0.47 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.13 + 0.087 \cdot \text{SL}$	$0.11 + 0.091 \cdot \text{SL}$	$0.09 + 0.092 \cdot \text{SL}$
	tF	0.18	$0.11 + 0.035 \cdot \text{SL}$	$0.10 + 0.037 \cdot \text{SL}$	$0.08 + 0.038 \cdot \text{SL}$
G to QN	tPLH	0.79	$0.71 + 0.040 \cdot \text{SL}$	$0.71 + 0.040 \cdot \text{SL}$	$0.71 + 0.040 \cdot \text{SL}$
	tPHL	0.72	$0.67 + 0.027 \cdot \text{SL}$	$0.69 + 0.021 \cdot \text{SL}$	$0.71 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.12 + 0.088 \cdot \text{SL}$	$0.11 + 0.091 \cdot \text{SL}$	$0.09 + 0.092 \cdot \text{SL}$
	tF	0.18	$0.11 + 0.036 \cdot \text{SL}$	$0.10 + 0.037 \cdot \text{SL}$	$0.07 + 0.038 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **LD4 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	tPWL	0.000

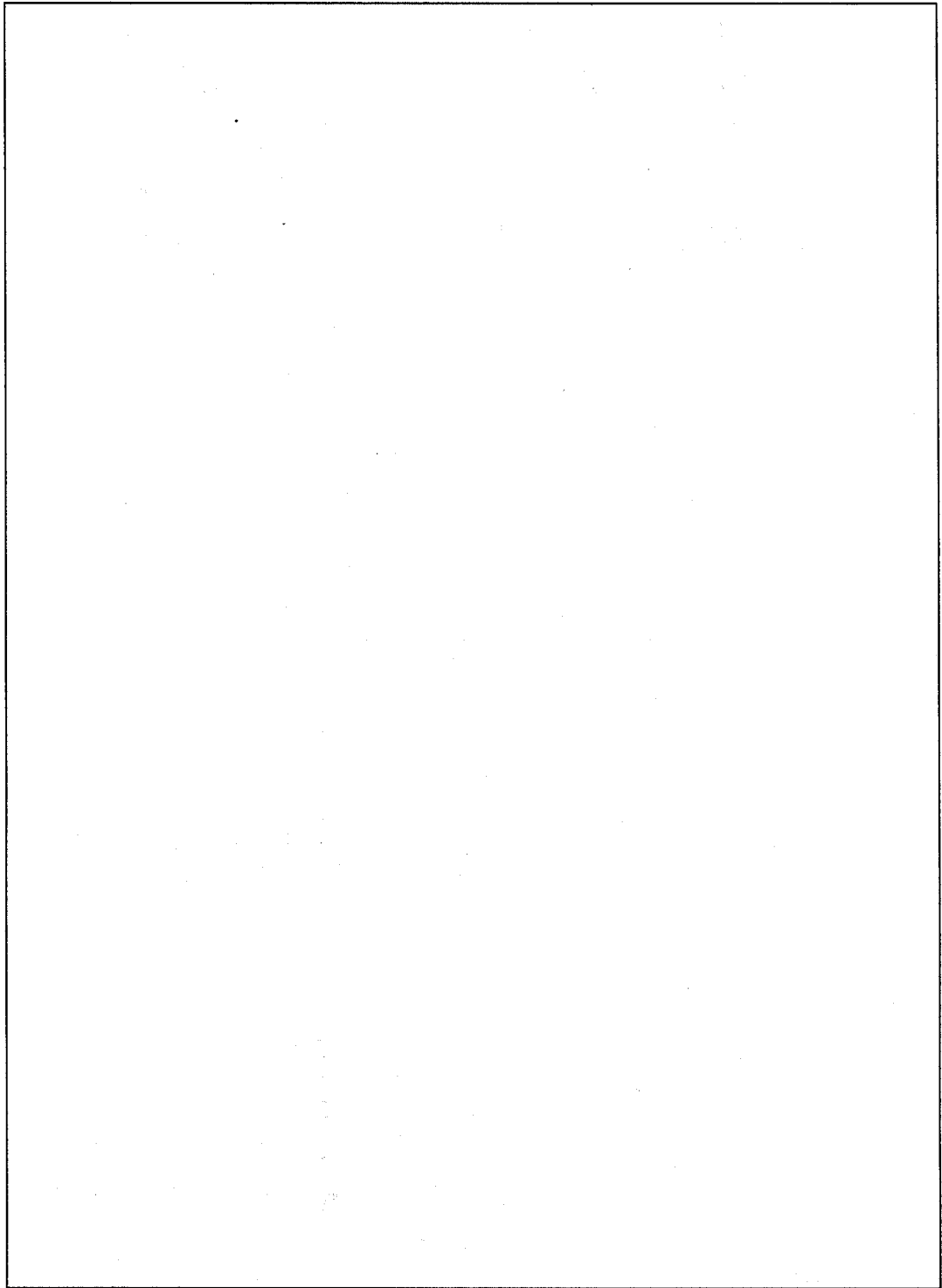
# LD4

## D-Latch Active High Gate with Set, Reset, 1X Drive

### LD4 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (SN)	tPWL	0.000
Pulse Width High (G)	tPWH	0.000
Input Hold Time (D to G)	tHD	0.000
Input Setup Time (D to G)	tSU	0.000
Recovery Time (RN)	tRC	0.000
Recovery Time (SN)	tRC	0.000



# LD4D2Q/LD4D4Q

D-Latch Active High Gate with Set and Reset, Q Output Only, 2X Drive or 4X Drive

Inputs: D, G, RN, SN

Output: Q

Input Loading (SL): All: D: 3, G, RN: 1,  
SN: 2

Maximum Fanout (Rec. SL):

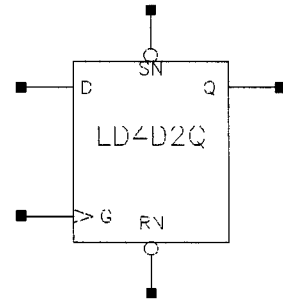
- LD4D2Q: 56

- LD4D4Q: 144

Gate Count:

- LD4D2Q: 6

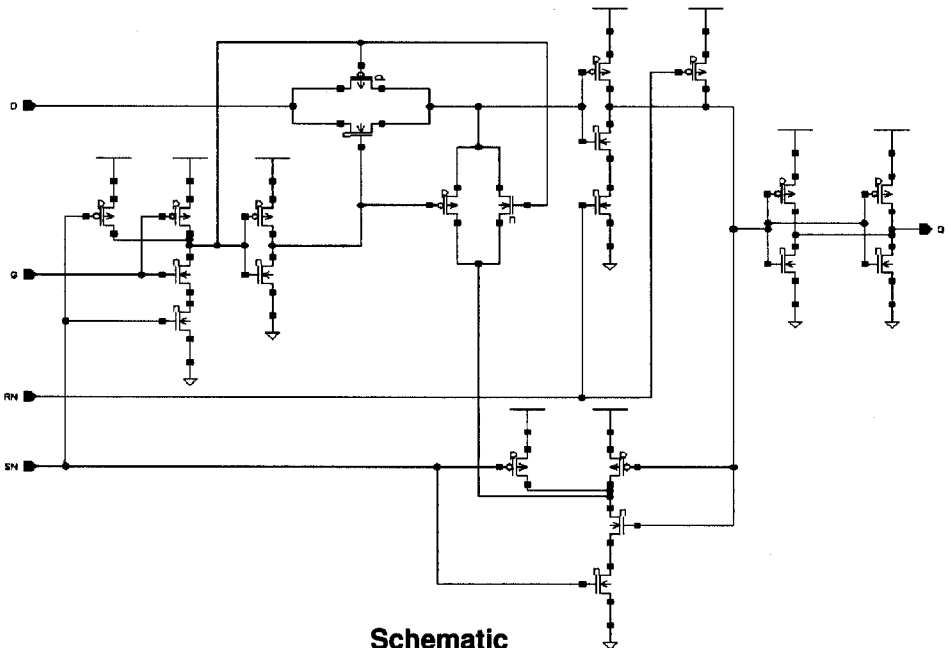
- LD4D4Q: 7



Symbol

D	G	RN	SN	Q <sub>n+1</sub>
0	1	1	1	0
1	1	1	1	1
x	x	0	0	0
x	x	0	1	0
x	x	1	0	1
x	0	1	1	Q <sub>n</sub>

Truth Table



Schematic

**LD4D2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	t <sub>PLH</sub>	0.33	$0.28 + 0.025^*SL$	$0.28 + 0.022^*SL$	$0.29 + 0.021^*SL$
	t <sub>PHL</sub>	0.46	$0.42 + 0.020^*SL$	$0.44 + 0.013^*SL$	$0.49 + 0.011^*SL$
	t <sub>R</sub>	0.26	$0.16 + 0.047^*SL$	$0.15 + 0.050^*SL$	$0.13 + 0.052^*SL$
	t <sub>F</sub>	0.21	$0.18 + 0.017^*SL$	$0.17 + 0.019^*SL$	$0.16 + 0.020^*SL$
SN to Q	t <sub>PLH</sub>	0.93	$0.88 + 0.023^*SL$	$0.89 + 0.022^*SL$	$0.90 + 0.021^*SL$
	t <sub>PHL</sub>	0.54	$0.51 + 0.018^*SL$	$0.52 + 0.013^*SL$	$0.56 + 0.011^*SL$
	t <sub>R</sub>	0.24	$0.15 + 0.048^*SL$	$0.14 + 0.051^*SL$	$0.11 + 0.052^*SL$
	t <sub>F</sub>	0.16	$0.13 + 0.019^*SL$	$0.12 + 0.020^*SL$	$0.12 + 0.020^*SL$
D to Q	t <sub>PLH</sub>	0.41	$0.36 + 0.024^*SL$	$0.37 + 0.022^*SL$	$0.38 + 0.021^*SL$
	t <sub>PHL</sub>	0.45	$0.41 + 0.019^*SL$	$0.43 + 0.013^*SL$	$0.47 + 0.011^*SL$
	t <sub>R</sub>	0.26	$0.16 + 0.049^*SL$	$0.15 + 0.050^*SL$	$0.13 + 0.052^*SL$
	t <sub>F</sub>	0.19	$0.16 + 0.019^*SL$	$0.15 + 0.019^*SL$	$0.14 + 0.020^*SL$
G to Q	t <sub>PLH</sub>	0.64	$0.59 + 0.024^*SL$	$0.59 + 0.022^*SL$	$0.61 + 0.021^*SL$
	t <sub>PHL</sub>	0.57	$0.54 + 0.018^*SL$	$0.55 + 0.013^*SL$	$0.59 + 0.011^*SL$
	t <sub>R</sub>	0.24	$0.14 + 0.048^*SL$	$0.14 + 0.051^*SL$	$0.11 + 0.052^*SL$
	t <sub>F</sub>	0.17	$0.13 + 0.020^*SL$	$0.13 + 0.020^*SL$	$0.12 + 0.020^*SL$

\*Range1 : SL &lt; 3.00, \*Range2 : 3.00 ≤ SL ≤ 20.00, \*Range3 : 20.00 &lt; SL

**LD4D2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	t <sub>PWL</sub>	0.920
Pulse Width Low (SN)	t <sub>PWL</sub>	0.920
Pulse Width High (G)	t <sub>PWH</sub>	0.920
Input Hold Time (D to G)	t <sub>HD</sub>	0.178
Input Setup Time (D to G)	t <sub>SU</sub>	0.178
Recovery Time (RN)	t <sub>RC</sub>	0.139
Recovery Time (SN)	t <sub>RC</sub>	0.412

# LD4D4Q

D-Latch Active High Gate with Set and Reset, Q Output Only, 4X Drive

## LD4D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

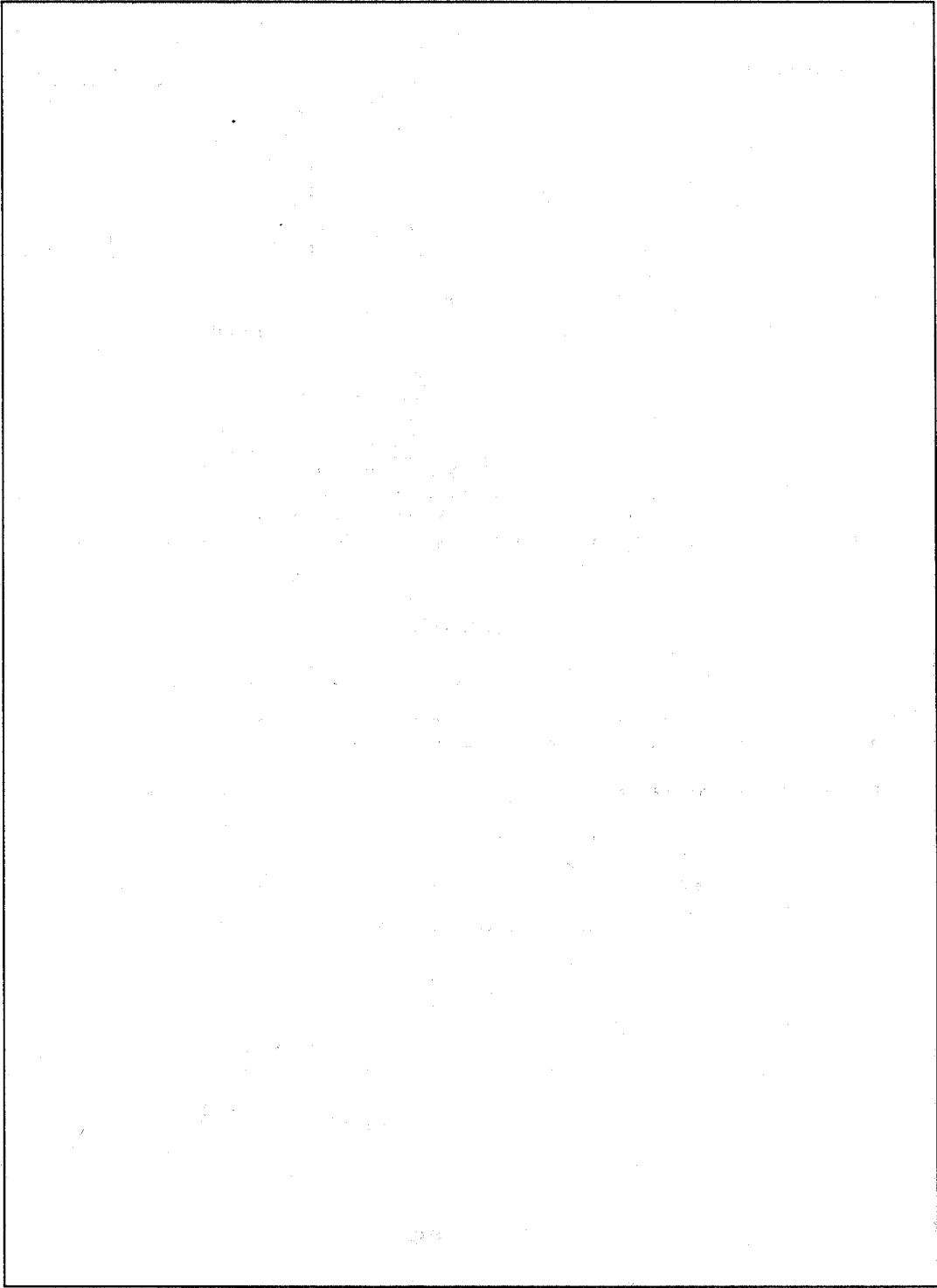
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.38	$0.36 + 0.013*SL$	$0.36 + 0.011*SL$	$0.38 + 0.011*SL$
	tPHL	0.51	$0.49 + 0.012*SL$	$0.50 + 0.008*SL$	$0.54 + 0.006*SL$
	tR	0.24	$0.20 + 0.021*SL$	$0.19 + 0.024*SL$	$0.17 + 0.025*SL$
	tF	0.23	$0.21 + 0.011*SL$	$0.21 + 0.010*SL$	$0.22 + 0.010*SL$
SN to Q	tPLH	0.99	$0.96 + 0.014*SL$	$0.97 + 0.011*SL$	$0.98 + 0.011*SL$
	tPHL	0.60	$0.57 + 0.011*SL$	$0.58 + 0.008*SL$	$0.62 + 0.006*SL$
	tR	0.23	$0.19 + 0.021*SL$	$0.18 + 0.024*SL$	$0.16 + 0.025*SL$
	tF	0.19	$0.18 + 0.009*SL$	$0.17 + 0.010*SL$	$0.17 + 0.010*SL$
D to Q	tPLH	0.49	$0.46 + 0.013*SL$	$0.46 + 0.011*SL$	$0.48 + 0.011*SL$
	tPHL	0.51	$0.48 + 0.011*SL$	$0.49 + 0.008*SL$	$0.53 + 0.006*SL$
	tR	0.24	$0.20 + 0.022*SL$	$0.19 + 0.024*SL$	$0.17 + 0.025*SL$
	tF	0.22	$0.20 + 0.011*SL$	$0.20 + 0.009*SL$	$0.19 + 0.010*SL$
G to Q	tPLH	0.69	$0.67 + 0.013*SL$	$0.67 + 0.012*SL$	$0.69 + 0.011*SL$
	tPHL	0.63	$0.60 + 0.011*SL$	$0.61 + 0.008*SL$	$0.65 + 0.006*SL$
	tR	0.23	$0.18 + 0.021*SL$	$0.17 + 0.025*SL$	$0.16 + 0.025*SL$
	tF	0.19	$0.18 + 0.009*SL$	$0.17 + 0.010*SL$	$0.17 + 0.010*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## LD4D4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (G)	tPWH	0.920
Input Hold Time (D to G)	tHD	0.123
Input Setup Time (D to G)	tSU	0.233
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.412





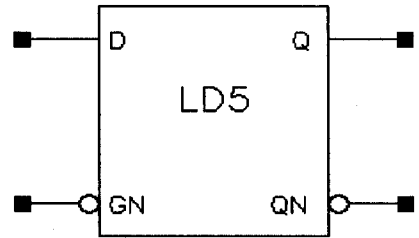
# LD5/LD5D2

D-Latch with Active Low Gate, 1X Drive or 2x Drive

Inputs: D, GN  
Outputs: Q, QN  
Input Loading (SL):  
- D: 3  
- GN: 1

Maximum Fanout (Rec. SL):  
LD5: All: 28  
LD5D2: All: 56

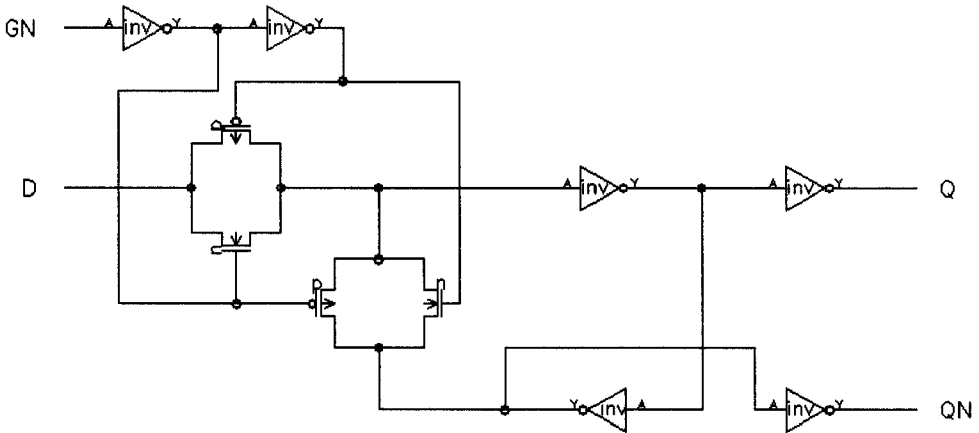
Gate Count:  
LD5: 4  
LD5D2: 5



Symbol

D	GN	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	0	0	1
1	0	1	0
X	1	Q <sub>n</sub>	Q <sub>Nn</sub>

Truth Table



Schematic

**LD5 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.28	$0.20 + 0.040 * SL$	$0.20 + 0.040 * SL$	$0.20 + 0.040 * SL$
	tPHL	0.44	$0.39 + 0.028 * SL$	$0.41 + 0.021 * SL$	$0.44 + 0.020 * SL$
	tR	0.29	$0.12 + 0.089 * SL$	$0.11 + 0.092 * SL$	$0.09 + 0.093 * SL$
	tF	0.19	$0.12 + 0.036 * SL$	$0.12 + 0.036 * SL$	$0.08 + 0.038 * SL$
GN to Q	tPLH	0.65	$0.57 + 0.041 * SL$	$0.57 + 0.040 * SL$	$0.57 + 0.040 * SL$
	tPHL	0.63	$0.58 + 0.027 * SL$	$0.59 + 0.021 * SL$	$0.62 + 0.020 * SL$
	tR	0.28	$0.10 + 0.089 * SL$	$0.09 + 0.092 * SL$	$0.08 + 0.093 * SL$
	tF	0.17	$0.09 + 0.038 * SL$	$0.10 + 0.037 * SL$	$0.07 + 0.038 * SL$
D to QN	tPLH	0.59	$0.51 + 0.040 * SL$	$0.51 + 0.040 * SL$	$0.50 + 0.040 * SL$
	tPHL	0.35	$0.30 + 0.026 * SL$	$0.31 + 0.021 * SL$	$0.33 + 0.020 * SL$
	tR	0.28	$0.10 + 0.089 * SL$	$0.09 + 0.092 * SL$	$0.08 + 0.092 * SL$
	tF	0.17	$0.09 + 0.037 * SL$	$0.09 + 0.037 * SL$	$0.06 + 0.038 * SL$
GN to QN	tPLH	0.77	$0.69 + 0.039 * SL$	$0.69 + 0.040 * SL$	$0.69 + 0.040 * SL$
	tPHL	0.73	$0.67 + 0.026 * SL$	$0.69 + 0.021 * SL$	$0.71 + 0.020 * SL$
	tR	0.28	$0.10 + 0.089 * SL$	$0.09 + 0.092 * SL$	$0.08 + 0.092 * SL$
	tF	0.16	$0.09 + 0.036 * SL$	$0.09 + 0.037 * SL$	$0.06 + 0.038 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD5 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.920
Input Hold Time (D to GN)	tHD	0.000
Input Setup Time (D to GN)	tSU	0.342

# LD5D2

## D-Latch with Active Low Gate and 2X Drive

### LD5D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

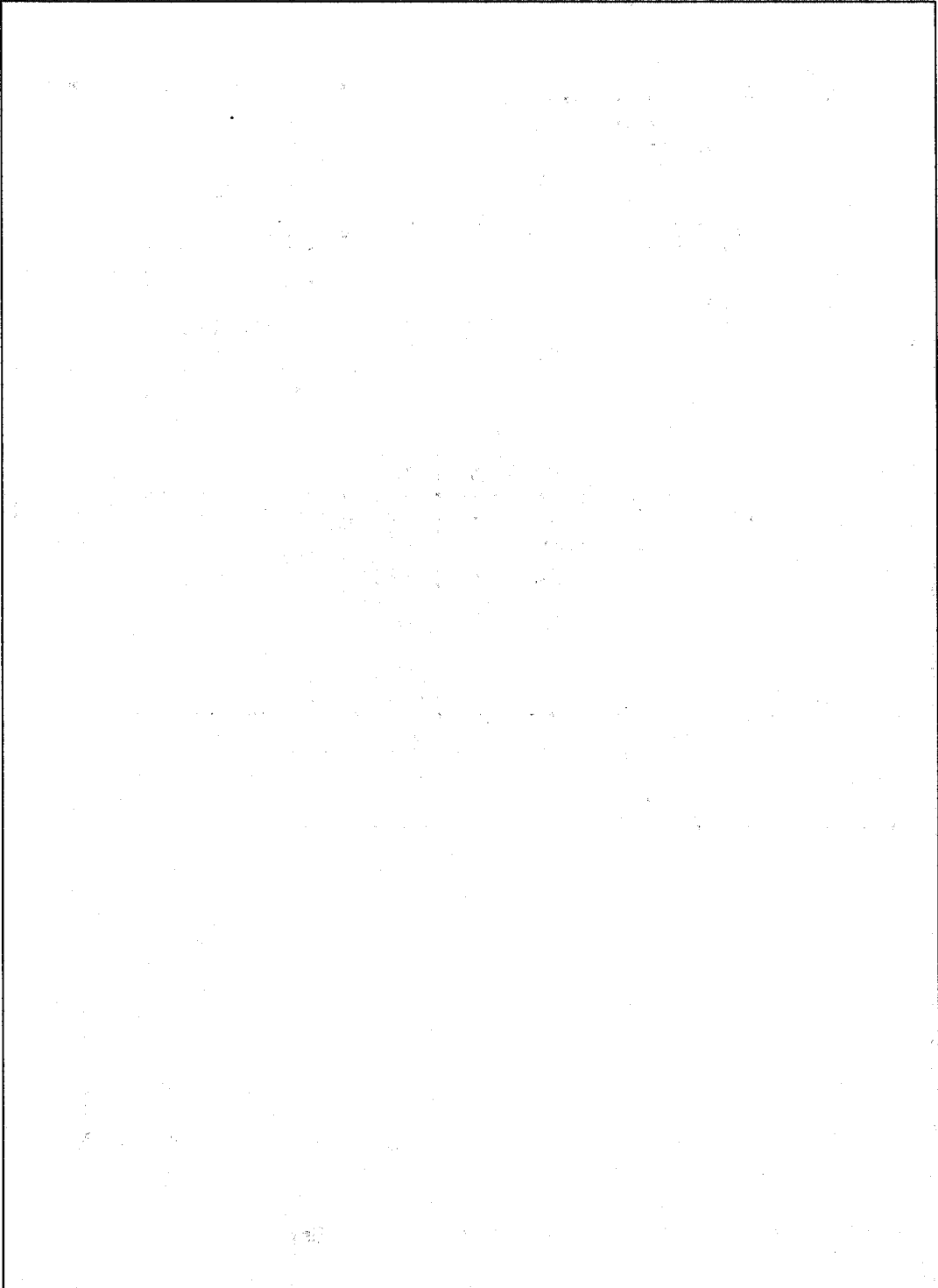
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.28	$0.24 + 0.021*SL$	$0.24 + 0.020*SL$	$0.24 + 0.020*SL$
	tPHL	0.46	$0.42 + 0.017*SL$	$0.44 + 0.012*SL$	$0.47 + 0.010*SL$
	tR	0.21	$0.13 + 0.044*SL$	$0.12 + 0.045*SL$	$0.10 + 0.047*SL$
	tF	0.18	$0.14 + 0.017*SL$	$0.14 + 0.018*SL$	$0.12 + 0.019*SL$
GN to Q	tPLH	0.64	$0.60 + 0.021*SL$	$0.60 + 0.020*SL$	$0.60 + 0.020*SL$
	tPHL	0.64	$0.60 + 0.017*SL$	$0.62 + 0.012*SL$	$0.65 + 0.010*SL$
	tR	0.19	$0.11 + 0.044*SL$	$0.10 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.15	$0.11 + 0.019*SL$	$0.12 + 0.018*SL$	$0.11 + 0.019*SL$
D to QN	tPLH	0.63	$0.59 + 0.018*SL$	$0.59 + 0.020*SL$	$0.58 + 0.020*SL$
	tPHL	0.41	$0.38 + 0.015*SL$	$0.39 + 0.012*SL$	$0.42 + 0.010*SL$
	tR	0.20	$0.11 + 0.044*SL$	$0.10 + 0.047*SL$	$0.08 + 0.048*SL$
	tF	0.15	$0.11 + 0.021*SL$	$0.12 + 0.018*SL$	$0.10 + 0.019*SL$
GN to QN	tPLH	0.81	$0.77 + 0.018*SL$	$0.77 + 0.020*SL$	$0.76 + 0.020*SL$
	tPHL	0.77	$0.74 + 0.016*SL$	$0.75 + 0.012*SL$	$0.78 + 0.010*SL$
	tR	0.20	$0.11 + 0.044*SL$	$0.10 + 0.047*SL$	$0.08 + 0.048*SL$
	tF	0.15	$0.11 + 0.019*SL$	$0.12 + 0.018*SL$	$0.10 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### LD5D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.920
Input Hold Time (D to GN)	tHD	0.000
Input Setup Time (D to GN)	tSU	0.397



# LD5D2Q/LD5D4Q

D-Latch with Active Low Gate, Q Output Only, 2X Drive or 4X Drive

Inputs: D, GN

Outputs: Q

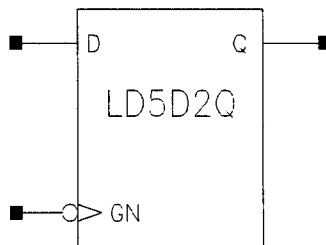
Input Loading (SL): All : D: 3, GN: 1

Maximum Fanout (Rec. SL):

- LD5D2Q: 56
- LD5D4Q: 112

Gate Count:

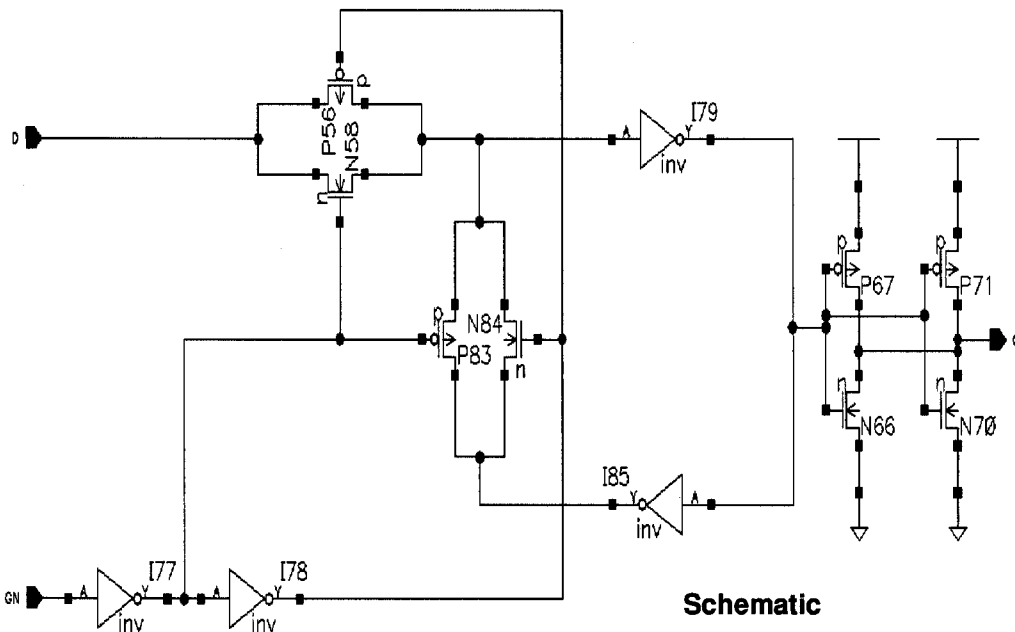
- LD5D2Q: 4
- LD5D4Q: 5



**Symbol**

D	GN	Q <sub>n+1</sub>
0	0	0
1	0	1
X	1	Q <sub>n</sub>

**Truth Table**



**Schematic**

**LD5D2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.29	$0.24 + 0.022^*SL$	$0.24 + 0.021^*SL$	$0.24 + 0.021^*SL$
	tPHL	0.46	$0.42 + 0.018^*SL$	$0.44 + 0.013^*SL$	$0.48 + 0.011^*SL$
	tR	0.23	$0.13 + 0.048^*SL$	$0.12 + 0.051^*SL$	$0.10 + 0.052^*SL$
	tF	0.19	$0.15 + 0.019^*SL$	$0.15 + 0.019^*SL$	$0.13 + 0.020^*SL$
GN to Q	tPLH	0.65	$0.60 + 0.023^*SL$	$0.60 + 0.022^*SL$	$0.61 + 0.022^*SL$
	tPHL	0.64	$0.61 + 0.018^*SL$	$0.62 + 0.012^*SL$	$0.66 + 0.011^*SL$
	tR	0.21	$0.11 + 0.050^*SL$	$0.11 + 0.052^*SL$	$0.09 + 0.052^*SL$
	tF	0.16	$0.12 + 0.020^*SL$	$0.12 + 0.020^*SL$	$0.11 + 0.020^*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD5D2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.920
Input Hold Time (D to GN)	tHD	0.000
Input Setup Time (D to GN)	tSU	0.342

**LD5D4Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D to Q	tPLH	0.34	$0.32 + 0.012^*SL$	$0.32 + 0.011^*SL$	$0.33 + 0.011^*SL$
	tPHL	0.52	$0.50 + 0.011^*SL$	$0.50 + 0.008^*SL$	$0.54 + 0.006^*SL$
	tR	0.20	$0.15 + 0.023^*SL$	$0.15 + 0.025^*SL$	$0.13 + 0.026^*SL$
	tF	0.21	$0.20 + 0.007^*SL$	$0.19 + 0.009^*SL$	$0.19 + 0.010^*SL$
GN to Q	tPLH	0.68	$0.65 + 0.012^*SL$	$0.66 + 0.011^*SL$	$0.66 + 0.011^*SL$
	tPHL	0.70	$0.67 + 0.011^*SL$	$0.68 + 0.008^*SL$	$0.72 + 0.006^*SL$
	tR	0.18	$0.13 + 0.024^*SL$	$0.13 + 0.025^*SL$	$0.11 + 0.026^*SL$
	tF	0.19	$0.18 + 0.007^*SL$	$0.17 + 0.010^*SL$	$0.17 + 0.010^*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD5D4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.920
Input Hold Time (D to GN)	tHD	0.000
Input Setup Time (D to GN)	tSU	0.397

# LD5X4

## 4-Bit D-Latch with Active Low Gate

Inputs: D0, D1, D2, D3, GN

Outputs: Q0, Q1, Q2, Q3

QN0, QN1, QN2, QN3

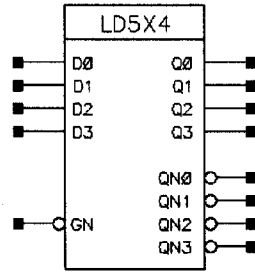
Input Loading (SL):

- D0, D1, D2, D3: 3

- GN: 1

Maximum Fanout (Rec. SL): All : 28

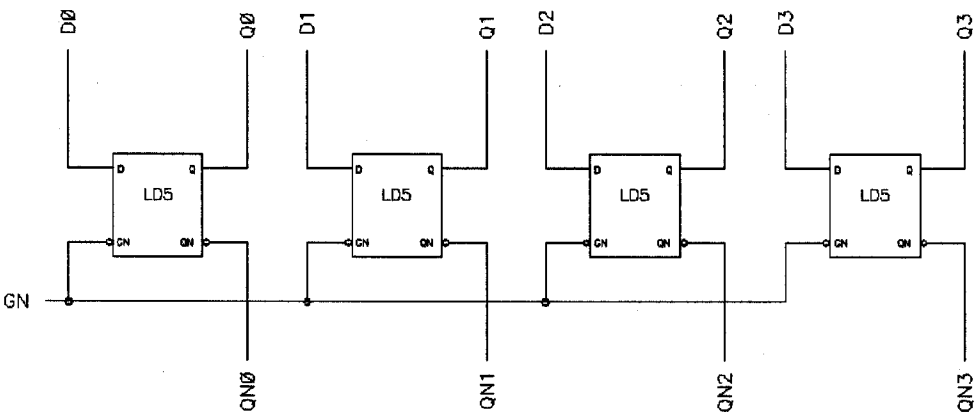
Gate Count: 13



Symbol

D	GN	Qn+1	QNn+1
0	0	0	1
1	0	1	0
x	1	Qn	QNn

Truth Table



Schematic

## LD5X4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D0 to Q0	tPLH	0.28	$0.20 + 0.043^*SL$	$0.20 + 0.043^*SL$	$0.20 + 0.043^*SL$
	tPHL	0.45	$0.39 + 0.029^*SL$	$0.41 + 0.022^*SL$	$0.44 + 0.020^*SL$
	tR	0.32	$0.12 + 0.099^*SL$	$0.11 + 0.101^*SL$	$0.09 + 0.102^*SL$
	tF	0.20	$0.12 + 0.038^*SL$	$0.12 + 0.039^*SL$	$0.08 + 0.041^*SL$
GN to Q0	tPLH	0.84	$0.76 + 0.044^*SL$	$0.76 + 0.043^*SL$	$0.76 + 0.043^*SL$
	tPHL	0.74	$0.68 + 0.028^*SL$	$0.70 + 0.022^*SL$	$0.73 + 0.020^*SL$
	tR	0.30	$0.10 + 0.101^*SL$	$0.10 + 0.102^*SL$	$0.09 + 0.102^*SL$
	tF	0.18	$0.10 + 0.041^*SL$	$0.10 + 0.040^*SL$	$0.07 + 0.041^*SL$
D1 to Q1	tPLH	0.27	$0.19 + 0.041^*SL$	$0.19 + 0.040^*SL$	$0.19 + 0.040^*SL$
	tPHL	0.44	$0.39 + 0.028^*SL$	$0.40 + 0.021^*SL$	$0.43 + 0.020^*SL$
	tR	0.29	$0.12 + 0.089^*SL$	$0.11 + 0.092^*SL$	$0.09 + 0.093^*SL$
	tF	0.19	$0.12 + 0.037^*SL$	$0.12 + 0.036^*SL$	$0.08 + 0.038^*SL$
GN to Q1	tPLH	0.84	$0.75 + 0.041^*SL$	$0.76 + 0.040^*SL$	$0.76 + 0.040^*SL$
	tPHL	0.73	$0.68 + 0.027^*SL$	$0.69 + 0.021^*SL$	$0.72 + 0.020^*SL$
	tR	0.28	$0.10 + 0.090^*SL$	$0.09 + 0.092^*SL$	$0.08 + 0.093^*SL$
	tF	0.17	$0.09 + 0.037^*SL$	$0.09 + 0.037^*SL$	$0.07 + 0.038^*SL$
D2 to Q2	tPLH	0.29	$0.20 + 0.043^*SL$	$0.20 + 0.043^*SL$	$0.20 + 0.043^*SL$
	tPHL	0.45	$0.39 + 0.029^*SL$	$0.41 + 0.022^*SL$	$0.44 + 0.020^*SL$
	tR	0.32	$0.12 + 0.099^*SL$	$0.11 + 0.101^*SL$	$0.09 + 0.102^*SL$
	tF	0.20	$0.12 + 0.038^*SL$	$0.12 + 0.039^*SL$	$0.08 + 0.041^*SL$
GN to Q2	tPLH	0.85	$0.76 + 0.043^*SL$	$0.76 + 0.043^*SL$	$0.76 + 0.043^*SL$
	tPHL	0.74	$0.68 + 0.028^*SL$	$0.70 + 0.022^*SL$	$0.73 + 0.020^*SL$
	tR	0.30	$0.10 + 0.100^*SL$	$0.10 + 0.102^*SL$	$0.09 + 0.102^*SL$
	tF	0.18	$0.10 + 0.041^*SL$	$0.10 + 0.040^*SL$	$0.07 + 0.041^*SL$
D3 to Q3	tPLH	0.27	$0.19 + 0.041^*SL$	$0.19 + 0.040^*SL$	$0.19 + 0.040^*SL$
	tPHL	0.44	$0.38 + 0.028^*SL$	$0.40 + 0.021^*SL$	$0.43 + 0.020^*SL$
	tR	0.29	$0.12 + 0.089^*SL$	$0.11 + 0.092^*SL$	$0.09 + 0.093^*SL$
	tF	0.19	$0.12 + 0.036^*SL$	$0.12 + 0.036^*SL$	$0.08 + 0.038^*SL$
GN to Q3	tPLH	0.84	$0.75 + 0.041^*SL$	$0.76 + 0.040^*SL$	$0.76 + 0.040^*SL$
	tPHL	0.73	$0.68 + 0.027^*SL$	$0.69 + 0.021^*SL$	$0.72 + 0.020^*SL$
	tR	0.28	$0.10 + 0.090^*SL$	$0.09 + 0.092^*SL$	$0.08 + 0.093^*SL$
	tF	0.17	$0.09 + 0.037^*SL$	$0.09 + 0.037^*SL$	$0.07 + 0.038^*SL$
D0 to QN0	tPLH	0.59	$0.51 + 0.040^*SL$	$0.51 + 0.041^*SL$	$0.50 + 0.041^*SL$
	tPHL	0.35	$0.30 + 0.026^*SL$	$0.31 + 0.021^*SL$	$0.33 + 0.020^*SL$
	tR	0.29	$0.10 + 0.090^*SL$	$0.09 + 0.095^*SL$	$0.08 + 0.095^*SL$
	tF	0.17	$0.09 + 0.038^*SL$	$0.09 + 0.038^*SL$	$0.06 + 0.040^*SL$
GN to QN0	tPLH	0.88	$0.80 + 0.040^*SL$	$0.80 + 0.041^*SL$	$0.79 + 0.041^*SL$
	tPHL	0.91	$0.86 + 0.026^*SL$	$0.87 + 0.021^*SL$	$0.89 + 0.020^*SL$
	tR	0.28	$0.10 + 0.091^*SL$	$0.09 + 0.095^*SL$	$0.08 + 0.095^*SL$
	tF	0.17	$0.10 + 0.037^*SL$	$0.09 + 0.038^*SL$	$0.06 + 0.040^*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# LD5X4

## 4-Bit D-Latch with Active Low Gate

### LD5X4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
D1 to QN1	tPLH	0.58	$0.51 + 0.039*SL$	$0.50 + 0.040*SL$	$0.50 + 0.040*SL$
	tPHL	0.35	$0.30 + 0.026*SL$	$0.31 + 0.021*SL$	$0.33 + 0.020*SL$
	tR	0.28	$0.10 + 0.087*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.09 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
GN to QN1	tPLH	0.87	$0.79 + 0.039*SL$	$0.79 + 0.040*SL$	$0.79 + 0.040*SL$
	tPHL	0.91	$0.86 + 0.026*SL$	$0.87 + 0.021*SL$	$0.89 + 0.020*SL$
	tR	0.28	$0.10 + 0.089*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.09 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
D2 to QN2	tPLH	0.59	$0.51 + 0.040*SL$	$0.51 + 0.041*SL$	$0.50 + 0.041*SL$
	tPHL	0.35	$0.30 + 0.026*SL$	$0.32 + 0.021*SL$	$0.33 + 0.020*SL$
	tR	0.29	$0.10 + 0.091*SL$	$0.09 + 0.095*SL$	$0.08 + 0.095*SL$
	tF	0.17	$0.09 + 0.038*SL$	$0.09 + 0.038*SL$	$0.06 + 0.040*SL$
GN to QN2	tPLH	0.88	$0.80 + 0.040*SL$	$0.80 + 0.041*SL$	$0.79 + 0.041*SL$
	tPHL	0.91	$0.86 + 0.026*SL$	$0.87 + 0.021*SL$	$0.89 + 0.020*SL$
	tR	0.28	$0.10 + 0.091*SL$	$0.09 + 0.095*SL$	$0.08 + 0.095*SL$
	tF	0.17	$0.10 + 0.036*SL$	$0.09 + 0.038*SL$	$0.06 + 0.040*SL$
D3 to QN3	tPLH	0.58	$0.51 + 0.039*SL$	$0.50 + 0.040*SL$	$0.50 + 0.040*SL$
	tPHL	0.35	$0.30 + 0.026*SL$	$0.31 + 0.021*SL$	$0.33 + 0.020*SL$
	tR	0.28	$0.10 + 0.087*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.09 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
GN to QN3	tPLH	0.87	$0.79 + 0.039*SL$	$0.79 + 0.040*SL$	$0.79 + 0.040*SL$
	tPHL	0.91	$0.86 + 0.026*SL$	$0.87 + 0.021*SL$	$0.89 + 0.020*SL$
	tR	0.28	$0.10 + 0.089*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.09 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### LD5X4 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.920
Input Hold Time (D0 to GN)	tHD	0.233
Input Hold Time (D1 to GN)	tHD	0.233
Input Hold Time (D2 to GN)	tHD	0.014
Input Hold Time (D3 to GN)	tHD	0.014
Input Setup Time (D0 to GN)	tSU	0.287
Input Setup Time (D1 to GN)	tSU	0.287

**LD5X4 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Input Setup Time (D2 to GN)	tSU	0.287
Input Setup Time (D3 to GN)	tSU	0.287

# LD6/LD6D2

D-Latch Active Low Gate with Reset, 1X Drive or 2X Drive

Inputs: D, GN, RN

Outputs: Q, QN

Input Loading (SL):

- D: 3

- GN, RN: 1

Maximum Fanout (Rec. SL):

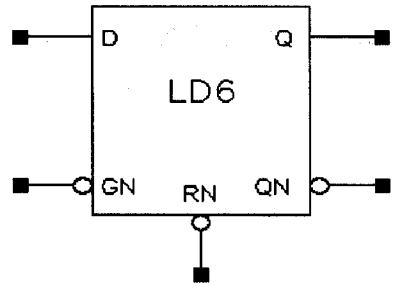
LD6: All: 28

LD6D2: All: 56

Gate Count:

LD6: 5

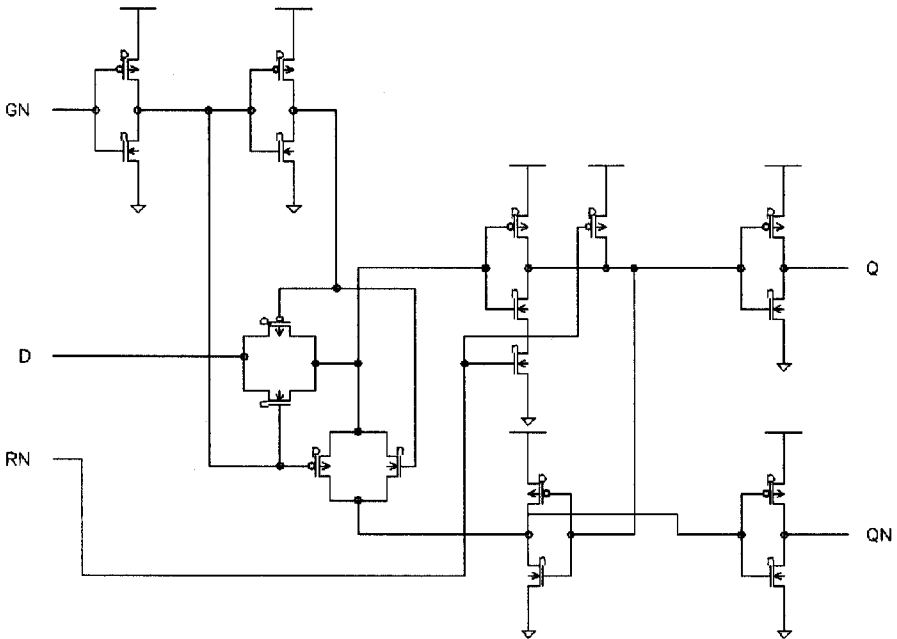
LD6D2: 6



Symbol

D	GN	RN	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	0	1	0	1
1	0	1	1	0
x	1	1	Q <sub>n</sub>	Q <sub>Nn</sub>
x	x	0	0	1

Truth Table



Schematic

**LD6 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.32	$0.23 + 0.043*SL$	$0.24 + 0.040*SL$	$0.24 + 0.040*SL$
	tPHL	0.46	$0.40 + 0.031*SL$	$0.42 + 0.022*SL$	$0.47 + 0.020*SL$
	tR	0.32	$0.14 + 0.086*SL$	$0.13 + 0.091*SL$	$0.10 + 0.092*SL$
	tF	0.22	$0.15 + 0.035*SL$	$0.15 + 0.035*SL$	$0.11 + 0.038*SL$
D to Q	tPLH	0.40	$0.31 + 0.043*SL$	$0.32 + 0.040*SL$	$0.32 + 0.040*SL$
	tPHL	0.44	$0.38 + 0.029*SL$	$0.40 + 0.021*SL$	$0.44 + 0.020*SL$
	tR	0.31	$0.14 + 0.087*SL$	$0.13 + 0.091*SL$	$0.10 + 0.092*SL$
	tF	0.20	$0.13 + 0.035*SL$	$0.13 + 0.036*SL$	$0.09 + 0.038*SL$
GN to Q	tPLH	0.73	$0.64 + 0.043*SL$	$0.65 + 0.040*SL$	$0.66 + 0.040*SL$
	tPHL	0.65	$0.59 + 0.028*SL$	$0.61 + 0.021*SL$	$0.64 + 0.020*SL$
	tR	0.30	$0.12 + 0.089*SL$	$0.12 + 0.091*SL$	$0.09 + 0.093*SL$
	tF	0.18	$0.10 + 0.037*SL$	$0.10 + 0.037*SL$	$0.08 + 0.038*SL$
RN to QN	tPLH	0.61	$0.53 + 0.039*SL$	$0.53 + 0.040*SL$	$0.53 + 0.040*SL$
	tPHL	0.40	$0.34 + 0.027*SL$	$0.36 + 0.021*SL$	$0.38 + 0.020*SL$
	tR	0.28	$0.11 + 0.088*SL$	$0.10 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.10 + 0.034*SL$	$0.10 + 0.037*SL$	$0.07 + 0.038*SL$
D to QN	tPLH	0.59	$0.51 + 0.039*SL$	$0.51 + 0.040*SL$	$0.50 + 0.040*SL$
	tPHL	0.48	$0.42 + 0.026*SL$	$0.44 + 0.021*SL$	$0.46 + 0.020*SL$
	tR	0.28	$0.10 + 0.089*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.10 + 0.035*SL$	$0.10 + 0.037*SL$	$0.07 + 0.038*SL$
GN to QN	tPLH	0.79	$0.72 + 0.039*SL$	$0.71 + 0.040*SL$	$0.71 + 0.040*SL$
	tPHL	0.81	$0.76 + 0.026*SL$	$0.77 + 0.021*SL$	$0.79 + 0.020*SL$
	tR	0.28	$0.10 + 0.088*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.10 + 0.034*SL$	$0.09 + 0.037*SL$	$0.07 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD6 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Input Hold Time (D to GN)	tHD	0.014
Input Setup Time (D to GN)	tSU	0.342
Recovery Time (RN)	tRC	0.139

# LD6D2

## D-Latch Active Low Gate with Reset, 2X Drive

### LD6D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{RQ}$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

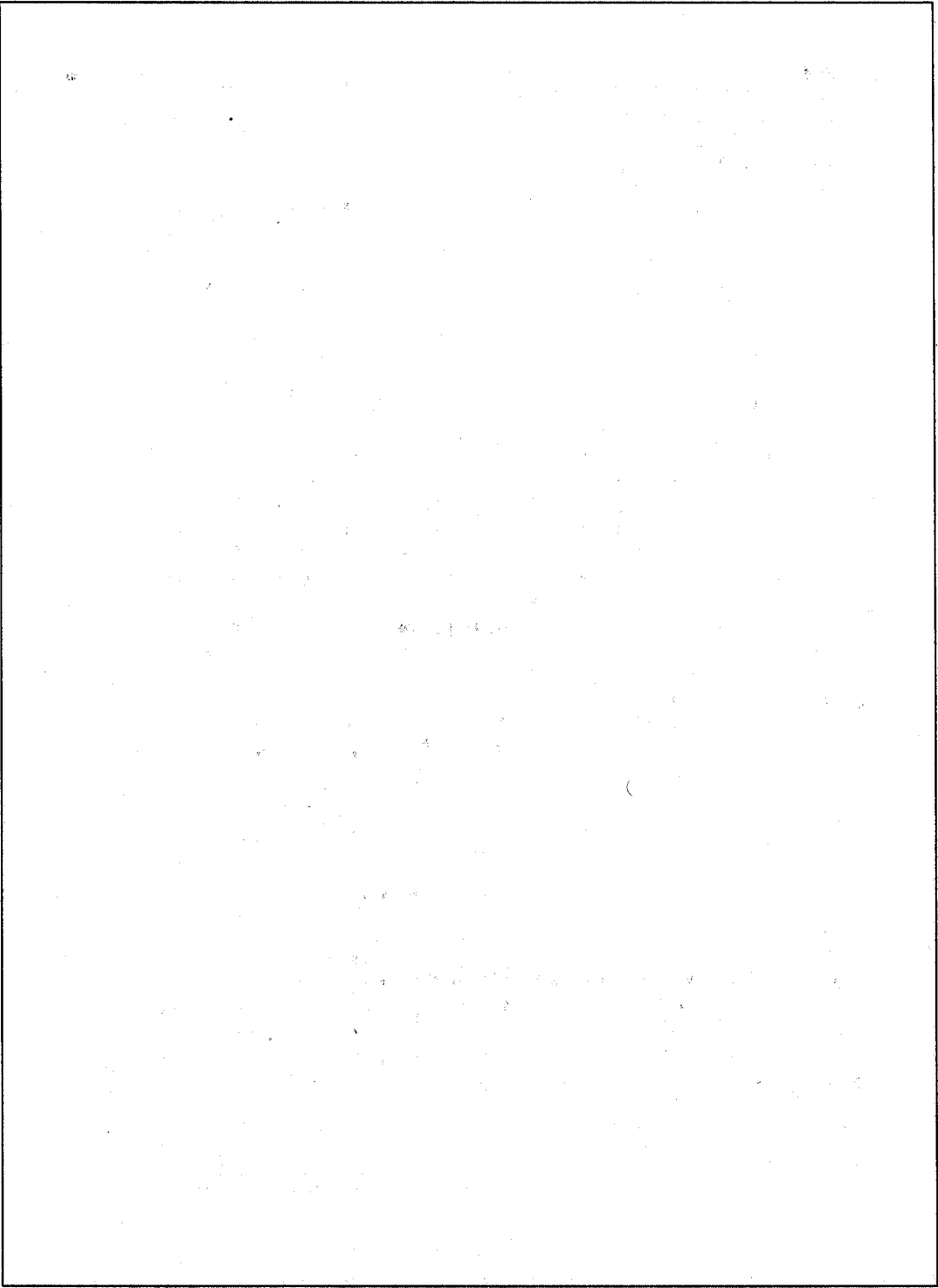
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.32	$0.27 + 0.023*SL$	$0.28 + 0.020*SL$	$0.29 + 0.020*SL$
	tPHL	0.46	$0.42 + 0.019*SL$	$0.44 + 0.013*SL$	$0.49 + 0.010*SL$
	tR	0.24	$0.15 + 0.044*SL$	$0.15 + 0.045*SL$	$0.12 + 0.046*SL$
	tF	0.21	$0.17 + 0.019*SL$	$0.17 + 0.017*SL$	$0.16 + 0.018*SL$
D to Q	tPLH	0.41	$0.36 + 0.023*SL$	$0.37 + 0.020*SL$	$0.38 + 0.020*SL$
	tPHL	0.45	$0.41 + 0.018*SL$	$0.43 + 0.012*SL$	$0.47 + 0.010*SL$
	tR	0.24	$0.15 + 0.043*SL$	$0.14 + 0.045*SL$	$0.12 + 0.046*SL$
	tF	0.19	$0.16 + 0.017*SL$	$0.15 + 0.018*SL$	$0.14 + 0.018*SL$
GN to Q	tPLH	0.73	$0.68 + 0.023*SL$	$0.69 + 0.021*SL$	$0.70 + 0.020*SL$
	tPHL	0.65	$0.62 + 0.018*SL$	$0.64 + 0.012*SL$	$0.67 + 0.010*SL$
	tR	0.23	$0.14 + 0.044*SL$	$0.13 + 0.045*SL$	$0.11 + 0.047*SL$
	tF	0.16	$0.12 + 0.020*SL$	$0.12 + 0.018*SL$	$0.12 + 0.019*SL$
RN to QN	tPLH	0.65	$0.62 + 0.018*SL$	$0.61 + 0.020*SL$	$0.60 + 0.020*SL$
	tPHL	0.46	$0.43 + 0.015*SL$	$0.44 + 0.012*SL$	$0.47 + 0.010*SL$
	tR	0.20	$0.11 + 0.044*SL$	$0.11 + 0.047*SL$	$0.08 + 0.048*SL$
	tF	0.16	$0.12 + 0.019*SL$	$0.13 + 0.018*SL$	$0.11 + 0.019*SL$
D to QN	tPLH	0.64	$0.60 + 0.019*SL$	$0.60 + 0.020*SL$	$0.58 + 0.020*SL$
	tPHL	0.55	$0.52 + 0.015*SL$	$0.53 + 0.012*SL$	$0.56 + 0.010*SL$
	tR	0.20	$0.11 + 0.044*SL$	$0.10 + 0.047*SL$	$0.08 + 0.048*SL$
	tF	0.16	$0.13 + 0.016*SL$	$0.13 + 0.018*SL$	$0.11 + 0.019*SL$
GN to QN	tPLH	0.84	$0.80 + 0.018*SL$	$0.79 + 0.020*SL$	$0.79 + 0.020*SL$
	tPHL	0.87	$0.84 + 0.015*SL$	$0.85 + 0.012*SL$	$0.88 + 0.010*SL$
	tR	0.20	$0.11 + 0.045*SL$	$0.10 + 0.047*SL$	$0.08 + 0.048*SL$
	tF	0.16	$0.12 + 0.021*SL$	$0.13 + 0.017*SL$	$0.11 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### LD6D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Input Hold Time (D to GN)	tHD	0.014
Input Setup Time (D to GN)	tSU	0.397
Recovery Time (RN)	tRC	0.139



# LD6Q/LD6D3Q

D-Latch Active Low Gate with Reset, Q Output Only, 1X Drive or 3X Drive

Inputs: D, GN, RN

Outputs: Q,

Input Loading (SL): All : D: 3, GN, RN: 1

Maximum Fanout (Rec. SL):

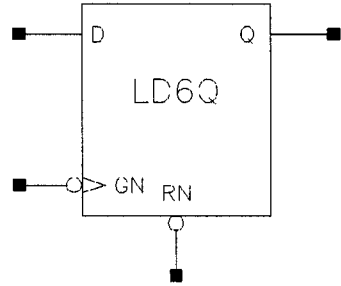
LD6Q: 28

LD6D3Q: 84

Gate Count:

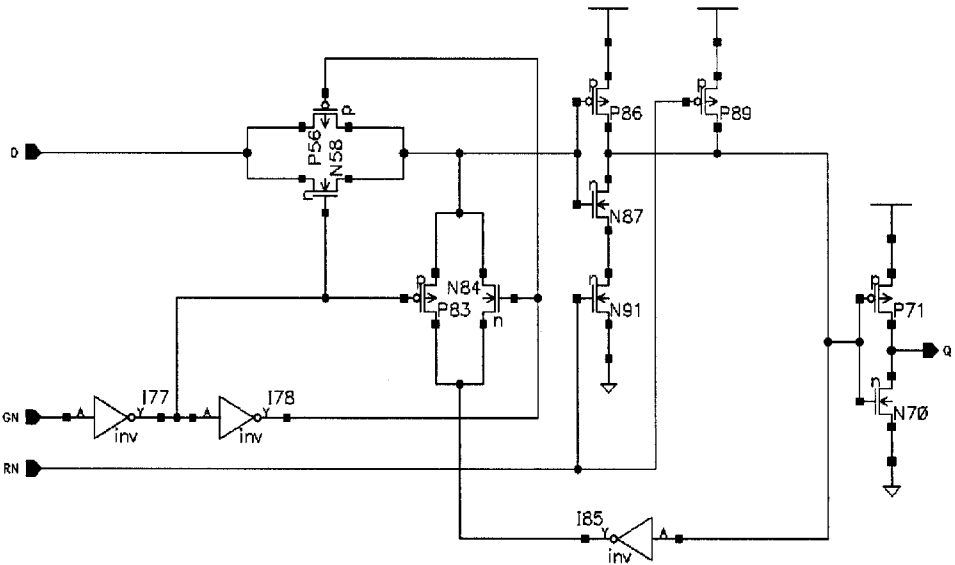
LD6Q: 4

LD6D3Q: 5



D	GN	RN	Q <sub>n+1</sub>
0	0	1	0
1	0	1	1
x	1	1	Q <sub>n</sub>
x	x	0	0

Truth Table



Schematic

**LD6Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.33	$0.24 + 0.046*SL$	$0.25 + 0.043*SL$	$0.25 + 0.043*SL$
	tPHL	0.46	$0.40 + 0.033*SL$	$0.43 + 0.022*SL$	$0.47 + 0.020*SL$
	tR	0.34	$0.15 + 0.094*SL$	$0.14 + 0.100*SL$	$0.10 + 0.102*SL$
	tF	0.23	$0.16 + 0.036*SL$	$0.16 + 0.038*SL$	$0.10 + 0.040*SL$
D to Q	tPLH	0.41	$0.32 + 0.046*SL$	$0.33 + 0.043*SL$	$0.33 + 0.043*SL$
	tPHL	0.44	$0.38 + 0.030*SL$	$0.41 + 0.022*SL$	$0.44 + 0.020*SL$
	tR	0.34	$0.15 + 0.095*SL$	$0.14 + 0.100*SL$	$0.10 + 0.102*SL$
	tF	0.21	$0.14 + 0.036*SL$	$0.13 + 0.038*SL$	$0.09 + 0.041*SL$
GN to Q	tPLH	0.74	$0.65 + 0.047*SL$	$0.66 + 0.043*SL$	$0.66 + 0.043*SL$
	tPHL	0.65	$0.59 + 0.030*SL$	$0.62 + 0.022*SL$	$0.64 + 0.020*SL$
	tR	0.33	$0.13 + 0.096*SL$	$0.12 + 0.101*SL$	$0.10 + 0.102*SL$
	tF	0.19	$0.11 + 0.040*SL$	$0.11 + 0.039*SL$	$0.08 + 0.041*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **LD6Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Input Hold Time (D to GN)	tHD	0.000
Input Setup Time (D to GN)	tSU	0.342
Recovery Time (RN)	tRC	0.139



## LD6D3Q

D-Latch Active Low Gate with Reset, Q Output Only, 3X Drive

### LD6D3Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

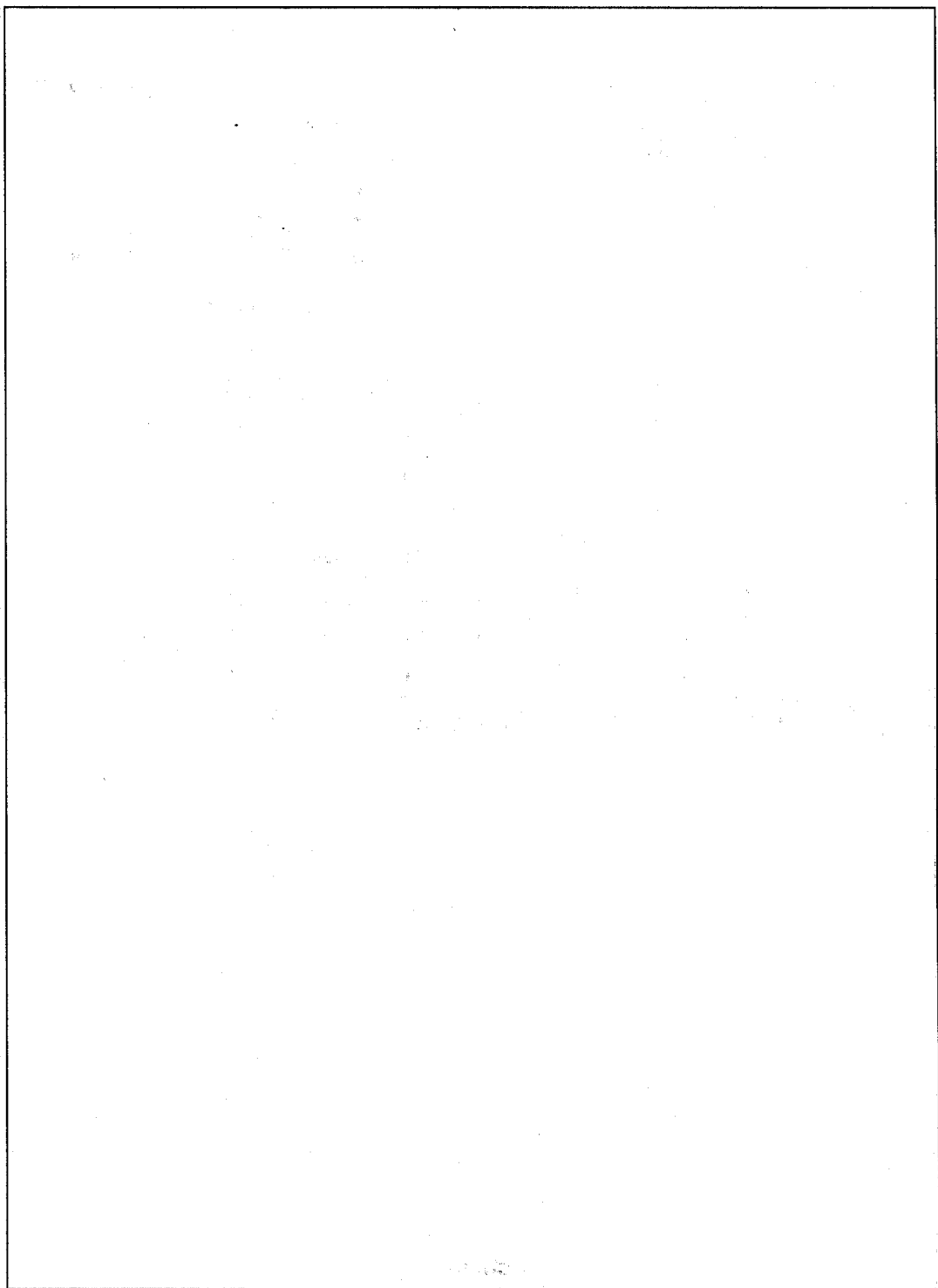
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPLH	0.35	$0.32 + 0.017*SL$	$0.32 + 0.015*SL$	$0.34 + 0.014*SL$
	tPHL	0.49	$0.46 + 0.015*SL$	$0.47 + 0.010*SL$	$0.52 + 0.008*SL$
	tR	0.24	$0.18 + 0.031*SL$	$0.17 + 0.033*SL$	$0.15 + 0.034*SL$
	tF	0.22	$0.20 + 0.014*SL$	$0.20 + 0.012*SL$	$0.20 + 0.013*SL$
D to Q	tPLH	0.45	$0.41 + 0.017*SL$	$0.42 + 0.015*SL$	$0.43 + 0.014*SL$
	tPHL	0.48	$0.45 + 0.014*SL$	$0.47 + 0.010*SL$	$0.51 + 0.008*SL$
	tR	0.24	$0.18 + 0.031*SL$	$0.17 + 0.033*SL$	$0.15 + 0.034*SL$
	tF	0.21	$0.19 + 0.010*SL$	$0.18 + 0.012*SL$	$0.17 + 0.013*SL$
GN to Q	tPLH	0.76	$0.72 + 0.017*SL$	$0.73 + 0.015*SL$	$0.74 + 0.014*SL$
	tPHL	0.68	$0.65 + 0.014*SL$	$0.67 + 0.010*SL$	$0.71 + 0.008*SL$
	tR	0.22	$0.16 + 0.032*SL$	$0.16 + 0.033*SL$	$0.14 + 0.034*SL$
	tF	0.18	$0.15 + 0.014*SL$	$0.15 + 0.013*SL$	$0.15 + 0.013*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### LD6D3Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (GN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Input Hold Time (D to GN)	tHD	0.000
Input Setup Time (D to GN)	tSU	0.397
Recovery Time (RN)	tRC	0.139



# LS1/LS1D3

SR Latch with separate Gate Inputs, 1X Drive, 2X Drive or 3X Drive

Inputs: SN1, SN2, SN, RN, RN1, RN2

Outputs: Q, QN

Input Loading (SL):

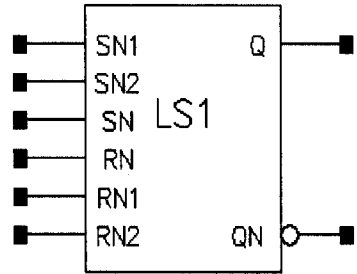
- LS1: All: 1
- LS1D3: All: 1

Maximum Fanout (Rec. SL):

- LS1: 14
- LS1D3: 84

Gate Count:

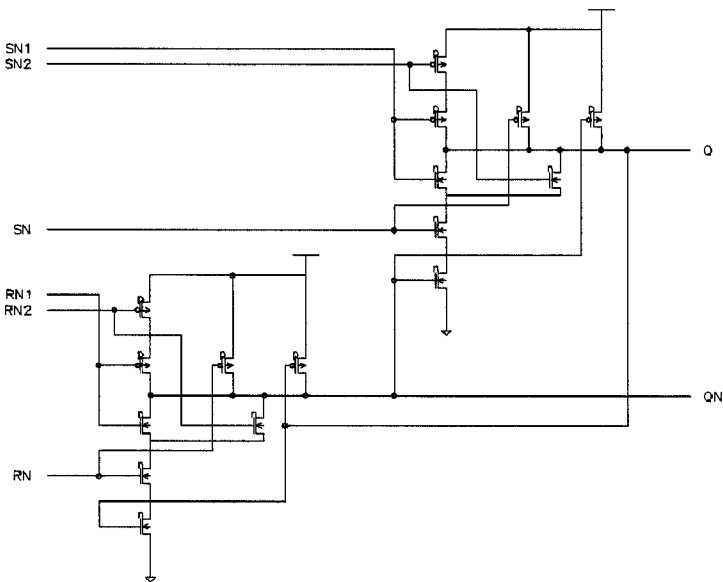
- LS1: 4
- LS1D3:



**Symbol**

SN1/SN2	RN1/RN2	SN	RN	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
x	1	0	1	1	0
1	x	1	0	0	1
x	x	0	0	1	1
1	1	1	1	Q <sub>n</sub>	Q <sub>Nn</sub>
1	0	1	1	0	1
0	1	1	1	1	0
0	0	1	1	1	1

**Truth Table**



**Schematic**

**LS1 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPHL	0.72	$0.55 + 0.082 * SL$	$0.56 + 0.079 * SL$	$0.56 + 0.079 * SL$
	tF	0.58	$0.41 + 0.087 * SL$	$0.39 + 0.092 * SL$	$0.37 + 0.093 * SL$
RN1 to Q	tPHL	0.82	$0.59 + 0.116 * SL$	$0.60 + 0.113 * SL$	$0.58 + 0.114 * SL$
	tF	0.61	$0.40 + 0.101 * SL$	$0.39 + 0.105 * SL$	$0.38 + 0.106 * SL$
RN2 to Q	tPHL	0.79	$0.56 + 0.114 * SL$	$0.56 + 0.114 * SL$	$0.55 + 0.114 * SL$
	tF	0.61	$0.41 + 0.099 * SL$	$0.40 + 0.105 * SL$	$0.38 + 0.106 * SL$
SN to Q	tPLH	0.47	$0.38 + 0.042 * SL$	$0.38 + 0.042 * SL$	$0.38 + 0.042 * SL$
	tPHL	0.29	$0.20 + 0.042 * SL$	$0.22 + 0.036 * SL$	$0.24 + 0.035 * SL$
	tR	0.75	$0.57 + 0.091 * SL$	$0.55 + 0.096 * SL$	$0.45 + 0.101 * SL$
	tF	0.66	$0.52 + 0.071 * SL$	$0.50 + 0.077 * SL$	$0.41 + 0.082 * SL$
SN1 to Q	tPLH	0.57	$0.42 + 0.078 * SL$	$0.42 + 0.077 * SL$	$0.40 + 0.078 * SL$
	tPHL	0.29	$0.19 + 0.053 * SL$	$0.22 + 0.043 * SL$	$0.23 + 0.043 * SL$
	tR	1.04	$0.70 + 0.175 * SL$	$0.66 + 0.186 * SL$	$0.59 + 0.190 * SL$
	tF	0.70	$0.52 + 0.087 * SL$	$0.50 + 0.094 * SL$	$0.40 + 0.099 * SL$
SN2 to Q	tPLH	0.54	$0.39 + 0.075 * SL$	$0.38 + 0.077 * SL$	$0.37 + 0.078 * SL$
	tPHL	0.34	$0.24 + 0.050 * SL$	$0.26 + 0.043 * SL$	$0.27 + 0.043 * SL$
	tR	1.04	$0.68 + 0.178 * SL$	$0.65 + 0.187 * SL$	$0.59 + 0.190 * SL$
	tF	0.79	$0.61 + 0.086 * SL$	$0.59 + 0.093 * SL$	$0.48 + 0.099 * SL$
RN to QN	tPLH	0.47	$0.38 + 0.042 * SL$	$0.38 + 0.042 * SL$	$0.38 + 0.042 * SL$
	tPHL	0.29	$0.20 + 0.042 * SL$	$0.22 + 0.036 * SL$	$0.24 + 0.035 * SL$
	tR	0.75	$0.57 + 0.091 * SL$	$0.55 + 0.096 * SL$	$0.45 + 0.101 * SL$
	tF	0.66	$0.52 + 0.071 * SL$	$0.50 + 0.077 * SL$	$0.40 + 0.082 * SL$
RN1 to QN	tPLH	0.57	$0.41 + 0.078 * SL$	$0.42 + 0.077 * SL$	$0.39 + 0.078 * SL$
	tPHL	0.29	$0.19 + 0.053 * SL$	$0.22 + 0.043 * SL$	$0.23 + 0.043 * SL$
	tR	1.04	$0.69 + 0.174 * SL$	$0.66 + 0.186 * SL$	$0.58 + 0.190 * SL$
	tF	0.69	$0.52 + 0.087 * SL$	$0.50 + 0.094 * SL$	$0.40 + 0.099 * SL$
RN2 to QN	tPLH	0.54	$0.39 + 0.075 * SL$	$0.38 + 0.077 * SL$	$0.37 + 0.078 * SL$
	tPHL	0.34	$0.24 + 0.050 * SL$	$0.26 + 0.043 * SL$	$0.27 + 0.043 * SL$
	tR	1.03	$0.68 + 0.178 * SL$	$0.65 + 0.186 * SL$	$0.58 + 0.190 * SL$
	tF	0.78	$0.61 + 0.086 * SL$	$0.59 + 0.093 * SL$	$0.47 + 0.099 * SL$
SN to QN	tPHL	0.72	$0.55 + 0.082 * SL$	$0.56 + 0.079 * SL$	$0.56 + 0.079 * SL$
	tF	0.58	$0.40 + 0.087 * SL$	$0.39 + 0.092 * SL$	$0.37 + 0.093 * SL$
SN1 to QN	tPHL	0.82	$0.59 + 0.116 * SL$	$0.60 + 0.113 * SL$	$0.58 + 0.114 * SL$
	tF	0.61	$0.41 + 0.099 * SL$	$0.39 + 0.105 * SL$	$0.38 + 0.106 * SL$
SN2 to QN	tPHL	0.79	$0.56 + 0.113 * SL$	$0.56 + 0.114 * SL$	$0.56 + 0.114 * SL$
	tF	0.61	$0.41 + 0.100 * SL$	$0.40 + 0.105 * SL$	$0.38 + 0.106 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# LS1D3

SR Latch with separate Gate Inputs, 3X Drive

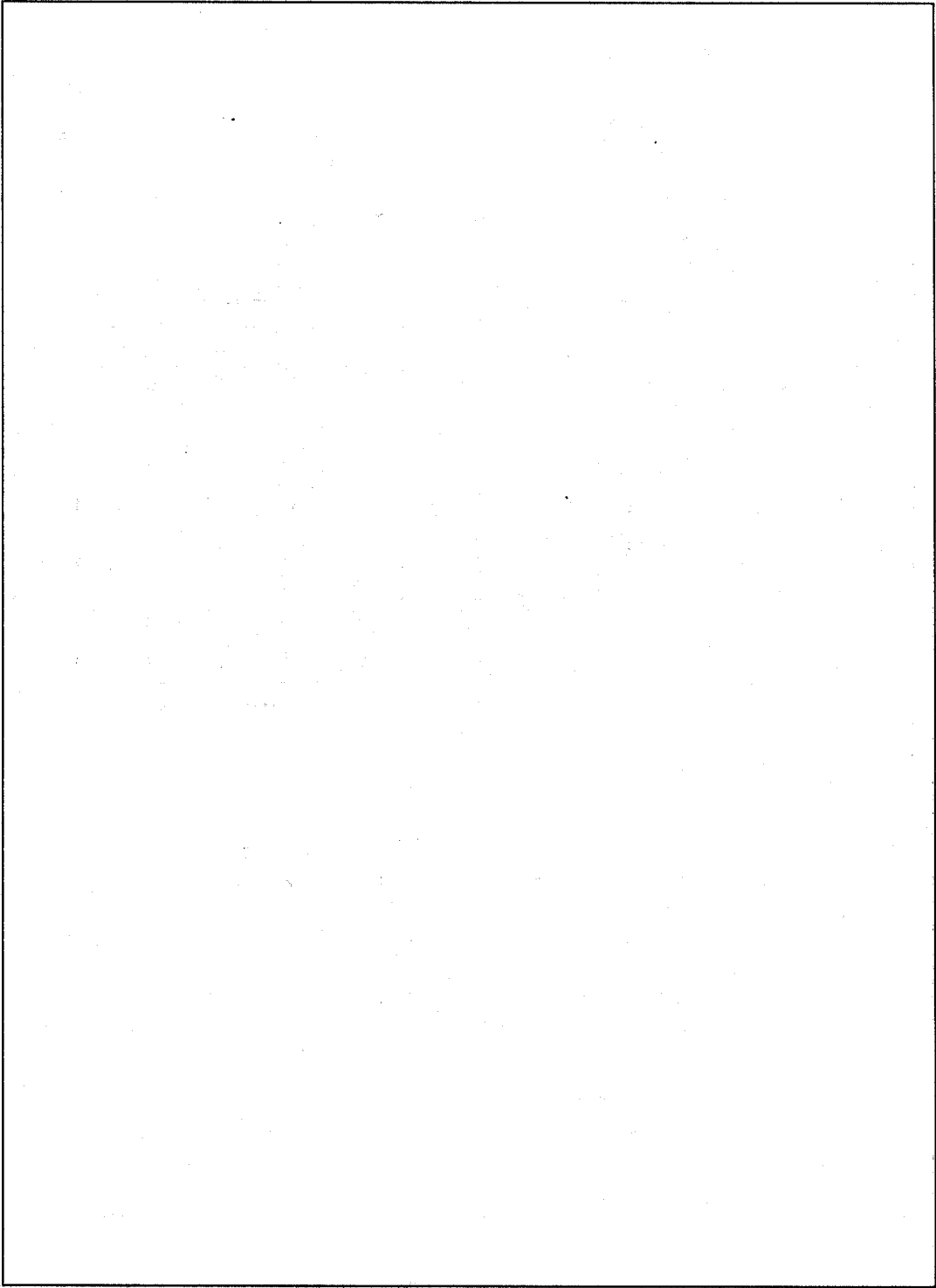
## LS1D3 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPHL	0.94	$0.92 + 0.012*SL$	$0.93 + 0.009*SL$	$0.96 + 0.007*SL$
	tF	0.18	$0.15 + 0.013*SL$	$0.15 + 0.012*SL$	$0.14 + 0.013*SL$
RN1 to Q	tPHL	1.01	$0.99 + 0.011*SL$	$1.00 + 0.009*SL$	$1.04 + 0.007*SL$
	tF	0.18	$0.15 + 0.014*SL$	$0.16 + 0.012*SL$	$0.14 + 0.013*SL$
RN2 to Q	tPHL	0.98	$0.96 + 0.012*SL$	$0.97 + 0.009*SL$	$1.00 + 0.007*SL$
	tF	0.18	$0.15 + 0.014*SL$	$0.15 + 0.012*SL$	$0.15 + 0.013*SL$
SN to Q	tPLH	0.64	$0.61 + 0.015*SL$	$0.61 + 0.014*SL$	$0.61 + 0.014*SL$
	tPHL	0.57	$0.54 + 0.015*SL$	$0.55 + 0.009*SL$	$0.59 + 0.007*SL$
	tR	0.19	$0.14 + 0.024*SL$	$0.12 + 0.033*SL$	$0.10 + 0.034*SL$
	tF	0.18	$0.15 + 0.017*SL$	$0.17 + 0.012*SL$	$0.15 + 0.012*SL$
SN1 to Q	tPLH	0.71	$0.68 + 0.017*SL$	$0.68 + 0.014*SL$	$0.69 + 0.014*SL$
	tPHL	0.55	$0.53 + 0.014*SL$	$0.54 + 0.009*SL$	$0.57 + 0.007*SL$
	tR	0.20	$0.14 + 0.030*SL$	$0.13 + 0.033*SL$	$0.10 + 0.034*SL$
	tF	0.17	$0.15 + 0.013*SL$	$0.15 + 0.012*SL$	$0.13 + 0.013*SL$
SN2 to Q	tPLH	0.68	$0.65 + 0.015*SL$	$0.65 + 0.014*SL$	$0.66 + 0.014*SL$
	tPHL	0.62	$0.60 + 0.012*SL$	$0.61 + 0.009*SL$	$0.65 + 0.007*SL$
	tR	0.20	$0.15 + 0.027*SL$	$0.13 + 0.033*SL$	$0.11 + 0.034*SL$
	tF	0.18	$0.15 + 0.014*SL$	$0.16 + 0.012*SL$	$0.15 + 0.012*SL$
RN to QN	tPLH	0.64	$0.61 + 0.017*SL$	$0.61 + 0.014*SL$	$0.61 + 0.014*SL$
	tPHL	0.57	$0.54 + 0.014*SL$	$0.55 + 0.009*SL$	$0.59 + 0.007*SL$
	tR	0.20	$0.15 + 0.025*SL$	$0.12 + 0.033*SL$	$0.10 + 0.034*SL$
	tF	0.18	$0.15 + 0.014*SL$	$0.16 + 0.012*SL$	$0.15 + 0.012*SL$
RN1 to QN	tPLH	0.71	$0.67 + 0.016*SL$	$0.68 + 0.014*SL$	$0.68 + 0.014*SL$
	tPHL	0.55	$0.53 + 0.013*SL$	$0.54 + 0.009*SL$	$0.57 + 0.007*SL$
	tR	0.20	$0.14 + 0.031*SL$	$0.13 + 0.033*SL$	$0.10 + 0.034*SL$
	tF	0.17	$0.15 + 0.012*SL$	$0.15 + 0.012*SL$	$0.14 + 0.013*SL$
RN2 to QN	tPLH	0.68	$0.65 + 0.015*SL$	$0.65 + 0.014*SL$	$0.65 + 0.014*SL$
	tPHL	0.62	$0.60 + 0.011*SL$	$0.61 + 0.009*SL$	$0.64 + 0.007*SL$
	tR	0.20	$0.15 + 0.027*SL$	$0.13 + 0.033*SL$	$0.11 + 0.034*SL$
	tF	0.18	$0.16 + 0.012*SL$	$0.16 + 0.012*SL$	$0.14 + 0.013*SL$
SN to QN	tPHL	0.94	$0.92 + 0.013*SL$	$0.93 + 0.009*SL$	$0.97 + 0.007*SL$
	tF	0.18	$0.16 + 0.009*SL$	$0.15 + 0.013*SL$	$0.16 + 0.012*SL$
SN1 to QN	tPHL	1.01	$0.98 + 0.013*SL$	$1.00 + 0.009*SL$	$1.04 + 0.007*SL$
	tF	0.18	$0.15 + 0.014*SL$	$0.15 + 0.012*SL$	$0.15 + 0.013*SL$
SN2 to QN	tPHL	0.98	$0.96 + 0.013*SL$	$0.97 + 0.009*SL$	$1.00 + 0.007*SL$
	tF	0.18	$0.15 + 0.013*SL$	$0.15 + 0.012*SL$	$0.14 + 0.013*SL$

\*Range1:  $SL < 3.00$ , \*Range2:  $3.00 \leq SL \leq 20.00$ , \*Range3:  $20.00 < SL$



# FA/FAD2/FAD4/FAD6

Full Adder with 1X Drive, 2X Drive, 4X Drive or 6X Drive

Inputs: C1, A, B

Outputs: S, C0

Input Loading (SL):

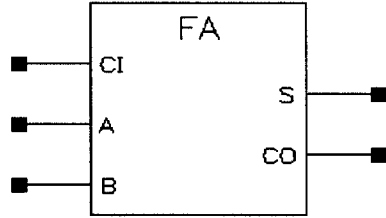
- FA: C1: 2, B: 2, A: 1
- FAD2: C1: 2,, B: 2, A: 1
- FAD4: C1: 2, B: 2, A: 1
- FAD6: C1: 2, B: 2, A: 1

Maximum Fanout (Rec. SL):

- FA: 14
- FAD2: 56
- FAD4: 112
- FAD6: 168

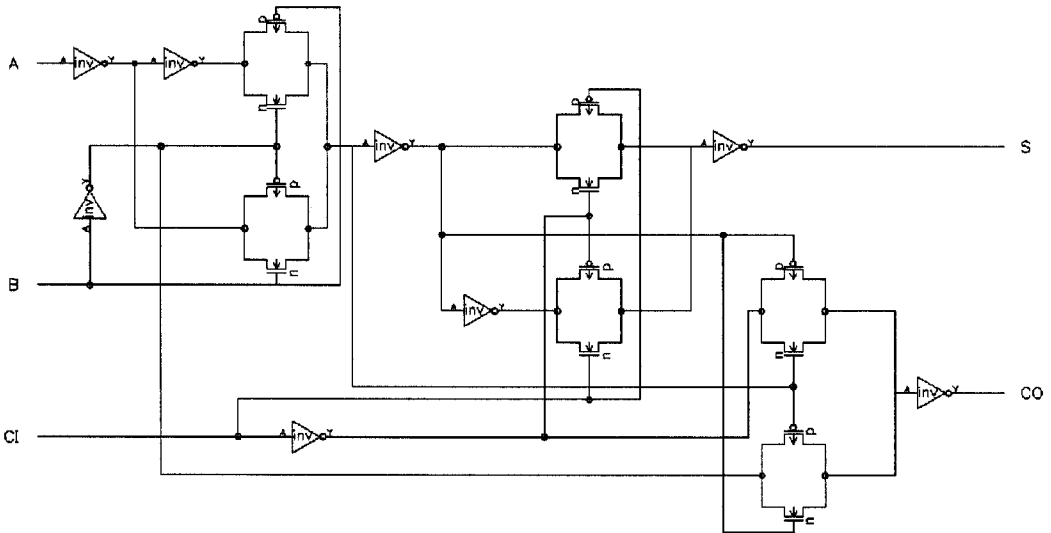
Gate Count:

- FA: 7
- FAD2: 8
- FAD4: 10
- FAD6: 12



A	B	C1	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table



Schematic

### FA Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	0.79	$0.70 + 0.044*SL$	$0.71 + 0.042*SL$	$0.70 + 0.042*SL$
	tPHL	0.91	$0.84 + 0.038*SL$	$0.88 + 0.025*SL$	$0.95 + 0.022*SL$
	tR	0.34	$0.16 + 0.094*SL$	$0.14 + 0.100*SL$	$0.10 + 0.102*SL$
	tF	0.26	$0.17 + 0.044*SL$	$0.19 + 0.040*SL$	$0.18 + 0.040*SL$
B to CO	tPLH	0.68	$0.59 + 0.044*SL$	$0.60 + 0.042*SL$	$0.59 + 0.042*SL$
	tPHL	0.78	$0.71 + 0.035*SL$	$0.75 + 0.024*SL$	$0.81 + 0.021*SL$
	tR	0.34	$0.15 + 0.095*SL$	$0.14 + 0.100*SL$	$0.10 + 0.102*SL$
	tF	0.23	$0.15 + 0.042*SL$	$0.15 + 0.040*SL$	$0.14 + 0.040*SL$
CI to CO	tPLH	0.40	$0.31 + 0.045*SL$	$0.31 + 0.043*SL$	$0.32 + 0.043*SL$
	tPHL	0.56	$0.48 + 0.037*SL$	$0.52 + 0.026*SL$	$0.60 + 0.022*SL$
	tR	0.34	$0.15 + 0.096*SL$	$0.14 + 0.101*SL$	$0.11 + 0.102*SL$
	tF	0.27	$0.18 + 0.045*SL$	$0.19 + 0.040*SL$	$0.19 + 0.040*SL$
A to S	tPLH	1.04	$0.95 + 0.045*SL$	$0.96 + 0.042*SL$	$0.96 + 0.042*SL$
	tPHL	0.94	$0.86 + 0.038*SL$	$0.90 + 0.025*SL$	$0.99 + 0.021*SL$
	tR	0.31	$0.13 + 0.092*SL$	$0.12 + 0.096*SL$	$0.09 + 0.098*SL$
	tF	0.26	$0.18 + 0.042*SL$	$0.19 + 0.037*SL$	$0.20 + 0.037*SL$
B to S	tPLH	0.94	$0.85 + 0.045*SL$	$0.86 + 0.042*SL$	$0.86 + 0.042*SL$
	tPHL	0.88	$0.81 + 0.035*SL$	$0.85 + 0.024*SL$	$0.92 + 0.020*SL$
	tR	0.31	$0.13 + 0.093*SL$	$0.12 + 0.096*SL$	$0.09 + 0.098*SL$
	tF	0.23	$0.14 + 0.041*SL$	$0.16 + 0.037*SL$	$0.15 + 0.037*SL$
CI to S	tPLH	0.67	$0.58 + 0.045*SL$	$0.59 + 0.042*SL$	$0.59 + 0.041*SL$
	tPHL	0.46	$0.40 + 0.033*SL$	$0.43 + 0.023*SL$	$0.49 + 0.020*SL$
	tR	0.33	$0.15 + 0.092*SL$	$0.14 + 0.095*SL$	$0.11 + 0.097*SL$
	tF	0.22	$0.14 + 0.039*SL$	$0.15 + 0.037*SL$	$0.15 + 0.037*SL$

\*Range1 : SL < 3.00, \*Range2 : 3.00 ≤ SL ≤ 20.00, \*Range3 : 20.00 < SL



# FAD2

Full Adder with 2X Drive

## FAD2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	0.81	$0.77 + 0.023*SL$	$0.77 + 0.021*SL$	$0.77 + 0.021*SL$
	tPHL	0.92	$0.87 + 0.023*SL$	$0.90 + 0.015*SL$	$0.97 + 0.012*SL$
	tR	0.26	$0.17 + 0.047*SL$	$0.16 + 0.050*SL$	$0.12 + 0.052*SL$
	tF	0.24	$0.19 + 0.025*SL$	$0.20 + 0.020*SL$	$0.21 + 0.020*SL$
B to CO	tPLH	0.70	$0.66 + 0.023*SL$	$0.66 + 0.021*SL$	$0.66 + 0.021*SL$
	tPHL	0.80	$0.75 + 0.022*SL$	$0.77 + 0.015*SL$	$0.84 + 0.012*SL$
	tR	0.26	$0.17 + 0.046*SL$	$0.16 + 0.050*SL$	$0.12 + 0.052*SL$
	tF	0.22	$0.17 + 0.024*SL$	$0.18 + 0.021*SL$	$0.19 + 0.020*SL$
CI to CO	tPLH	0.40	$0.35 + 0.024*SL$	$0.36 + 0.022*SL$	$0.37 + 0.021*SL$
	tPHL	0.55	$0.50 + 0.022*SL$	$0.52 + 0.015*SL$	$0.59 + 0.012*SL$
	tR	0.26	$0.17 + 0.046*SL$	$0.15 + 0.050*SL$	$0.12 + 0.052*SL$
	tF	0.24	$0.19 + 0.022*SL$	$0.20 + 0.021*SL$	$0.21 + 0.020*SL$
A to S	tPLH	1.02	$0.97 + 0.023*SL$	$0.98 + 0.021*SL$	$0.99 + 0.020*SL$
	tPHL	0.94	$0.89 + 0.024*SL$	$0.91 + 0.015*SL$	$0.99 + 0.012*SL$
	tR	0.22	$0.13 + 0.044*SL$	$0.13 + 0.046*SL$	$0.10 + 0.047*SL$
	tF	0.25	$0.20 + 0.024*SL$	$0.21 + 0.020*SL$	$0.23 + 0.018*SL$
B to S	tPLH	0.93	$0.88 + 0.024*SL$	$0.89 + 0.021*SL$	$0.90 + 0.020*SL$
	tPHL	0.88	$0.84 + 0.021*SL$	$0.86 + 0.014*SL$	$0.92 + 0.011*SL$
	tR	0.22	$0.13 + 0.045*SL$	$0.13 + 0.046*SL$	$0.10 + 0.047*SL$
	tF	0.21	$0.17 + 0.019*SL$	$0.17 + 0.019*SL$	$0.18 + 0.018*SL$
CI to S	tPLH	0.65	$0.61 + 0.022*SL$	$0.61 + 0.020*SL$	$0.62 + 0.020*SL$
	tPHL	0.46	$0.42 + 0.020*SL$	$0.44 + 0.014*SL$	$0.50 + 0.011*SL$
	tR	0.24	$0.15 + 0.044*SL$	$0.14 + 0.046*SL$	$0.12 + 0.047*SL$
	tF	0.19	$0.15 + 0.022*SL$	$0.16 + 0.020*SL$	$0.18 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FAD4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	0.92	$0.90 + 0.012^*SL$	$0.90 + 0.011^*SL$	$0.91 + 0.010^*SL$
	tPHL	0.97	$0.94 + 0.014^*SL$	$0.95 + 0.010^*SL$	$1.00 + 0.008^*SL$
	tR	0.26	$0.22 + 0.019^*SL$	$0.21 + 0.024^*SL$	$0.18 + 0.025^*SL$
	tF	0.26	$0.24 + 0.012^*SL$	$0.24 + 0.012^*SL$	$0.27 + 0.010^*SL$
B to CO	tPLH	0.81	$0.79 + 0.012^*SL$	$0.79 + 0.011^*SL$	$0.80 + 0.010^*SL$
	tPHL	0.85	$0.82 + 0.014^*SL$	$0.83 + 0.010^*SL$	$0.88 + 0.007^*SL$
	tR	0.26	$0.22 + 0.019^*SL$	$0.21 + 0.024^*SL$	$0.18 + 0.025^*SL$
	tF	0.24	$0.21 + 0.014^*SL$	$0.21 + 0.012^*SL$	$0.24 + 0.010^*SL$
Cl to CO	tPLH	0.46	$0.43 + 0.013^*SL$	$0.44 + 0.011^*SL$	$0.45 + 0.011^*SL$
	tPHL	0.61	$0.58 + 0.013^*SL$	$0.59 + 0.010^*SL$	$0.63 + 0.007^*SL$
	tR	0.24	$0.19 + 0.022^*SL$	$0.19 + 0.024^*SL$	$0.16 + 0.025^*SL$
	tF	0.26	$0.24 + 0.012^*SL$	$0.24 + 0.011^*SL$	$0.26 + 0.010^*SL$
A to S	tPLH	1.08	$1.06 + 0.013^*SL$	$1.06 + 0.011^*SL$	$1.08 + 0.011^*SL$
	tPHL	1.00	$0.97 + 0.014^*SL$	$0.98 + 0.010^*SL$	$1.03 + 0.008^*SL$
	tR	0.22	$0.18 + 0.021^*SL$	$0.17 + 0.025^*SL$	$0.15 + 0.025^*SL$
	tF	0.28	$0.26 + 0.013^*SL$	$0.26 + 0.012^*SL$	$0.28 + 0.010^*SL$
B to S	tPLH	1.00	$0.97 + 0.013^*SL$	$0.98 + 0.011^*SL$	$0.99 + 0.011^*SL$
	tPHL	0.95	$0.92 + 0.013^*SL$	$0.93 + 0.009^*SL$	$0.97 + 0.007^*SL$
	tR	0.22	$0.18 + 0.022^*SL$	$0.17 + 0.024^*SL$	$0.15 + 0.025^*SL$
	tF	0.24	$0.21 + 0.013^*SL$	$0.22 + 0.011^*SL$	$0.24 + 0.010^*SL$
Cl to S	tPLH	0.76	$0.73 + 0.012^*SL$	$0.74 + 0.011^*SL$	$0.75 + 0.011^*SL$
	tPHL	0.50	$0.48 + 0.012^*SL$	$0.49 + 0.010^*SL$	$0.53 + 0.007^*SL$
	tR	0.25	$0.21 + 0.020^*SL$	$0.20 + 0.024^*SL$	$0.17 + 0.025^*SL$
	tF	0.22	$0.20 + 0.012^*SL$	$0.19 + 0.012^*SL$	$0.22 + 0.011^*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# FAD6

## Full Adder with 6X Drive

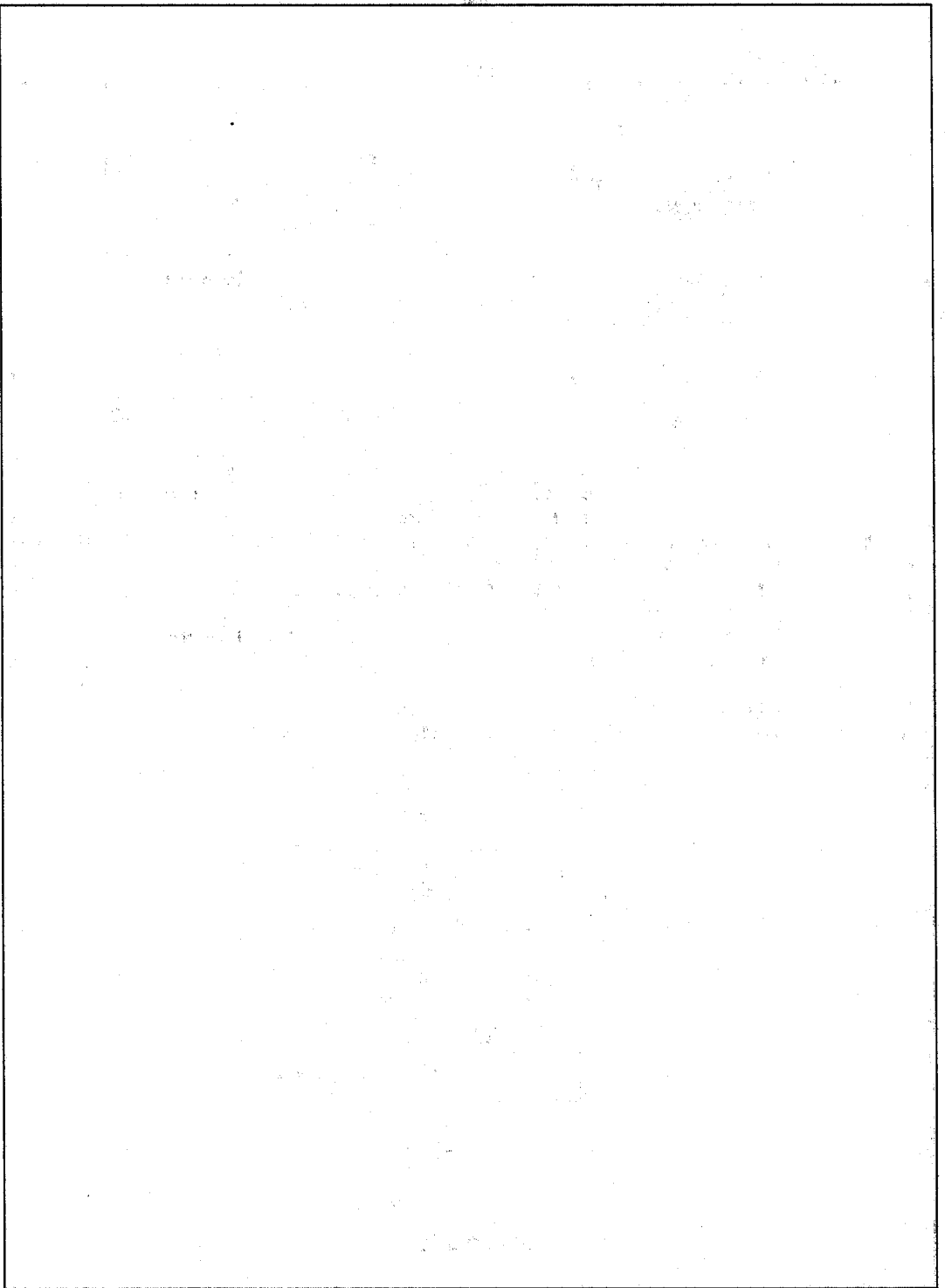
### FAD6 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	1.04	$1.02 + 0.009*SL$	$1.03 + 0.007*SL$	$1.03 + 0.007*SL$
	tPHL	1.02	$1.00 + 0.010*SL$	$1.01 + 0.008*SL$	$1.05 + 0.006*SL$
	tR	0.30	$0.28 + 0.010*SL$	$0.26 + 0.015*SL$	$0.23 + 0.016*SL$
	tF	0.30	$0.29 + 0.009*SL$	$0.29 + 0.009*SL$	$0.31 + 0.007*SL$
B to CO	tPLH	0.93	$0.91 + 0.009*SL$	$0.92 + 0.007*SL$	$0.93 + 0.007*SL$
	tPHL	0.93	$0.88 + 0.010*SL$	$0.89 + 0.008*SL$	$0.93 + 0.006*SL$
	tR	0.30	$0.28 + 0.011*SL$	$0.26 + 0.015*SL$	$0.23 + 0.016*SL$
	tF	0.27	$0.26 + 0.009*SL$	$0.26 + 0.009*SL$	$0.28 + 0.008*SL$
CI to CO	tPLH	0.52	$0.50 + 0.010*SL$	$0.51 + 0.008*SL$	$0.52 + 0.007*SL$
	tPHL	0.69	$0.67 + 0.010*SL$	$0.68 + 0.007*SL$	$0.71 + 0.006*SL$
	tR	0.26	$0.24 + 0.012*SL$	$0.23 + 0.015*SL$	$0.20 + 0.017*SL$
	tF	0.31	$0.29 + 0.009*SL$	$0.29 + 0.008*SL$	$0.31 + 0.007*SL$
A to S	tPLH	1.14	$1.12 + 0.010*SL$	$1.13 + 0.008*SL$	$1.14 + 0.007*SL$
	tPHL	1.07	$1.05 + 0.010*SL$	$1.05 + 0.008*SL$	$1.09 + 0.006*SL$
	tR	0.29	$0.27 + 0.010*SL$	$0.26 + 0.015*SL$	$0.22 + 0.016*SL$
	tF	0.32	$0.30 + 0.010*SL$	$0.31 + 0.008*SL$	$0.32 + 0.007*SL$
B to S	tPLH	1.06	$1.04 + 0.010*SL$	$1.05 + 0.008*SL$	$1.06 + 0.007*SL$
	tPHL	1.01	$0.99 + 0.010*SL$	$1.00 + 0.007*SL$	$1.03 + 0.006*SL$
	tR	0.24	$0.22 + 0.014*SL$	$0.21 + 0.015*SL$	$0.19 + 0.017*SL$
	tF	0.28	$0.26 + 0.009*SL$	$0.26 + 0.008*SL$	$0.28 + 0.007*SL$
CI to S	tPLH	0.89	$0.87 + 0.008*SL$	$0.88 + 0.007*SL$	$0.88 + 0.007*SL$
	tPHL	0.56	$0.54 + 0.010*SL$	$0.55 + 0.008*SL$	$0.58 + 0.006*SL$
	tR	0.29	$0.27 + 0.011*SL$	$0.26 + 0.015*SL$	$0.22 + 0.016*SL$
	tF	0.25	$0.23 + 0.013*SL$	$0.24 + 0.009*SL$	$0.26 + 0.008*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# HA/HAD2/HAD4

Half Adder with 1x Drive, 2X Drive or 4X Drive

Inputs: A, B

Outputs: S, CO

Input Loading (SL):

- HA: A: 2, B: 3

- HAD2: A: 2, B: 3

- HAD4: A: 2, B: 3

Maximum Fanout (Rec. SL):

- HA: 28

- HAD2: 56

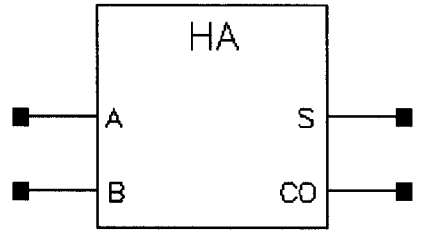
- HAD4: 112

Gate Count:

- HA: 5

- HAD2: 6

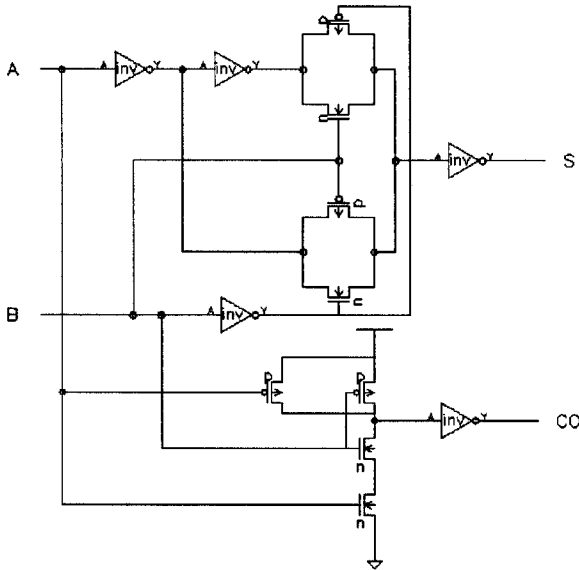
- HAD4: 8



Symbol

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table



Schematic

### HA Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	0.26	$0.18 + 0.041 * SL$	$0.19 + 0.040 * SL$	$0.18 + 0.040 * SL$
	tPHL	0.41	$0.35 + 0.029 * SL$	$0.38 + 0.021 * SL$	$0.39 + 0.020 * SL$
	tR	0.30	$0.13 + 0.085 * SL$	$0.12 + 0.091 * SL$	$0.09 + 0.092 * SL$
	tF	0.20	$0.13 + 0.035 * SL$	$0.12 + 0.038 * SL$	$0.07 + 0.041 * SL$
B to CO	tPLH	0.29	$0.20 + 0.041 * SL$	$0.21 + 0.040 * SL$	$0.20 + 0.040 * SL$
	tPHL	0.34	$0.29 + 0.027 * SL$	$0.31 + 0.021 * SL$	$0.32 + 0.020 * SL$
	tR	0.30	$0.12 + 0.088 * SL$	$0.11 + 0.091 * SL$	$0.09 + 0.092 * SL$
	tF	0.19	$0.12 + 0.035 * SL$	$0.10 + 0.039 * SL$	$0.07 + 0.041 * SL$
A to S	tPLH	0.66	$0.58 + 0.042 * SL$	$0.58 + 0.041 * SL$	$0.58 + 0.041 * SL$
	tPHL	0.57	$0.50 + 0.034 * SL$	$0.53 + 0.024 * SL$	$0.60 + 0.021 * SL$
	tR	0.36	$0.18 + 0.090 * SL$	$0.17 + 0.094 * SL$	$0.15 + 0.095 * SL$
	tF	0.28	$0.20 + 0.040 * SL$	$0.21 + 0.037 * SL$	$0.20 + 0.038 * SL$
B to S	tPLH	0.53	$0.44 + 0.042 * SL$	$0.45 + 0.041 * SL$	$0.45 + 0.041 * SL$
	tPHL	0.45	$0.39 + 0.031 * SL$	$0.41 + 0.023 * SL$	$0.47 + 0.021 * SL$
	tR	0.36	$0.18 + 0.091 * SL$	$0.17 + 0.094 * SL$	$0.15 + 0.095 * SL$
	tF	0.24	$0.15 + 0.042 * SL$	$0.16 + 0.039 * SL$	$0.16 + 0.039 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### HAD2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	0.27	$0.22 + 0.022 * SL$	$0.23 + 0.020 * SL$	$0.23 + 0.020 * SL$
	tPHL	0.42	$0.38 + 0.018 * SL$	$0.40 + 0.012 * SL$	$0.44 + 0.010 * SL$
	tR	0.22	$0.14 + 0.044 * SL$	$0.13 + 0.045 * SL$	$0.10 + 0.047 * SL$
	tF	0.19	$0.15 + 0.017 * SL$	$0.15 + 0.017 * SL$	$0.13 + 0.018 * SL$
B to CO	tPLH	0.30	$0.25 + 0.022 * SL$	$0.26 + 0.020 * SL$	$0.26 + 0.020 * SL$
	tPHL	0.37	$0.34 + 0.016 * SL$	$0.36 + 0.012 * SL$	$0.39 + 0.010 * SL$
	tR	0.22	$0.13 + 0.043 * SL$	$0.13 + 0.045 * SL$	$0.10 + 0.047 * SL$
	tF	0.17	$0.13 + 0.019 * SL$	$0.14 + 0.017 * SL$	$0.12 + 0.018 * SL$
A to S	tPLH	0.63	$0.59 + 0.022 * SL$	$0.59 + 0.021 * SL$	$0.60 + 0.020 * SL$
	tPHL	0.55	$0.51 + 0.021 * SL$	$0.53 + 0.015 * SL$	$0.60 + 0.012 * SL$
	tR	0.23	$0.14 + 0.044 * SL$	$0.13 + 0.046 * SL$	$0.11 + 0.047 * SL$
	tF	0.24	$0.20 + 0.021 * SL$	$0.20 + 0.019 * SL$	$0.22 + 0.019 * SL$
B to S	tPLH	0.49	$0.45 + 0.024 * SL$	$0.46 + 0.021 * SL$	$0.46 + 0.020 * SL$
	tPHL	0.43	$0.39 + 0.020 * SL$	$0.40 + 0.014 * SL$	$0.46 + 0.011 * SL$
	tR	0.22	$0.14 + 0.044 * SL$	$0.13 + 0.046 * SL$	$0.11 + 0.047 * SL$
	tF	0.19	$0.14 + 0.022 * SL$	$0.15 + 0.020 * SL$	$0.17 + 0.019 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# HAD4

## Half Adder with 4X Drive

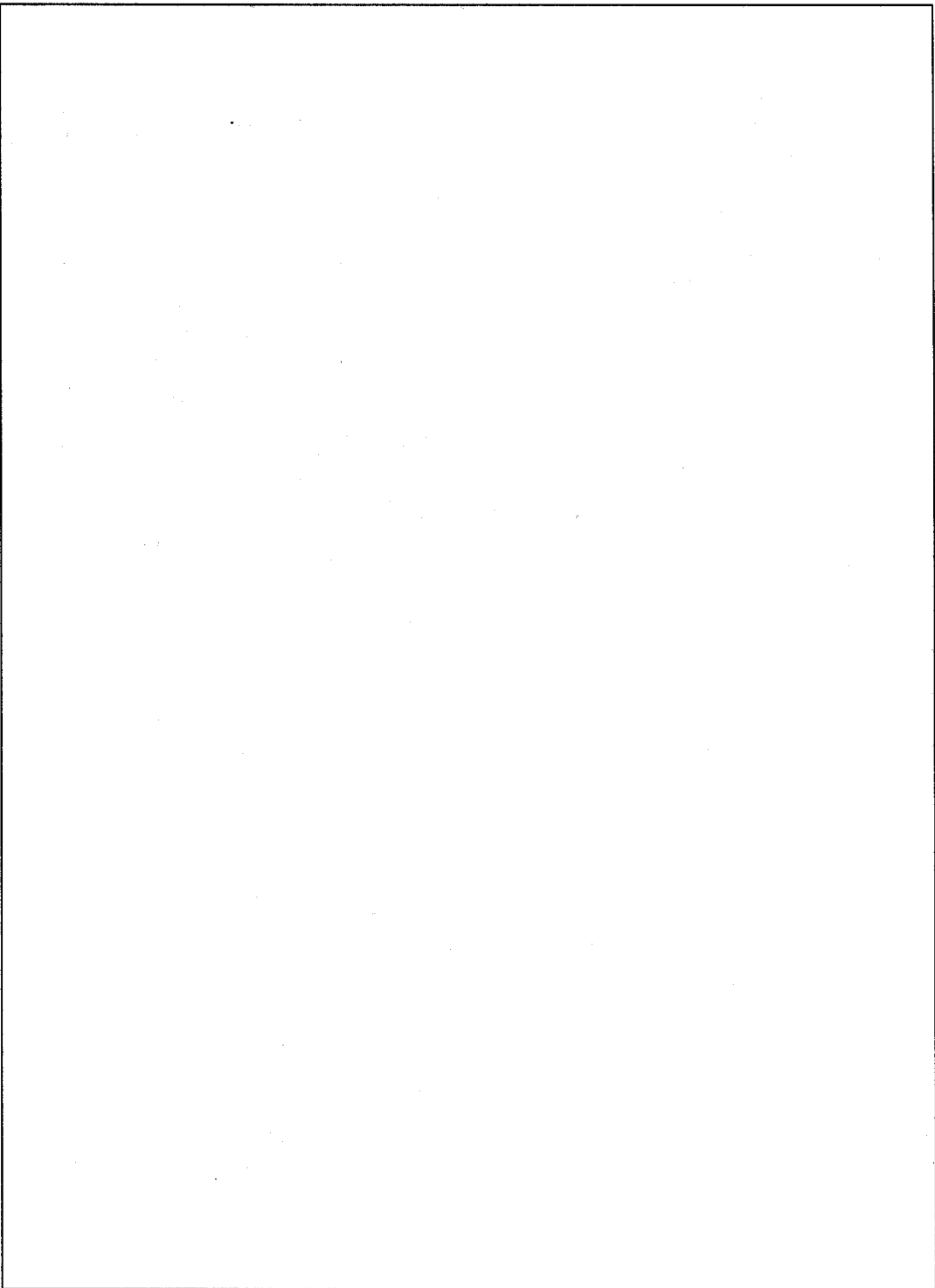
### HAD4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to CO	tPLH	0.34	$0.31 + 0.013*SL$	$0.32 + 0.011*SL$	$0.33 + 0.011*SL$
	tPHL	0.48	$0.46 + 0.011*SL$	$0.47 + 0.008*SL$	$0.50 + 0.006*SL$
	tR	0.22	$0.18 + 0.021*SL$	$0.17 + 0.024*SL$	$0.15 + 0.025*SL$
	tF	0.21	$0.19 + 0.011*SL$	$0.20 + 0.009*SL$	$0.19 + 0.009*SL$
B to CO	tPLH	0.38	$0.35 + 0.013*SL$	$0.36 + 0.011*SL$	$0.37 + 0.011*SL$
	tPHL	0.44	$0.42 + 0.010*SL$	$0.43 + 0.008*SL$	$0.46 + 0.006*SL$
	tR	0.22	$0.17 + 0.023*SL$	$0.17 + 0.024*SL$	$0.15 + 0.025*SL$
	tF	0.20	$0.18 + 0.010*SL$	$0.18 + 0.009*SL$	$0.18 + 0.010*SL$
A to S	tPLH	0.68	$0.66 + 0.013*SL$	$0.66 + 0.011*SL$	$0.68 + 0.011*SL$
	tPHL	0.61	$0.58 + 0.014*SL$	$0.59 + 0.010*SL$	$0.64 + 0.007*SL$
	tR	0.22	$0.18 + 0.021*SL$	$0.17 + 0.024*SL$	$0.15 + 0.025*SL$
	tF	0.27	$0.24 + 0.013*SL$	$0.25 + 0.011*SL$	$0.27 + 0.010*SL$
B to S	tPLH	0.55	$0.52 + 0.014*SL$	$0.53 + 0.011*SL$	$0.54 + 0.011*SL$
	tPHL	0.47	$0.45 + 0.012*SL$	$0.46 + 0.009*SL$	$0.50 + 0.007*SL$
	tR	0.22	$0.18 + 0.021*SL$	$0.17 + 0.025*SL$	$0.15 + 0.025*SL$
	tF	0.21	$0.19 + 0.011*SL$	$0.19 + 0.012*SL$	$0.21 + 0.011*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$





# FD1/FD1D2

D Flip-Flop with Positive Edge Trigger with 1X Drive or 2X Drive

Inputs: D, CK

Outputs: Q, QN

Input Loading (SL):

- D: 3

- CK: 1

Maximum Fanout (Rec. SL): All :

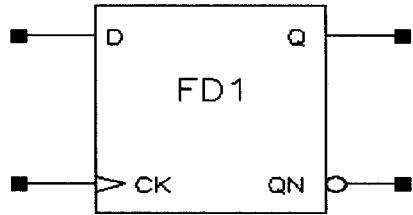
FD1: 28

FD1D2: 56

Gate Count:

FD1: 6

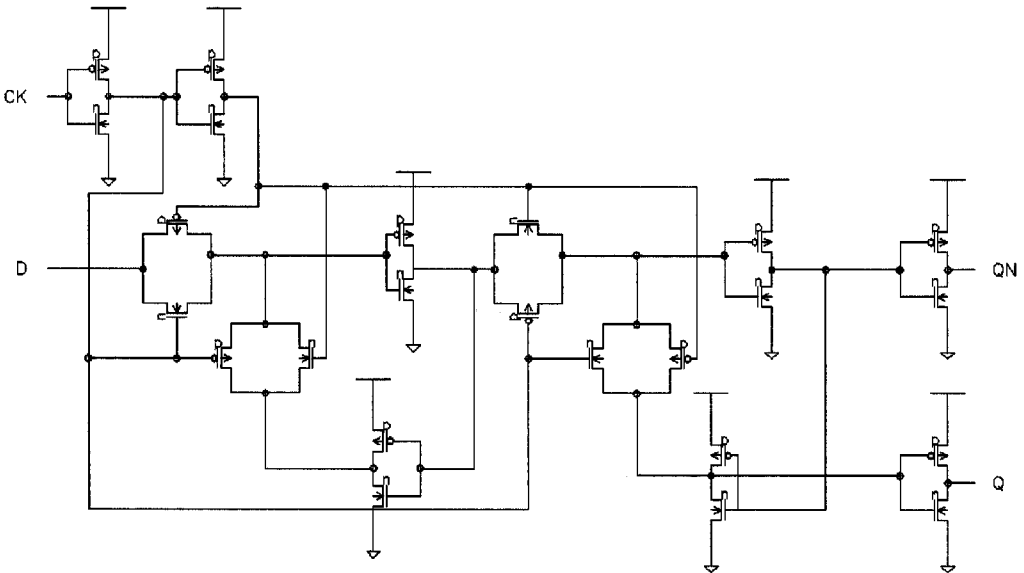
FD1D2: 7



Symbol

D	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0		0	1
1		1	0
x		Q <sub>n</sub>	Q <sub>Nn</sub>

Truth Table



Schematic

**FD1 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.70	$0.61 + 0.041*SL$	$0.61 + 0.041*SL$	$0.61 + 0.041*SL$
	tPHL	0.63	$0.58 + 0.026*SL$	$0.60 + 0.021*SL$	$0.61 + 0.020*SL$
	tR	0.29	$0.10 + 0.093*SL$	$0.09 + 0.097*SL$	$0.08 + 0.097*SL$
	tF	0.17	$0.10 + 0.036*SL$	$0.09 + 0.038*SL$	$0.06 + 0.039*SL$
CK to QN	tPLH	0.57	$0.48 + 0.044*SL$	$0.49 + 0.043*SL$	$0.49 + 0.043*SL$
	tPHL	0.55	$0.50 + 0.028*SL$	$0.52 + 0.022*SL$	$0.54 + 0.020*SL$
	tR	0.31	$0.11 + 0.099*SL$	$0.10 + 0.101*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.039*SL$	$0.10 + 0.040*SL$	$0.08 + 0.041*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD1 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.233
Input Setup Time (D to CK)	tSU	0.342

**FD1D2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.73	$0.70 + 0.018*SL$	$0.69 + 0.020*SL$	$0.68 + 0.020*SL$
	tPHL	0.68	$0.65 + 0.015*SL$	$0.66 + 0.012*SL$	$0.69 + 0.010*SL$
	tR	0.20	$0.11 + 0.044*SL$	$0.10 + 0.047*SL$	$0.08 + 0.048*SL$
	tF	0.15	$0.12 + 0.017*SL$	$0.11 + 0.018*SL$	$0.10 + 0.019*SL$
CK to QN	tPLH	0.56	$0.51 + 0.022*SL$	$0.52 + 0.021*SL$	$0.52 + 0.021*SL$
	tPHL	0.56	$0.53 + 0.017*SL$	$0.54 + 0.012*SL$	$0.58 + 0.010*SL$
	tR	0.21	$0.12 + 0.045*SL$	$0.11 + 0.049*SL$	$0.09 + 0.050*SL$
	tF	0.16	$0.12 + 0.019*SL$	$0.12 + 0.019*SL$	$0.11 + 0.020*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD1D2 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.233
Input Setup Time (D to CK)	tSU	0.342

# FD1D2Q/FD1D4Q

D Flip-Flop with Positive Edge Trigger, Q Output only, with 2X Drive or 4X Drive

Inputs: D, CK

Output: Q

Input Loading (SL): All: D: 3, CK: 1

Maximum Fanout (Rec. SL):

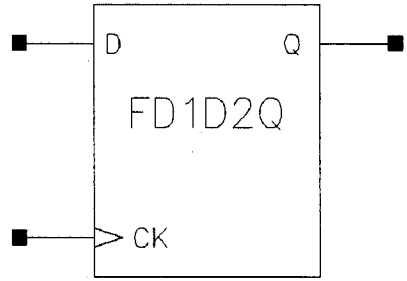
- FD1D2Q: 56

- FD1D4Q: 112

Gate Count:

- FD1D2Q: 6

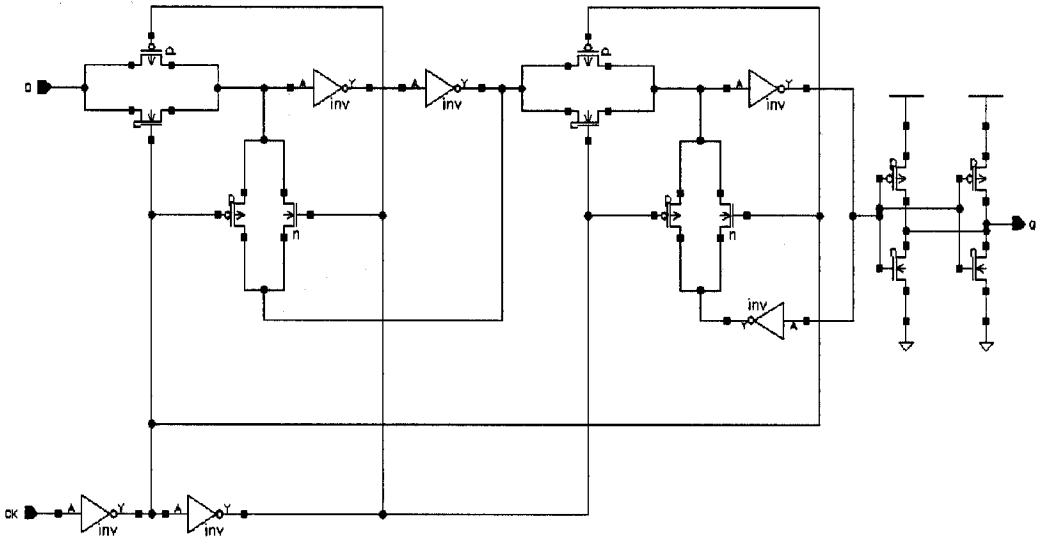
- FD1D4Q: 7



Symbol

D	CK	Q <sub>n+1</sub>
0		0
1		1
x		Q <sub>n</sub>

Truth Table



Schematic

**FD1D2Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.49	$0.45 + 0.025*SL$	$0.45 + 0.022*SL$	$0.47 + 0.021*SL$
	tPHL	0.44	$0.40 + 0.023*SL$	$0.42 + 0.016*SL$	$0.49 + 0.012*SL$
	tR	0.25	$0.15 + 0.050*SL$	$0.15 + 0.051*SL$	$0.12 + 0.052*SL$
	tF	0.21	$0.15 + 0.029*SL$	$0.17 + 0.022*SL$	$0.21 + 0.021*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD1D2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.233
Input Setup Time (D to CK)	tSU	0.342

**FD1D4Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.53	$0.51 + 0.014*SL$	$0.51 + 0.012*SL$	$0.53 + 0.011*SL$
	tPHL	0.48	$0.45 + 0.014*SL$	$0.46 + 0.010*SL$	$0.51 + 0.008*SL$
	tR	0.23	$0.18 + 0.023*SL$	$0.18 + 0.024*SL$	$0.16 + 0.025*SL$
	tF	0.24	$0.20 + 0.016*SL$	$0.21 + 0.013*SL$	$0.25 + 0.011*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD1D4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.287
Input Setup Time (D to CK)	tSU	0.342

# FD1S/FD1SD2

D Flip-Flop with Scan, Positive Edge Trigger, 1X Drive or 2X Drive

Inputs: D, TI, TE, CK

Outputs: Q, QN

Input Loading (SL):

- D, TI, CK: 1

- TE: 2

Maximum Fanout (Rec. SL): All :

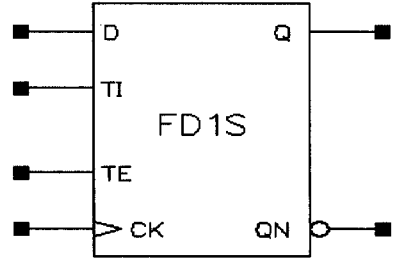
FD1S: 28

FD1SD2: 56

Gate Count:

FD1S: 9

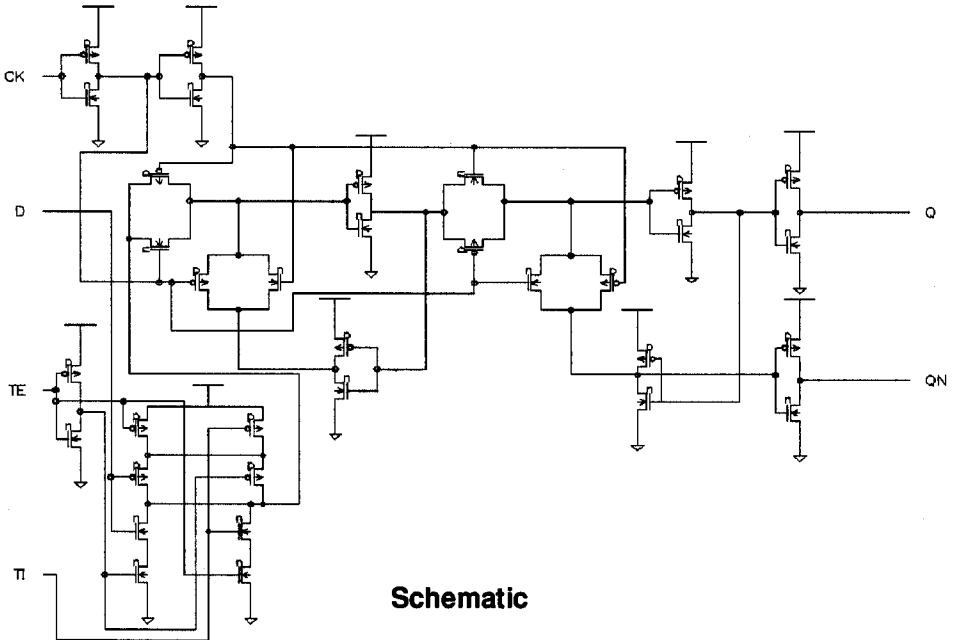
FD1SD2: 10



**Symbol**

D	TI	TE	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	x	0		0	1
1	x	0		1	0
x	0	1		0	1
x	1	1		1	0
x	x	x		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FD1S Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{q}$  and  $t_{f}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.56	$0.48 + 0.043 \cdot SL$	$0.48 + 0.043 \cdot SL$	$0.48 + 0.043 \cdot SL$
	tPHL	0.56	$0.50 + 0.028 \cdot SL$	$0.52 + 0.022 \cdot SL$	$0.55 + 0.020 \cdot SL$
	tR	0.31	$0.11 + 0.099 \cdot SL$	$0.10 + 0.102 \cdot SL$	$0.09 + 0.102 \cdot SL$
	tF	0.18	$0.10 + 0.040 \cdot SL$	$0.10 + 0.039 \cdot SL$	$0.07 + 0.041 \cdot SL$
CK to QN	tPLH	0.70	$0.62 + 0.041 \cdot SL$	$0.62 + 0.041 \cdot SL$	$0.62 + 0.041 \cdot SL$
	tPHL	0.63	$0.58 + 0.026 \cdot SL$	$0.59 + 0.021 \cdot SL$	$0.61 + 0.020 \cdot SL$
	tR	0.29	$0.10 + 0.094 \cdot SL$	$0.09 + 0.096 \cdot SL$	$0.08 + 0.097 \cdot SL$
	tF	0.17	$0.10 + 0.037 \cdot SL$	$0.09 + 0.037 \cdot SL$	$0.06 + 0.039 \cdot SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD1S Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.616
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.670

# FD1SD2

D Flip-Flop with Scan, Positive Edge Trigger, 2X Drive

## FD1SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

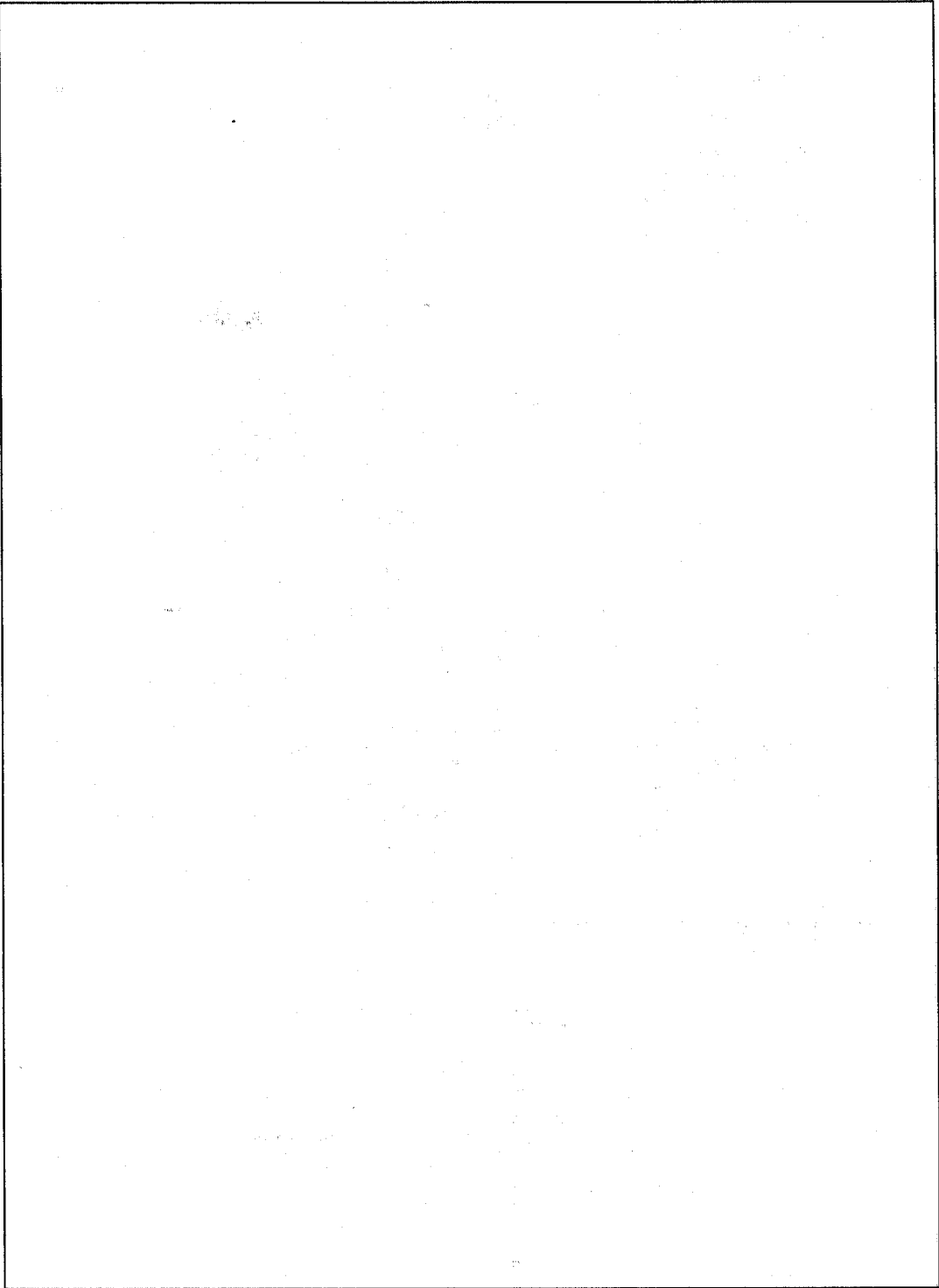
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.55	$0.51 + 0.022*SL$	$0.51 + 0.021*SL$	$0.51 + 0.021*SL$
	tPHL	0.57	$0.53 + 0.017*SL$	$0.55 + 0.012*SL$	$0.58 + 0.010*SL$
	tR	0.21	$0.12 + 0.046*SL$	$0.11 + 0.049*SL$	$0.09 + 0.050*SL$
	tF	0.16	$0.12 + 0.020*SL$	$0.13 + 0.019*SL$	$0.11 + 0.020*SL$
CK to QN	tPLH	0.74	$0.70 + 0.018*SL$	$0.70 + 0.020*SL$	$0.69 + 0.020*SL$
	tPHL	0.68	$0.65 + 0.016*SL$	$0.66 + 0.011*SL$	$0.69 + 0.010*SL$
	tR	0.20	$0.11 + 0.044*SL$	$0.10 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.15	$0.11 + 0.018*SL$	$0.11 + 0.018*SL$	$0.10 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD1SD2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.616
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.670





# FD1SD2Q/FD1SD4Q

D Flip-Flop with Scan, Positive Edge Trigger, Q Output Only, 2X Drive or 4X Drive

Inputs: D, TI, TE, CK

Output: Q

Input Loading (SL):

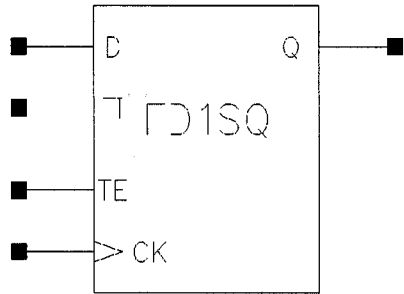
- FD1SD2Q: D: 1, CK: 1, TI: 1, TE: 2
- FD1SD4Q: D: 1, CK: 1, TI: 1, TE: 2

Maximum Fanout (Rec. SL):

- FD1SD2Q: 56
- FD1SD4Q: 112

Gate Count:

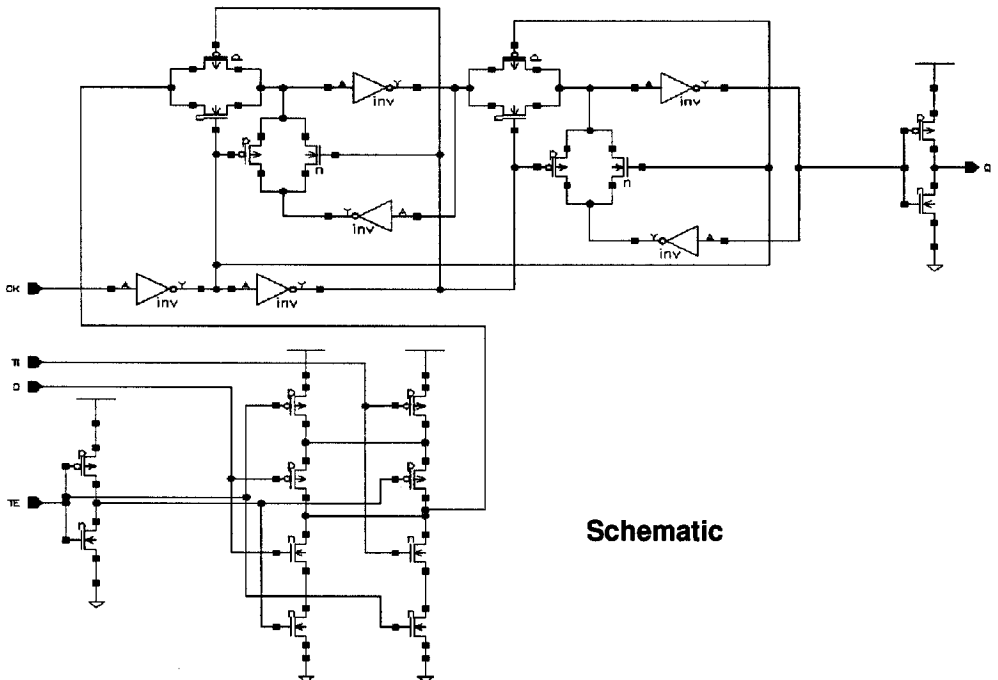
- FD1SD2Q: 9
- FD1SD4Q: 10



**Symbol**

D	TI	TE	CK	Q <sub>n+1</sub>
0	x	0		0
1	x	0		1
x	0	1		0
x	1	1		1
x	x	x		Q <sub>n</sub>

**Truth Table**



**Schematic**

**FD1SD2Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.54	$0.50 + 0.023*SL$	$0.50 + 0.022*SL$	$0.50 + 0.022*SL$
	tPHL	0.55	$0.52 + 0.018*SL$	$0.53 + 0.012*SL$	$0.57 + 0.010*SL$
	tR	0.22	$0.12 + 0.050*SL$	$0.11 + 0.051*SL$	$0.09 + 0.052*SL$
	tF	0.16	$0.12 + 0.021*SL$	$0.13 + 0.019*SL$	$0.11 + 0.020*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD1SD2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.616
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.670

**FD1SD4Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.59	$0.56 + 0.012*SL$	$0.57 + 0.011*SL$	$0.57 + 0.011*SL$
	tPHL	0.60	$0.58 + 0.011*SL$	$0.59 + 0.008*SL$	$0.63 + 0.006*SL$
	tR	0.18	$0.14 + 0.024*SL$	$0.13 + 0.025*SL$	$0.12 + 0.026*SL$
	tF	0.19	$0.17 + 0.010*SL$	$0.17 + 0.010*SL$	$0.17 + 0.010*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD1SD4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.616
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.670

# FD1X4

## 4-Bit D Flip-Flop with Positive Edge Trigger

Inputs: D0, D1, D2, D3, CK

Outputs: Q0, Q1, Q2, Q3,  
QN0, QN1, QN2, QN3

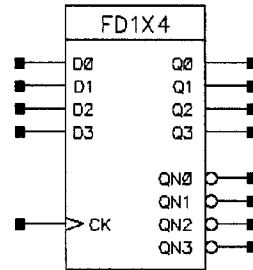
Input Loading (SL):

- D0, D1, D2, D3: 3

- CK: 1

Maximum Fanout (Rec. SL): All : 28

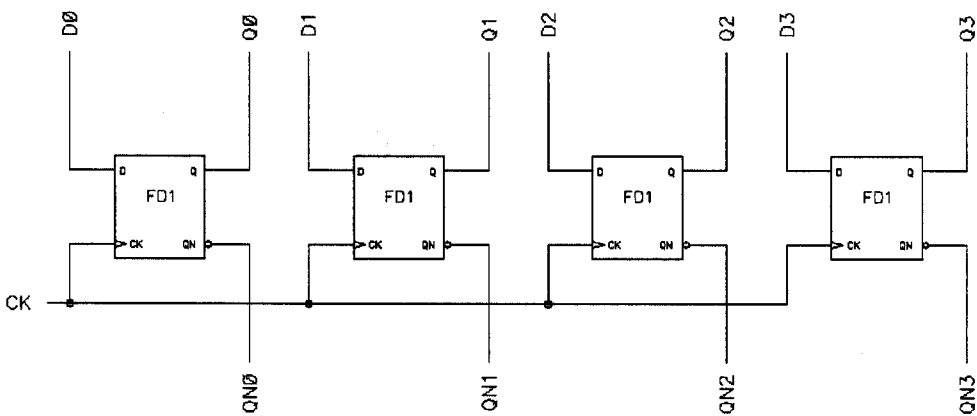
Gate Count: 21



**Symbol**

D	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0		0	1
1		1	0
x		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FD1X4 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	tPLH	1.01	$0.93 + 0.041*SL$	$0.93 + 0.041*SL$	$0.93 + 0.041*SL$
	tPHL	0.80	$0.75 + 0.026*SL$	$0.77 + 0.021*SL$	$0.78 + 0.020*SL$
	tR	0.29	$0.10 + 0.093*SL$	$0.09 + 0.096*SL$	$0.08 + 0.097*SL$
	tF	0.17	$0.09 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
CK to Q1	tPLH	1.02	$0.94 + 0.041*SL$	$0.94 + 0.043*SL$	$0.93 + 0.043*SL$
	tPHL	0.81	$0.76 + 0.027*SL$	$0.78 + 0.021*SL$	$0.79 + 0.020*SL$
	tR	0.30	$0.10 + 0.099*SL$	$0.09 + 0.102*SL$	$0.08 + 0.102*SL$
	tF	0.17	$0.10 + 0.035*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
CK to Q2	tPLH	1.02	$0.94 + 0.041*SL$	$0.94 + 0.043*SL$	$0.93 + 0.043*SL$
	tPHL	0.81	$0.76 + 0.027*SL$	$0.78 + 0.021*SL$	$0.79 + 0.020*SL$
	tR	0.30	$0.10 + 0.099*SL$	$0.09 + 0.102*SL$	$0.08 + 0.102*SL$
	tF	0.17	$0.10 + 0.035*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
CK to Q3	tPLH	1.01	$0.93 + 0.041*SL$	$0.93 + 0.041*SL$	$0.93 + 0.041*SL$
	tPHL	0.80	$0.75 + 0.026*SL$	$0.77 + 0.021*SL$	$0.78 + 0.020*SL$
	tR	0.29	$0.10 + 0.093*SL$	$0.09 + 0.096*SL$	$0.08 + 0.097*SL$
	tF	0.17	$0.09 + 0.036*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
CK to QN0	tPLH	0.74	$0.65 + 0.043*SL$	$0.65 + 0.043*SL$	$0.65 + 0.043*SL$
	tPHL	0.87	$0.82 + 0.027*SL$	$0.83 + 0.021*SL$	$0.86 + 0.020*SL$
	tR	0.31	$0.11 + 0.099*SL$	$0.10 + 0.102*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.038*SL$	$0.11 + 0.037*SL$	$0.07 + 0.039*SL$
CK to QN1	tPLH	0.75	$0.66 + 0.044*SL$	$0.66 + 0.043*SL$	$0.66 + 0.043*SL$
	tPHL	0.87	$0.82 + 0.027*SL$	$0.84 + 0.021*SL$	$0.86 + 0.020*SL$
	tR	0.31	$0.11 + 0.099*SL$	$0.10 + 0.102*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.038*SL$	$0.11 + 0.037*SL$	$0.08 + 0.039*SL$
CK to QN2	tPLH	0.75	$0.66 + 0.044*SL$	$0.66 + 0.043*SL$	$0.66 + 0.043*SL$
	tPHL	0.87	$0.82 + 0.027*SL$	$0.84 + 0.021*SL$	$0.86 + 0.020*SL$
	tR	0.31	$0.11 + 0.099*SL$	$0.10 + 0.102*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.038*SL$	$0.11 + 0.037*SL$	$0.08 + 0.039*SL$
CK to QN3	tPLH	0.74	$0.65 + 0.043*SL$	$0.65 + 0.043*SL$	$0.65 + 0.043*SL$
	tPHL	0.87	$0.82 + 0.027*SL$	$0.83 + 0.021*SL$	$0.86 + 0.020*SL$
	tR	0.31	$0.11 + 0.099*SL$	$0.10 + 0.102*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.038*SL$	$0.11 + 0.037*SL$	$0.07 + 0.039*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD1X4 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920

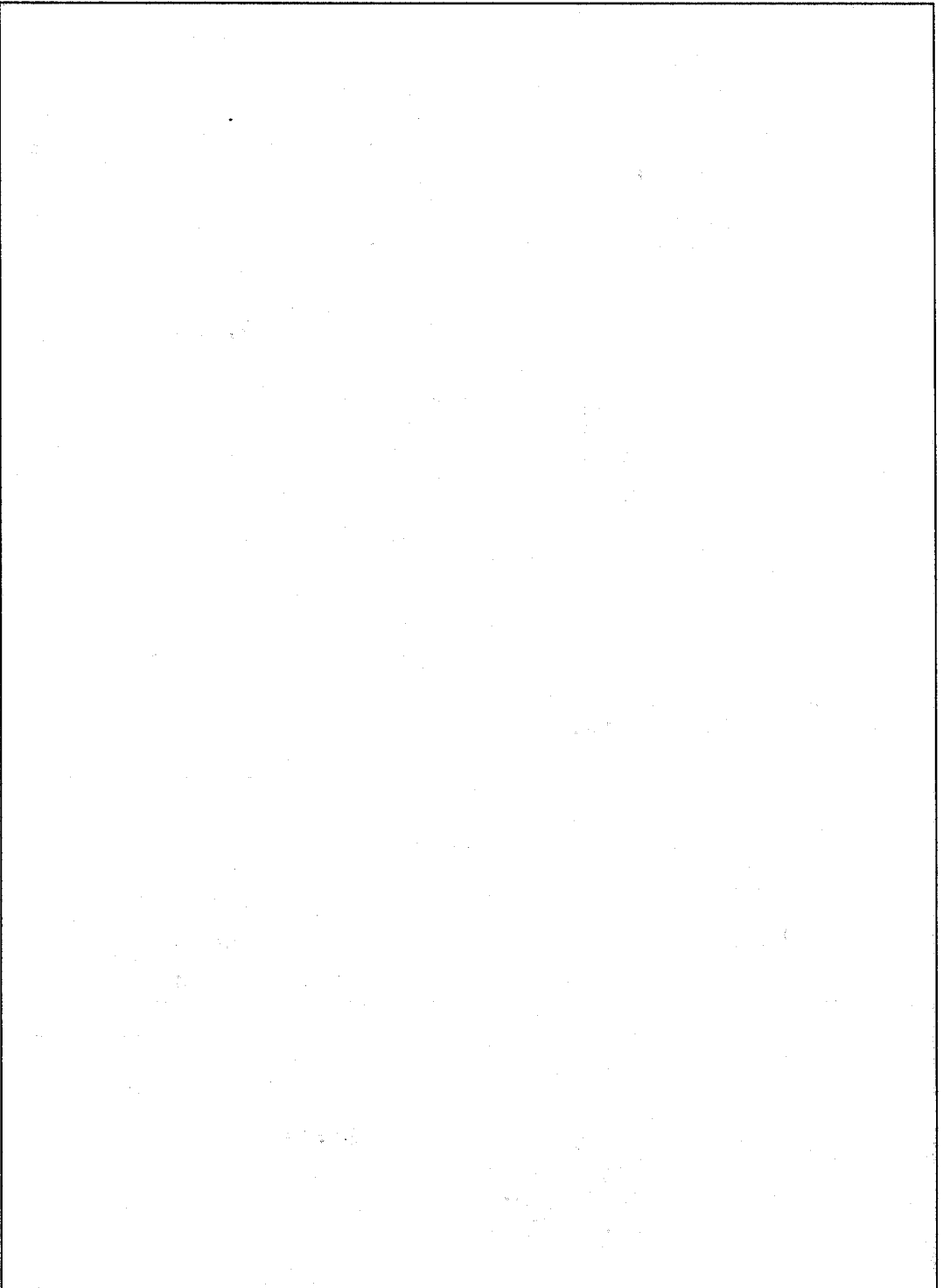
# FD1X4

## 4-Bit D Flip-Flop with Positive Edge Trigger

### FD1X4 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D0 to CK)	tHD	0.452
Input Hold Time (D1 to CK)	tHD	0.452
Input Hold Time (D2 to CK)	tHD	0.452
Input Hold Time (D3 to CK)	tHD	0.452
Input Setup Time (D0 to CK)	tSU	0.233
Input Setup Time (D1 to CK)	tSU	0.233
Input Setup Time (D2 to CK)	tSU	0.233
Input Setup Time (D3 to CK)	tSU	0.233



# FD1D2X4Q/FD1D4X4Q

4-Bit D Flip-Flop, Positive Edge Trigger, Q Output Only, with 2X Drive or 4X Drive

Inputs: D0, D1, D2, D3, CK

Output: Q0, Q1, Q2, Q3

Input Loading (SL): All: D0, D1, D2, D3: 3

CK: 1

Maximum Fanout (Rec. SL):

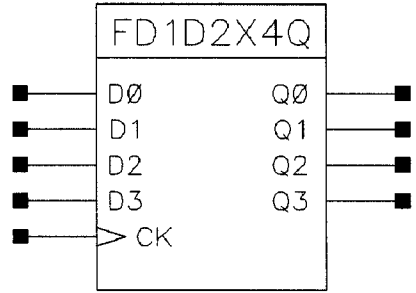
- FD1D2XQ: 56

- FD1D4XQ: 112

Gate Count:

- FD1D2X4Q: 21

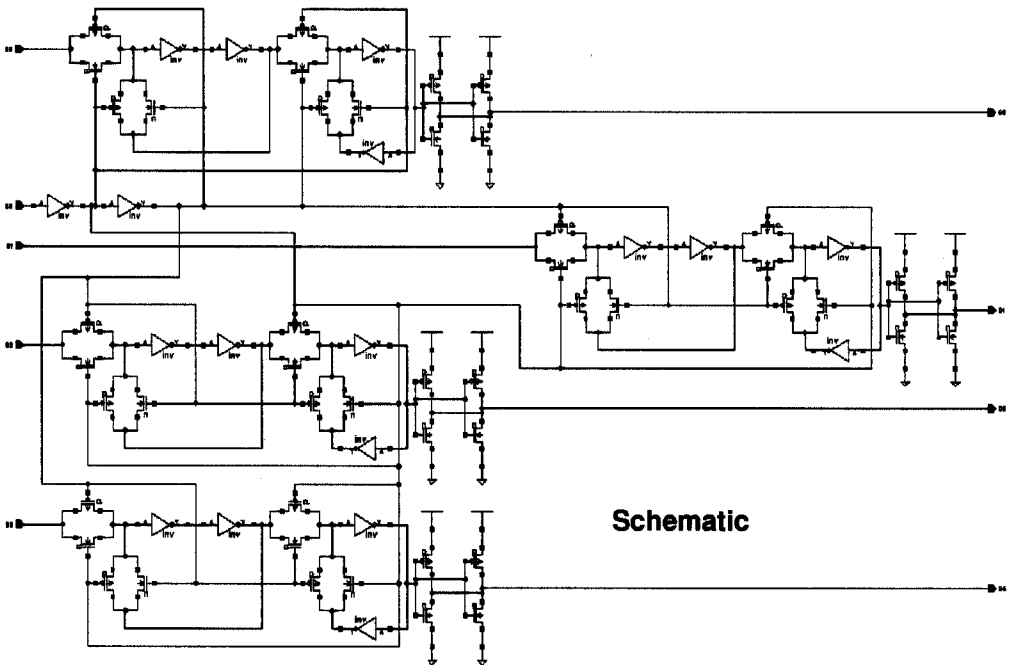
- FD1D4X4Q: 25



**Symbol**

D	CK	Q <sub>n+1</sub>
0		0
1		1
x		Q <sub>n</sub>

**Truth Table**



**Schematic**

**FD1D2X4Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	tPLH	0.83	$0.78 + 0.024 * SL$	$0.79 + 0.022 * SL$	$0.80 + 0.021 * SL$
	tPHL	0.68	$0.64 + 0.023 * SL$	$0.66 + 0.016 * SL$	$0.73 + 0.012 * SL$
	tR	0.27	$0.17 + 0.048 * SL$	$0.16 + 0.050 * SL$	$0.13 + 0.052 * SL$
	tF	0.26	$0.21 + 0.026 * SL$	$0.22 + 0.021 * SL$	$0.23 + 0.020 * SL$
CK to Q1	tPLH	0.82	$0.78 + 0.024 * SL$	$0.78 + 0.021 * SL$	$0.79 + 0.020 * SL$
	tPHL	0.68	$0.63 + 0.023 * SL$	$0.66 + 0.015 * SL$	$0.73 + 0.012 * SL$
	tR	0.25	$0.16 + 0.046 * SL$	$0.16 + 0.047 * SL$	$0.13 + 0.049 * SL$
	tF	0.25	$0.20 + 0.025 * SL$	$0.22 + 0.020 * SL$	$0.23 + 0.019 * SL$
CK to Q2	tPLH	0.82	$0.78 + 0.024 * SL$	$0.78 + 0.021 * SL$	$0.79 + 0.020 * SL$
	tPHL	0.68	$0.63 + 0.023 * SL$	$0.66 + 0.015 * SL$	$0.73 + 0.012 * SL$
	tR	0.25	$0.16 + 0.046 * SL$	$0.16 + 0.047 * SL$	$0.13 + 0.049 * SL$
	tF	0.25	$0.20 + 0.025 * SL$	$0.22 + 0.020 * SL$	$0.23 + 0.019 * SL$
CK to Q3	tPLH	0.83	$0.78 + 0.024 * SL$	$0.79 + 0.022 * SL$	$0.80 + 0.021 * SL$
	tPHL	0.68	$0.64 + 0.023 * SL$	$0.66 + 0.016 * SL$	$0.73 + 0.012 * SL$
	tR	0.27	$0.17 + 0.048 * SL$	$0.16 + 0.050 * SL$	$0.13 + 0.052 * SL$
	tF	0.26	$0.21 + 0.026 * SL$	$0.22 + 0.021 * SL$	$0.23 + 0.020 * SL$

\*Range1 : SL < 3.00, \*Range2 : 3.00 ≤ SL ≤ 20.00, \*Range3 : 20.00 < SL

**FD1D2X4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.959
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D0 to CK)	tHD	0.452
Input Hold Time (D1 to CK)	tHD	0.452
Input Hold Time (D2 to CK)	tHD	0.452
Input Hold Time (D3 to CK)	tHD	0.452
Input Setup Time (D0 to CK)	tSU	0.233
Input Setup Time (D1 to CK)	tSU	0.233
Input Setup Time (D2 to CK)	tSU	1.655
Input Setup Time (D3 to CK)	tSU	0.233



# FD1D4X4Q

4-Bit D Flip-Flop, Positive Edge Trigger, Q Output Only, with 4X Drive

## FD1D4X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

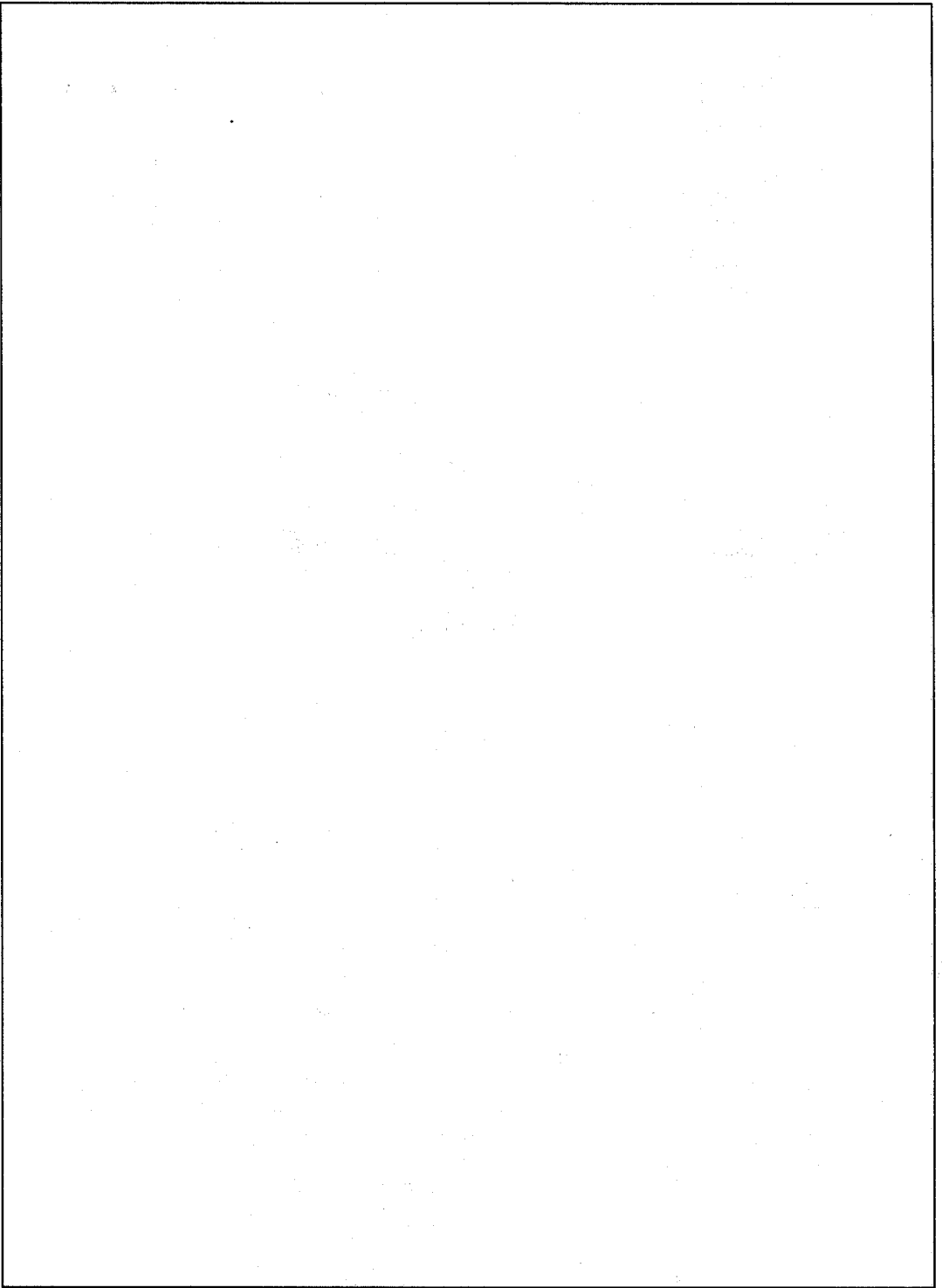
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	tPLH	0.88	$0.85 + 0.014 \cdot SL$	$0.86 + 0.011 \cdot SL$	$0.87 + 0.011 \cdot SL$
	tPHL	0.78	$0.75 + 0.014 \cdot SL$	$0.76 + 0.010 \cdot SL$	$0.81 + 0.008 \cdot SL$
	tR	0.25	$0.21 + 0.021 \cdot SL$	$0.20 + 0.024 \cdot SL$	$0.18 + 0.025 \cdot SL$
	tF	0.31	$0.28 + 0.014 \cdot SL$	$0.29 + 0.011 \cdot SL$	$0.32 + 0.010 \cdot SL$
CK to Q1	tPLH	0.88	$0.85 + 0.014 \cdot SL$	$0.86 + 0.011 \cdot SL$	$0.87 + 0.010 \cdot SL$
	tPHL	0.79	$0.76 + 0.014 \cdot SL$	$0.77 + 0.010 \cdot SL$	$0.82 + 0.008 \cdot SL$
	tR	0.24	$0.20 + 0.019 \cdot SL$	$0.19 + 0.022 \cdot SL$	$0.18 + 0.023 \cdot SL$
	tF	0.31	$0.28 + 0.014 \cdot SL$	$0.29 + 0.011 \cdot SL$	$0.32 + 0.010 \cdot SL$
CK to Q2	tPLH	0.88	$0.85 + 0.014 \cdot SL$	$0.86 + 0.011 \cdot SL$	$0.87 + 0.010 \cdot SL$
	tPHL	0.79	$0.76 + 0.014 \cdot SL$	$0.77 + 0.010 \cdot SL$	$0.82 + 0.008 \cdot SL$
	tR	0.24	$0.20 + 0.019 \cdot SL$	$0.19 + 0.022 \cdot SL$	$0.18 + 0.023 \cdot SL$
	tF	0.31	$0.28 + 0.014 \cdot SL$	$0.29 + 0.011 \cdot SL$	$0.32 + 0.010 \cdot SL$
CK to Q3	tPLH	0.88	$0.85 + 0.014 \cdot SL$	$0.86 + 0.011 \cdot SL$	$0.87 + 0.011 \cdot SL$
	tPHL	0.78	$0.75 + 0.014 \cdot SL$	$0.76 + 0.010 \cdot SL$	$0.81 + 0.008 \cdot SL$
	tR	0.25	$0.21 + 0.020 \cdot SL$	$0.20 + 0.024 \cdot SL$	$0.18 + 0.025 \cdot SL$
	tF	0.31	$0.28 + 0.014 \cdot SL$	$0.29 + 0.011 \cdot SL$	$0.32 + 0.010 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD1D4X4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.959
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D0 to CK)	tHD	0.452
Input Hold Time (D1 to CK)	tHD	0.452
Input Hold Time (D2 to CK)	tHD	0.452
Input Hold Time (D3 to CK)	tHD	0.452
Input Setup Time (D0 to CK)	tSU	0.178
Input Setup Time (D1 to CK)	tSU	0.178
Input Setup Time (D2 to CK)	tSU	0.178
Input Setup Time (D3 to CK)	tSU	0.178



# FD2/FD2D2

D Flip-Flop with Reset, 1X Drive or 2X Drive

Inputs: D, CK, RN

Outputs: Q, QN

Input Loading (SL):

- D: 3

- CK: 1

- RN: 2

Maximum Fanout (Rec. SL):

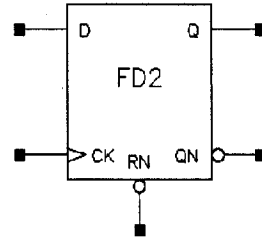
- FD2: All : 28

- FD2D2: All : 56

Gate Count:

- FD2: 7

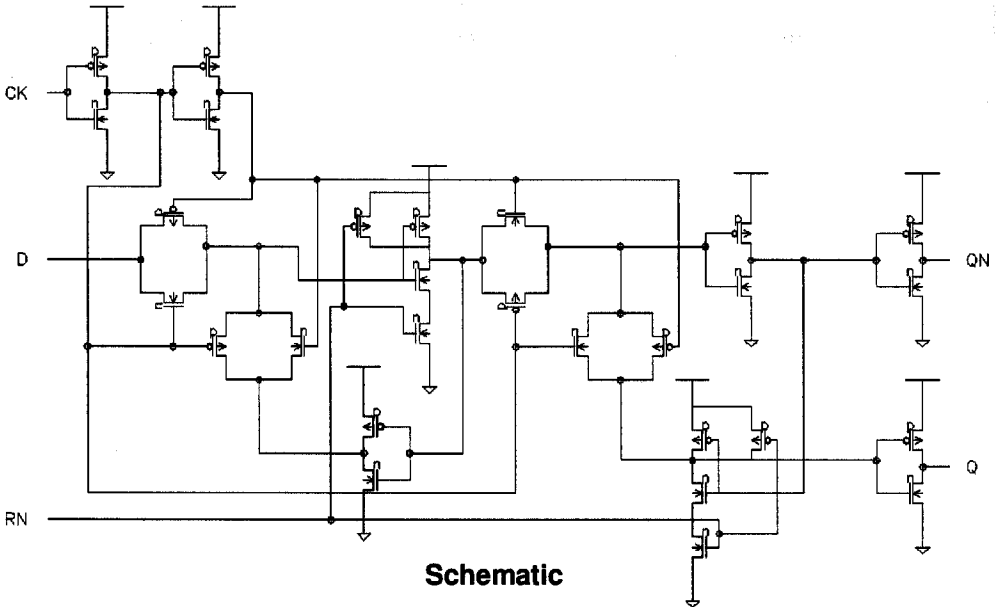
- FD2D2: 8



**Symbol**

D	RN	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1		0	1
1	1		1	0
x	0	x	0	1
x	1		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FD2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{rj}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.82	$0.74 + 0.039*SL$	$0.74 + 0.040*SL$	$0.74 + 0.040*SL$
	tPHL	0.65	$0.60 + 0.027*SL$	$0.62 + 0.021*SL$	$0.64 + 0.020*SL$
	tR	0.30	$0.12 + 0.089*SL$	$0.11 + 0.091*SL$	$0.09 + 0.093*SL$
	tF	0.17	$0.10 + 0.038*SL$	$0.10 + 0.037*SL$	$0.07 + 0.038*SL$
RN to Q	tPHL	0.45	$0.39 + 0.030*SL$	$0.42 + 0.021*SL$	$0.45 + 0.020*SL$
	tF	0.22	$0.15 + 0.032*SL$	$0.14 + 0.035*SL$	$0.09 + 0.038*SL$
CK to QN	tPLH	0.56	$0.48 + 0.040*SL$	$0.48 + 0.040*SL$	$0.48 + 0.040*SL$
	tPHL	0.60	$0.54 + 0.028*SL$	$0.56 + 0.021*SL$	$0.59 + 0.020*SL$
	tR	0.28	$0.11 + 0.088*SL$	$0.10 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.18	$0.11 + 0.034*SL$	$0.10 + 0.037*SL$	$0.08 + 0.038*SL$
RN to QN	tPLH	0.77	$0.69 + 0.040*SL$	$0.69 + 0.040*SL$	$0.69 + 0.040*SL$
	tR	0.29	$0.11 + 0.088*SL$	$0.10 + 0.092*SL$	$0.08 + 0.092*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD2 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.178
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (RN)	tRC	0.139

# FD2D2

## D Flip-Flop with Reset with 2X Drive

### FD2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

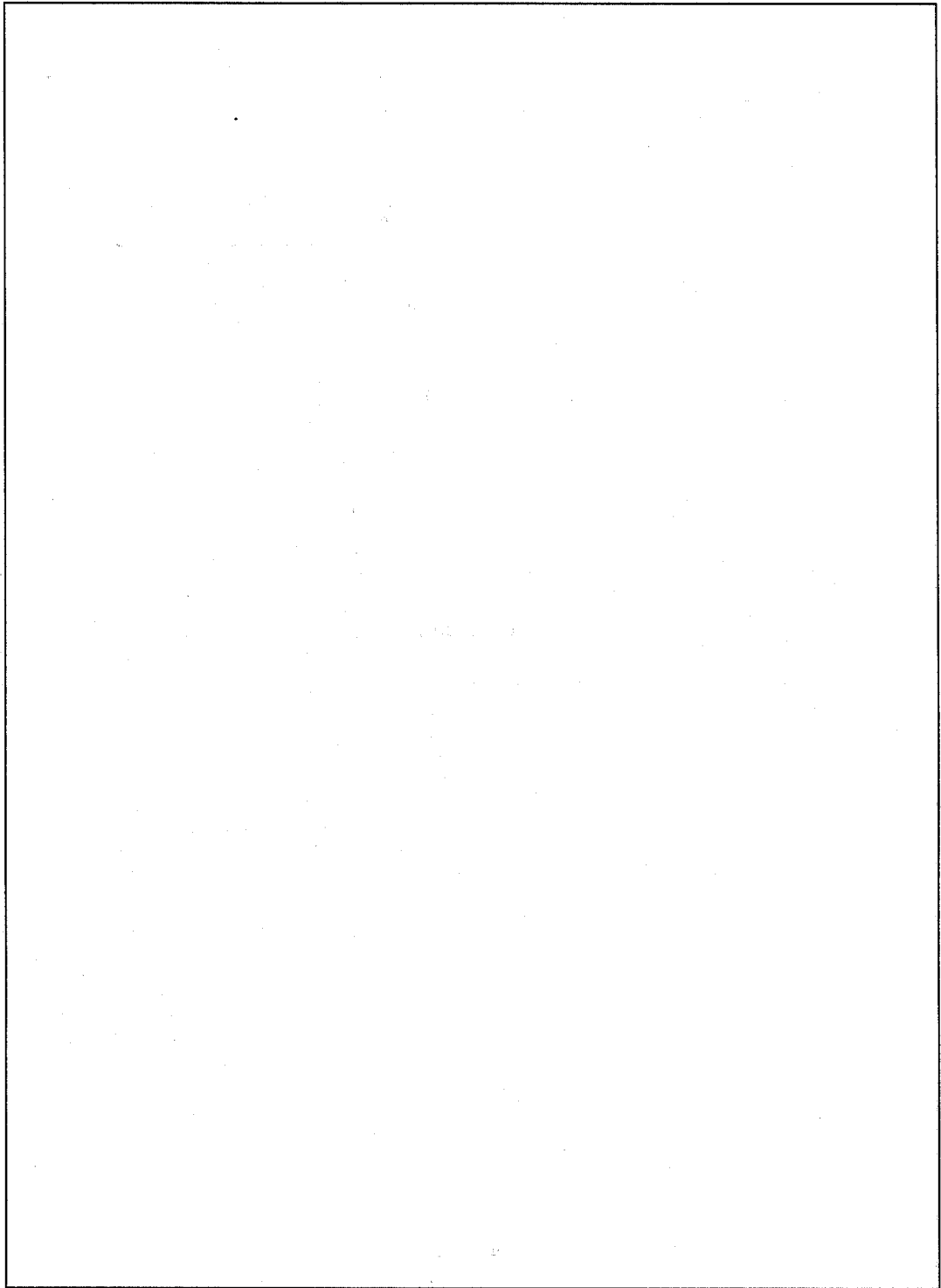
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.88	$0.84 + 0.020*SL$	$0.84 + 0.020*SL$	$0.84 + 0.020*SL$
	tPHL	0.70	$0.67 + 0.017*SL$	$0.68 + 0.012*SL$	$0.72 + 0.010*SL$
	tR	0.22	$0.14 + 0.043*SL$	$0.13 + 0.045*SL$	$0.10 + 0.047*SL$
	tF	0.16	$0.12 + 0.021*SL$	$0.13 + 0.018*SL$	$0.11 + 0.019*SL$
RN to Q	tPHL	0.46	$0.42 + 0.019*SL$	$0.44 + 0.012*SL$	$0.48 + 0.010*SL$
	tF	0.20	$0.17 + 0.018*SL$	$0.17 + 0.017*SL$	$0.14 + 0.018*SL$
CK to QN	tPLH	0.56	$0.51 + 0.021*SL$	$0.52 + 0.020*SL$	$0.52 + 0.020*SL$
	tPHL	0.61	$0.58 + 0.018*SL$	$0.59 + 0.012*SL$	$0.63 + 0.010*SL$
	tR	0.20	$0.12 + 0.043*SL$	$0.11 + 0.046*SL$	$0.09 + 0.047*SL$
	tF	0.17	$0.13 + 0.020*SL$	$0.13 + 0.018*SL$	$0.12 + 0.019*SL$
RN to QN	tPLH	0.77	$0.73 + 0.020*SL$	$0.73 + 0.020*SL$	$0.73 + 0.020*SL$
	tR	0.21	$0.12 + 0.043*SL$	$0.11 + 0.046*SL$	$0.09 + 0.047*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### FD2D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.178
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (RN)	tRC	0.139



# FD2D2Q/FD2D4Q

D Flip-Flop with Reset with Q Output Only, 2X Drive or 4X Drive

Inputs: D, CK, RN

Output: Q

Input Loading (SL):

- FD2D2Q: D: 3, CK: 1, RN: 2

- FD2D4Q: D: 3, CK: 1, RN: 2

Maximum Fanout (Rec. SL):

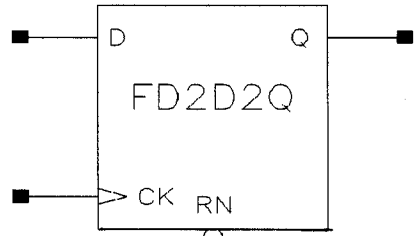
- FD2D2Q: 56

- FD2D4Q: 112

Gate Count:

- FD2D2Q: 7

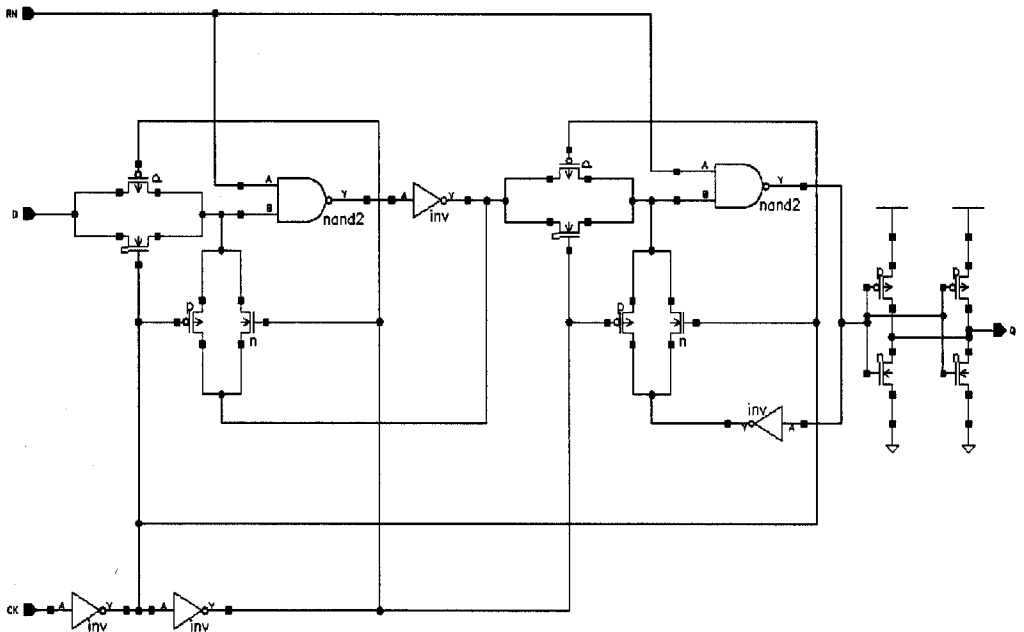
- FD2D4Q: 8



Symbol

D	RN	CK	Q <sub>n+1</sub>
0	1		0
1	1		1
x	0	x	0
x	1		Q <sub>n</sub>

Truth Table



Schematic

**FD2D2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{rj}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.57	$0.51 + 0.027*SL$	$0.53 + 0.022*SL$	$0.56 + 0.020*SL$
	tPHL	0.44	$0.40 + 0.022*SL$	$0.42 + 0.016*SL$	$0.49 + 0.012*SL$
	tR	0.29	$0.20 + 0.044*SL$	$0.20 + 0.045*SL$	$0.18 + 0.047*SL$
	tF	0.21	$0.16 + 0.027*SL$	$0.17 + 0.021*SL$	$0.21 + 0.019*SL$
RN to Q	tPHL	0.65	$0.60 + 0.025*SL$	$0.63 + 0.016*SL$	$0.72 + 0.012*SL$
	tF	0.30	$0.25 + 0.025*SL$	$0.27 + 0.018*SL$	$0.28 + 0.018*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD2D2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.233
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (RN)	tRC	0.139

**FD2D4Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{rj}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.64	$0.61 + 0.016*SL$	$0.62 + 0.012*SL$	$0.65 + 0.011*SL$
	tPHL	0.48	$0.45 + 0.014*SL$	$0.47 + 0.010*SL$	$0.51 + 0.008*SL$
	tR	0.31	$0.27 + 0.019*SL$	$0.27 + 0.021*SL$	$0.24 + 0.022*SL$
	tF	0.23	$0.20 + 0.015*SL$	$0.21 + 0.013*SL$	$0.25 + 0.011*SL$
RN to Q	tPHL	0.71	$0.68 + 0.015*SL$	$0.70 + 0.010*SL$	$0.75 + 0.007*SL$
	tF	0.32	$0.29 + 0.013*SL$	$0.30 + 0.010*SL$	$0.33 + 0.009*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD2D4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.233
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (RN)	tRC	0.178



# FD2S/FD2SD2

D Flip-Flop with Scan and Reset, Positive Edge Trigger, 1X Drive or 2X Drive

Inputs: D, TI, TE, CK, RN

Outputs: Q, QN

Input Loading (SL):

- D, TI, CK: 1

- TE, RN: 2

Maximum Fanout (Rec. SL):

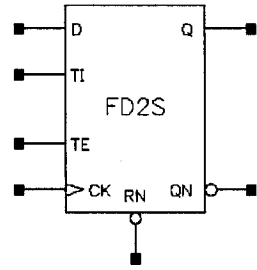
- FD2S: All : 28

- D2SD2: All : 56

Gate Count:

- FD2S: 10

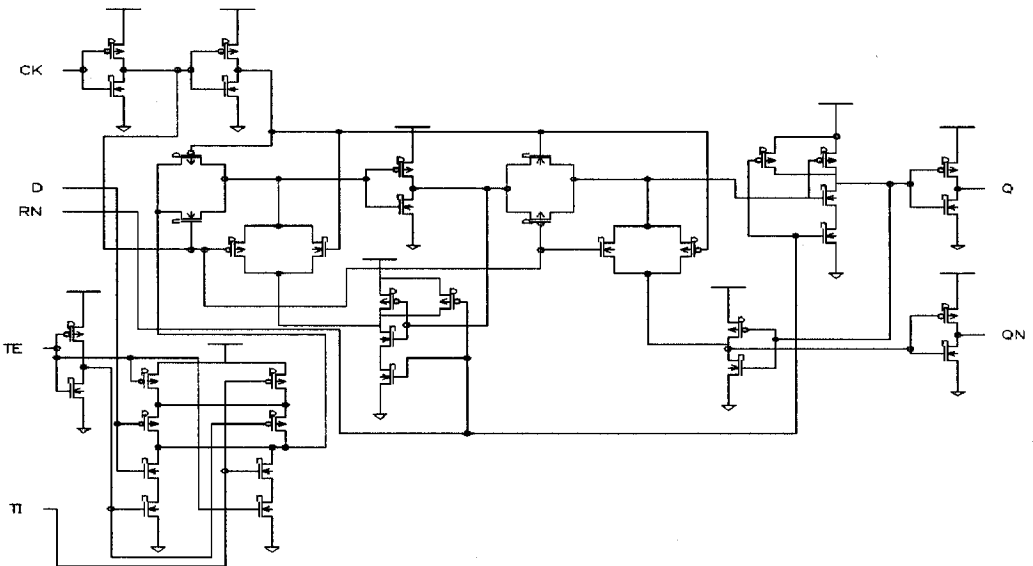
- FD2SD2: 10



**Symbol**

D	RN	TI	TE	CK	Qn+1	QNn+1
0	1	x	0		0	1
1	1	x	0		1	0
x	1	0	1		0	1
x	1	1	1		1	0
x	0	x	x	x	0	1
x	1	x	x		Qn	QNn

**Truth Table**



**Schematic**

**FD2S Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.64	$0.56 + 0.042*SL$	$0.56 + 0.040*SL$	$0.57 + 0.040*SL$
	tPHL	0.57	$0.51 + 0.029*SL$	$0.53 + 0.022*SL$	$0.56 + 0.020*SL$
	tR	0.30	$0.13 + 0.089*SL$	$0.12 + 0.090*SL$	$0.10 + 0.091*SL$
	tF	0.19	$0.10 + 0.041*SL$	$0.11 + 0.039*SL$	$0.08 + 0.041*SL$
RN to Q	tPHL	0.46	$0.40 + 0.032*SL$	$0.43 + 0.022*SL$	$0.47 + 0.020*SL$
	tF	0.23	$0.16 + 0.037*SL$	$0.15 + 0.038*SL$	$0.10 + 0.040*SL$
CK to QN	tPLH	0.71	$0.63 + 0.039*SL$	$0.63 + 0.039*SL$	$0.63 + 0.040*SL$
	tPHL	0.72	$0.67 + 0.026*SL$	$0.69 + 0.021*SL$	$0.70 + 0.020*SL$
	tR	0.28	$0.10 + 0.087*SL$	$0.09 + 0.091*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.10 + 0.035*SL$	$0.09 + 0.038*SL$	$0.07 + 0.039*SL$
RN to QN	tPLH	0.61	$0.53 + 0.038*SL$	$0.53 + 0.039*SL$	$0.52 + 0.040*SL$
	tR	0.28	$0.10 + 0.087*SL$	$0.09 + 0.091*SL$	$0.08 + 0.092*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD2S Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.616
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.670
Recovery Time (RN)	tRC	0.139

# FD2SD2

D Flip-Flop with Scan and Reset, Positive Edge Trigger, 2X Drive

## FD2SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_q$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

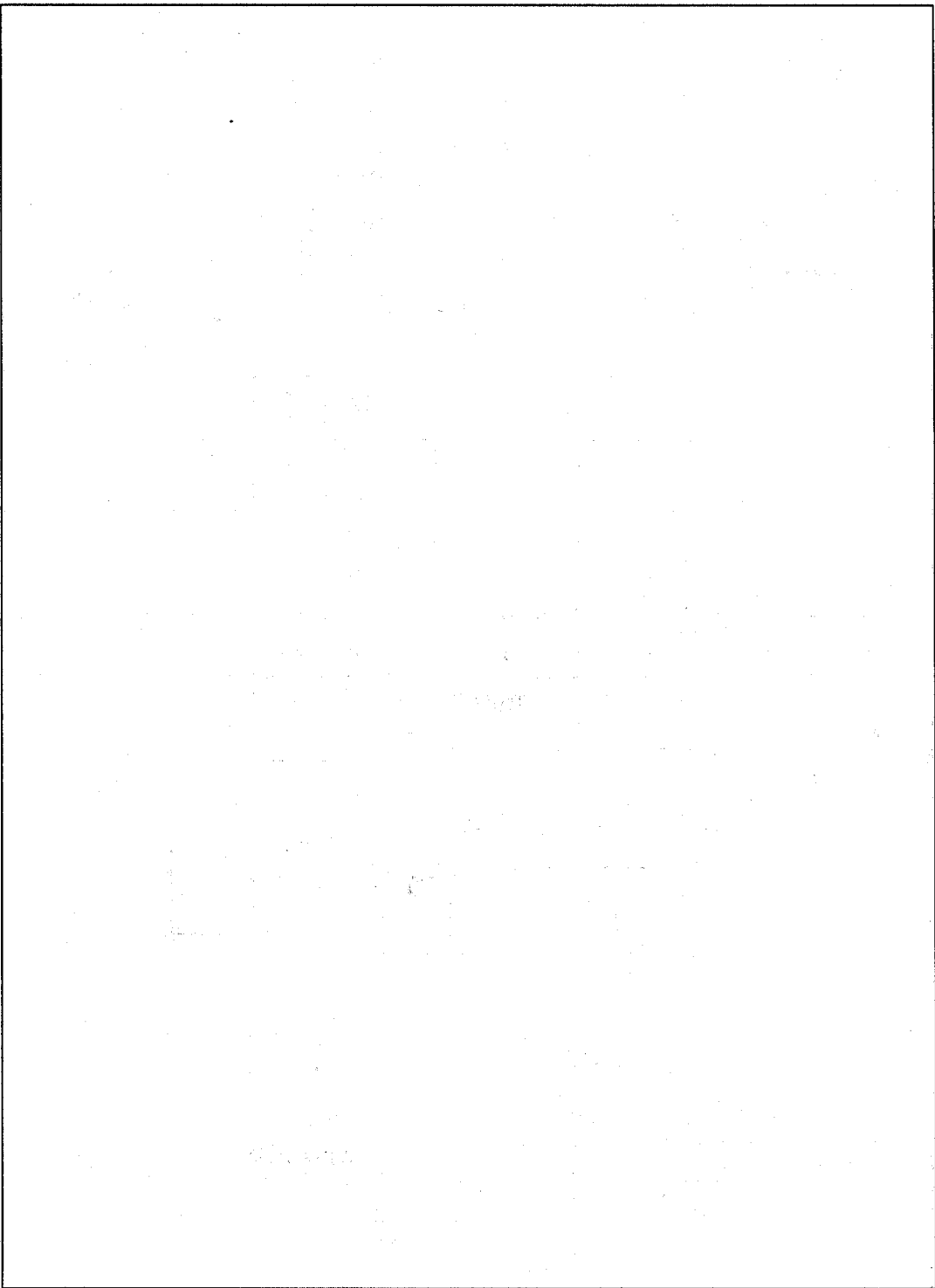
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.64	$0.60 + 0.023 * SL$	$0.61 + 0.020 * SL$	$0.61 + 0.020 * SL$
	tPHL	0.57	$0.54 + 0.018 * SL$	$0.55 + 0.013 * SL$	$0.59 + 0.011 * SL$
	tR	0.23	$0.14 + 0.042 * SL$	$0.14 + 0.045 * SL$	$0.11 + 0.046 * SL$
	tF	0.17	$0.12 + 0.021 * SL$	$0.13 + 0.019 * SL$	$0.12 + 0.020 * SL$
RN to Q	tPHL	0.47	$0.43 + 0.019 * SL$	$0.45 + 0.013 * SL$	$0.50 + 0.010 * SL$
	tF	0.21	$0.17 + 0.019 * SL$	$0.18 + 0.018 * SL$	$0.16 + 0.019 * SL$
CK to QN	tPLH	0.75	$0.72 + 0.018 * SL$	$0.71 + 0.019 * SL$	$0.70 + 0.020 * SL$
	tPHL	0.78	$0.75 + 0.015 * SL$	$0.76 + 0.012 * SL$	$0.79 + 0.010 * SL$
	tR	0.20	$0.11 + 0.042 * SL$	$0.10 + 0.045 * SL$	$0.08 + 0.046 * SL$
	tF	0.16	$0.12 + 0.019 * SL$	$0.13 + 0.018 * SL$	$0.11 + 0.019 * SL$
RN to QN	tPLH	0.65	$0.61 + 0.018 * SL$	$0.61 + 0.019 * SL$	$0.60 + 0.020 * SL$
	tR	0.20	$0.12 + 0.041 * SL$	$0.10 + 0.045 * SL$	$0.08 + 0.046 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD2SD2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.616
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.670
Recovery Time (RN)	tRC	0.139



# FD2SD2Q/FD2SD4Q

D Flip-Flop with Scan and Reset, Positive Edge-Trigger, Q Output Only, 2X or 4X Drive

Inputs: D, TI, TE, CK, RN

Output: Q

Input Loading (SL):

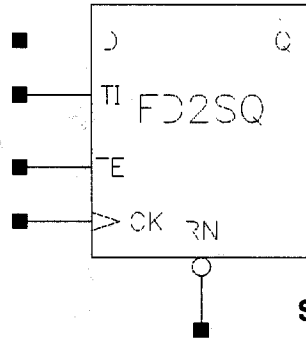
- FD2SD2Q: D: 1, CK: 1, RN: 2, TI: 1, TE: 2
- FD2SD4Q: D: 1, CK: 1, RN: 2, TI: 1, TE: 2

Maximum Fanout (Rec. SL):

- FD2SD2Q: 56
- FD2SD4Q: 112

Gate Count:

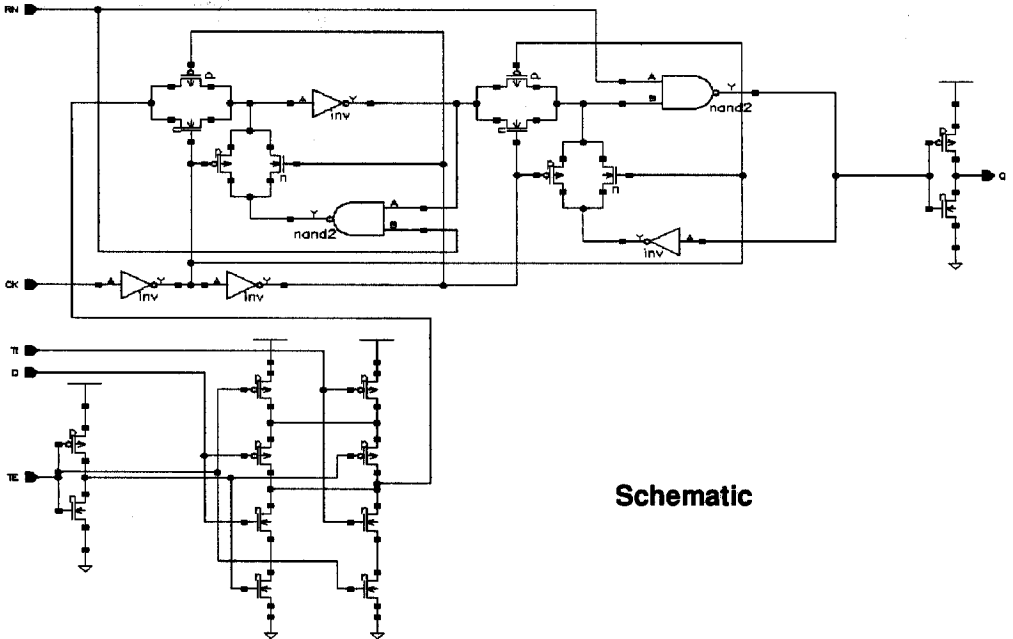
- FD2SD2Q: 10
- FD2SD4Q: 11



Symbol

D	RN	TI	TE	CK	Q <sub>n+1</sub>
0	1	x	0		0
1	1	x	0		1
x	1	0	1		0
x	1	1	1		1
x	0	x	x	x	0
x	1	x	x		Q <sub>n</sub>

Truth Table



Schematic

**FD2SD2Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.64	$0.59 + 0.023 \cdot SL$	$0.60 + 0.021 \cdot SL$	$0.60 + 0.020 \cdot SL$
	tPHL	0.58	$0.54 + 0.018 \cdot SL$	$0.56 + 0.012 \cdot SL$	$0.60 + 0.010 \cdot SL$
	tR	0.23	$0.13 + 0.046 \cdot SL$	$0.13 + 0.046 \cdot SL$	$0.11 + 0.047 \cdot SL$
	tF	0.17	$0.13 + 0.019 \cdot SL$	$0.13 + 0.018 \cdot SL$	$0.13 + 0.019 \cdot SL$
RN to Q	tPHL	0.47	$0.43 + 0.020 \cdot SL$	$0.45 + 0.013 \cdot SL$	$0.51 + 0.010 \cdot SL$
	tF	0.21	$0.17 + 0.019 \cdot SL$	$0.18 + 0.017 \cdot SL$	$0.16 + 0.018 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD2SD2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.616
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.670
Recovery Time (RN)	tRC	0.139

# FD2SD4Q

D Flip-Flop with Scan and Reset, Positive Edge Trigger, Q Output Only, 4X Drive

## FD2SD4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

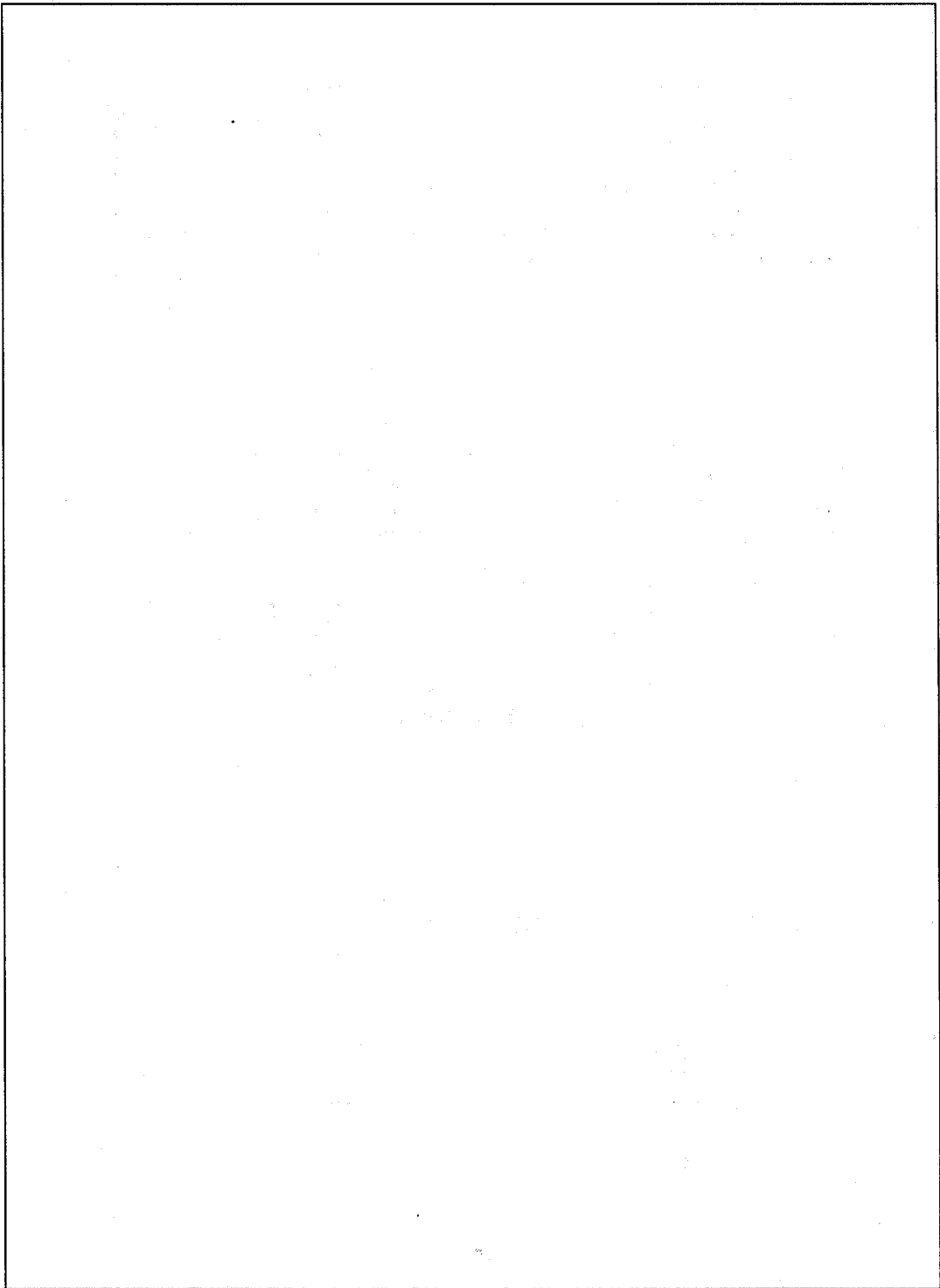
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.71	$0.68 + 0.013 \cdot \text{SL}$	$0.69 + 0.011 \cdot \text{SL}$	$0.70 + 0.010 \cdot \text{SL}$
	tPHL	0.63	$0.61 + 0.011 \cdot \text{SL}$	$0.62 + 0.008 \cdot \text{SL}$	$0.65 + 0.006 \cdot \text{SL}$
	tR	0.22	$0.18 + 0.021 \cdot \text{SL}$	$0.17 + 0.022 \cdot \text{SL}$	$0.16 + 0.023 \cdot \text{SL}$
	tF	0.19	$0.18 + 0.008 \cdot \text{SL}$	$0.17 + 0.009 \cdot \text{SL}$	$0.18 + 0.009 \cdot \text{SL}$
RN to Q	tPHL	0.52	$0.50 + 0.012 \cdot \text{SL}$	$0.51 + 0.008 \cdot \text{SL}$	$0.56 + 0.006 \cdot \text{SL}$
	tF	0.23	$0.21 + 0.010 \cdot \text{SL}$	$0.22 + 0.008 \cdot \text{SL}$	$0.22 + 0.008 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

## FD2SD4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.616
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.670
Recovery Time (RN)	tRC	0.139





# FD2X4

## 4-Bit D Flip-Flop with Reset, Positive Edge Trigger, 1X Drive

Inputs: D0, D1, D2, D3, CK, RN

Outputs: Q0, Q1, Q2, Q3

QN0, QN1, QN2, QN3

Input Loading (SL):

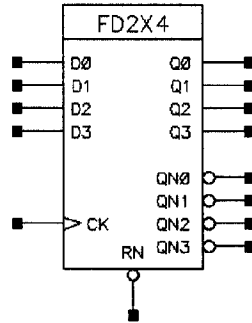
- D0, D1, D2, D3: 3

- CK: 1

- RN: 8

Maximum Fanout (Rec. SL): All : 28

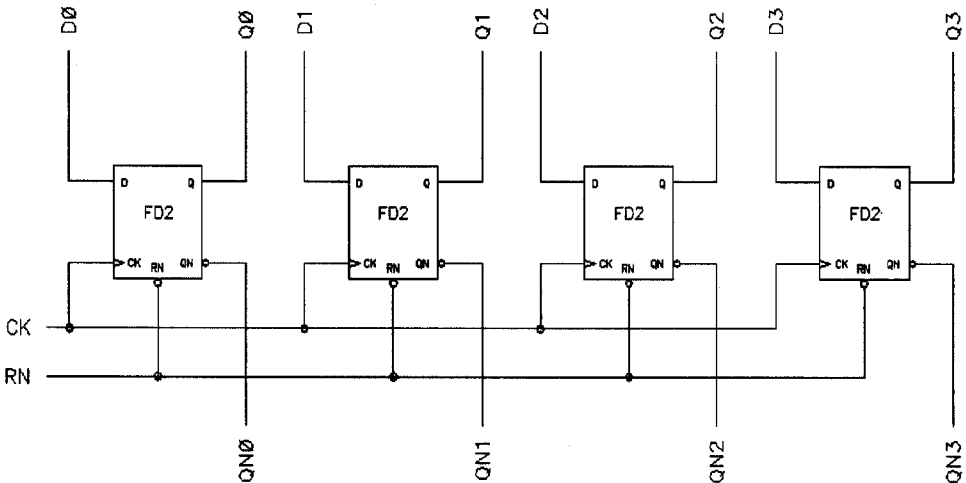
Gate Count: 25



**Symbol**

D	RN	CK	Qn+ 1	QNn+ 1
0	1		0	1
1	1		1	0
x	0	x	0	1
x	1		Qn	QNn

**Truth Table**



**Schematic**

## FD2X4 Switching Characteristics

(Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ )

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q0	tPHL	0.45	$0.39 + 0.030 * SL$	$0.42 + 0.021 * SL$	$0.45 + 0.020 * SL$
	tF	0.22	$0.15 + 0.033 * SL$	$0.14 + 0.035 * SL$	$0.09 + 0.038 * SL$
CK to Q0	tPLH	1.16	$1.08 + 0.039 * SL$	$1.08 + 0.040 * SL$	$1.08 + 0.040 * SL$
	tPHL	0.85	$0.79 + 0.027 * SL$	$0.81 + 0.021 * SL$	$0.83 + 0.020 * SL$
	tR	0.30	$0.12 + 0.087 * SL$	$0.11 + 0.092 * SL$	$0.09 + 0.093 * SL$
	tF	0.18	$0.10 + 0.036 * SL$	$0.10 + 0.037 * SL$	$0.07 + 0.038 * SL$
	tR	0.30	$0.12 + 0.087 * SL$	$0.11 + 0.092 * SL$	$0.09 + 0.093 * SL$
RN to Q1	tPHL	0.45	$0.39 + 0.031 * SL$	$0.42 + 0.022 * SL$	$0.45 + 0.020 * SL$
	tF	0.22	$0.15 + 0.035 * SL$	$0.15 + 0.038 * SL$	$0.09 + 0.041 * SL$
CK to Q1	tPLH	1.17	$1.09 + 0.041 * SL$	$1.08 + 0.042 * SL$	$1.08 + 0.043 * SL$
	tPHL	0.85	$0.79 + 0.028 * SL$	$0.81 + 0.022 * SL$	$0.83 + 0.020 * SL$
	tR	0.32	$0.13 + 0.099 * SL$	$0.12 + 0.101 * SL$	$0.09 + 0.102 * SL$
	tF	0.18	$0.11 + 0.038 * SL$	$0.10 + 0.040 * SL$	$0.07 + 0.041 * SL$
	tR	0.32	$0.13 + 0.099 * SL$	$0.12 + 0.101 * SL$	$0.09 + 0.102 * SL$
RN to Q2	tPHL	0.45	$0.39 + 0.031 * SL$	$0.42 + 0.022 * SL$	$0.45 + 0.020 * SL$
	tF	0.22	$0.15 + 0.035 * SL$	$0.15 + 0.038 * SL$	$0.09 + 0.041 * SL$
CK to Q2	tPLH	1.17	$1.09 + 0.041 * SL$	$1.08 + 0.042 * SL$	$1.08 + 0.043 * SL$
	tPHL	0.85	$0.79 + 0.028 * SL$	$0.81 + 0.022 * SL$	$0.83 + 0.020 * SL$
	tR	0.32	$0.13 + 0.099 * SL$	$0.12 + 0.101 * SL$	$0.09 + 0.102 * SL$
	tF	0.18	$0.11 + 0.038 * SL$	$0.10 + 0.040 * SL$	$0.07 + 0.041 * SL$
	tR	0.32	$0.13 + 0.099 * SL$	$0.12 + 0.101 * SL$	$0.09 + 0.102 * SL$
RN to Q3	tPHL	0.45	$0.39 + 0.030 * SL$	$0.42 + 0.021 * SL$	$0.45 + 0.020 * SL$
	tF	0.22	$0.15 + 0.033 * SL$	$0.14 + 0.035 * SL$	$0.09 + 0.038 * SL$
CK to Q3	tPLH	1.16	$1.08 + 0.039 * SL$	$1.08 + 0.040 * SL$	$1.08 + 0.040 * SL$
	tPHL	0.85	$0.79 + 0.027 * SL$	$0.81 + 0.021 * SL$	$0.83 + 0.020 * SL$
	tR	0.30	$0.12 + 0.087 * SL$	$0.11 + 0.092 * SL$	$0.09 + 0.093 * SL$
	tF	0.18	$0.10 + 0.036 * SL$	$0.10 + 0.037 * SL$	$0.07 + 0.038 * SL$
	tR	0.30	$0.12 + 0.087 * SL$	$0.11 + 0.092 * SL$	$0.09 + 0.093 * SL$
RN to QN0	tPLH	0.77	$0.69 + 0.040 * SL$	$0.69 + 0.040 * SL$	$0.69 + 0.040 * SL$
	tR	0.29	$0.11 + 0.089 * SL$	$0.10 + 0.091 * SL$	$0.08 + 0.092 * SL$
CK to QN0	tPLH	0.75	$0.67 + 0.041 * SL$	$0.67 + 0.040 * SL$	$0.68 + 0.040 * SL$
	tPHL	0.95	$0.89 + 0.027 * SL$	$0.91 + 0.021 * SL$	$0.94 + 0.020 * SL$
	tR	0.28	$0.11 + 0.088 * SL$	$0.10 + 0.092 * SL$	$0.08 + 0.092 * SL$
	tF	0.18	$0.11 + 0.035 * SL$	$0.11 + 0.037 * SL$	$0.08 + 0.038 * SL$
	tR	0.28	$0.11 + 0.088 * SL$	$0.10 + 0.092 * SL$	$0.08 + 0.092 * SL$
RN to QN1	tPLH	0.77	$0.69 + 0.042 * SL$	$0.69 + 0.042 * SL$	$0.68 + 0.042 * SL$
	tR	0.31	$0.11 + 0.099 * SL$	$0.10 + 0.101 * SL$	$0.09 + 0.102 * SL$
CK to QN1	tPLH	0.76	$0.67 + 0.044 * SL$	$0.68 + 0.043 * SL$	$0.68 + 0.043 * SL$
	tPHL	0.94	$0.89 + 0.028 * SL$	$0.91 + 0.022 * SL$	$0.94 + 0.020 * SL$
	tR	0.31	$0.11 + 0.098 * SL$	$0.10 + 0.102 * SL$	$0.09 + 0.102 * SL$
	tF	0.19	$0.11 + 0.037 * SL$	$0.11 + 0.038 * SL$	$0.08 + 0.039 * SL$
	tR	0.31	$0.11 + 0.098 * SL$	$0.10 + 0.102 * SL$	$0.09 + 0.102 * SL$
RN to QN2	tPLH	0.77	$0.69 + 0.042 * SL$	$0.69 + 0.042 * SL$	$0.68 + 0.042 * SL$
	tR	0.31	$0.11 + 0.099 * SL$	$0.10 + 0.101 * SL$	$0.09 + 0.102 * SL$
CK to QN2	tPLH	0.76	$0.67 + 0.044 * SL$	$0.68 + 0.043 * SL$	$0.68 + 0.043 * SL$
	tPHL	0.94	$0.89 + 0.028 * SL$	$0.91 + 0.022 * SL$	$0.94 + 0.020 * SL$
	tR	0.31	$0.11 + 0.098 * SL$	$0.10 + 0.102 * SL$	$0.09 + 0.102 * SL$
	tF	0.19	$0.11 + 0.037 * SL$	$0.11 + 0.038 * SL$	$0.08 + 0.039 * SL$
	tR	0.31	$0.11 + 0.098 * SL$	$0.10 + 0.102 * SL$	$0.09 + 0.102 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# FD2X4

4-Bit D Flip-Flop with Reset, Positive Edge Trigger, 1X Drive

## FD2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

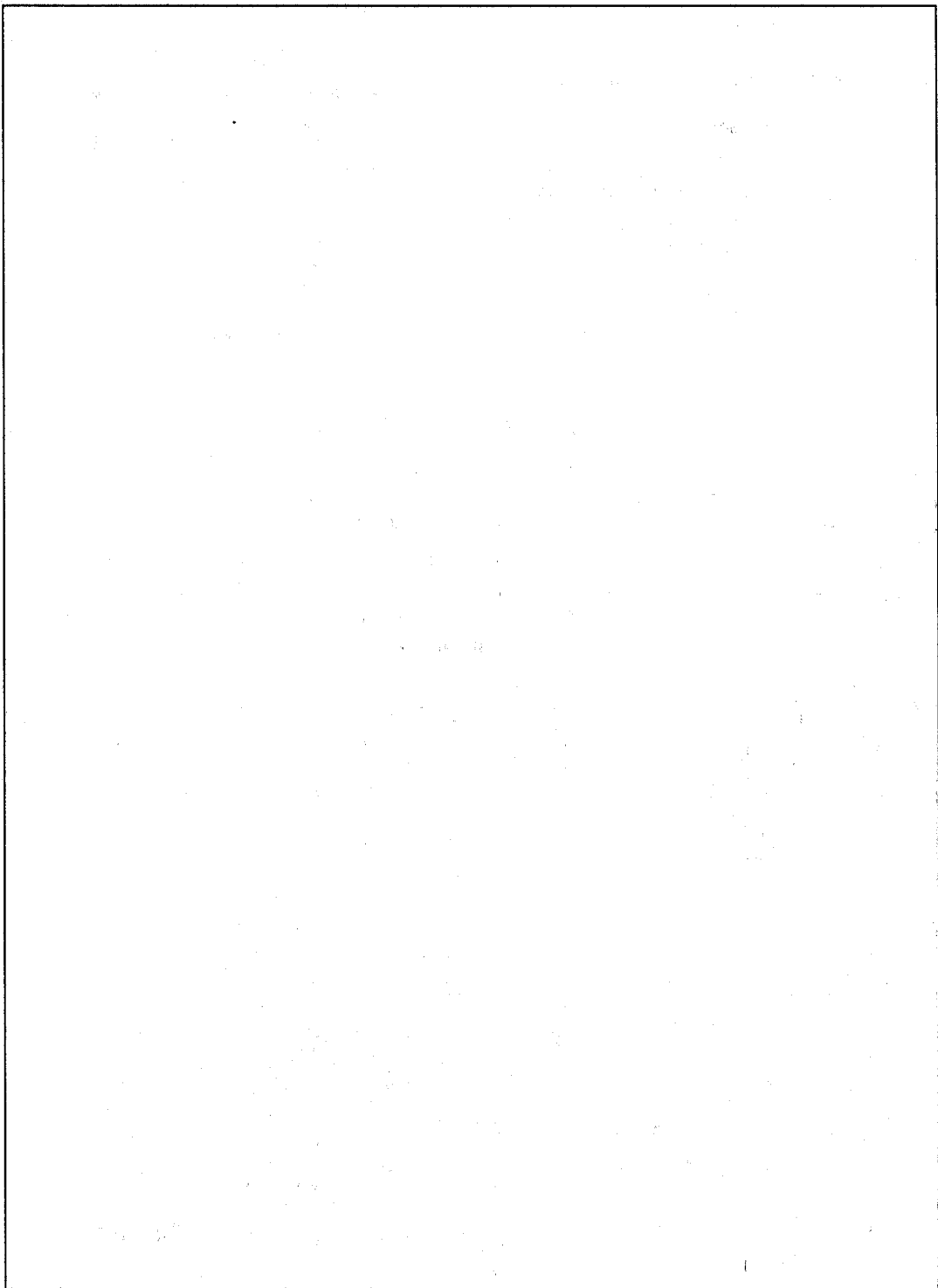
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to QN3	tPLH	0.77	$0.69 + 0.040 \cdot SL$	$0.69 + 0.040 \cdot SL$	$0.69 + 0.040 \cdot SL$
	tR	0.29	$0.11 + 0.089 \cdot SL$	$0.10 + 0.092 \cdot SL$	$0.08 + 0.093 \cdot SL$
CK to QN3	tPLH	0.75	$0.67 + 0.041 \cdot SL$	$0.67 + 0.040 \cdot SL$	$0.68 + 0.040 \cdot SL$
	tPHL	0.95	$0.89 + 0.027 \cdot SL$	$0.91 + 0.021 \cdot SL$	$0.94 + 0.020 \cdot SL$
	tR	0.28	$0.11 + 0.088 \cdot SL$	$0.10 + 0.092 \cdot SL$	$0.08 + 0.093 \cdot SL$
	tF	0.18	$0.11 + 0.035 \cdot SL$	$0.11 + 0.037 \cdot SL$	$0.08 + 0.038 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD2X4 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D0 to CK)	tHD	0.397
Input Hold Time (D1 to CK)	tHD	0.397
Input Hold Time (D2 to CK)	tHD	0.452
Input Hold Time (D3 to CK)	tHD	0.397
Input Setup Time (D0 to CK)	tSU	0.233
Input Setup Time (D1 to CK)	tSU	0.233
Input Setup Time (D2 to CK)	tSU	0.233
Input Setup Time (D3 to CK)	tSU	0.233
Recovery Time (RN)	tRC	0.139



# FD2D2X4Q/FD2D4X4Q

4-Bit D Flip-Flop with Reset, Positive Edge Trigger, Q Output Only, 2X Drive or 4X Drive

Inputs: D0, D1, D2, D3, CK, RN

Output: Q

Input Loading (SL): All: D0, D1, D2, D3: 3,

CK: 1, RN: 8

Maximum Fanout (Rec. SL):

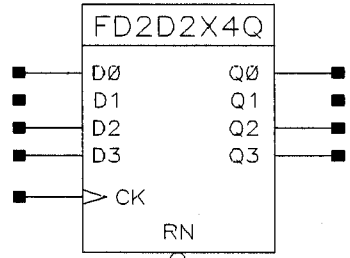
- FD2D2X4Q: 56

- FD2D4X4Q: 112

Gate Count:

- FD2D2X4Q: 25

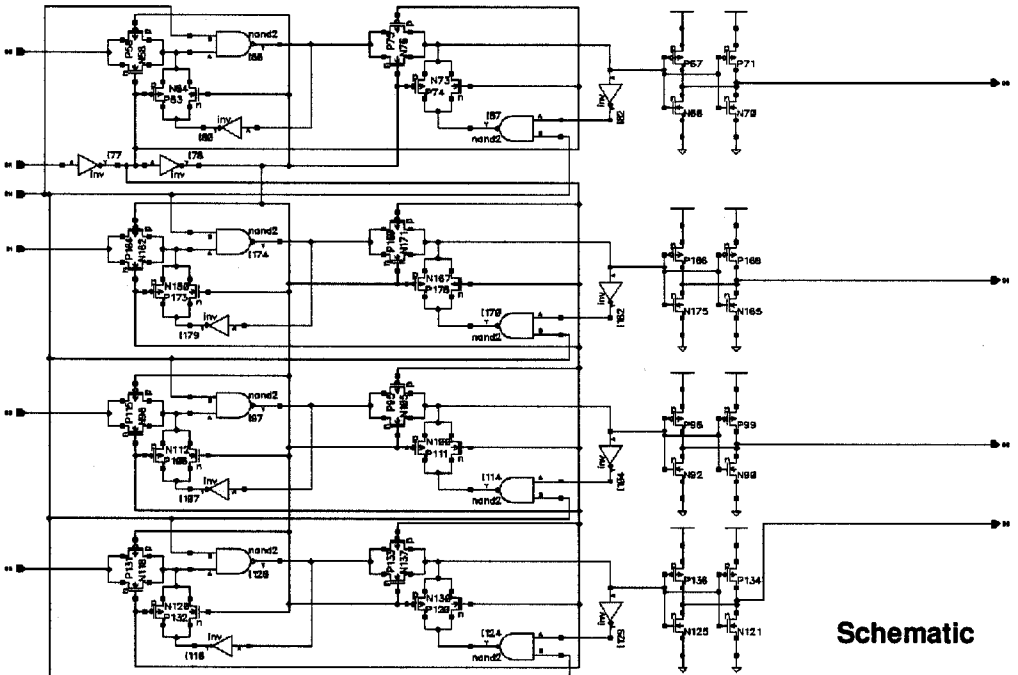
- FD2D4X4Q: 29



Symbol

D	RN	CK	Qn+1
0	1		0
1	1		1
x	0	x	0
x	1		Qn

Truth Table



Schematic

**FD2D2X4Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q0	tPHL	0.66	$0.61 + 0.025 \cdot SL$	$0.63 + 0.016 \cdot SL$	$0.72 + 0.012 \cdot SL$
	tF	0.30	$0.25 + 0.024 \cdot SL$	$0.27 + 0.019 \cdot SL$	$0.28 + 0.018 \cdot SL$
CK to Q0	tPLH	0.92	$0.87 + 0.027 \cdot SL$	$0.89 + 0.022 \cdot SL$	$0.92 + 0.020 \cdot SL$
	tPHL	0.69	$0.65 + 0.024 \cdot SL$	$0.67 + 0.016 \cdot SL$	$0.75 + 0.012 \cdot SL$
	tR	0.30	$0.22 + 0.043 \cdot SL$	$0.21 + 0.045 \cdot SL$	$0.19 + 0.046 \cdot SL$
	tF	0.26	$0.21 + 0.026 \cdot SL$	$0.23 + 0.020 \cdot SL$	$0.25 + 0.019 \cdot SL$
	tR	0.30	$0.22 + 0.043 \cdot SL$	$0.21 + 0.045 \cdot SL$	$0.19 + 0.046 \cdot SL$
RN to Q1	tPHL	0.65	$0.60 + 0.025 \cdot SL$	$0.63 + 0.016 \cdot SL$	$0.72 + 0.012 \cdot SL$
	tF	0.31	$0.26 + 0.025 \cdot SL$	$0.27 + 0.020 \cdot SL$	$0.28 + 0.019 \cdot SL$
CK to Q1	tPLH	0.92	$0.86 + 0.027 \cdot SL$	$0.88 + 0.022 \cdot SL$	$0.91 + 0.021 \cdot SL$
	tPHL	0.69	$0.64 + 0.025 \cdot SL$	$0.66 + 0.016 \cdot SL$	$0.74 + 0.012 \cdot SL$
	tR	0.31	$0.22 + 0.046 \cdot SL$	$0.21 + 0.048 \cdot SL$	$0.19 + 0.050 \cdot SL$
	tF	0.27	$0.21 + 0.027 \cdot SL$	$0.23 + 0.021 \cdot SL$	$0.25 + 0.020 \cdot SL$
	tR	0.31	$0.22 + 0.046 \cdot SL$	$0.21 + 0.048 \cdot SL$	$0.19 + 0.050 \cdot SL$
RN to Q2	tPHL	0.65	$0.60 + 0.025 \cdot SL$	$0.63 + 0.016 \cdot SL$	$0.72 + 0.012 \cdot SL$
	tF	0.31	$0.26 + 0.025 \cdot SL$	$0.27 + 0.020 \cdot SL$	$0.28 + 0.019 \cdot SL$
CK to Q2	tPLH	0.92	$0.87 + 0.028 \cdot SL$	$0.88 + 0.022 \cdot SL$	$0.91 + 0.021 \cdot SL$
	tPHL	0.69	$0.64 + 0.024 \cdot SL$	$0.67 + 0.016 \cdot SL$	$0.75 + 0.012 \cdot SL$
	tR	0.31	$0.22 + 0.046 \cdot SL$	$0.21 + 0.048 \cdot SL$	$0.19 + 0.050 \cdot SL$
	tF	0.27	$0.21 + 0.027 \cdot SL$	$0.23 + 0.021 \cdot SL$	$0.25 + 0.020 \cdot SL$
	tR	0.31	$0.22 + 0.046 \cdot SL$	$0.21 + 0.048 \cdot SL$	$0.19 + 0.050 \cdot SL$
RN to Q3	tPHL	0.66	$0.61 + 0.025 \cdot SL$	$0.63 + 0.016 \cdot SL$	$0.72 + 0.012 \cdot SL$
	tF	0.30	$0.25 + 0.024 \cdot SL$	$0.27 + 0.019 \cdot SL$	$0.28 + 0.018 \cdot SL$
CK to Q3	tPLH	0.92	$0.87 + 0.027 \cdot SL$	$0.89 + 0.022 \cdot SL$	$0.92 + 0.020 \cdot SL$
	tPHL	0.70	$0.65 + 0.023 \cdot SL$	$0.67 + 0.016 \cdot SL$	$0.75 + 0.012 \cdot SL$
	tR	0.30	$0.22 + 0.043 \cdot SL$	$0.21 + 0.045 \cdot SL$	$0.19 + 0.046 \cdot SL$
	tF	0.26	$0.21 + 0.026 \cdot SL$	$0.23 + 0.020 \cdot SL$	$0.25 + 0.019 \cdot SL$
	tR	0.30	$0.22 + 0.043 \cdot SL$	$0.21 + 0.045 \cdot SL$	$0.19 + 0.046 \cdot SL$

\*Range1:  $SL < 3.00$ , \*Range2:  $3.00 \leq SL \leq 20.00$ , \*Range3:  $20.00 < SL$

**FD2D2X4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.959
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D0 to CK)	tHD	0.452
Input Hold Time (D1 to CK)	tHD	0.452
Input Hold Time (D2 to CK)	tHD	0.452
Input Hold Time (D3 to CK)	tHD	0.452
Input Setup Time (D0 to CK)	tSU	0.233

# FD2D2X4Q

4-Bit D Flip-Flop with Reset, Positive Edge Trigger, Q Output Only, 4X Drive

## FD2D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Input Setup Time (D1 to CK)	tSU	0.233
Input Setup Time (D2 to CK)	tSU	0.233
Input Setup Time (D3 to CK)	tSU	0.233
Recovery Time (RN)	tRC	0.139

**FD2D4X4Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{RQ}$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q0	tPHL	0.71	$0.69 + 0.015 \cdot SL$	$0.70 + 0.010 \cdot SL$	$0.75 + 0.007 \cdot SL$
	tF	0.32	$0.29 + 0.013 \cdot SL$	$0.30 + 0.011 \cdot SL$	$0.33 + 0.009 \cdot SL$
CK to Q0	tPLH	1.00	$0.97 + 0.016 \cdot SL$	$0.98 + 0.012 \cdot SL$	$1.01 + 0.011 \cdot SL$
	tPHL	0.80	$0.77 + 0.014 \cdot SL$	$0.78 + 0.010 \cdot SL$	$0.84 + 0.008 \cdot SL$
	tR	0.32	$0.28 + 0.020 \cdot SL$	$0.27 + 0.021 \cdot SL$	$0.25 + 0.023 \cdot SL$
	tF	0.32	$0.29 + 0.013 \cdot SL$	$0.30 + 0.011 \cdot SL$	$0.33 + 0.010 \cdot SL$
RN to Q1	tPHL	0.71	$0.68 + 0.015 \cdot SL$	$0.69 + 0.010 \cdot SL$	$0.74 + 0.007 \cdot SL$
	tF	0.32	$0.29 + 0.014 \cdot SL$	$0.30 + 0.011 \cdot SL$	$0.33 + 0.009 \cdot SL$
CK to Q1	tPLH	0.99	$0.96 + 0.016 \cdot SL$	$0.97 + 0.012 \cdot SL$	$1.00 + 0.011 \cdot SL$
	tPHL	0.79	$0.76 + 0.014 \cdot SL$	$0.77 + 0.010 \cdot SL$	$0.83 + 0.008 \cdot SL$
	tR	0.31	$0.28 + 0.019 \cdot SL$	$0.27 + 0.022 \cdot SL$	$0.25 + 0.023 \cdot SL$
	tF	0.32	$0.29 + 0.014 \cdot SL$	$0.30 + 0.011 \cdot SL$	$0.33 + 0.010 \cdot SL$
RN to Q2	tPHL	0.71	$0.68 + 0.015 \cdot SL$	$0.69 + 0.010 \cdot SL$	$0.74 + 0.007 \cdot SL$
	tF	0.32	$0.29 + 0.014 \cdot SL$	$0.30 + 0.011 \cdot SL$	$0.33 + 0.009 \cdot SL$
CK to Q2	tPLH	0.99	$0.96 + 0.016 \cdot SL$	$0.97 + 0.012 \cdot SL$	$1.00 + 0.011 \cdot SL$
	tPHL	0.79	$0.76 + 0.014 \cdot SL$	$0.78 + 0.010 \cdot SL$	$0.83 + 0.008 \cdot SL$
	tR	0.31	$0.28 + 0.019 \cdot SL$	$0.27 + 0.022 \cdot SL$	$0.25 + 0.023 \cdot SL$
	tF	0.32	$0.29 + 0.014 \cdot SL$	$0.30 + 0.011 \cdot SL$	$0.33 + 0.010 \cdot SL$
RN to Q3	tPHL	0.71	$0.69 + 0.015 \cdot SL$	$0.70 + 0.010 \cdot SL$	$0.75 + 0.007 \cdot SL$
	tF	0.32	$0.29 + 0.013 \cdot SL$	$0.30 + 0.011 \cdot SL$	$0.33 + 0.009 \cdot SL$
CK to Q3	tPLH	1.00	$0.97 + 0.016 \cdot SL$	$0.98 + 0.012 \cdot SL$	$1.01 + 0.011 \cdot SL$
	tPHL	0.80	$0.77 + 0.014 \cdot SL$	$0.79 + 0.010 \cdot SL$	$0.84 + 0.008 \cdot SL$
	tR	0.32	$0.28 + 0.020 \cdot SL$	$0.27 + 0.021 \cdot SL$	$0.25 + 0.023 \cdot SL$
	tF	0.32	$0.29 + 0.013 \cdot SL$	$0.30 + 0.011 \cdot SL$	$0.33 + 0.010 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD2D4X4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.998
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D0 to CK)	tHD	0.452
Input Hold Time (D1 to CK)	tHD	0.452
Input Hold Time (D2 to CK)	tHD	0.452
Input Hold Time (D3 to CK)	tHD	0.452
Input Setup Time (D0 to CK)	tSU	0.178



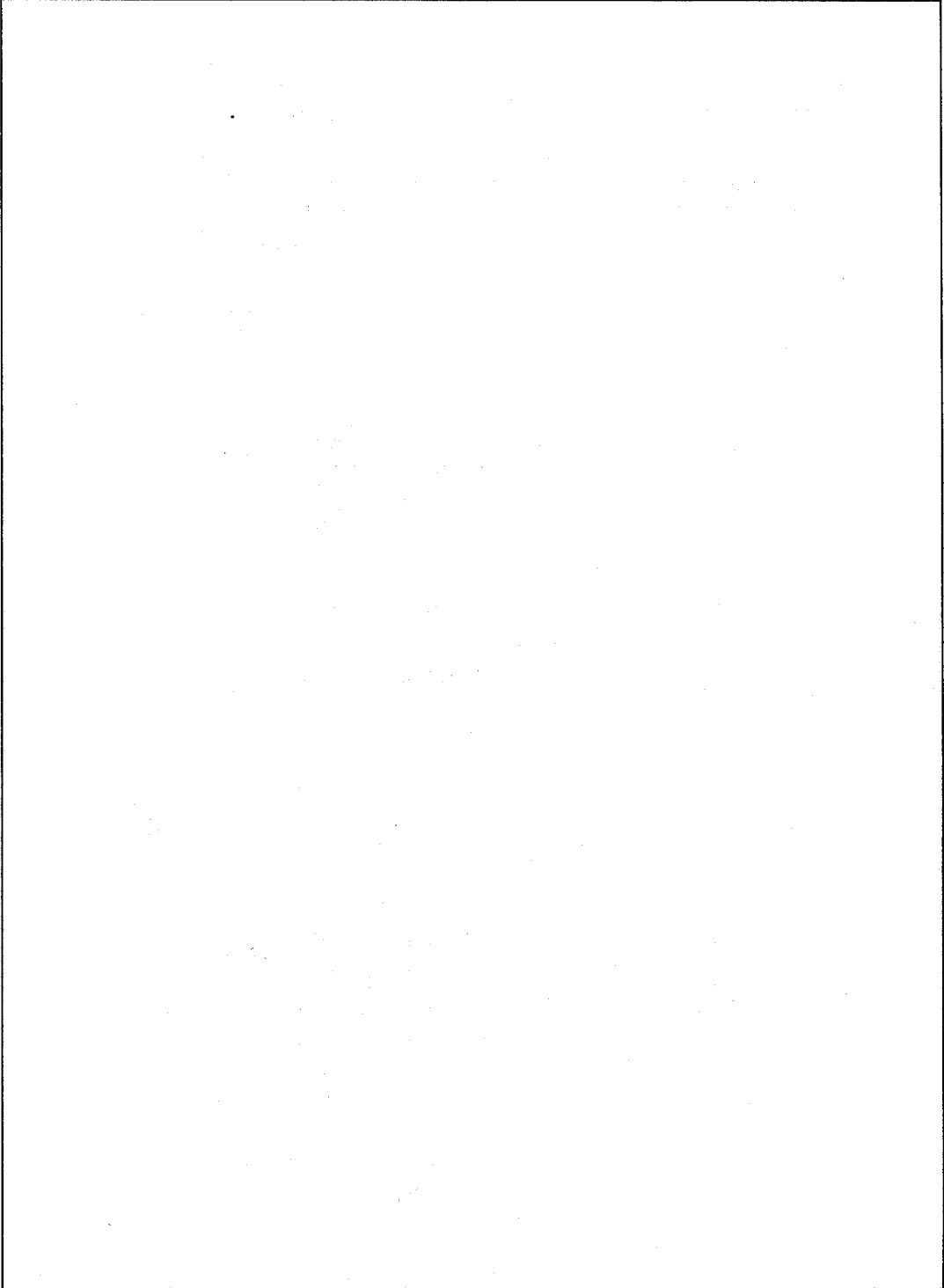
# FD2D4X4Q

4-Bit D Flip-Flop with Reset, Positive Edge Trigger, Q Output Only, 4X Drive

## FD2D4X4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Input Setup Time (D1 to CK)	tSU	0.178
Input Setup Time (D2 to CK)	tSU	0.178
Input Setup Time (D3 to CK)	tSU	0.178
Recovery Time (RN)	tRC	0.139



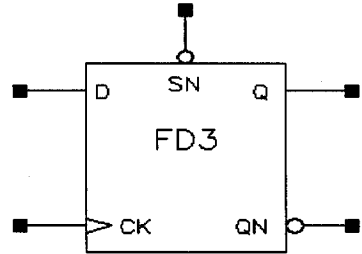
# FD3/FD3D2

D Flip-Flop with Set, Positive Edge Trigger, 1X Drive or 2X Drive

Inputs: D, CK, SN  
 Outputs: Q, QN  
 Input Loading (SL):  
 - D: 3  
 - CK: 1  
 - SN: 2

Maximum Fanout (Rec. SL):  
 FD3: All : 28  
 FD3D2: All : 56

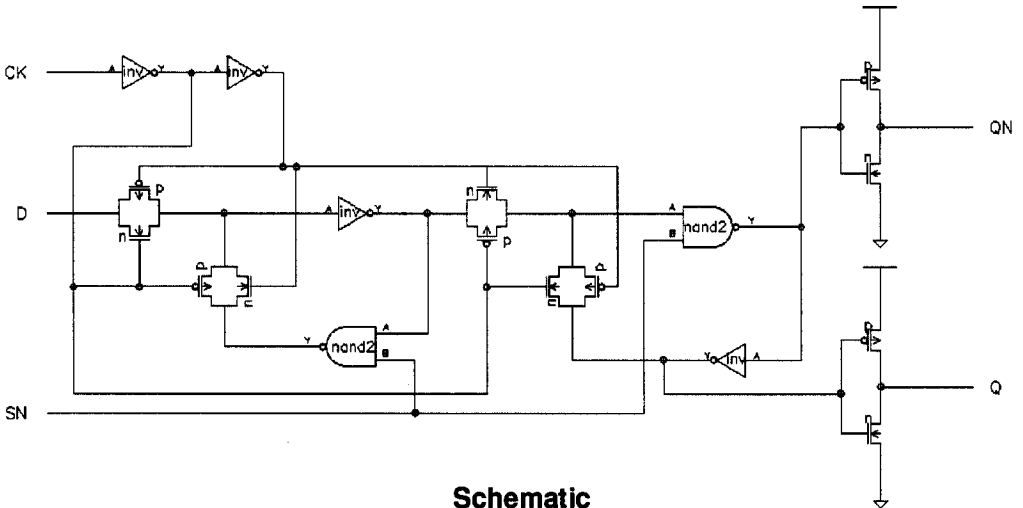
Gate Count:  
 FD3: 7  
 FD3D2: 8



**Symbol**

D	SN	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1		0	1
1	1		1	0
x	0	x	1	0
x	1		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FD3 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.61	$0.53 + 0.038 \cdot \text{SL}$	$0.53 + 0.039 \cdot \text{SL}$	$0.52 + 0.040 \cdot \text{SL}$
	tR	0.28	$0.10 + 0.087 \cdot \text{SL}$	$0.09 + 0.091 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
CK to Q	tPLH	0.71	$0.63 + 0.039 \cdot \text{SL}$	$0.63 + 0.039 \cdot \text{SL}$	$0.63 + 0.040 \cdot \text{SL}$
	tPHL	0.73	$0.68 + 0.026 \cdot \text{SL}$	$0.69 + 0.021 \cdot \text{SL}$	$0.71 + 0.020 \cdot \text{SL}$
	tR	0.28	$0.10 + 0.087 \cdot \text{SL}$	$0.09 + 0.091 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
	tF	0.17	$0.10 + 0.034 \cdot \text{SL}$	$0.09 + 0.038 \cdot \text{SL}$	$0.07 + 0.039 \cdot \text{SL}$
SN to QN	tPHL	0.46	$0.40 + 0.032 \cdot \text{SL}$	$0.43 + 0.022 \cdot \text{SL}$	$0.47 + 0.020 \cdot \text{SL}$
	tF	0.23	$0.16 + 0.037 \cdot \text{SL}$	$0.15 + 0.038 \cdot \text{SL}$	$0.10 + 0.040 \cdot \text{SL}$
CK to QN	tPLH	0.65	$0.56 + 0.042 \cdot \text{SL}$	$0.57 + 0.040 \cdot \text{SL}$	$0.57 + 0.040 \cdot \text{SL}$
	tPHL	0.57	$0.51 + 0.029 \cdot \text{SL}$	$0.53 + 0.022 \cdot \text{SL}$	$0.56 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.13 + 0.088 \cdot \text{SL}$	$0.12 + 0.090 \cdot \text{SL}$	$0.10 + 0.091 \cdot \text{SL}$
	tF	0.19	$0.11 + 0.041 \cdot \text{SL}$	$0.11 + 0.039 \cdot \text{SL}$	$0.08 + 0.041 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **FD3 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.233
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (SN)	tRC	0.139

## FD3D2

D Flip-Flop with Set, Positive Edge Trigger, 2X Drive

### FD3D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

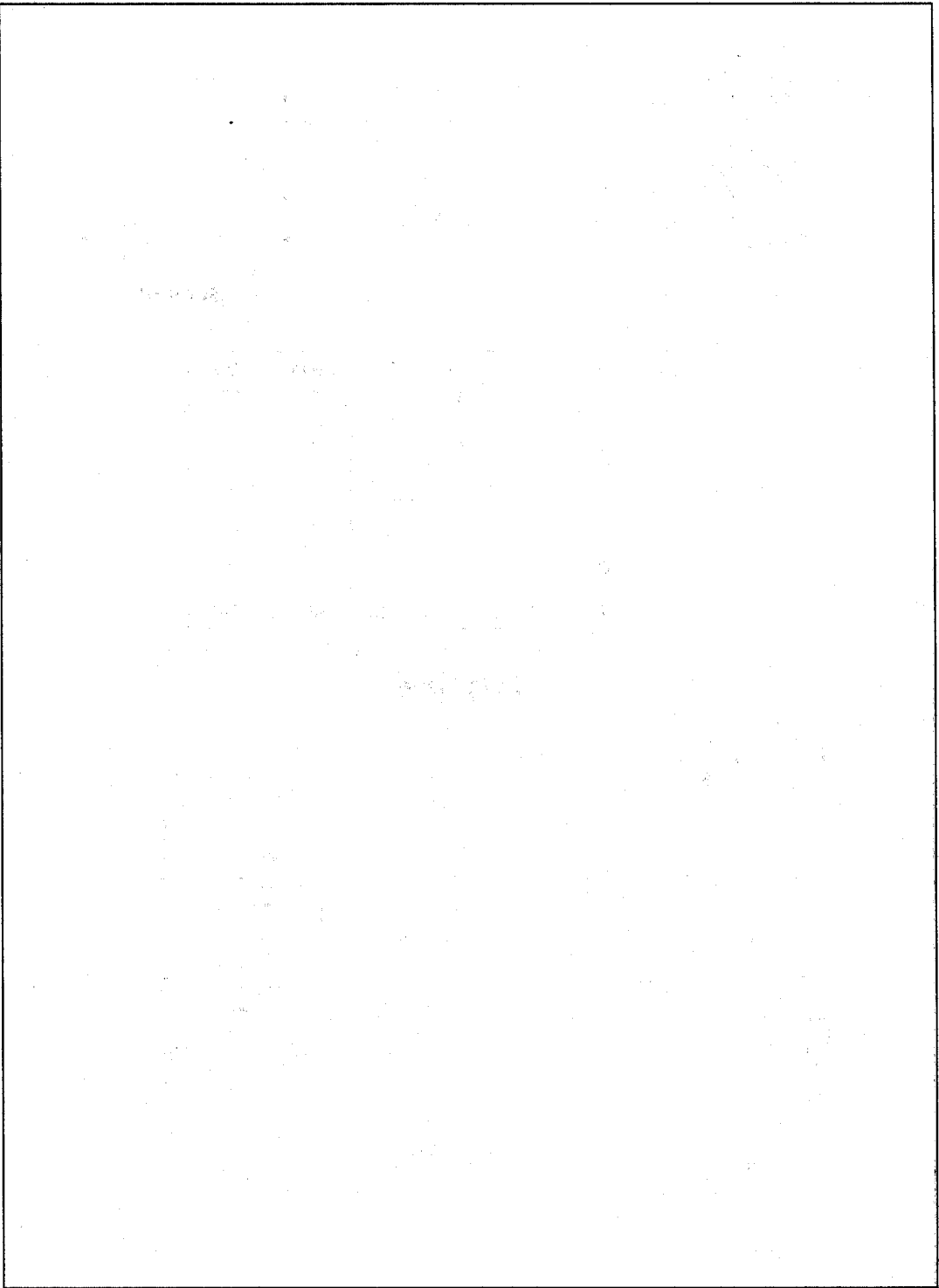
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.65	$0.61 + 0.018 \cdot SL$	$0.61 + 0.019 \cdot SL$	$0.60 + 0.020 \cdot SL$
	tR	0.20	$0.12 + 0.041 \cdot SL$	$0.10 + 0.045 \cdot SL$	$0.08 + 0.046 \cdot SL$
CK to Q	tPLH	0.75	$0.72 + 0.018 \cdot SL$	$0.71 + 0.019 \cdot SL$	$0.70 + 0.020 \cdot SL$
	tPHL	0.79	$0.76 + 0.015 \cdot SL$	$0.77 + 0.012 \cdot SL$	$0.80 + 0.010 \cdot SL$
	tR	0.20	$0.11 + 0.041 \cdot SL$	$0.10 + 0.045 \cdot SL$	$0.08 + 0.046 \cdot SL$
	tF	0.16	$0.12 + 0.021 \cdot SL$	$0.13 + 0.017 \cdot SL$	$0.11 + 0.019 \cdot SL$
SN to QN	tPHL	0.47	$0.43 + 0.020 \cdot SL$	$0.45 + 0.013 \cdot SL$	$0.50 + 0.010 \cdot SL$
	tF	0.21	$0.17 + 0.020 \cdot SL$	$0.18 + 0.018 \cdot SL$	$0.16 + 0.019 \cdot SL$
CK to QN	tPLH	0.65	$0.60 + 0.023 \cdot SL$	$0.61 + 0.020 \cdot SL$	$0.62 + 0.020 \cdot SL$
	tPHL	0.58	$0.54 + 0.018 \cdot SL$	$0.56 + 0.012 \cdot SL$	$0.60 + 0.011 \cdot SL$
	tR	0.23	$0.14 + 0.042 \cdot SL$	$0.14 + 0.045 \cdot SL$	$0.11 + 0.046 \cdot SL$
	tF	0.17	$0.12 + 0.022 \cdot SL$	$0.13 + 0.019 \cdot SL$	$0.12 + 0.020 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### FD3D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.233
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (SN)	tRC	0.139



# FD3S/FD3SD2

D Flip-Flop with Scan and Set, Positive Edge Trigger, X Drive or 2X Drive

Inputs: D, TI, TE, CK, SN

Outputs: Q, QN

Input Loading (SL):

- D, TI, CK: 1

- TE, SN: 2

Maximum Fanout (Rec. SL):

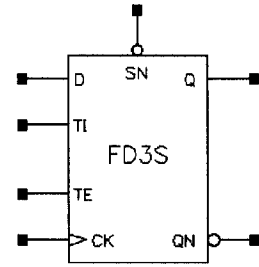
FD3S: All : 28

FD3SD2: All : 56

Gate Count:

FD3S 10

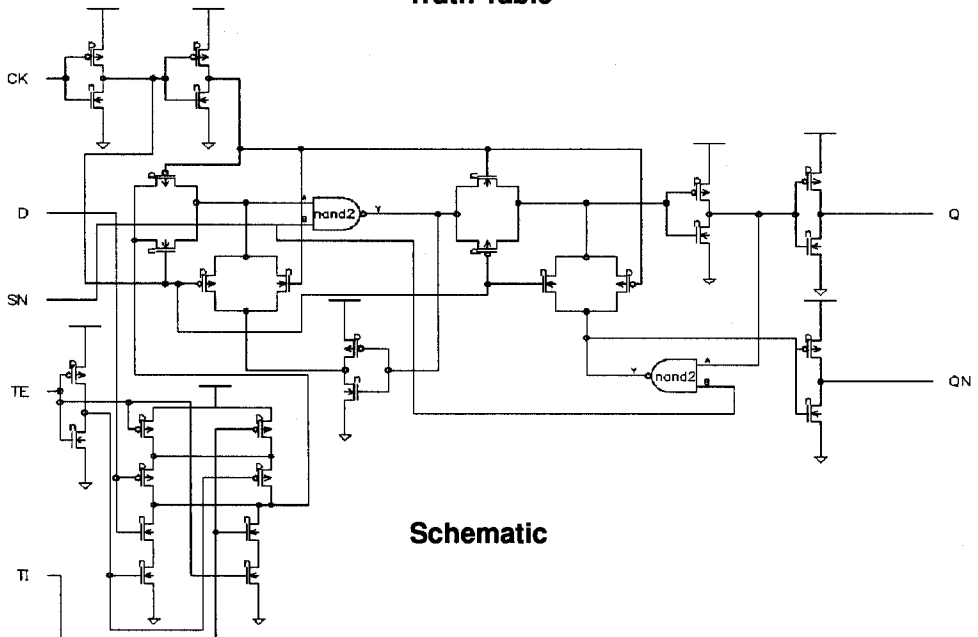
FD3SD2: 11



**Symbol**

D	SN	TI	TE	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	x	0		0	1
1	1	x	0		1	0
x	1	0	1		0	1
x	1	1	1		1	0
x	0	x	x	x	1	0
x	1	x	x		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FD3S Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.77	$0.69 + 0.040 \cdot \text{SL}$	$0.69 + 0.040 \cdot \text{SL}$	$0.69 + 0.040 \cdot \text{SL}$
	tR	0.29	$0.11 + 0.088 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
CK to Q	tPLH	0.56	$0.48 + 0.041 \cdot \text{SL}$	$0.48 + 0.040 \cdot \text{SL}$	$0.48 + 0.040 \cdot \text{SL}$
	tPHL	0.60	$0.55 + 0.028 \cdot \text{SL}$	$0.56 + 0.021 \cdot \text{SL}$	$0.59 + 0.020 \cdot \text{SL}$
	tR	0.28	$0.11 + 0.089 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
	tF	0.18	$0.11 + 0.034 \cdot \text{SL}$	$0.10 + 0.037 \cdot \text{SL}$	$0.08 + 0.038 \cdot \text{SL}$
SN to QN	tPHL	0.45	$0.39 + 0.030 \cdot \text{SL}$	$0.42 + 0.021 \cdot \text{SL}$	$0.45 + 0.020 \cdot \text{SL}$
	tF	0.22	$0.15 + 0.032 \cdot \text{SL}$	$0.14 + 0.035 \cdot \text{SL}$	$0.09 + 0.038 \cdot \text{SL}$
CK to QN	tPLH	0.82	$0.74 + 0.039 \cdot \text{SL}$	$0.74 + 0.040 \cdot \text{SL}$	$0.74 + 0.040 \cdot \text{SL}$
	tPHL	0.65	$0.60 + 0.028 \cdot \text{SL}$	$0.62 + 0.021 \cdot \text{SL}$	$0.64 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.12 + 0.088 \cdot \text{SL}$	$0.11 + 0.091 \cdot \text{SL}$	$0.09 + 0.093 \cdot \text{SL}$
	tF	0.18	$0.10 + 0.037 \cdot \text{SL}$	$0.10 + 0.037 \cdot \text{SL}$	$0.07 + 0.038 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **FD3S Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.725
Input Setup Time (TE to CK)	tSU	0.944
Input Setup Time (TI to CK)	tSU	0.780
Recovery Time (SN)	tRC	0.139



# FD3SD2

D Flip-Flop with Scan and Set, Positive Edge Trigger, 2X Drive

## FD3SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

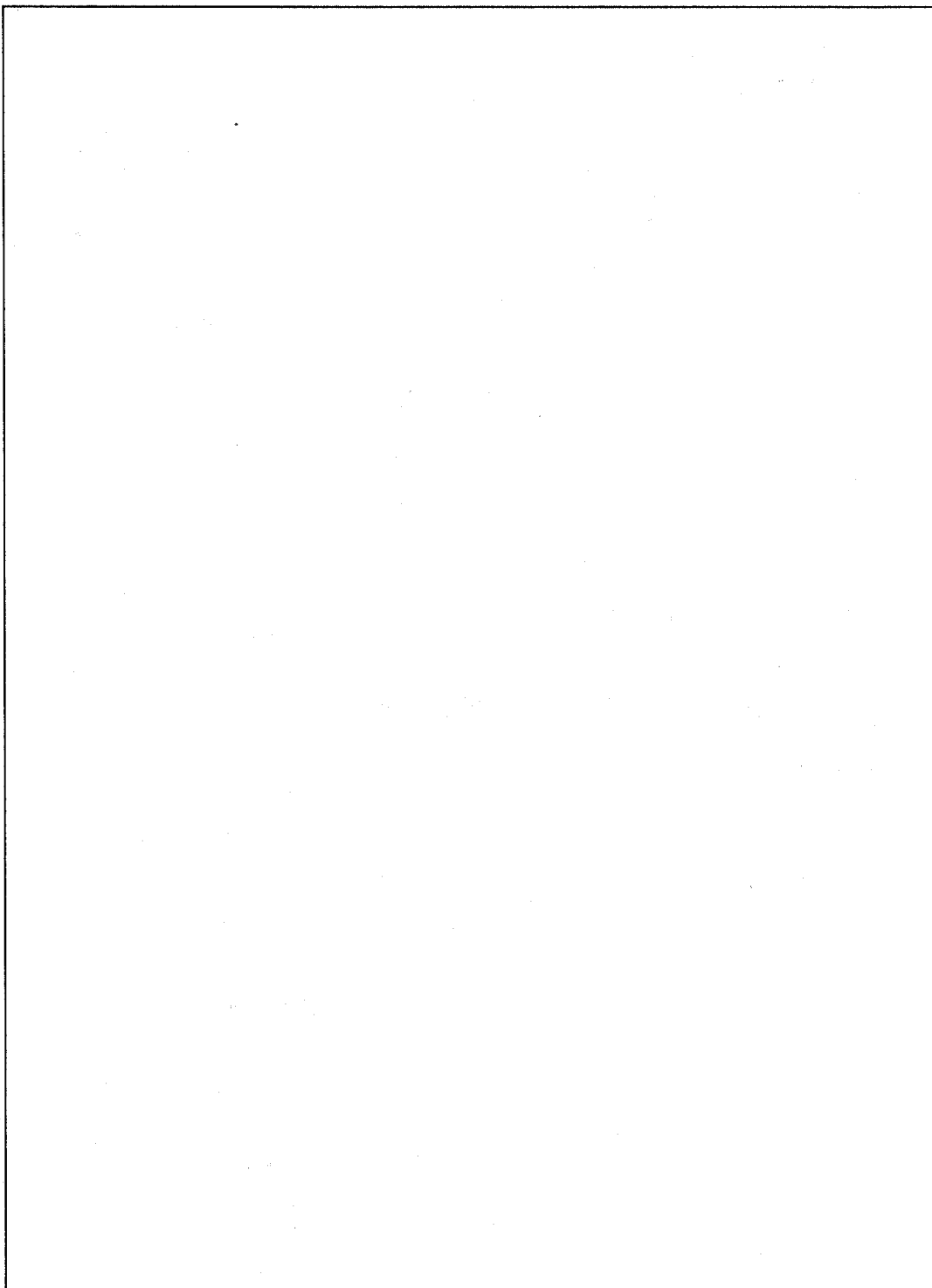
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.77	$0.73 + 0.020 \cdot \text{SL}$	$0.73 + 0.020 \cdot \text{SL}$	$0.73 + 0.020 \cdot \text{SL}$
	tR	0.21	$0.12 + 0.043 \cdot \text{SL}$	$0.11 + 0.046 \cdot \text{SL}$	$0.09 + 0.047 \cdot \text{SL}$
CK to Q	tPLH	0.55	$0.51 + 0.021 \cdot \text{SL}$	$0.51 + 0.020 \cdot \text{SL}$	$0.51 + 0.020 \cdot \text{SL}$
	tPHL	0.61	$0.57 + 0.018 \cdot \text{SL}$	$0.59 + 0.012 \cdot \text{SL}$	$0.62 + 0.010 \cdot \text{SL}$
	tR	0.20	$0.11 + 0.044 \cdot \text{SL}$	$0.11 + 0.046 \cdot \text{SL}$	$0.09 + 0.047 \cdot \text{SL}$
	tF	0.17	$0.13 + 0.020 \cdot \text{SL}$	$0.13 + 0.018 \cdot \text{SL}$	$0.12 + 0.018 \cdot \text{SL}$
SN to QN	tPHL	0.46	$0.42 + 0.019 \cdot \text{SL}$	$0.44 + 0.012 \cdot \text{SL}$	$0.48 + 0.010 \cdot \text{SL}$
	tF	0.20	$0.17 + 0.018 \cdot \text{SL}$	$0.17 + 0.017 \cdot \text{SL}$	$0.14 + 0.018 \cdot \text{SL}$
CK to QN	tPLH	0.88	$0.84 + 0.020 \cdot \text{SL}$	$0.84 + 0.020 \cdot \text{SL}$	$0.83 + 0.020 \cdot \text{SL}$
	tPHL	0.69	$0.66 + 0.017 \cdot \text{SL}$	$0.67 + 0.012 \cdot \text{SL}$	$0.71 + 0.010 \cdot \text{SL}$
	tR	0.22	$0.13 + 0.044 \cdot \text{SL}$	$0.13 + 0.045 \cdot \text{SL}$	$0.10 + 0.047 \cdot \text{SL}$
	tF	0.16	$0.12 + 0.020 \cdot \text{SL}$	$0.12 + 0.018 \cdot \text{SL}$	$0.11 + 0.019 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

## FD3SD2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.780
Input Setup Time (TE to CK)	tSU	0.944
Input Setup Time (TI to CK)	tSU	0.780
Recovery Time (SN)	tRC	0.178



# FD4/FD4D2

D Flip-Flop with Set and Reset, Positive Edge Trigger, 1X Drive or 2X Drive

Inputs: D, CK, SN, RN

Outputs: Q, QN

Input Loading (SL):

- D: 3

- CK: 1

- SN, RN: 2

Maximum Fanout (Rec. SL):

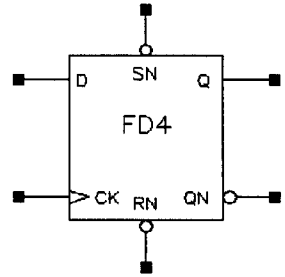
FD4: All : 28

FD4D2: All : 56

Gate Count:

FD4: 8

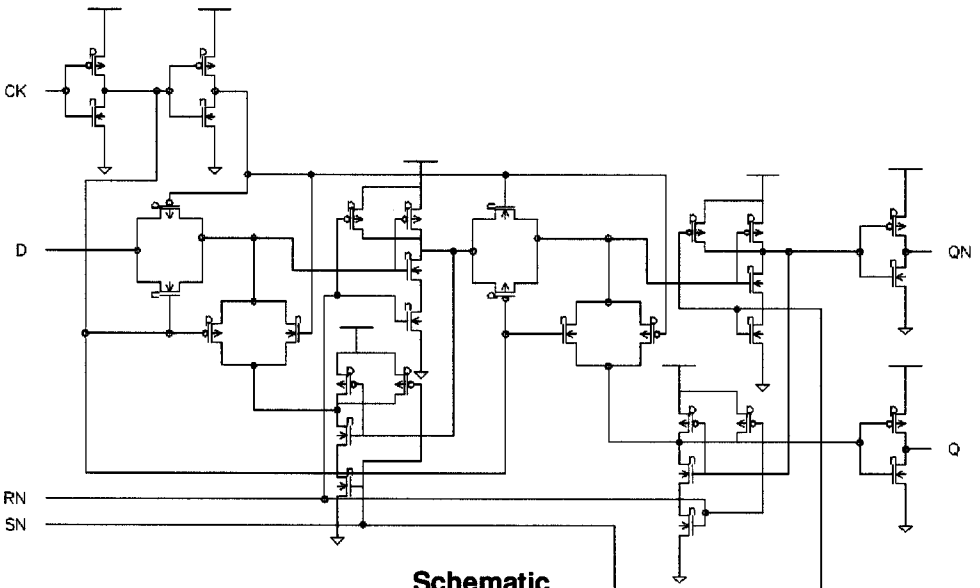
FD4D2: 9



Symbol

D	SN	RN	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	1		0	1
1	1	1		1	0
x	0	1	x	1	0
x	1	0	x	0	1
x	0	0	x	0	0
x	1	1		Q <sub>n</sub>	Q <sub>Nn</sub>

Truth Table



Schematic

**FD4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.85	$0.77 + 0.041 * SL$	$0.77 + 0.041 * SL$	$0.76 + 0.041 * SL$
	tPHL	0.73	$0.67 + 0.026 * SL$	$0.69 + 0.021 * SL$	$0.71 + 0.020 * SL$
	tR	0.31	$0.13 + 0.092 * SL$	$0.12 + 0.096 * SL$	$0.09 + 0.097 * SL$
	tF	0.18	$0.11 + 0.034 * SL$	$0.10 + 0.037 * SL$	$0.07 + 0.038 * SL$
RN to Q	tPLH	0.32	$0.23 + 0.044 * SL$	$0.24 + 0.041 * SL$	$0.24 + 0.041 * SL$
	tPHL	0.44	$0.38 + 0.031 * SL$	$0.41 + 0.021 * SL$	$0.44 + 0.020 * SL$
	tR	0.32	$0.14 + 0.091 * SL$	$0.13 + 0.095 * SL$	$0.10 + 0.097 * SL$
	tF	0.22	$0.15 + 0.033 * SL$	$0.14 + 0.035 * SL$	$0.09 + 0.038 * SL$
SN to Q	tPLH	0.70	$0.62 + 0.041 * SL$	$0.62 + 0.041 * SL$	$0.62 + 0.041 * SL$
	tR	0.31	$0.13 + 0.093 * SL$	$0.12 + 0.096 * SL$	$0.09 + 0.097 * SL$
CK to QN	tPLH	0.65	$0.56 + 0.045 * SL$	$0.56 + 0.043 * SL$	$0.57 + 0.043 * SL$
	tPHL	0.61	$0.55 + 0.029 * SL$	$0.58 + 0.022 * SL$	$0.61 + 0.020 * SL$
	tR	0.33	$0.13 + 0.099 * SL$	$0.12 + 0.101 * SL$	$0.10 + 0.102 * SL$
	tF	0.19	$0.12 + 0.036 * SL$	$0.11 + 0.037 * SL$	$0.09 + 0.038 * SL$
RN to QN	tPLH	0.86	$0.77 + 0.044 * SL$	$0.78 + 0.042 * SL$	$0.77 + 0.043 * SL$
	tR	0.33	$0.13 + 0.097 * SL$	$0.12 + 0.101 * SL$	$0.10 + 0.102 * SL$
SN to QN	tPLH	0.30	$0.22 + 0.045 * SL$	$0.22 + 0.042 * SL$	$0.22 + 0.043 * SL$
	tPHL	0.46	$0.40 + 0.031 * SL$	$0.42 + 0.022 * SL$	$0.46 + 0.020 * SL$
	tR	0.33	$0.14 + 0.097 * SL$	$0.13 + 0.100 * SL$	$0.10 + 0.102 * SL$
	tF	0.22	$0.15 + 0.034 * SL$	$0.15 + 0.035 * SL$	$0.11 + 0.038 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD4 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.178
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

# FD4D2

D Flip-Flop with Set and Reset, Positive Edge Trigger, 2X Drive

## FD4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.90	$0.86 + 0.020 \cdot \text{SL}$	$0.86 + 0.020 \cdot \text{SL}$	$0.85 + 0.020 \cdot \text{SL}$
	tPHL	0.79	$0.76 + 0.016 \cdot \text{SL}$	$0.77 + 0.012 \cdot \text{SL}$	$0.80 + 0.010 \cdot \text{SL}$
	tR	0.23	$0.14 + 0.043 \cdot \text{SL}$	$0.13 + 0.045 \cdot \text{SL}$	$0.11 + 0.047 \cdot \text{SL}$
	tF	0.17	$0.13 + 0.020 \cdot \text{SL}$	$0.13 + 0.019 \cdot \text{SL}$	$0.11 + 0.020 \cdot \text{SL}$
RN to Q	tPLH	0.32	$0.27 + 0.023 \cdot \text{SL}$	$0.28 + 0.020 \cdot \text{SL}$	$0.29 + 0.020 \cdot \text{SL}$
	tPHL	0.45	$0.42 + 0.019 \cdot \text{SL}$	$0.43 + 0.013 \cdot \text{SL}$	$0.48 + 0.010 \cdot \text{SL}$
	tR	0.24	$0.15 + 0.043 \cdot \text{SL}$	$0.15 + 0.045 \cdot \text{SL}$	$0.12 + 0.046 \cdot \text{SL}$
	tF	0.20	$0.16 + 0.019 \cdot \text{SL}$	$0.17 + 0.018 \cdot \text{SL}$	$0.14 + 0.019 \cdot \text{SL}$
SN to Q	tPLH	0.75	$0.71 + 0.020 \cdot \text{SL}$	$0.72 + 0.020 \cdot \text{SL}$	$0.71 + 0.020 \cdot \text{SL}$
	tR	0.23	$0.14 + 0.044 \cdot \text{SL}$	$0.14 + 0.045 \cdot \text{SL}$	$0.11 + 0.047 \cdot \text{SL}$
CK to QN	tPLH	0.64	$0.59 + 0.022 \cdot \text{SL}$	$0.60 + 0.020 \cdot \text{SL}$	$0.61 + 0.020 \cdot \text{SL}$
	tPHL	0.62	$0.59 + 0.018 \cdot \text{SL}$	$0.60 + 0.012 \cdot \text{SL}$	$0.64 + 0.010 \cdot \text{SL}$
	tR	0.22	$0.14 + 0.042 \cdot \text{SL}$	$0.13 + 0.045 \cdot \text{SL}$	$0.11 + 0.046 \cdot \text{SL}$
	tF	0.17	$0.14 + 0.019 \cdot \text{SL}$	$0.14 + 0.018 \cdot \text{SL}$	$0.13 + 0.019 \cdot \text{SL}$
RN to QN	tPLH	0.87	$0.82 + 0.022 \cdot \text{SL}$	$0.83 + 0.020 \cdot \text{SL}$	$0.84 + 0.020 \cdot \text{SL}$
	tR	0.23	$0.14 + 0.042 \cdot \text{SL}$	$0.14 + 0.044 \cdot \text{SL}$	$0.11 + 0.046 \cdot \text{SL}$
SN to QN	tPLH	0.30	$0.26 + 0.023 \cdot \text{SL}$	$0.27 + 0.020 \cdot \text{SL}$	$0.27 + 0.020 \cdot \text{SL}$
	tPHL	0.46	$0.42 + 0.019 \cdot \text{SL}$	$0.44 + 0.013 \cdot \text{SL}$	$0.49 + 0.010 \cdot \text{SL}$
	tR	0.23	$0.14 + 0.043 \cdot \text{SL}$	$0.14 + 0.044 \cdot \text{SL}$	$0.11 + 0.046 \cdot \text{SL}$
	tF	0.21	$0.17 + 0.018 \cdot \text{SL}$	$0.17 + 0.017 \cdot \text{SL}$	$0.16 + 0.018 \cdot \text{SL}$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

## FD4D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.178
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



# FD4D2Q/FD4D4Q

D Flip-Flop with Set, Reset, Positive Edge Trigger, Q Output Only, 2X Drive or 4X Drive

Inputs: D, CK, RN, SN

Output: Q

Input Loading (SL):

- FD4D2Q: CK: 1, RN, SN: 2  
D: 3

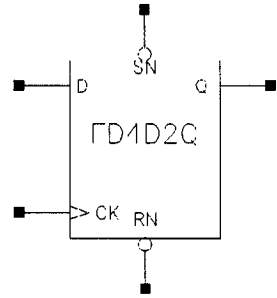
- FD4D4Q: CK: 1, RN, SN: 2  
D: 3

Maximum Fanout (Rec. SL):

- FD4D2Q: 56  
- FD4D4Q: 112

Gate Count:

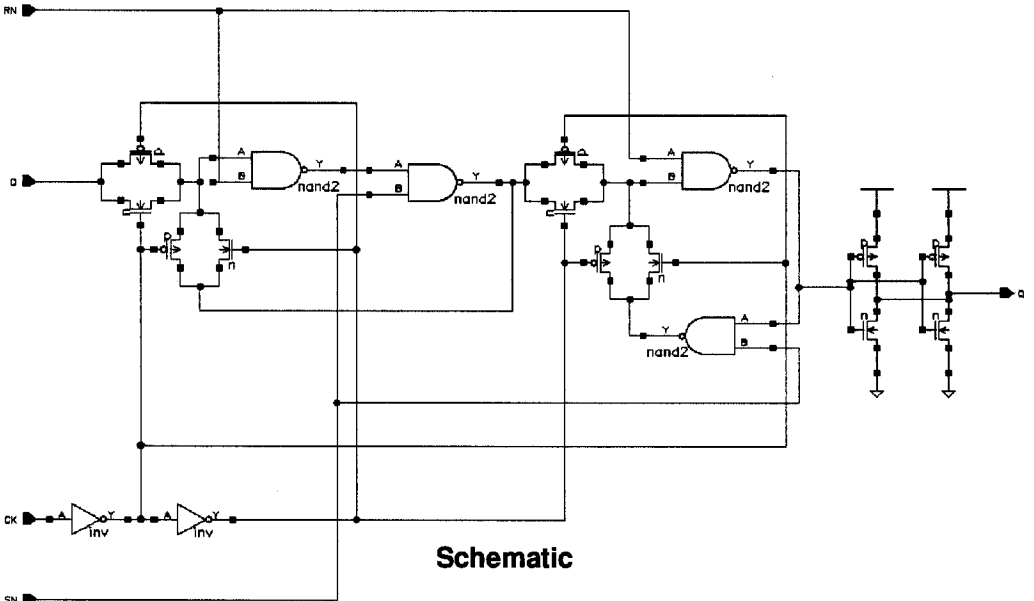
- FD4D2Q: 8  
- FD4D4Q: 9



Symbol

D	SN	RN	CK	Qn+1
0	1	1		0
1	1	1		1
x	0	1	x	1
x	1	0	x	0
x	0	0	x	0
x	1	1		Qn

Truth Table



Schematic

**FD4D2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.56	$0.51 + 0.027 \cdot SL$	$0.52 + 0.022 \cdot SL$	$0.55 + 0.021 \cdot SL$
	tPHL	0.43	$0.39 + 0.022 \cdot SL$	$0.41 + 0.015 \cdot SL$	$0.47 + 0.012 \cdot SL$
	tR	0.29	$0.20 + 0.043 \cdot SL$	$0.19 + 0.046 \cdot SL$	$0.17 + 0.047 \cdot SL$
	tF	0.20	$0.15 + 0.025 \cdot SL$	$0.16 + 0.022 \cdot SL$	$0.20 + 0.019 \cdot SL$
RN to Q	tPLH	0.53	$0.48 + 0.026 \cdot SL$	$0.49 + 0.021 \cdot SL$	$0.52 + 0.020 \cdot SL$
	tPHL	0.64	$0.59 + 0.025 \cdot SL$	$0.62 + 0.016 \cdot SL$	$0.71 + 0.012 \cdot SL$
	tR	0.29	$0.21 + 0.042 \cdot SL$	$0.20 + 0.045 \cdot SL$	$0.17 + 0.047 \cdot SL$
	tF	0.29	$0.24 + 0.025 \cdot SL$	$0.26 + 0.019 \cdot SL$	$0.29 + 0.018 \cdot SL$
SN to Q	tPLH	1.06	$1.01 + 0.026 \cdot SL$	$1.02 + 0.022 \cdot SL$	$1.05 + 0.020 \cdot SL$
	tR	0.29	$0.21 + 0.043 \cdot SL$	$0.20 + 0.045 \cdot SL$	$0.17 + 0.047 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD4D2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.233
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



# FD4D4Q

D Flip-Flop with Set, Reset, Positive Edge Trigger, Q Output Only, 4X Drive

## FD4D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

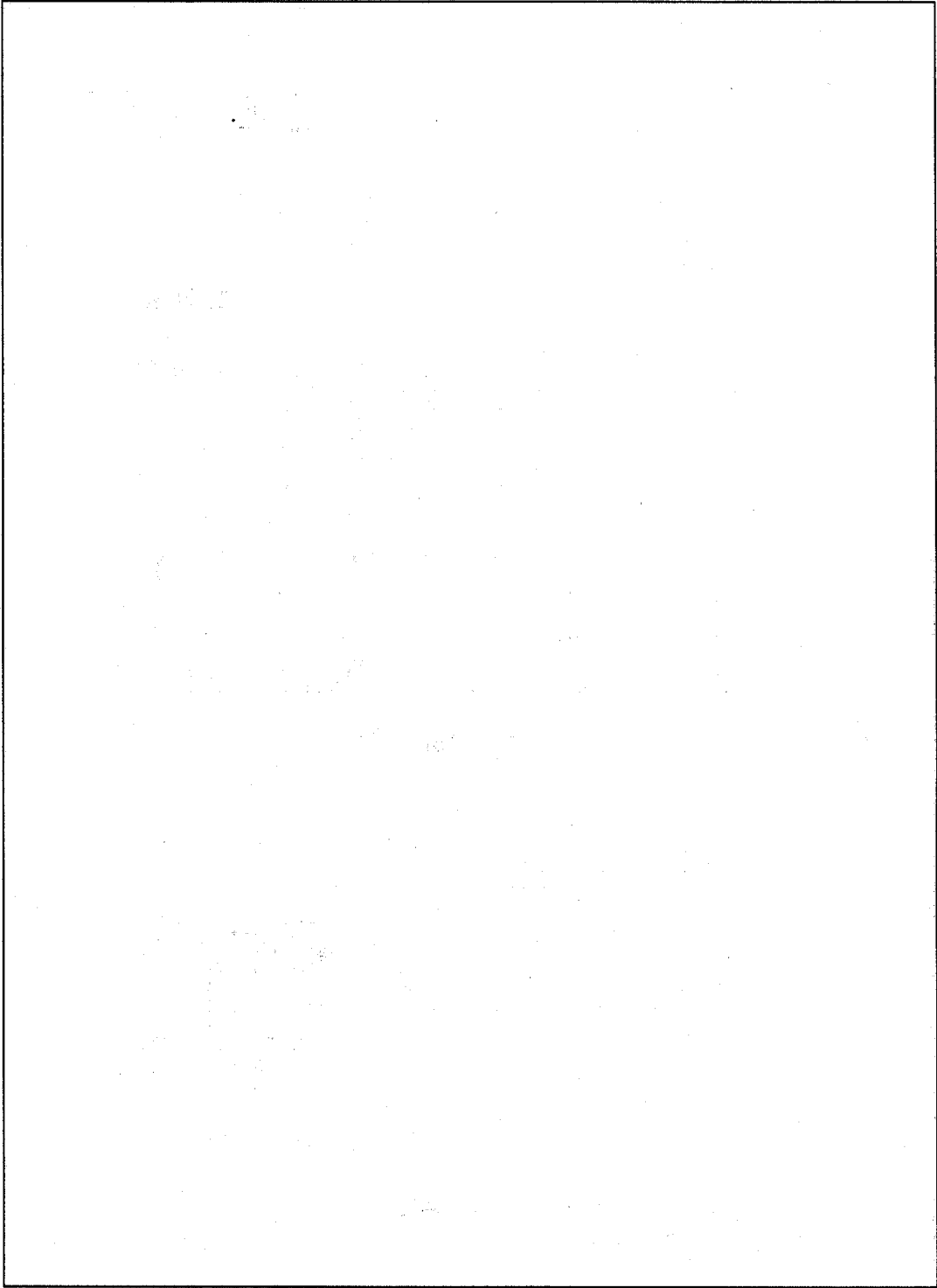
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.63	$0.60 + 0.016 * SL$	$0.61 + 0.012 * SL$	$0.63 + 0.011 * SL$
	tPHL	0.46	$0.44 + 0.014 * SL$	$0.45 + 0.010 * SL$	$0.49 + 0.008 * SL$
	tR	0.30	$0.26 + 0.019 * SL$	$0.26 + 0.021 * SL$	$0.24 + 0.022 * SL$
	tF	0.22	$0.19 + 0.013 * SL$	$0.19 + 0.012 * SL$	$0.23 + 0.010 * SL$
RN to Q	tPLH	0.60	$0.57 + 0.015 * SL$	$0.58 + 0.012 * SL$	$0.61 + 0.010 * SL$
	tPHL	0.70	$0.67 + 0.015 * SL$	$0.68 + 0.010 * SL$	$0.73 + 0.008 * SL$
	tR	0.30	$0.26 + 0.019 * SL$	$0.25 + 0.021 * SL$	$0.23 + 0.022 * SL$
	tF	0.31	$0.29 + 0.013 * SL$	$0.29 + 0.011 * SL$	$0.33 + 0.009 * SL$
SN to Q	tPLH	1.13	$1.10 + 0.016 * SL$	$1.11 + 0.012 * SL$	$1.14 + 0.010 * SL$
	tR	0.30	$0.26 + 0.018 * SL$	$0.25 + 0.021 * SL$	$0.23 + 0.022 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD4D4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.233
Input Setup Time (D to CK)	tSU	0.342
Recovery Time (RN)	tRC	0.178
Recovery Time (SN)	tRC	0.139



# FD4S/FD4SD2

D Flip-Flop with Set, Reset, and Scan, Positive Edge Trigger, 1X Drive or 2X Drive

Inputs: D, TI, TE, CK, SN, RN

Outputs: Q, QN

Input Loading (SL):

- D, TI, CK: 1

- TE, SN, RN: 2

Maximum Fanout (Rec. SL):

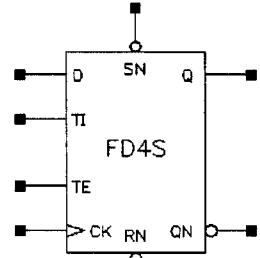
FD4S: All : 28

FD4SD2: All : 56

Gate Count:

FD4S: 11

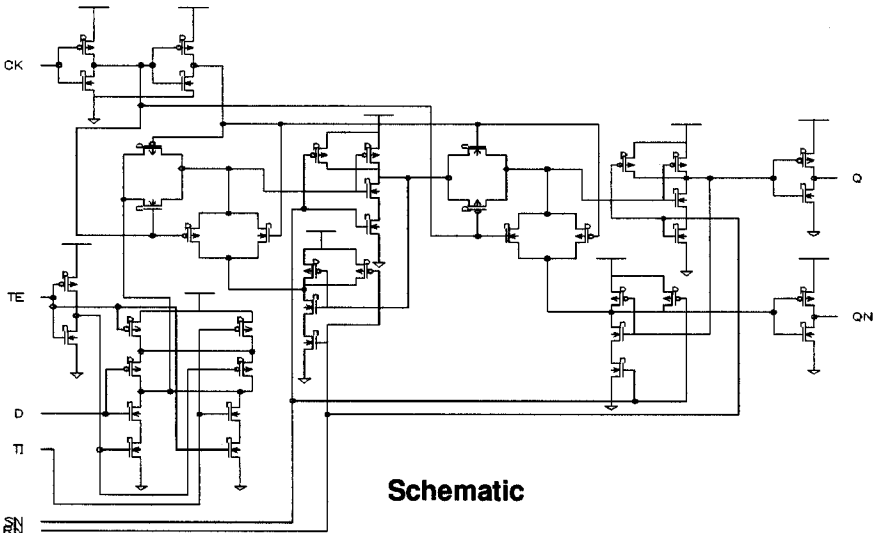
FD4SD2: 12



**Symbol**

D	SN	RN	TI	TE	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	1	x	0		0	1
1	1	1	x	0		1	0
x	1	1	0	1		0	1
x	1	1	1	1		1	0
x	0	1	x	x	x	1	0
x	1	0	x	x	x	0	1
x	0	0	x	x	x	0	0
x	1	1	x	x		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FD4S Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_r$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.86	$0.77 + 0.044 \cdot SL$	$0.78 + 0.042 \cdot SL$	$0.77 + 0.043 \cdot SL$
	tR	0.33	$0.13 + 0.097 \cdot SL$	$0.12 + 0.101 \cdot SL$	$0.10 + 0.102 \cdot SL$
RN to Q	tPLH	0.31	$0.22 + 0.045 \cdot SL$	$0.22 + 0.042 \cdot SL$	$0.22 + 0.043 \cdot SL$
	tPHL	0.46	$0.40 + 0.031 \cdot SL$	$0.42 + 0.022 \cdot SL$	$0.46 + 0.020 \cdot SL$
	tR	0.33	$0.14 + 0.097 \cdot SL$	$0.13 + 0.100 \cdot SL$	$0.10 + 0.102 \cdot SL$
	tF	0.22	$0.15 + 0.034 \cdot SL$	$0.15 + 0.035 \cdot SL$	$0.11 + 0.038 \cdot SL$
CK to Q	tPLH	0.65	$0.56 + 0.045 \cdot SL$	$0.57 + 0.043 \cdot SL$	$0.57 + 0.043 \cdot SL$
	tPHL	0.61	$0.55 + 0.029 \cdot SL$	$0.58 + 0.022 \cdot SL$	$0.61 + 0.020 \cdot SL$
	tR	0.33	$0.13 + 0.098 \cdot SL$	$0.12 + 0.101 \cdot SL$	$0.10 + 0.102 \cdot SL$
	tF	0.19	$0.12 + 0.035 \cdot SL$	$0.11 + 0.037 \cdot SL$	$0.09 + 0.038 \cdot SL$
SN to QN	tPLH	0.32	$0.23 + 0.044 \cdot SL$	$0.24 + 0.041 \cdot SL$	$0.24 + 0.041 \cdot SL$
	tPHL	0.44	$0.38 + 0.030 \cdot SL$	$0.41 + 0.021 \cdot SL$	$0.44 + 0.020 \cdot SL$
	tR	0.32	$0.14 + 0.091 \cdot SL$	$0.13 + 0.095 \cdot SL$	$0.09 + 0.097 \cdot SL$
	tF	0.22	$0.15 + 0.033 \cdot SL$	$0.14 + 0.035 \cdot SL$	$0.09 + 0.038 \cdot SL$
RN to QN	tPLH	0.70	$0.62 + 0.041 \cdot SL$	$0.62 + 0.041 \cdot SL$	$0.61 + 0.041 \cdot SL$
	tR	0.31	$0.12 + 0.093 \cdot SL$	$0.12 + 0.096 \cdot SL$	$0.09 + 0.097 \cdot SL$
CK to QN	tPLH	0.85	$0.76 + 0.041 \cdot SL$	$0.76 + 0.041 \cdot SL$	$0.76 + 0.041 \cdot SL$
	tPHL	0.73	$0.67 + 0.027 \cdot SL$	$0.69 + 0.021 \cdot SL$	$0.72 + 0.020 \cdot SL$
	tR	0.31	$0.12 + 0.093 \cdot SL$	$0.12 + 0.096 \cdot SL$	$0.09 + 0.097 \cdot SL$
	tF	0.18	$0.11 + 0.033 \cdot SL$	$0.10 + 0.036 \cdot SL$	$0.07 + 0.038 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD4S Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.725
Input Setup Time (TE to CK)	tSU	0.944
Input Setup Time (TI to CK)	tSU	0.780

# FD4S

D Flip-Flop with Set, Reset, and Scan, Positive Edge Trigger, 1X Drive

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## FD4S Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Recovery Time (RN)	t <sub>RC</sub>	0.139
Recovery Time (SN)	t <sub>RC</sub>	0.139

**FD4SD2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.86	$0.82 + 0.023^*SL$	$0.82 + 0.021^*SL$	$0.83 + 0.021^*SL$
	tR	0.24	$0.15 + 0.045^*SL$	$0.14 + 0.049^*SL$	$0.11 + 0.050^*SL$
RN to Q	tPLH	0.30	$0.25 + 0.023^*SL$	$0.26 + 0.021^*SL$	$0.27 + 0.021^*SL$
	tPHL	0.46	$0.42 + 0.019^*SL$	$0.44 + 0.013^*SL$	$0.49 + 0.010^*SL$
	tR	0.24	$0.14 + 0.048^*SL$	$0.14 + 0.048^*SL$	$0.11 + 0.050^*SL$
	tF	0.21	$0.17 + 0.018^*SL$	$0.17 + 0.017^*SL$	$0.16 + 0.018^*SL$
CK to Q	tPLH	0.65	$0.60 + 0.024^*SL$	$0.61 + 0.021^*SL$	$0.61 + 0.021^*SL$
	tPHL	0.62	$0.59 + 0.018^*SL$	$0.60 + 0.012^*SL$	$0.64 + 0.010^*SL$
	tR	0.23	$0.14 + 0.047^*SL$	$0.13 + 0.049^*SL$	$0.11 + 0.050^*SL$
	tF	0.17	$0.14 + 0.019^*SL$	$0.14 + 0.018^*SL$	$0.13 + 0.018^*SL$
SN to QN	tPLH	0.32	$0.27 + 0.023^*SL$	$0.28 + 0.020^*SL$	$0.28 + 0.020^*SL$
	tPHL	0.45	$0.41 + 0.019^*SL$	$0.43 + 0.012^*SL$	$0.48 + 0.010^*SL$
	tR	0.23	$0.14 + 0.044^*SL$	$0.14 + 0.045^*SL$	$0.11 + 0.046^*SL$
	tF	0.20	$0.16 + 0.017^*SL$	$0.17 + 0.017^*SL$	$0.14 + 0.018^*SL$
RN to QN	tPLH	0.75	$0.71 + 0.020^*SL$	$0.71 + 0.020^*SL$	$0.71 + 0.020^*SL$
	tR	0.22	$0.14 + 0.044^*SL$	$0.13 + 0.045^*SL$	$0.11 + 0.047^*SL$
CK to QN	tPLH	0.90	$0.86 + 0.020^*SL$	$0.86 + 0.020^*SL$	$0.86 + 0.020^*SL$
	tPHL	0.79	$0.76 + 0.016^*SL$	$0.77 + 0.012^*SL$	$0.80 + 0.010^*SL$
	tR	0.22	$0.14 + 0.044^*SL$	$0.13 + 0.045^*SL$	$0.11 + 0.047^*SL$
	tF	0.16	$0.13 + 0.019^*SL$	$0.13 + 0.018^*SL$	$0.11 + 0.019^*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD4SD2 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.725
Input Setup Time (TE to CK)	tSU	0.944
Input Setup Time (TI to CK)	tSU	0.780

## FD4SD2

D Flip-Flop with Set, Reset, Scan, Positive Edge Trigger and 2X Drive

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### FD4SD2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Recovery Time (RN)	t <sub>RC</sub>	0.139
Recovery Time (SN)	t <sub>RC</sub>	0.139





# FD4SD2Q /FD4SD4Q

D Flip-Flop with Set, Reset, Scan, Positive Edge Trigger, Q Output Only, 2X or 4X Drive

Inputs: D, TI, TE, CK, SN, RN

Output: Q

Input Loading (SL):

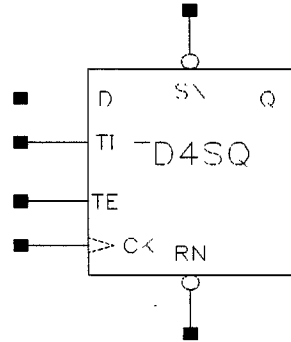
- FD4SD2Q: D, CK, TI: 1  
RN, SN, TE: 2
- FD4SD4Q: D, CK, TI: 1  
RN, SN, TE: 2

Maximum Fanout (Rec. SL):

- FD4SD2Q: 56
- FD4SD4Q: 112

Gate Count:

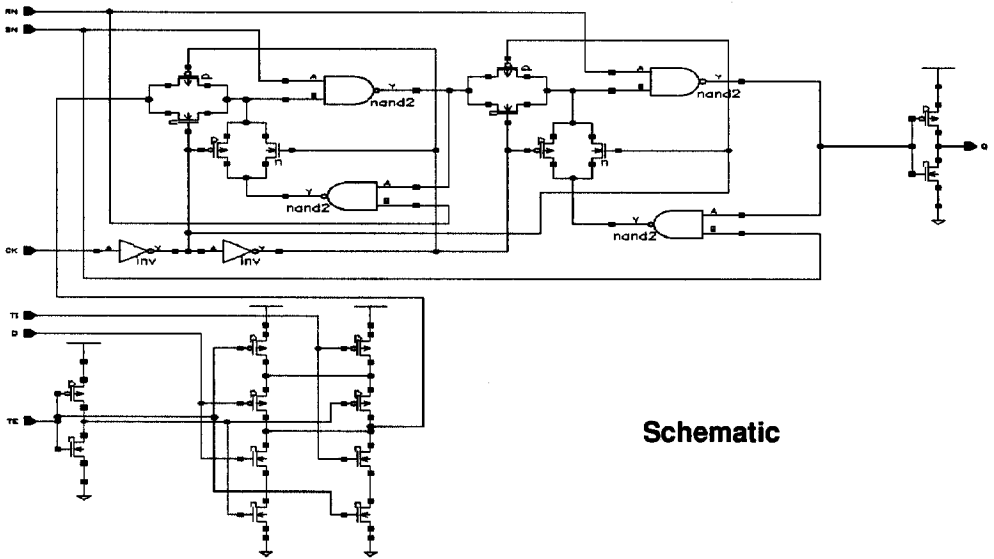
- FD4SD2Q: 11
- FD4SD4Q: 12



Symbol

D	SN	RN	TI	TE	CK	Qn+1
0	1	1	x	0		0
1	1	1	x	0		1
x	1	1	0	1		0
x	1	1	1	1		1
x	0	1	x	x	x	1
x	1	0	x	x	x	0
x	0	0	x	x	x	0
x	1	1	x	x		Qn

Truth Table



Schematic

**FD4SD2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.86	$0.81 + 0.023 \cdot SL$	$0.82 + 0.020 \cdot SL$	$0.83 + 0.020 \cdot SL$
	tR	0.23	$0.15 + 0.042 \cdot SL$	$0.14 + 0.046 \cdot SL$	$0.11 + 0.047 \cdot SL$
RN to Q	tPLH	0.30	$0.26 + 0.023 \cdot SL$	$0.26 + 0.020 \cdot SL$	$0.27 + 0.020 \cdot SL$
	tPHL	0.45	$0.41 + 0.019 \cdot SL$	$0.43 + 0.013 \cdot SL$	$0.48 + 0.010 \cdot SL$
	tR	0.23	$0.15 + 0.044 \cdot SL$	$0.14 + 0.046 \cdot SL$	$0.12 + 0.047 \cdot SL$
	tF	0.20	$0.16 + 0.020 \cdot SL$	$0.17 + 0.017 \cdot SL$	$0.15 + 0.018 \cdot SL$
CK to Q	tPLH	0.65	$0.60 + 0.023 \cdot SL$	$0.61 + 0.021 \cdot SL$	$0.62 + 0.020 \cdot SL$
	tPHL	0.62	$0.58 + 0.018 \cdot SL$	$0.60 + 0.012 \cdot SL$	$0.64 + 0.010 \cdot SL$
	tR	0.23	$0.14 + 0.046 \cdot SL$	$0.14 + 0.046 \cdot SL$	$0.11 + 0.047 \cdot SL$
	tF	0.17	$0.13 + 0.018 \cdot SL$	$0.13 + 0.018 \cdot SL$	$0.12 + 0.019 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD4SD2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.725
Input Setup Time (TE to CK)	tSU	0.944
Input Setup Time (TI to CK)	tSU	0.780
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

# FD4SD4Q

D Flip-Flop with Set, Reset, and Scan, Positive Edge Trigger, Q Output Only, 4X Drive

## FD4SD4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.93	$0.91 + 0.012*SL$	$0.91 + 0.011*SL$	$0.92 + 0.010*SL$
	tR	0.21	$0.17 + 0.022*SL$	$0.17 + 0.022*SL$	$0.15 + 0.023*SL$
RN to Q	tPLH	0.36	$0.34 + 0.013*SL$	$0.34 + 0.011*SL$	$0.36 + 0.010*SL$
	tPHL	0.50	$0.48 + 0.012*SL$	$0.49 + 0.008*SL$	$0.53 + 0.006*SL$
	tR	0.22	$0.18 + 0.019*SL$	$0.17 + 0.022*SL$	$0.16 + 0.023*SL$
	tF	0.22	$0.20 + 0.010*SL$	$0.20 + 0.009*SL$	$0.21 + 0.008*SL$
CK to Q	tPLH	0.71	$0.69 + 0.013*SL$	$0.69 + 0.011*SL$	$0.71 + 0.010*SL$
	tPHL	0.67	$0.65 + 0.010*SL$	$0.66 + 0.008*SL$	$0.69 + 0.006*SL$
	tR	0.22	$0.18 + 0.020*SL$	$0.17 + 0.022*SL$	$0.15 + 0.023*SL$
	tF	0.20	$0.18 + 0.011*SL$	$0.18 + 0.009*SL$	$0.18 + 0.009*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD4SD4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (D to CK)	tSU	0.725
Input Setup Time (TE to CK)	tSU	0.944
Input Setup Time (TI to CK)	tSU	0.780
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



# FD4D2X4Q /FD4D4X4Q

4-Bit D Flip-Flop with Set, Reset, Positive Edge Trigger, Q Output Only, 2X or 4X Drive

Inputs: D0, D1, D2, D3, CK, RN, SN

Outputs: Q, Q1, Q2, Q3

Input Loading (SL):

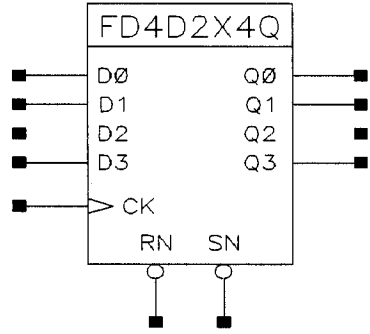
- FD4D2X4Q: CK: 1, RN, SN: 8  
D0, D1, D2, D3: 3
- FD4D4X4Q: CK: 1, RN, SN: 8  
D0, D1, D2, D3: 3

Maximum Fanout (Rec. SL):

- FD4D2X4Q: 56
- FD4D4X4Q: 112

Gate Count:

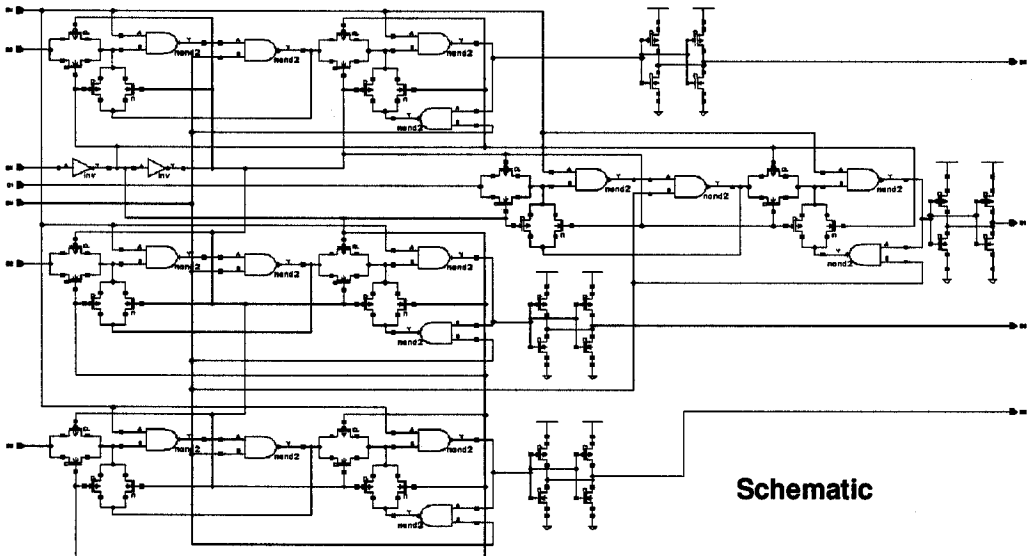
- FD4D2X4Q: 29
- FD4D4X4Q: 33



Symbol

D	SN	RN	CK	Qn+1
0	1	1		0
1	1	1		1
x	0	1	x	1
x	1	0	x	0
x	0	0	x	0
x	1	1		Qn

Truth Table



Schematic

## FD4D2X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	tPLH	0.93	$0.88 + 0.026^*SL$	$0.89 + 0.022^*SL$	$0.92 + 0.020^*SL$
	tPHL	0.69	$0.64 + 0.023^*SL$	$0.66 + 0.015^*SL$	$0.73 + 0.012^*SL$
	tR	0.29	$0.21 + 0.044^*SL$	$0.20 + 0.046^*SL$	$0.18 + 0.047^*SL$
	tF	0.25	$0.20 + 0.022^*SL$	$0.21 + 0.020^*SL$	$0.23 + 0.019^*SL$
RN to Q0	tPLH	0.53	$0.48 + 0.026^*SL$	$0.50 + 0.022^*SL$	$0.52 + 0.020^*SL$
	tPHL	0.64	$0.59 + 0.025^*SL$	$0.61 + 0.016^*SL$	$0.70 + 0.012^*SL$
	tR	0.29	$0.21 + 0.042^*SL$	$0.20 + 0.045^*SL$	$0.17 + 0.047^*SL$
	tF	0.29	$0.24 + 0.025^*SL$	$0.25 + 0.019^*SL$	$0.28 + 0.018^*SL$
SN to Q0	tPLH	1.06	$1.01 + 0.026^*SL$	$1.02 + 0.022^*SL$	$1.05 + 0.021^*SL$
	tR	0.29	$0.21 + 0.043^*SL$	$0.20 + 0.045^*SL$	$0.17 + 0.047^*SL$
CK to Q1	tPLH	0.93	$0.87 + 0.026^*SL$	$0.89 + 0.022^*SL$	$0.91 + 0.021^*SL$
	tPHL	0.68	$0.64 + 0.023^*SL$	$0.66 + 0.015^*SL$	$0.73 + 0.012^*SL$
	tR	0.30	$0.21 + 0.046^*SL$	$0.20 + 0.049^*SL$	$0.18 + 0.050^*SL$
	tF	0.25	$0.21 + 0.023^*SL$	$0.21 + 0.020^*SL$	$0.23 + 0.019^*SL$
RN to Q1	tPLH	0.53	$0.48 + 0.027^*SL$	$0.49 + 0.022^*SL$	$0.52 + 0.021^*SL$
	tPHL	0.63	$0.58 + 0.025^*SL$	$0.61 + 0.016^*SL$	$0.70 + 0.012^*SL$
	tR	0.30	$0.21 + 0.045^*SL$	$0.20 + 0.048^*SL$	$0.17 + 0.050^*SL$
	tF	0.29	$0.24 + 0.024^*SL$	$0.26 + 0.019^*SL$	$0.28 + 0.018^*SL$
SN to Q1	tPLH	1.06	$1.01 + 0.027^*SL$	$1.02 + 0.022^*SL$	$1.04 + 0.021^*SL$
	tR	0.30	$0.21 + 0.045^*SL$	$0.20 + 0.048^*SL$	$0.17 + 0.050^*SL$
CK to Q2	tPLH	0.93	$0.88 + 0.027^*SL$	$0.89 + 0.022^*SL$	$0.92 + 0.021^*SL$
	tPHL	0.68	$0.64 + 0.023^*SL$	$0.66 + 0.015^*SL$	$0.73 + 0.012^*SL$
	tR	0.30	$0.21 + 0.046^*SL$	$0.20 + 0.049^*SL$	$0.18 + 0.050^*SL$
	tF	0.25	$0.21 + 0.023^*SL$	$0.21 + 0.020^*SL$	$0.23 + 0.019^*SL$
RN to Q2	tPLH	0.53	$0.48 + 0.027^*SL$	$0.49 + 0.022^*SL$	$0.52 + 0.021^*SL$
	tPHL	0.63	$0.58 + 0.025^*SL$	$0.61 + 0.016^*SL$	$0.70 + 0.012^*SL$
	tR	0.30	$0.21 + 0.045^*SL$	$0.20 + 0.048^*SL$	$0.17 + 0.050^*SL$
	tF	0.29	$0.24 + 0.024^*SL$	$0.26 + 0.019^*SL$	$0.28 + 0.018^*SL$
SN to Q2	tPLH	1.06	$1.01 + 0.027^*SL$	$1.02 + 0.022^*SL$	$1.04 + 0.021^*SL$
	tR	0.30	$0.21 + 0.045^*SL$	$0.20 + 0.048^*SL$	$0.17 + 0.050^*SL$
CK to Q3	tPLH	0.93	$0.88 + 0.026^*SL$	$0.89 + 0.022^*SL$	$0.92 + 0.021^*SL$
	tPHL	0.69	$0.64 + 0.023^*SL$	$0.66 + 0.015^*SL$	$0.73 + 0.012^*SL$
	tR	0.30	$0.21 + 0.044^*SL$	$0.20 + 0.047^*SL$	$0.18 + 0.048^*SL$
	tF	0.25	$0.20 + 0.022^*SL$	$0.21 + 0.020^*SL$	$0.23 + 0.019^*SL$
RN to Q3	tPLH	0.54	$0.48 + 0.027^*SL$	$0.50 + 0.022^*SL$	$0.52 + 0.021^*SL$
	tPHL	0.64	$0.59 + 0.025^*SL$	$0.61 + 0.016^*SL$	$0.70 + 0.012^*SL$
	tR	0.30	$0.21 + 0.043^*SL$	$0.20 + 0.046^*SL$	$0.18 + 0.048^*SL$
	tF	0.29	$0.24 + 0.025^*SL$	$0.25 + 0.019^*SL$	$0.28 + 0.018^*SL$
SN to Q3	tPLH	1.06	$1.01 + 0.027^*SL$	$1.02 + 0.022^*SL$	$1.05 + 0.021^*SL$
	tR	0.29	$0.21 + 0.044^*SL$	$0.20 + 0.046^*SL$	$0.17 + 0.048^*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# FD4D2X4Q

4-Bit D Flip-Flop with Set, Reset, Positive Edge Trigger, Q Output Only, 2X Drive

## FD4D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.959
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D0 to CK)	tHD	0.452
Input Hold Time (D1 to CK)	tHD	0.452
Input Hold Time (D2 to CK)	tHD	0.452
Input Hold Time (D3 to CK)	tHD	0.452
Input Setup Time (D0 to CK)	tSU	0.233
Input Setup Time (D1 to CK)	tSU	0.233
Input Setup Time (D2 to CK)	tSU	0.233
Input Setup Time (D3 to CK)	tSU	0.233
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

**FD4D4X4Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	tPLH	1.02	$0.99 + 0.016 * SL$	$1.00 + 0.012 * SL$	$1.02 + 0.011 * SL$
	tPHL	0.78	$0.76 + 0.014 * SL$	$0.77 + 0.010 * SL$	$0.82 + 0.008 * SL$
	tR	0.31	$0.27 + 0.021 * SL$	$0.27 + 0.021 * SL$	$0.24 + 0.023 * SL$
	tF	0.30	$0.27 + 0.014 * SL$	$0.28 + 0.011 * SL$	$0.31 + 0.009 * SL$
RN to Q0	tPLH	0.61	$0.58 + 0.015 * SL$	$0.59 + 0.012 * SL$	$0.61 + 0.010 * SL$
	tPHL	0.69	$0.66 + 0.014 * SL$	$0.68 + 0.010 * SL$	$0.73 + 0.008 * SL$
	tR	0.30	$0.26 + 0.020 * SL$	$0.26 + 0.021 * SL$	$0.23 + 0.022 * SL$
	tF	0.31	$0.28 + 0.013 * SL$	$0.29 + 0.011 * SL$	$0.33 + 0.009 * SL$
SN to Q0	tPLH	1.13	$1.10 + 0.016 * SL$	$1.11 + 0.012 * SL$	$1.14 + 0.010 * SL$
	tR	0.30	$0.26 + 0.018 * SL$	$0.25 + 0.021 * SL$	$0.23 + 0.022 * SL$
CK to Q1	tPLH	1.01	$0.98 + 0.016 * SL$	$0.99 + 0.012 * SL$	$1.02 + 0.011 * SL$
	tPHL	0.78	$0.75 + 0.014 * SL$	$0.77 + 0.010 * SL$	$0.81 + 0.008 * SL$
	tR	0.31	$0.27 + 0.021 * SL$	$0.27 + 0.022 * SL$	$0.24 + 0.023 * SL$
	tF	0.30	$0.28 + 0.014 * SL$	$0.29 + 0.011 * SL$	$0.31 + 0.010 * SL$
RN to Q1	tPLH	0.60	$0.57 + 0.015 * SL$	$0.58 + 0.012 * SL$	$0.61 + 0.011 * SL$
	tPHL	0.69	$0.66 + 0.015 * SL$	$0.67 + 0.010 * SL$	$0.72 + 0.008 * SL$
	tR	0.30	$0.26 + 0.020 * SL$	$0.26 + 0.022 * SL$	$0.23 + 0.023 * SL$
	tF	0.31	$0.29 + 0.013 * SL$	$0.29 + 0.011 * SL$	$0.33 + 0.009 * SL$
SN to Q1	tPLH	1.13	$1.10 + 0.015 * SL$	$1.11 + 0.012 * SL$	$1.14 + 0.011 * SL$
	tR	0.30	$0.26 + 0.019 * SL$	$0.25 + 0.022 * SL$	$0.23 + 0.023 * SL$
CK to Q2	tPLH	1.01	$0.98 + 0.015 * SL$	$0.99 + 0.012 * SL$	$1.02 + 0.011 * SL$
	tPHL	0.78	$0.75 + 0.014 * SL$	$0.77 + 0.010 * SL$	$0.81 + 0.008 * SL$
	tR	0.31	$0.27 + 0.020 * SL$	$0.27 + 0.022 * SL$	$0.24 + 0.023 * SL$
	tF	0.30	$0.28 + 0.014 * SL$	$0.29 + 0.011 * SL$	$0.31 + 0.010 * SL$
RN to Q2	tPLH	0.60	$0.57 + 0.015 * SL$	$0.58 + 0.012 * SL$	$0.61 + 0.011 * SL$
	tPHL	0.69	$0.66 + 0.015 * SL$	$0.67 + 0.010 * SL$	$0.72 + 0.008 * SL$
	tR	0.30	$0.26 + 0.020 * SL$	$0.26 + 0.022 * SL$	$0.23 + 0.023 * SL$
	tF	0.31	$0.29 + 0.013 * SL$	$0.29 + 0.011 * SL$	$0.33 + 0.009 * SL$
SN to Q2	tPLH	1.13	$1.10 + 0.016 * SL$	$1.11 + 0.012 * SL$	$1.14 + 0.011 * SL$
	tR	0.30	$0.26 + 0.020 * SL$	$0.25 + 0.022 * SL$	$0.23 + 0.023 * SL$
CK to Q3	tPLH	1.02	$0.99 + 0.016 * SL$	$1.00 + 0.012 * SL$	$1.03 + 0.011 * SL$
	tPHL	0.78	$0.76 + 0.014 * SL$	$0.77 + 0.010 * SL$	$0.82 + 0.008 * SL$
	tR	0.31	$0.27 + 0.021 * SL$	$0.27 + 0.021 * SL$	$0.24 + 0.023 * SL$
	tF	0.30	$0.27 + 0.014 * SL$	$0.28 + 0.011 * SL$	$0.31 + 0.009 * SL$
RN to Q3	tPLH	0.61	$0.58 + 0.016 * SL$	$0.59 + 0.012 * SL$	$0.61 + 0.011 * SL$
	tPHL	0.69	$0.66 + 0.014 * SL$	$0.68 + 0.010 * SL$	$0.73 + 0.008 * SL$
	tR	0.30	$0.26 + 0.020 * SL$	$0.26 + 0.021 * SL$	$0.23 + 0.023 * SL$
	tF	0.31	$0.28 + 0.013 * SL$	$0.29 + 0.011 * SL$	$0.33 + 0.009 * SL$
SN to Q3	tPLH	1.13	$1.10 + 0.016 * SL$	$1.12 + 0.012 * SL$	$1.14 + 0.011 * SL$
	tR	0.30	$0.26 + 0.018 * SL$	$0.25 + 0.022 * SL$	$0.23 + 0.023 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



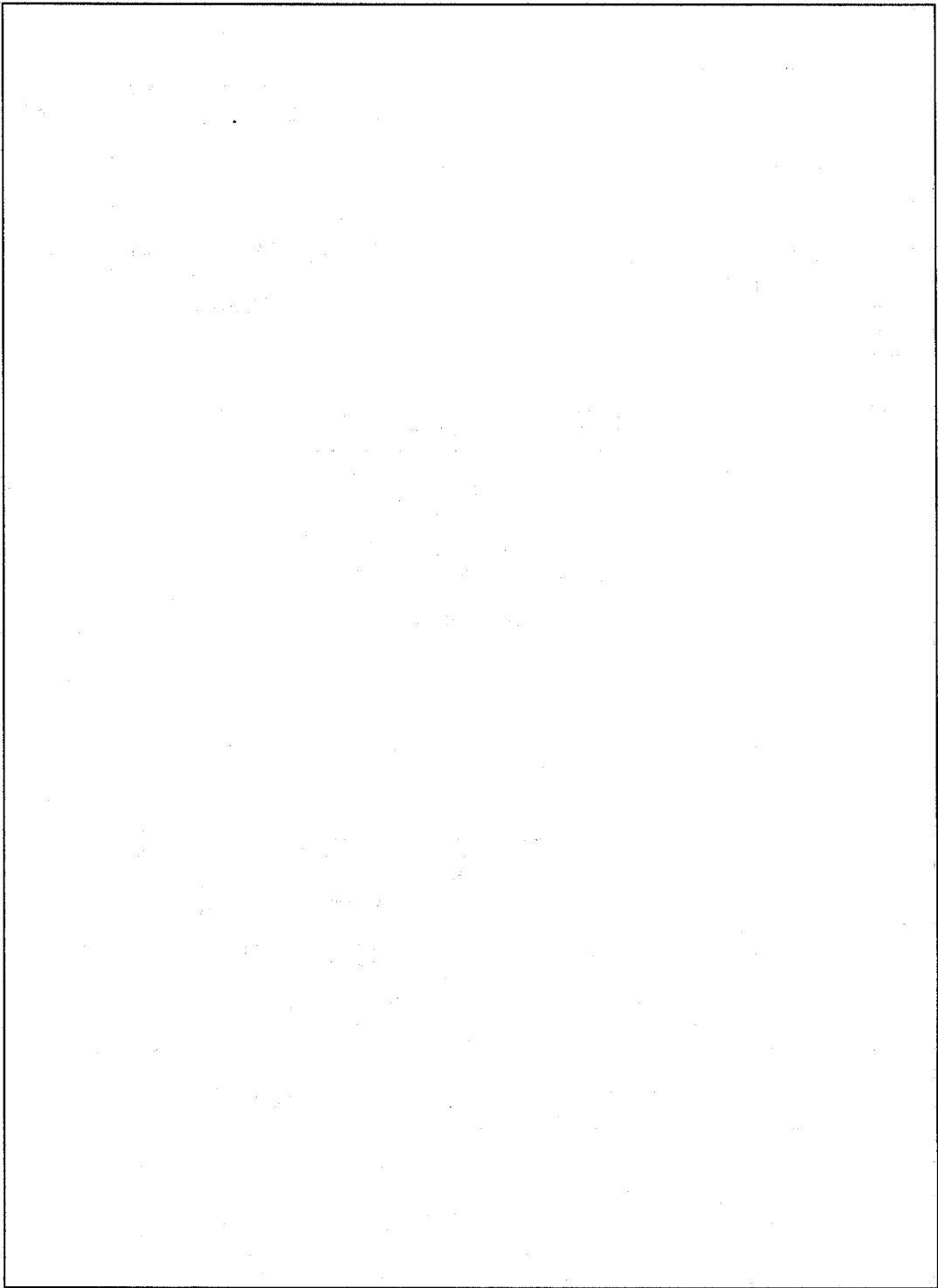
# FD4D4X4Q

4-Bit D Flip-Flop with Set, Reset, Positive Edge Trigger, Q Output Only, 4X Drive

## FD4D4X4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.998
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (D0 to CK)	tHD	0.452
Input Hold Time (D1 to CK)	tHD	0.452
Input Hold Time (D2 to CK)	tHD	0.452
Input Hold Time (D3 to CK)	tHD	0.452
Input Setup Time (D0 to CK)	tSU	0.233
Input Setup Time (D1 to CK)	tSU	0.233
Input Setup Time (D2 to CK)	tSU	0.233
Input Setup Time (D3 to CK)	tSU	0.233
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



# FD5/FD5D2

D Flip-Flop with Negative Edge Trigger, 1X Drive or 2X Drive

Inputs: D, CKN

Outputs: Q, QN

Input Loading (SL):

FD5: All: 1

FD5D2: All: 1

Maximum Fanout (Rec. SL):

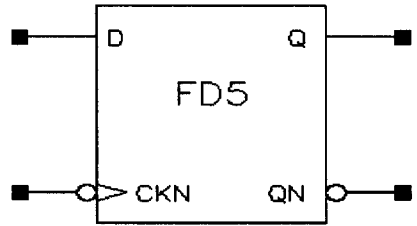
FD5: All: 28

FD5D2: All: 56

Gate Count

FD5: 6

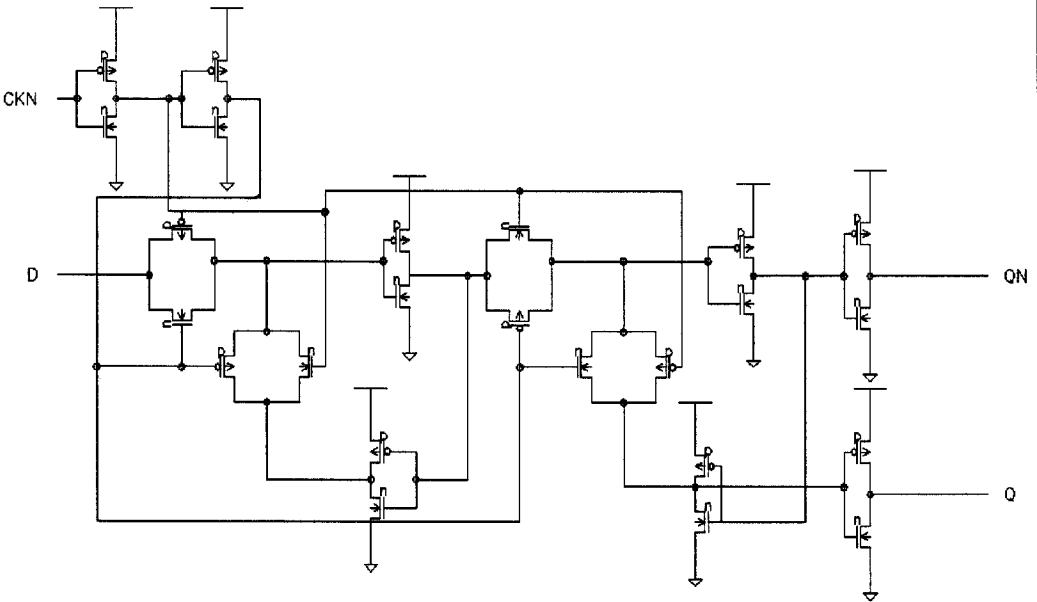
FD5D2 : 7



Symbol

D	CK	Qn+1	QNn+1
0		0	1
1		1	0
x		Qn	QNn

Truth Table



Schematic

**FD5 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.86	$0.78 + 0.040*SL$	$0.77 + 0.041*SL$	$0.77 + 0.041*SL$
	tPHL	0.84	$0.79 + 0.026*SL$	$0.80 + 0.021*SL$	$0.82 + 0.020*SL$
	tR	0.29	$0.10 + 0.093*SL$	$0.09 + 0.097*SL$	$0.08 + 0.097*SL$
	tF	0.16	$0.10 + 0.035*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$
CKN to QN	tPLH	0.77	$0.69 + 0.044*SL$	$0.69 + 0.043*SL$	$0.69 + 0.043*SL$
	tPHL	0.71	$0.66 + 0.027*SL$	$0.68 + 0.021*SL$	$0.70 + 0.020*SL$
	tR	0.31	$0.11 + 0.099*SL$	$0.10 + 0.102*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.037*SL$	$0.10 + 0.037*SL$	$0.07 + 0.039*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD5 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.342
Input Setup Time (D to CKN)	tSU	0.178

# FD5D2

## D Flip-Flop with Negative Edge Trigger, 2X Drive

### FD5D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

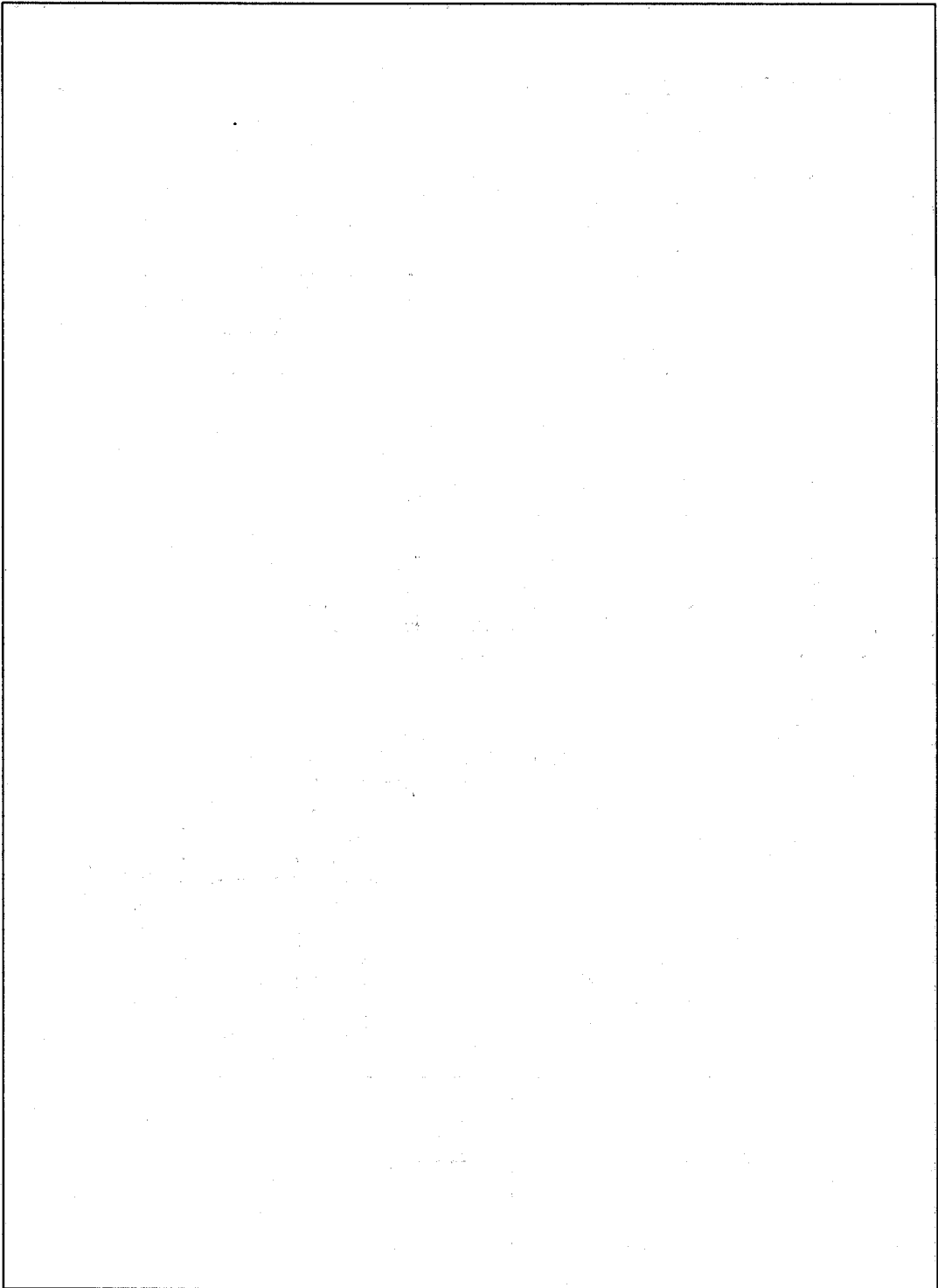
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.89	$0.86 + 0.018 \cdot \text{SL}$	$0.85 + 0.020 \cdot \text{SL}$	$0.85 + 0.020 \cdot \text{SL}$
	tPHL	0.89	$0.86 + 0.016 \cdot \text{SL}$	$0.87 + 0.012 \cdot \text{SL}$	$0.90 + 0.010 \cdot \text{SL}$
	tR	0.20	$0.11 + 0.045 \cdot \text{SL}$	$0.10 + 0.046 \cdot \text{SL}$	$0.08 + 0.047 \cdot \text{SL}$
	tF	0.15	$0.12 + 0.017 \cdot \text{SL}$	$0.11 + 0.018 \cdot \text{SL}$	$0.10 + 0.019 \cdot \text{SL}$
CKN to QN	tPLH	0.77	$0.72 + 0.022 \cdot \text{SL}$	$0.73 + 0.021 \cdot \text{SL}$	$0.73 + 0.021 \cdot \text{SL}$
	tPHL	0.72	$0.69 + 0.017 \cdot \text{SL}$	$0.70 + 0.012 \cdot \text{SL}$	$0.74 + 0.010 \cdot \text{SL}$
	tR	0.21	$0.12 + 0.046 \cdot \text{SL}$	$0.11 + 0.049 \cdot \text{SL}$	$0.09 + 0.050 \cdot \text{SL}$
	tF	0.16	$0.13 + 0.019 \cdot \text{SL}$	$0.13 + 0.019 \cdot \text{SL}$	$0.12 + 0.020 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

### FD5D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.342
Input Setup Time (D to CKN)	tSU	0.178



# FD5D2Q/FD5D4Q

D Flip-Flop with Negative Edge Trigger, Q Output Only, 2X Drive or 4X Drive

Inputs: D, CK

Output: Q

Input Loading (SL): All: D: 3, CKN: 1

Maximum Fanout (Rec. SL):

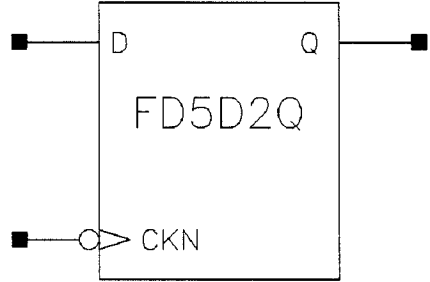
- FD5D2Q: 56

- FD5D4Q: 112

Gate Count:

- FD5D2Q: 6

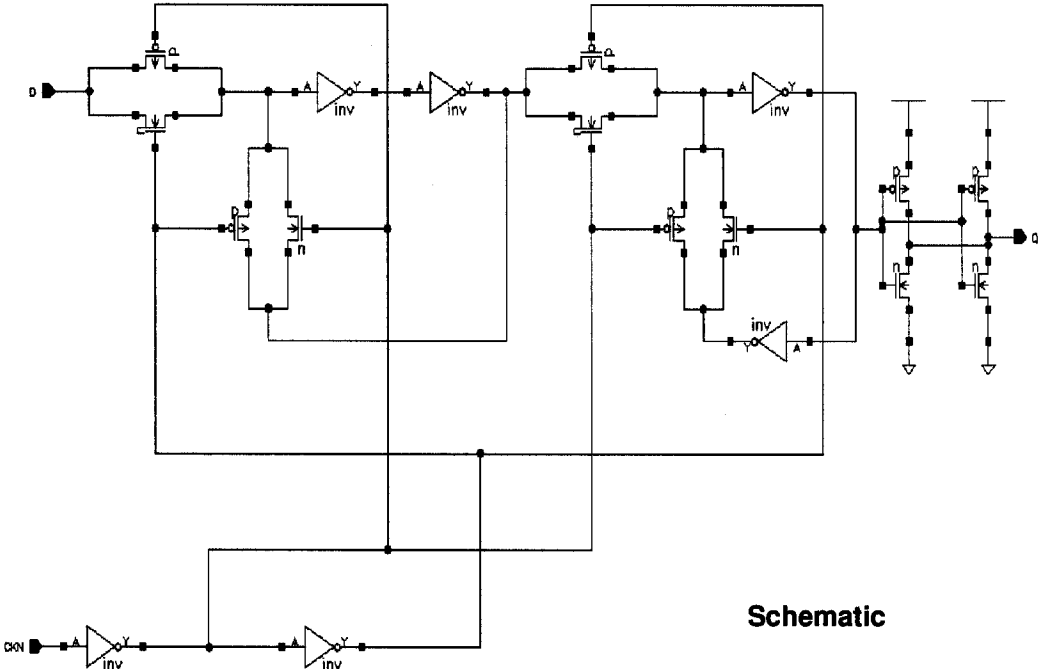
- FD5D4Q: 7



Symbol

D	CK	Q <sub>n+1</sub>
0		0
1		1
x		Q <sub>n</sub>

Truth Table



Schematic

**FD5D2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_{tr} = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.67	$0.62 + 0.025*SL$	$0.62 + 0.022*SL$	$0.64 + 0.021*SL$
	tPHL	0.63	$0.59 + 0.023*SL$	$0.61 + 0.016*SL$	$0.69 + 0.012*SL$
	tR	0.25	$0.15 + 0.051*SL$	$0.15 + 0.050*SL$	$0.13 + 0.052*SL$
	tF	0.22	$0.16 + 0.029*SL$	$0.18 + 0.022*SL$	$0.21 + 0.020*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD5D2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.397
Input Setup Time (D to CKN)	tSU	0.178

**FD5D4Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_{tr} = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.72	$0.69 + 0.014*SL$	$0.70 + 0.012*SL$	$0.71 + 0.011*SL$
	tPHL	0.67	$0.65 + 0.014*SL$	$0.66 + 0.010*SL$	$0.71 + 0.008*SL$
	tR	0.24	$0.20 + 0.021*SL$	$0.19 + 0.024*SL$	$0.17 + 0.025*SL$
	tF	0.24	$0.21 + 0.015*SL$	$0.22 + 0.013*SL$	$0.26 + 0.011*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD5D4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.397
Input Setup Time (D to CKN)	tSU	0.178



# FD5SD2Q/FD5SD4Q

D Flip-Flop with Scan, Negative Edge Trigger, Q Output Only, 2X Drive or 4X Drive

Inputs: D, TI, TE, CKN

Output: Q

Input Loading (SL):

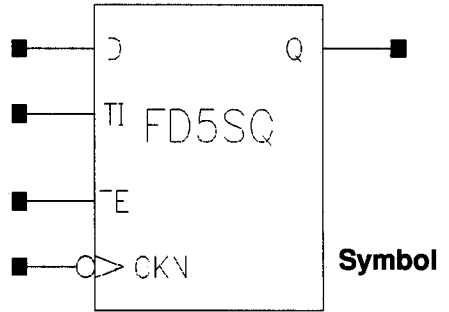
- FD5SD2Q: D, CKN, TI : 1  
TE : 2
- FD5SD4Q: D, CKN, TI : 1  
TE : 2

Maximum Fanout (Rec. SL):

- FD5SD2Q: 56
- FD5SD4Q: 112

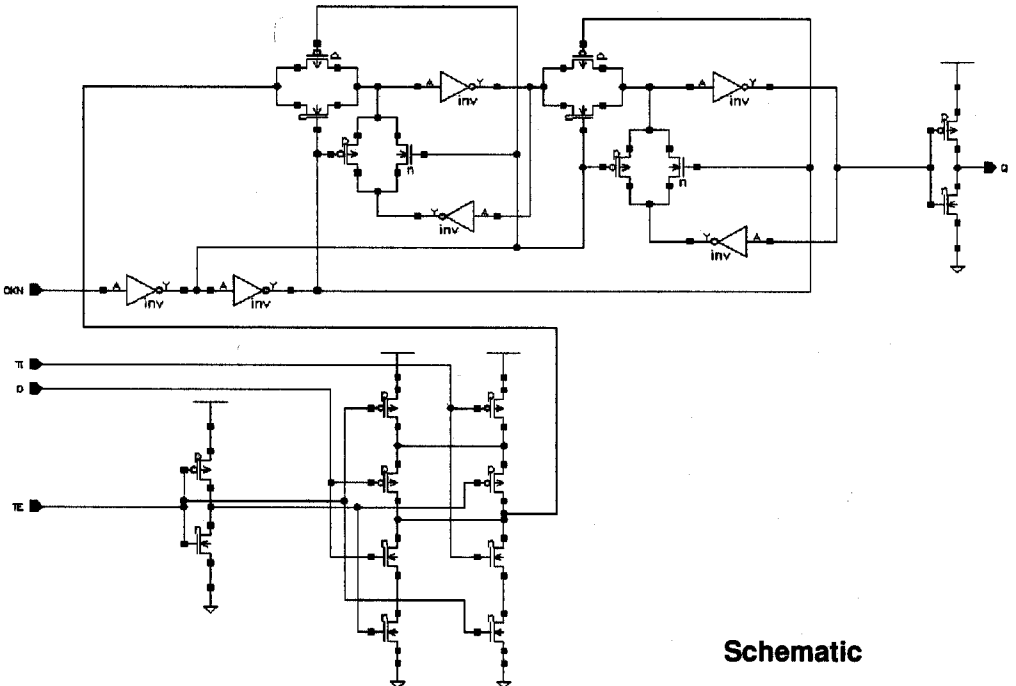
Gate Count:

- FD5SD2Q: 9
- FD5SD4Q: 10



D	TI	TE	CKN	Q <sub>n+1</sub>
0	x	0		0
1	x	0		1
x	0	1		0
x	1	1		1
x	x	x		QN

Truth Table



**FD5SD2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.76	$0.72 + 0.023*SL$	$0.72 + 0.022*SL$	$0.72 + 0.021*SL$
	tPHL	0.72	$0.69 + 0.018*SL$	$0.70 + 0.012*SL$	$0.74 + 0.011*SL$
	tR	0.21	$0.12 + 0.049*SL$	$0.11 + 0.051*SL$	$0.09 + 0.052*SL$
	tF	0.17	$0.13 + 0.021*SL$	$0.13 + 0.019*SL$	$0.12 + 0.020*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD5SD2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.123
Input Hold Time (TE to CKN)	tHD	0.123
Input Hold Time (TI to CKN)	tHD	0.069
Input Setup Time (D to CKN)	tSU	0.452
Input Setup Time (TE to CKN)	tSU	0.616
Input Setup Time (TI to CKN)	tSU	0.506

# FD5SD4Q

D Flip-Flop with Scan, Negative Edge Trigger, Q Output Only, 4X Drive

## FD5SD4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

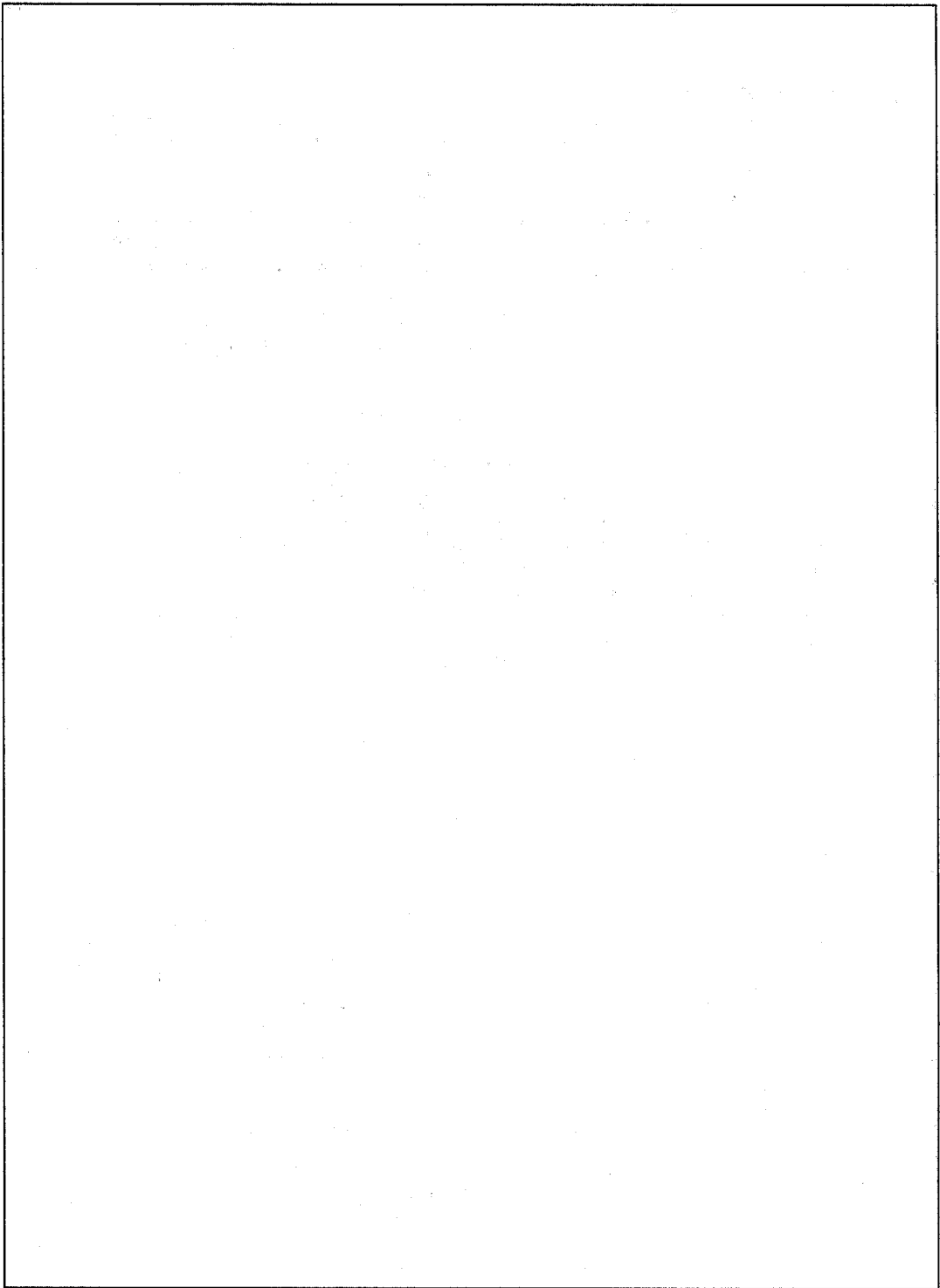
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.81	$0.78 + 0.012 * SL$	$0.78 + 0.011 * SL$	$0.79 + 0.011 * SL$
	tPHL	0.78	$0.76 + 0.011 * SL$	$0.77 + 0.008 * SL$	$0.80 + 0.006 * SL$
	tR	0.18	$0.14 + 0.022 * SL$	$0.13 + 0.025 * SL$	$0.12 + 0.026 * SL$
	tF	0.19	$0.18 + 0.009 * SL$	$0.17 + 0.010 * SL$	$0.18 + 0.010 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD5SD4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

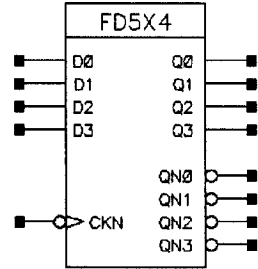
Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.123
Input Hold Time (TE to CKN)	tHD	0.123
Input Hold Time (TI to CKN)	tHD	0.069
Input Setup Time (D to CKN)	tSU	0.452
Input Setup Time (TE to CKN)	tSU	0.616
Input Setup Time (TI to CKN)	tSU	0.506



# FD5X4

## 4-Bit D Flip-Flop with Negative Edge Trigger

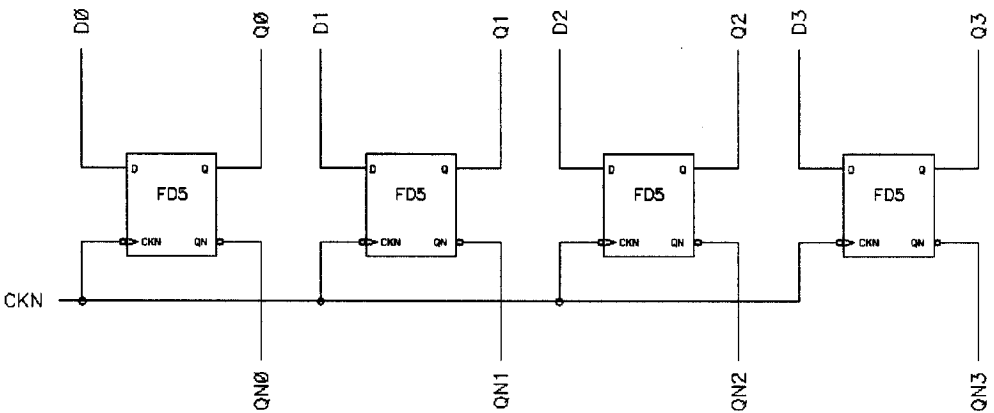
Inputs: D0, D1, D2, D3, CKN  
 Outputs: Q0, Q1, Q2, Q3,  
 QN0, QN1, QN2, QN3  
 Input Loading (SL):  
 - D0, D1, D2, D3: 3  
 - CKN: 1  
 Maximum Fanout (Rec. SL): 28  
 Gate Count: 21



**Symbol**

D	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0		0	1
1		1	0
x		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FD5X4 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	1.05	$0.97 + 0.040 * SL$	$0.97 + 0.041 * SL$	$0.97 + 0.041 * SL$
	tPHL	1.21	$1.16 + 0.026 * SL$	$1.17 + 0.021 * SL$	$1.19 + 0.020 * SL$
	tR	0.29	$0.10 + 0.093 * SL$	$0.09 + 0.097 * SL$	$0.08 + 0.097 * SL$
	tF	0.17	$0.10 + 0.035 * SL$	$0.09 + 0.038 * SL$	$0.06 + 0.039 * SL$
CKN to Q1	tPLH	1.05	$0.97 + 0.039 * SL$	$0.97 + 0.040 * SL$	$0.97 + 0.040 * SL$
	tPHL	1.21	$1.15 + 0.026 * SL$	$1.17 + 0.021 * SL$	$1.18 + 0.020 * SL$
	tR	0.28	$0.10 + 0.089 * SL$	$0.09 + 0.092 * SL$	$0.08 + 0.093 * SL$
	tF	0.17	$0.09 + 0.037 * SL$	$0.09 + 0.038 * SL$	$0.06 + 0.040 * SL$
CKN to Q2	tPLH	1.05	$0.97 + 0.039 * SL$	$0.97 + 0.040 * SL$	$0.97 + 0.040 * SL$
	tPHL	1.21	$1.15 + 0.026 * SL$	$1.17 + 0.021 * SL$	$1.18 + 0.020 * SL$
	tR	0.28	$0.10 + 0.089 * SL$	$0.09 + 0.092 * SL$	$0.08 + 0.093 * SL$
	tF	0.17	$0.09 + 0.037 * SL$	$0.09 + 0.038 * SL$	$0.06 + 0.040 * SL$
CKN to Q3	tPLH	1.05	$0.97 + 0.040 * SL$	$0.97 + 0.041 * SL$	$0.97 + 0.041 * SL$
	tPHL	1.21	$1.16 + 0.026 * SL$	$1.17 + 0.021 * SL$	$1.19 + 0.020 * SL$
	tR	0.29	$0.10 + 0.093 * SL$	$0.09 + 0.097 * SL$	$0.08 + 0.097 * SL$
	tF	0.17	$0.10 + 0.036 * SL$	$0.09 + 0.037 * SL$	$0.06 + 0.039 * SL$
CKN to QN0	tPLH	1.14	$1.06 + 0.044 * SL$	$1.06 + 0.043 * SL$	$1.06 + 0.043 * SL$
	tPHL	0.92	$0.86 + 0.028 * SL$	$0.88 + 0.022 * SL$	$0.91 + 0.020 * SL$
	tR	0.31	$0.11 + 0.099 * SL$	$0.10 + 0.101 * SL$	$0.09 + 0.102 * SL$
	tF	0.18	$0.10 + 0.039 * SL$	$0.10 + 0.039 * SL$	$0.08 + 0.041 * SL$
CKN to QN1	tPLH	1.14	$1.05 + 0.041 * SL$	$1.06 + 0.040 * SL$	$1.06 + 0.040 * SL$
	tPHL	0.92	$0.86 + 0.027 * SL$	$0.88 + 0.022 * SL$	$0.90 + 0.020 * SL$
	tR	0.29	$0.11 + 0.091 * SL$	$0.10 + 0.095 * SL$	$0.09 + 0.095 * SL$
	tF	0.18	$0.10 + 0.038 * SL$	$0.10 + 0.040 * SL$	$0.07 + 0.041 * SL$
CKN to QN2	tPLH	1.14	$1.05 + 0.041 * SL$	$1.06 + 0.040 * SL$	$1.06 + 0.041 * SL$
	tPHL	0.92	$0.86 + 0.027 * SL$	$0.88 + 0.022 * SL$	$0.90 + 0.020 * SL$
	tR	0.29	$0.11 + 0.091 * SL$	$0.10 + 0.095 * SL$	$0.09 + 0.095 * SL$
	tF	0.18	$0.10 + 0.038 * SL$	$0.10 + 0.040 * SL$	$0.07 + 0.041 * SL$
CKN to QN3	tPLH	1.14	$1.06 + 0.043 * SL$	$1.06 + 0.043 * SL$	$1.06 + 0.043 * SL$
	tPHL	0.92	$0.86 + 0.028 * SL$	$0.88 + 0.022 * SL$	$0.91 + 0.020 * SL$
	tR	0.31	$0.11 + 0.099 * SL$	$0.10 + 0.101 * SL$	$0.09 + 0.102 * SL$
	tF	0.18	$0.10 + 0.039 * SL$	$0.10 + 0.039 * SL$	$0.08 + 0.041 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD5X4 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

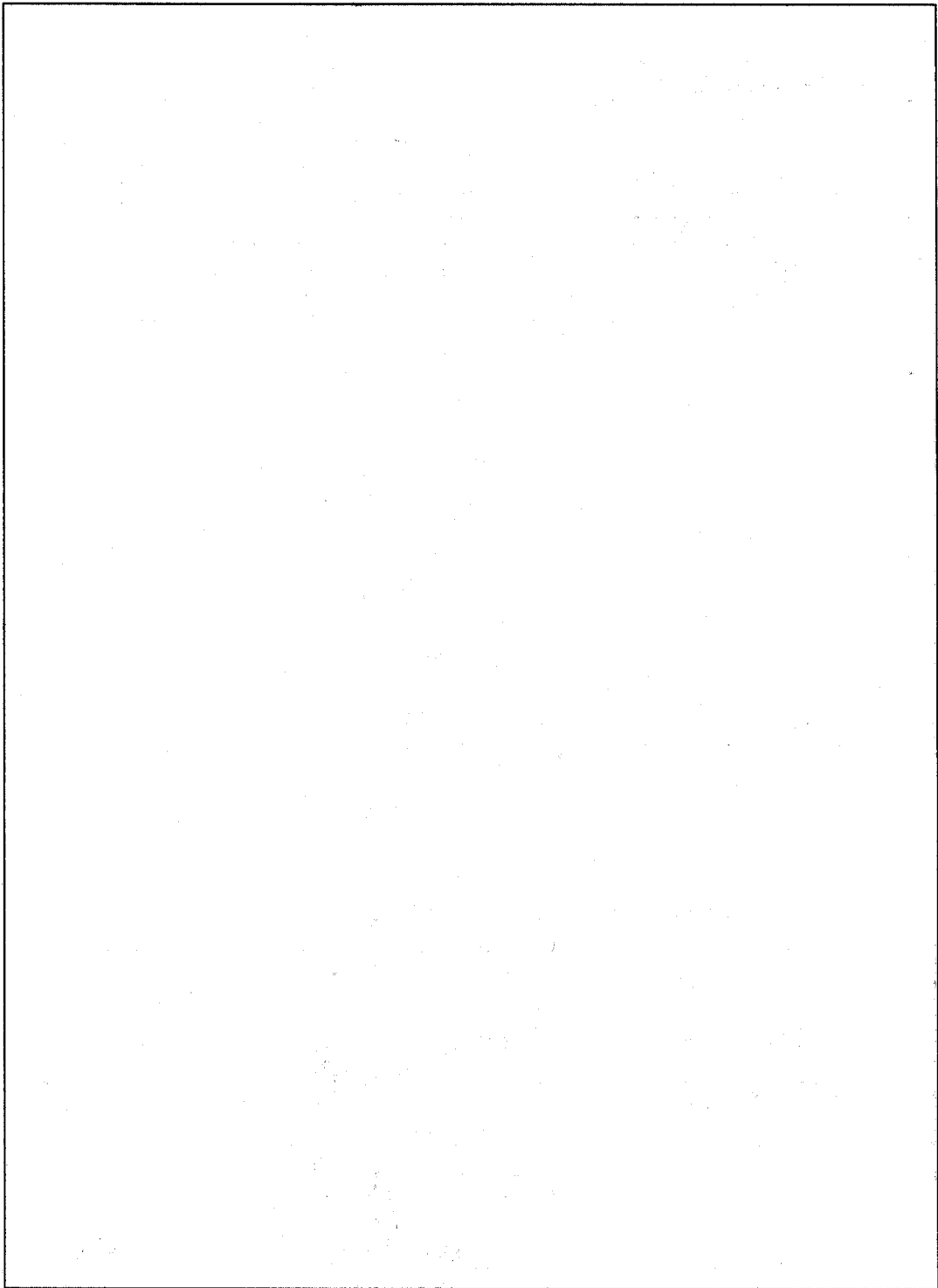
Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920

# FD5X4

## 4-Bit D Flip-Flop with Negative Edge Trigger

### FD5X4 Timing Requirements [Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D0 to CKN)	tHD	0.561
Input Hold Time (D1 to CKN)	tHD	0.561
Input Hold Time (D2 to CKN)	tHD	0.561
Input Hold Time (D3 to CKN)	tHD	0.561
Input Setup Time (D0 to CKN)	tSU	0.000
Input Setup Time (D1 to CKN)	tSU	0.000
Input Setup Time (D2 to CKN)	tSU	0.000
Input Setup Time (D3 to CKN)	tSU	0.000





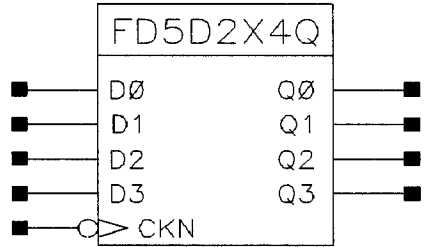
# FD5D2X4Q/FD5D4X4Q

4-Bit D Flip-Flop with Negative Edge Trigger, Q Output Only, 2X Drive or 4X Drive

Inputs: D0, D1, D2, D3, CKN  
 Output: Q0, Q1, Q2, Q3  
 Input Loading (SL): All : D0, D1, D2, D3: 3  
 CKN: 1

Maximum Fanout (Rec. SL):  
 - FD5D2x4Q: 112  
 - FD5D4X4Q: 112

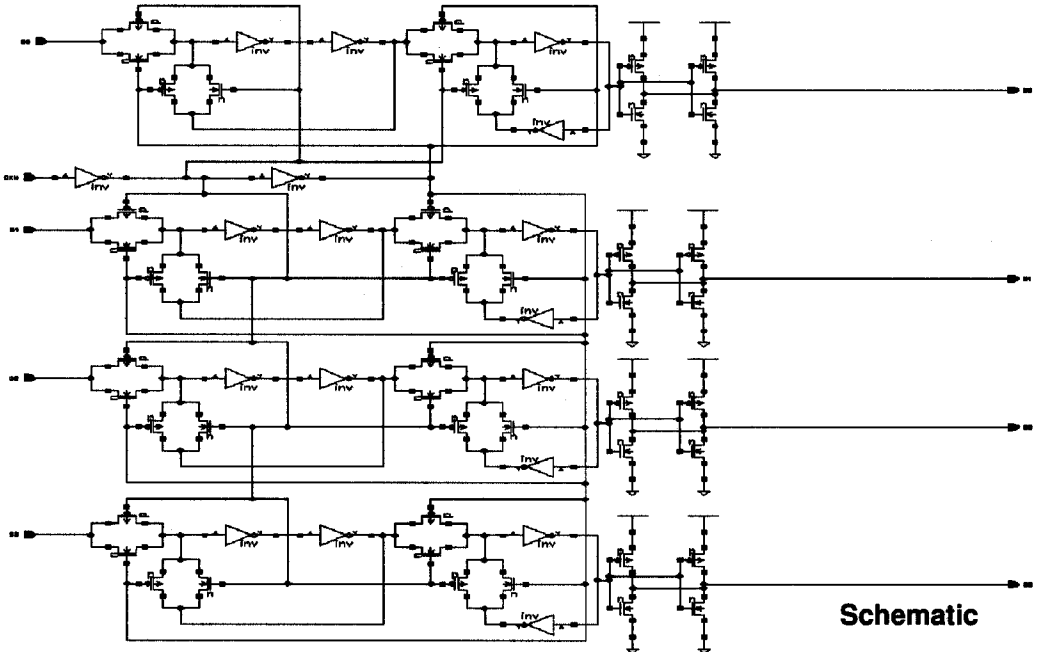
Gate Count:  
 - FD5D2X4Q: 21  
 - FD5D4X4Q: 25



Symbol

D	CK	Q <sub>n+1</sub>
0		0
1		1
x		Q <sub>n</sub>

Truth Table



Schematic

**FD5D2X4Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	0.88	$0.83 + 0.024*SL$	$0.84 + 0.022*SL$	$0.85 + 0.021*SL$
	tPHL	0.97	$0.92 + 0.023*SL$	$0.94 + 0.016*SL$	$1.02 + 0.012*SL$
	tR	0.26	$0.15 + 0.052*SL$	$0.16 + 0.050*SL$	$0.13 + 0.052*SL$
	tF	0.25	$0.19 + 0.028*SL$	$0.21 + 0.021*SL$	$0.24 + 0.020*SL$
CKN to Q1	tPLH	0.87	$0.83 + 0.023*SL$	$0.83 + 0.021*SL$	$0.85 + 0.020*SL$
	tPHL	0.96	$0.92 + 0.023*SL$	$0.94 + 0.016*SL$	$1.02 + 0.012*SL$
	tR	0.24	$0.15 + 0.049*SL$	$0.15 + 0.047*SL$	$0.13 + 0.049*SL$
	tF	0.24	$0.19 + 0.026*SL$	$0.21 + 0.020*SL$	$0.24 + 0.019*SL$
CKN to Q2	tPLH	0.87	$0.83 + 0.023*SL$	$0.83 + 0.021*SL$	$0.85 + 0.020*SL$
	tPHL	0.96	$0.92 + 0.023*SL$	$0.94 + 0.016*SL$	$1.02 + 0.012*SL$
	tR	0.24	$0.15 + 0.049*SL$	$0.15 + 0.047*SL$	$0.13 + 0.049*SL$
	tF	0.24	$0.19 + 0.026*SL$	$0.21 + 0.020*SL$	$0.24 + 0.019*SL$
CKN to Q3	tPLH	0.88	$0.83 + 0.024*SL$	$0.84 + 0.022*SL$	$0.85 + 0.022*SL$
	tPHL	0.97	$0.92 + 0.023*SL$	$0.94 + 0.016*SL$	$1.02 + 0.012*SL$
	tR	0.26	$0.15 + 0.052*SL$	$0.16 + 0.051*SL$	$0.13 + 0.052*SL$
	tF	0.25	$0.19 + 0.028*SL$	$0.21 + 0.021*SL$	$0.23 + 0.020*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD5D2X4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D0 to CKN)	tHD	0.561
Input Hold Time (D1 to CKN)	tHD	0.561
Input Hold Time (D2 to CKN)	tHD	0.561
Input Hold Time (D3 to CKN)	tHD	0.561
Input Setup Time (D0 to CKN)	tSU	0.000
Input Setup Time (D1 to CKN)	tSU	0.000
Input Setup Time (D2 to CKN)	tSU	0.000
Input Setup Time (D3 to CKN)	tSU	0.000

# FD5D4X4Q

4-Bit D Flip-Flop with Negative Edge Trigger, Q Output Only, 4X Drive

## FD5D4X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{R}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	0.95	$0.93 + 0.014 \cdot \text{SL}$	$0.93 + 0.012 \cdot \text{SL}$	$0.95 + 0.011 \cdot \text{SL}$
	tPHL	1.00	$0.98 + 0.013 \cdot \text{SL}$	$0.98 + 0.010 \cdot \text{SL}$	$1.04 + 0.008 \cdot \text{SL}$
	tR	0.24	$0.20 + 0.022 \cdot \text{SL}$	$0.19 + 0.024 \cdot \text{SL}$	$0.17 + 0.026 \cdot \text{SL}$
	tF	0.26	$0.24 + 0.013 \cdot \text{SL}$	$0.24 + 0.012 \cdot \text{SL}$	$0.28 + 0.010 \cdot \text{SL}$
CKN to Q1	tPLH	0.95	$0.92 + 0.013 \cdot \text{SL}$	$0.93 + 0.011 \cdot \text{SL}$	$0.94 + 0.010 \cdot \text{SL}$
	tPHL	1.00	$0.98 + 0.014 \cdot \text{SL}$	$0.99 + 0.010 \cdot \text{SL}$	$1.04 + 0.008 \cdot \text{SL}$
	tR	0.24	$0.19 + 0.021 \cdot \text{SL}$	$0.19 + 0.022 \cdot \text{SL}$	$0.17 + 0.023 \cdot \text{SL}$
	tF	0.26	$0.23 + 0.015 \cdot \text{SL}$	$0.24 + 0.012 \cdot \text{SL}$	$0.27 + 0.010 \cdot \text{SL}$
CKN to Q2	tPLH	0.95	$0.92 + 0.013 \cdot \text{SL}$	$0.93 + 0.011 \cdot \text{SL}$	$0.94 + 0.010 \cdot \text{SL}$
	tPHL	1.00	$0.98 + 0.014 \cdot \text{SL}$	$0.99 + 0.010 \cdot \text{SL}$	$1.04 + 0.008 \cdot \text{SL}$
	tR	0.24	$0.19 + 0.021 \cdot \text{SL}$	$0.19 + 0.022 \cdot \text{SL}$	$0.17 + 0.023 \cdot \text{SL}$
	tF	0.26	$0.23 + 0.015 \cdot \text{SL}$	$0.24 + 0.012 \cdot \text{SL}$	$0.27 + 0.010 \cdot \text{SL}$
CKN to Q3	tPLH	0.95	$0.93 + 0.014 \cdot \text{SL}$	$0.93 + 0.012 \cdot \text{SL}$	$0.95 + 0.011 \cdot \text{SL}$
	tPHL	1.00	$0.98 + 0.013 \cdot \text{SL}$	$0.98 + 0.010 \cdot \text{SL}$	$1.04 + 0.008 \cdot \text{SL}$
	tR	0.24	$0.20 + 0.022 \cdot \text{SL}$	$0.19 + 0.024 \cdot \text{SL}$	$0.17 + 0.025 \cdot \text{SL}$
	tF	0.26	$0.24 + 0.013 \cdot \text{SL}$	$0.24 + 0.012 \cdot \text{SL}$	$0.28 + 0.010 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

## FD5D4X4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.959
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D0 to CKN)	tHD	0.616
Input Hold Time (D1 to CKN)	tHD	0.616
Input Hold Time (D2 to CKN)	tHD	0.616
Input Hold Time (D3 to CKN)	tHD	0.616
Input Setup Time (D0 to CKN)	tSU	0.000
Input Setup Time (D1 to CKN)	tSU	0.000
Input Setup Time (D2 to CKN)	tSU	0.000
Input Setup Time (D3 to CKN)	tSU	0.000



# FD6/FD6D2

D Flip-Flop with Reset, Negative Edge Trigger, 1X Drive or 2X Drive

Inputs: D, CKN, RN

Outputs: Q, QN

Input Loading (SL):

- D: 3

- CKN: 1

- RN: 2

Maximum Fanout (Rec. SL):

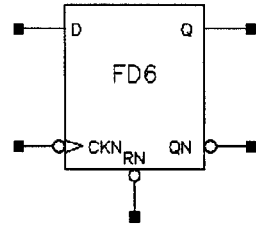
FD6: All : 28

FD6D2: All : 56

Gate Count:

FD6: 7

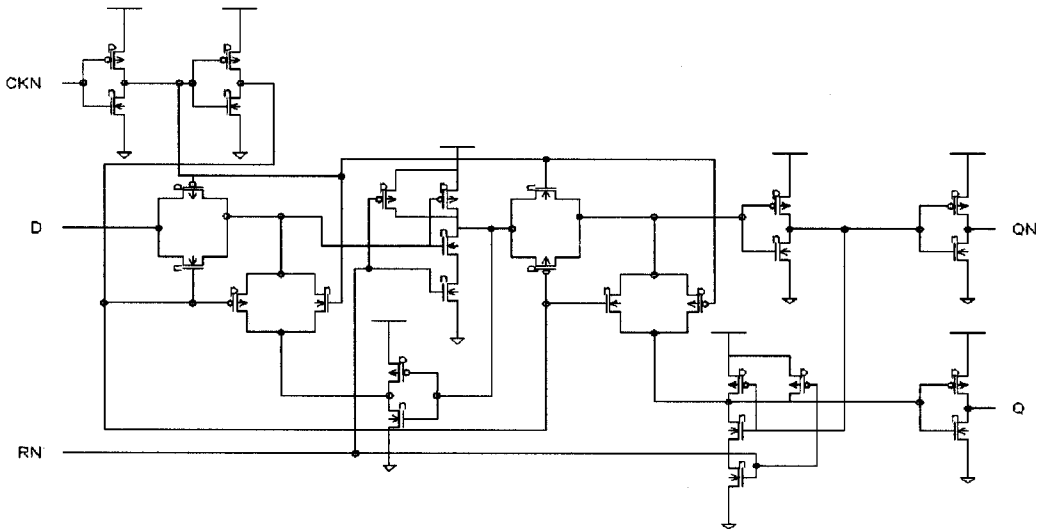
FD6D2: 8



**Symbol**

D	RN	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1		0	1
1	1		1	0
x	0	x	0	1
x	1		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FD6 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.98	$0.90 + 0.040 \cdot \text{SL}$	$0.90 + 0.040 \cdot \text{SL}$	$0.90 + 0.040 \cdot \text{SL}$
	tPHL	0.87	$0.81 + 0.027 \cdot \text{SL}$	$0.83 + 0.021 \cdot \text{SL}$	$0.85 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.13 + 0.089 \cdot \text{SL}$	$0.11 + 0.093 \cdot \text{SL}$	$0.09 + 0.095 \cdot \text{SL}$
	tF	0.18	$0.10 + 0.036 \cdot \text{SL}$	$0.10 + 0.037 \cdot \text{SL}$	$0.07 + 0.039 \cdot \text{SL}$
RN to Q	tPHL	0.45	$0.39 + 0.030 \cdot \text{SL}$	$0.42 + 0.021 \cdot \text{SL}$	$0.45 + 0.020 \cdot \text{SL}$
	tF	0.22	$0.15 + 0.033 \cdot \text{SL}$	$0.14 + 0.035 \cdot \text{SL}$	$0.09 + 0.038 \cdot \text{SL}$
CKN to QN	tPLH	0.77	$0.69 + 0.041 \cdot \text{SL}$	$0.69 + 0.040 \cdot \text{SL}$	$0.69 + 0.040 \cdot \text{SL}$
	tPHL	0.76	$0.70 + 0.028 \cdot \text{SL}$	$0.72 + 0.021 \cdot \text{SL}$	$0.75 + 0.020 \cdot \text{SL}$
	tR	0.28	$0.11 + 0.087 \cdot \text{SL}$	$0.10 + 0.091 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
	tF	0.18	$0.11 + 0.035 \cdot \text{SL}$	$0.11 + 0.037 \cdot \text{SL}$	$0.08 + 0.038 \cdot \text{SL}$
RN to QN	tPLH	0.77	$0.69 + 0.040 \cdot \text{SL}$	$0.69 + 0.039 \cdot \text{SL}$	$0.69 + 0.039 \cdot \text{SL}$
	tR	0.29	$0.11 + 0.088 \cdot \text{SL}$	$0.10 + 0.091 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **FD6 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.342
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (RN)	tRC	0.139

# FD6D2

## D Flip-Flop with Reset and 2X Drive

### FD6D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	1.03	$0.99 + 0.020 \cdot \text{SL}$	$0.99 + 0.020 \cdot \text{SL}$	$0.99 + 0.020 \cdot \text{SL}$
	tPHL	0.92	$0.88 + 0.016 \cdot \text{SL}$	$0.90 + 0.012 \cdot \text{SL}$	$0.93 + 0.010 \cdot \text{SL}$
	tR	0.23	$0.14 + 0.043 \cdot \text{SL}$	$0.13 + 0.045 \cdot \text{SL}$	$0.11 + 0.047 \cdot \text{SL}$
	tF	0.16	$0.12 + 0.022 \cdot \text{SL}$	$0.13 + 0.019 \cdot \text{SL}$	$0.11 + 0.020 \cdot \text{SL}$
RN to Q	tPHL	0.46	$0.42 + 0.019 \cdot \text{SL}$	$0.44 + 0.012 \cdot \text{SL}$	$0.48 + 0.010 \cdot \text{SL}$
	tF	0.21	$0.17 + 0.019 \cdot \text{SL}$	$0.17 + 0.018 \cdot \text{SL}$	$0.15 + 0.019 \cdot \text{SL}$
CKN to QN	tPLH	0.77	$0.73 + 0.021 \cdot \text{SL}$	$0.73 + 0.020 \cdot \text{SL}$	$0.73 + 0.020 \cdot \text{SL}$
	tPHL	0.76	$0.73 + 0.017 \cdot \text{SL}$	$0.74 + 0.012 \cdot \text{SL}$	$0.78 + 0.010 \cdot \text{SL}$
	tR	0.20	$0.12 + 0.043 \cdot \text{SL}$	$0.11 + 0.046 \cdot \text{SL}$	$0.09 + 0.047 \cdot \text{SL}$
	tF	0.16	$0.13 + 0.018 \cdot \text{SL}$	$0.13 + 0.018 \cdot \text{SL}$	$0.12 + 0.019 \cdot \text{SL}$
RN to QN	tPLH	0.78	$0.74 + 0.021 \cdot \text{SL}$	$0.74 + 0.020 \cdot \text{SL}$	$0.74 + 0.020 \cdot \text{SL}$
	tR	0.21	$0.12 + 0.044 \cdot \text{SL}$	$0.12 + 0.045 \cdot \text{SL}$	$0.09 + 0.047 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

### FD6D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.342
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (RN)	tRC	0.139





# FD6D2Q/FD6D4Q

D Flip-Flop with Reset, Negative Edge Trigger, Q Output Only, 2X Drive or 4X Drive

Inputs: D, CKN, RN

Output: Q

Input Loading (SL):

- FD6D2Q: D: 3, CKN : 1

RN : 2

- FD6D4Q: D: 3, CKN : 1

RN : 2

Maximum Fanout (Rec. SL): All :

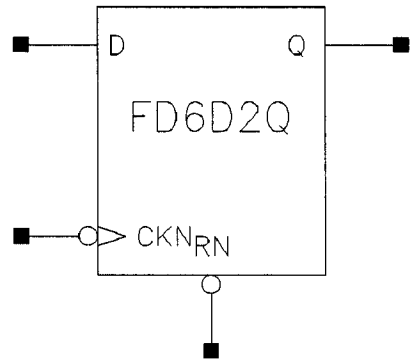
- FD6D2Q: 56

- FD6D4Q: 112

Gate Count:

- FD6D2Q: 7

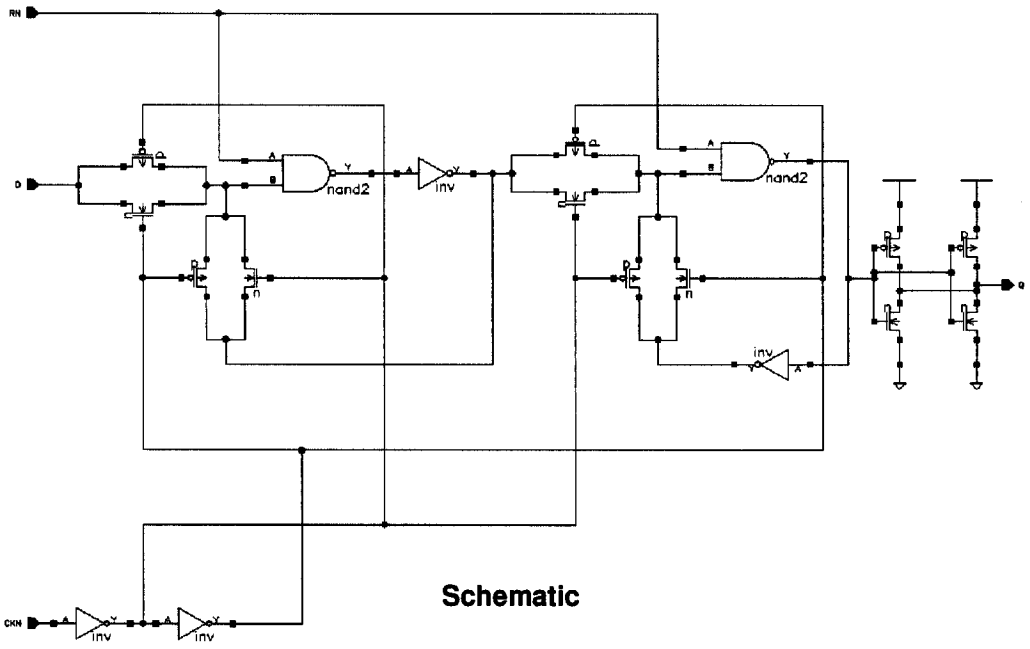
- FD6D4Q: 8



Symbol

D	RN	CK	Q <sub>n+1</sub>
0	1		0
1	1		1
x	0	x	0
x	1		Q <sub>n</sub>

Truth Table



Schematic

**FD6D2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.73	$0.67 + 0.027*SL$	$0.69 + 0.022*SL$	$0.72 + 0.020*SL$
	tPHL	0.63	$0.59 + 0.023*SL$	$0.61 + 0.016*SL$	$0.68 + 0.012*SL$
	tR	0.29	$0.20 + 0.044*SL$	$0.20 + 0.045*SL$	$0.18 + 0.047*SL$
	tF	0.22	$0.16 + 0.029*SL$	$0.18 + 0.021*SL$	$0.22 + 0.019*SL$
RN to Q	tPHL	0.65	$0.60 + 0.025*SL$	$0.63 + 0.016*SL$	$0.72 + 0.012*SL$
	tF	0.30	$0.25 + 0.024*SL$	$0.27 + 0.018*SL$	$0.28 + 0.018*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD6D2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.397
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (RN)	tRC	0.139

# FD6D4Q

D Flip-Flop with Reset, Negative Edge Trigger, Q Output Only, 4X Drive

## FD6D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.90ns$ ]

(SL: Standard Load)

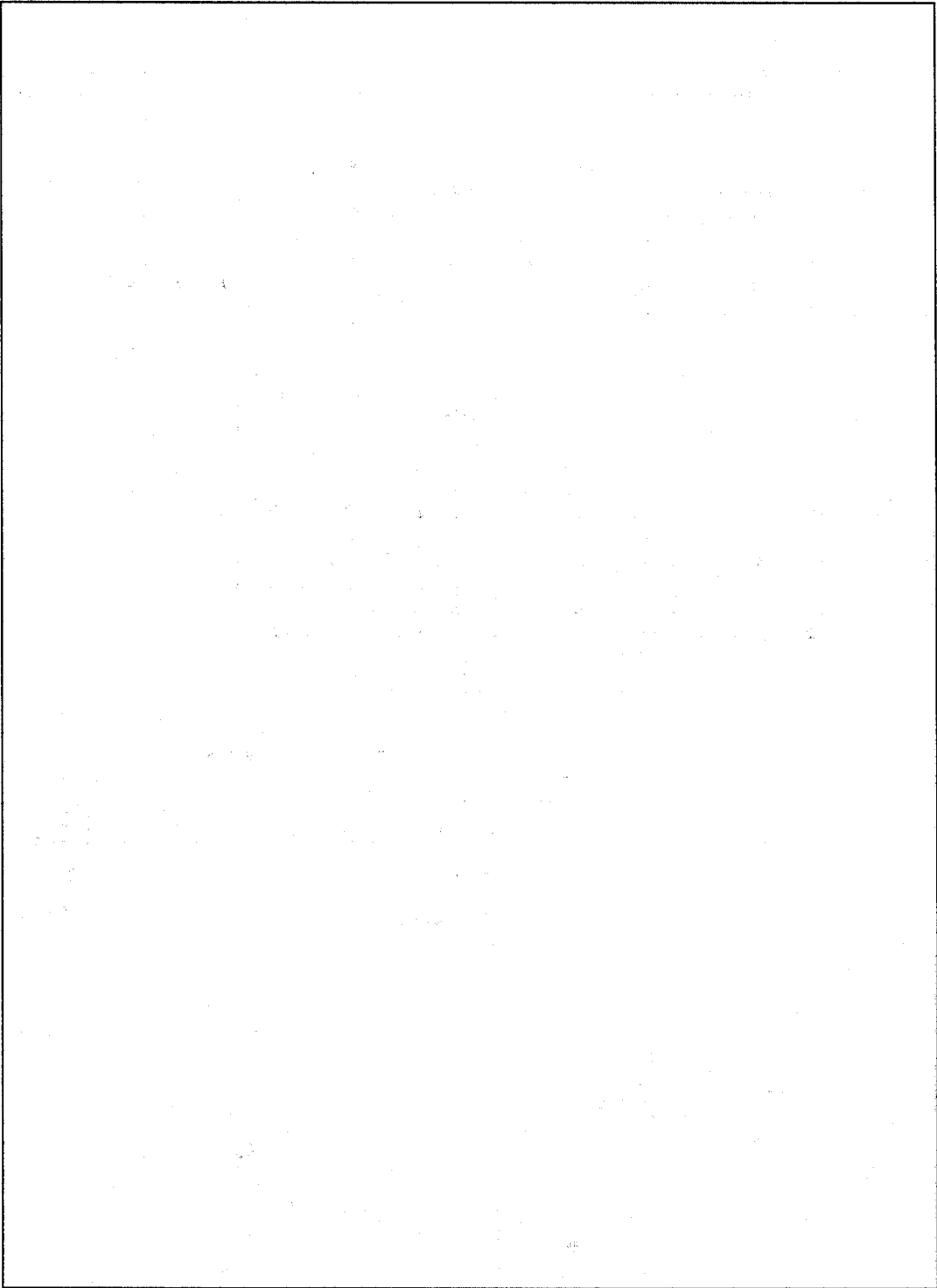
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.81	$0.77 + 0.016 * SL$	$0.78 + 0.012 * SL$	$0.81 + 0.011 * SL$
	tPHL	0.67	$0.65 + 0.014 * SL$	$0.66 + 0.010 * SL$	$0.71 + 0.008 * SL$
	tR	0.31	$0.28 + 0.020 * SL$	$0.27 + 0.021 * SL$	$0.24 + 0.022 * SL$
	tF	0.24	$0.21 + 0.017 * SL$	$0.22 + 0.012 * SL$	$0.26 + 0.010 * SL$
RN to Q	tPHL	0.71	$0.68 + 0.015 * SL$	$0.70 + 0.010 * SL$	$0.75 + 0.007 * SL$
	tF	0.32	$0.29 + 0.013 * SL$	$0.30 + 0.010 * SL$	$0.32 + 0.009 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD6D4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.397
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (RN)	tRC	0.139



# FD6SD2Q/FD6SD4Q

D Flip-Flop with Scan, Reset, Negative Edge Trigger, Q Output Only, 2X or 4X Drive

Inputs: D, TI, TE, CK

Output: Q

Input Loading (SL):

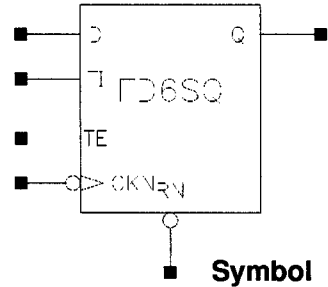
- FD6SD2Q: D, CK, TI : 1  
RN, TE : 2
- FD6SD4Q: D, CK, TI : 1  
RN, TE : 2

Maximum Fanout (Rec. SL):

- FD6SD2Q: 56
- FD6SD4Q: 112

Gate Count:

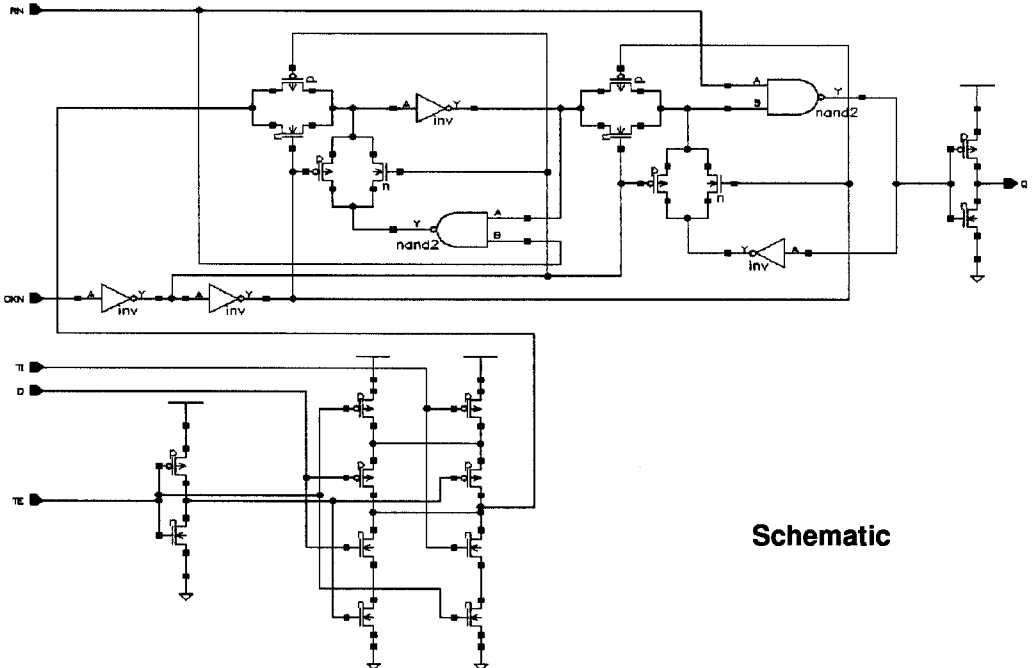
- FD6SD2Q: 10
- FD6SD4Q: 11



Symbol

D	RN	TI	TE	CK	Q <sub>n+1</sub>
0	1	x	0		0
1	1	x	0		1
x	1	0	1		0
x	1	1	1		1
x	0	x	x	x	0
x	1	x	x		Q <sub>n</sub>

Truth Table



Schematic

**FD6SD2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{F}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.86	$0.81 + 0.023^*SL$	$0.82 + 0.021^*SL$	$0.83 + 0.020^*SL$
	tPHL	0.74	$0.70 + 0.018^*SL$	$0.72 + 0.012^*SL$	$0.76 + 0.010^*SL$
	tR	0.23	$0.14 + 0.046^*SL$	$0.13 + 0.046^*SL$	$0.11 + 0.047^*SL$
	tF	0.17	$0.13 + 0.020^*SL$	$0.13 + 0.018^*SL$	$0.13 + 0.019^*SL$
RN to Q	tPHL	0.47	$0.43 + 0.020^*SL$	$0.45 + 0.013^*SL$	$0.51 + 0.010^*SL$
	tF	0.21	$0.17 + 0.020^*SL$	$0.18 + 0.017^*SL$	$0.16 + 0.018^*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD6SD2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.123
Input Hold Time (TE to CKN)	tHD	0.123
Input Hold Time (TI to CKN)	tHD	0.069
Input Setup Time (D to CKN)	tSU	0.452
Input Setup Time (TE to CKN)	tSU	0.616
Input Setup Time (TI to CKN)	tSU	0.506
Recovery Time (RN)	tRC	0.139

# FD6SD4Q

D Flip-Flop with Scan, Reset, Negative Edge Trigger, Q Output Only, 4X Drive

## FD6SD4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

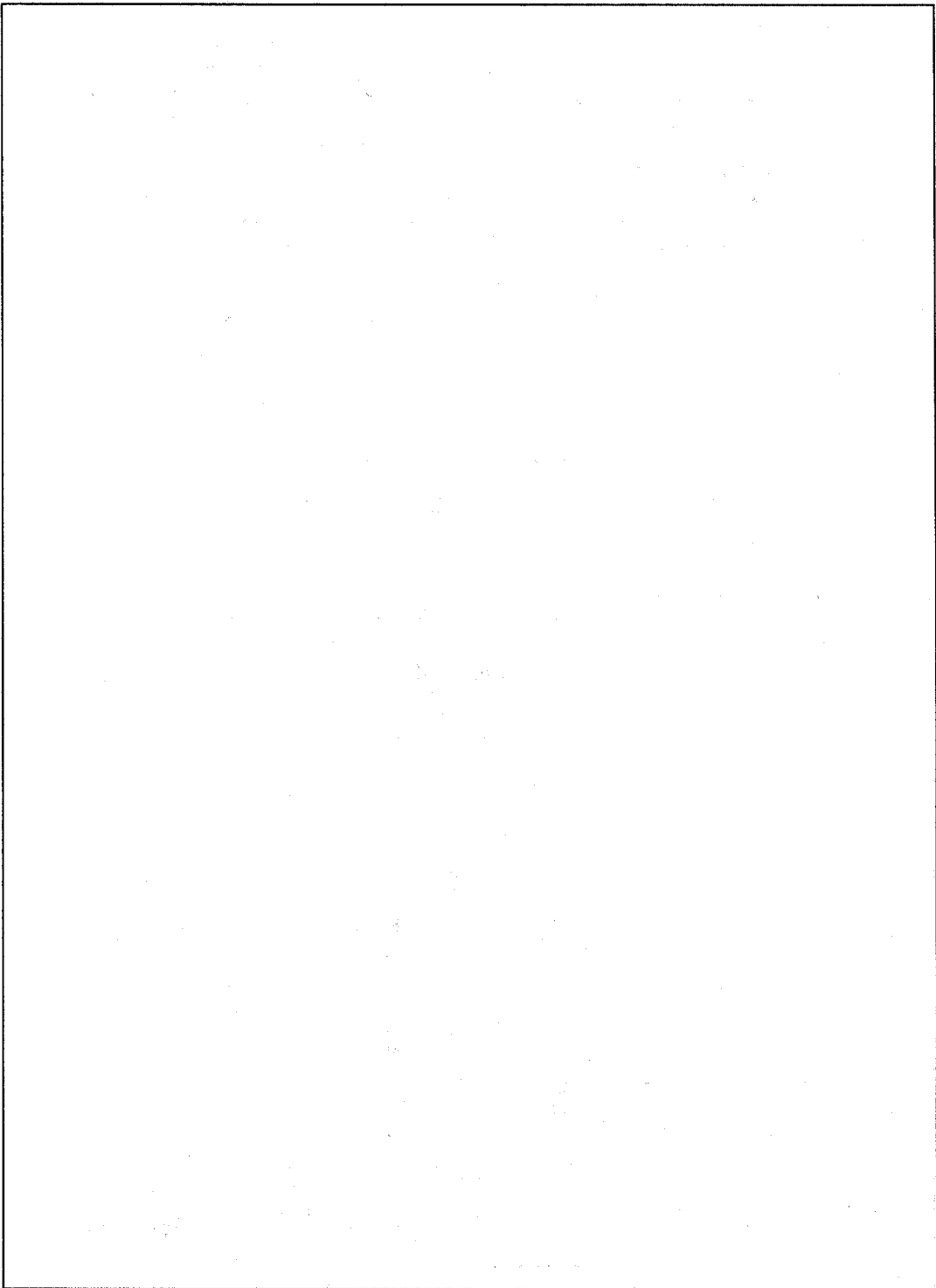
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.93	$0.90 + 0.013*SL$	$0.91 + 0.011*SL$	$0.92 + 0.010*SL$
	tPHL	0.79	$0.77 + 0.011*SL$	$0.78 + 0.008*SL$	$0.82 + 0.006*SL$
	tR	0.22	$0.18 + 0.020*SL$	$0.17 + 0.022*SL$	$0.15 + 0.023*SL$
	tF	0.19	$0.17 + 0.010*SL$	$0.17 + 0.010*SL$	$0.18 + 0.009*SL$
RN to Q	tPHL	0.53	$0.50 + 0.012*SL$	$0.51 + 0.008*SL$	$0.56 + 0.006*SL$
	tF	0.23	$0.21 + 0.011*SL$	$0.22 + 0.008*SL$	$0.22 + 0.008*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD6SD4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.123
Input Hold Time (TE to CKN)	tHD	0.123
Input Hold Time (TI to CKN)	tHD	0.069
Input Setup Time (D to CKN)	tSU	0.452
Input Setup Time (TE to CKN)	tSU	0.616
Input Setup Time (TI to CKN)	tSU	0.506
Recovery Time (RN)	tRC	0.139

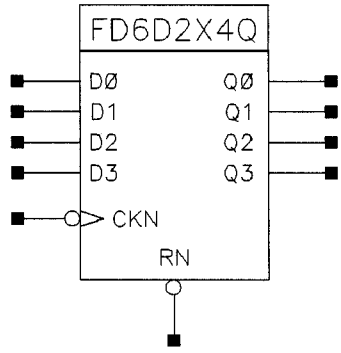




# FD6D2X4Q/FD6D4X4Q

4-Bit D Flip-Flop with Reset, Negative Edge Trigger, Q Output Only, 2X Drive or 4X Drive

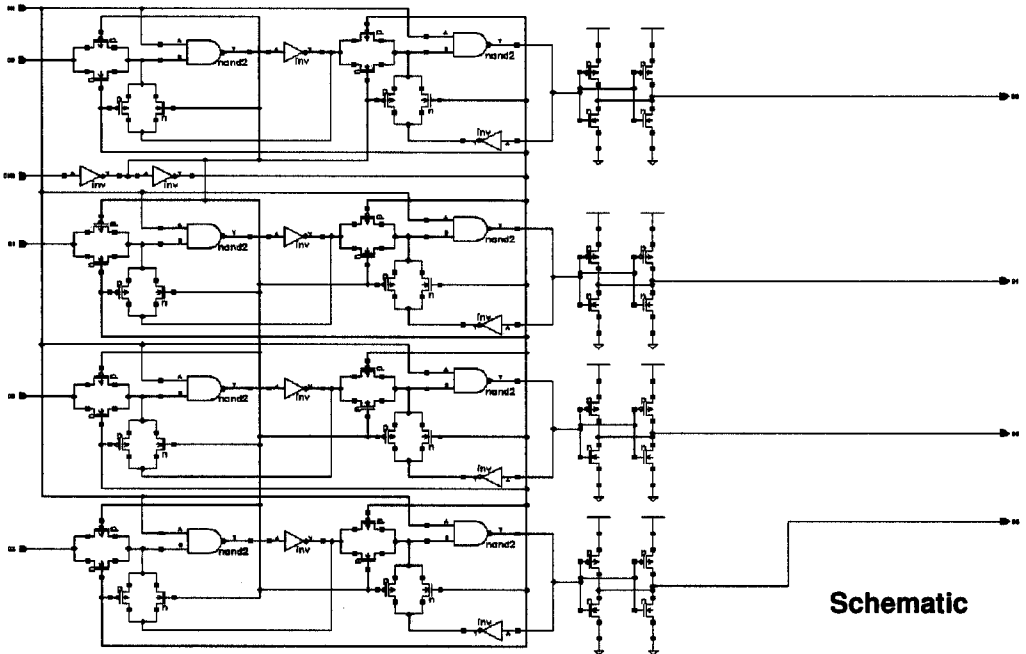
Inputs: D0, D1, D2, D3, CKN, RN  
 Output: Q0, Q1, Q2, Q3  
 Input Loading (SL): All: D0,D1,D2,D3: 3  
 CKN: 1, RN: 8  
 Maximum Fanout (Rec. SL):  
 - FD6D2X4Q: 56  
 - FD6D4X4Q: 112  
 Gate Count:  
 - FD6D2X4Q: 25  
 - FD6D4X4Q: 29



**Symbol**

D	RN	CK	Qn+1
0	1		0
1	1		1
x	0	x	0
x	1		Qn

**Truth Table**



**Schematic**

**FD6D2X4Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	0.96	$0.91 + 0.026*SL$	$0.92 + 0.022*SL$	$0.95 + 0.020*SL$
	tPHL	0.97	$0.92 + 0.023*SL$	$0.94 + 0.016*SL$	$1.02 + 0.012*SL$
	tR	0.29	$0.20 + 0.045*SL$	$0.19 + 0.046*SL$	$0.18 + 0.047*SL$
	tF	0.25	$0.20 + 0.027*SL$	$0.22 + 0.021*SL$	$0.25 + 0.019*SL$
RN to Q0	tPHL	0.66	$0.61 + 0.025*SL$	$0.63 + 0.016*SL$	$0.72 + 0.012*SL$
	tF	0.30	$0.25 + 0.023*SL$	$0.27 + 0.018*SL$	$0.28 + 0.018*SL$
CKN to Q1	tPLH	0.96	$0.90 + 0.027*SL$	$0.92 + 0.023*SL$	$0.95 + 0.021*SL$
	tPHL	0.96	$0.91 + 0.024*SL$	$0.93 + 0.016*SL$	$1.02 + 0.012*SL$
	tR	0.29	$0.20 + 0.046*SL$	$0.19 + 0.049*SL$	$0.18 + 0.050*SL$
	tF	0.26	$0.20 + 0.028*SL$	$0.22 + 0.021*SL$	$0.25 + 0.020*SL$
RN to Q1	tPHL	0.65	$0.60 + 0.025*SL$	$0.63 + 0.016*SL$	$0.72 + 0.012*SL$
	tF	0.30	$0.25 + 0.025*SL$	$0.27 + 0.019*SL$	$0.28 + 0.019*SL$
CKN to Q2	tPLH	0.96	$0.90 + 0.027*SL$	$0.92 + 0.023*SL$	$0.95 + 0.021*SL$
	tPHL	0.96	$0.91 + 0.024*SL$	$0.93 + 0.016*SL$	$1.02 + 0.012*SL$
	tR	0.29	$0.20 + 0.046*SL$	$0.19 + 0.049*SL$	$0.18 + 0.050*SL$
	tF	0.26	$0.20 + 0.028*SL$	$0.22 + 0.021*SL$	$0.25 + 0.020*SL$
RN to Q2	tPHL	0.65	$0.60 + 0.025*SL$	$0.63 + 0.016*SL$	$0.72 + 0.012*SL$
	tF	0.30	$0.25 + 0.025*SL$	$0.27 + 0.019*SL$	$0.28 + 0.019*SL$
CKN to Q3	tPLH	0.96	$0.91 + 0.026*SL$	$0.92 + 0.022*SL$	$0.95 + 0.020*SL$
	tPHL	0.97	$0.92 + 0.023*SL$	$0.94 + 0.016*SL$	$1.02 + 0.012*SL$
	tR	0.29	$0.20 + 0.045*SL$	$0.19 + 0.046*SL$	$0.18 + 0.047*SL$
	tF	0.25	$0.20 + 0.027*SL$	$0.22 + 0.021*SL$	$0.25 + 0.019*SL$
RN to Q3	tPHL	0.66	$0.61 + 0.025*SL$	$0.63 + 0.016*SL$	$0.72 + 0.012*SL$
	tF	0.30	$0.25 + 0.023*SL$	$0.27 + 0.018*SL$	$0.28 + 0.018*SL$

\*Range1:  $SL < 3.00$ , \*Range2:  $3.00 \leq SL \leq 20.00$ , \*Range3:  $20.00 < SL$ **FD6D2X4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.959
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D0 to CKN)	tHD	0.561
Input Hold Time (D1 to CKN)	tHD	0.561
Input Hold Time (D2 to CKN)	tHD	0.561
Input Hold Time (D3 to CKN)	tHD	0.561
Input Setup Time (D0 to CKN)	tSU	0.000

## FD6D2X4Q

4-Bit D Flip-Flop with Reset, Negative Edge Trigger, Q Output Only, 2X Drive

### FD6D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Input Setup Time (D1 to CKN)	tSU	0.000
Input Setup Time (D2 to CKN)	tSU	0.000
Input Setup Time (D3 to CKN)	tSU	0.000
Recovery Time (RN)	tRC	0.139

**FD6D4X4Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	1.06	$1.03 + 0.016*SL$	$1.04 + 0.012*SL$	$1.07 + 0.011*SL$
	tPHL	1.01	$0.98 + 0.014*SL$	$0.99 + 0.010*SL$	$1.04 + 0.008*SL$
	tR	0.31	$0.27 + 0.020*SL$	$0.26 + 0.021*SL$	$0.24 + 0.023*SL$
	tF	0.27	$0.24 + 0.015*SL$	$0.25 + 0.012*SL$	$0.29 + 0.010*SL$
RN to Q0	tPHL	0.72	$0.69 + 0.015*SL$	$0.70 + 0.010*SL$	$0.76 + 0.007*SL$
	tF	0.32	$0.29 + 0.013*SL$	$0.30 + 0.011*SL$	$0.33 + 0.009*SL$
CKN to Q1	tPLH	1.05	$1.02 + 0.015*SL$	$1.03 + 0.012*SL$	$1.06 + 0.011*SL$
	tPHL	1.00	$0.97 + 0.014*SL$	$0.98 + 0.010*SL$	$1.03 + 0.008*SL$
	tR	0.31	$0.27 + 0.021*SL$	$0.26 + 0.022*SL$	$0.24 + 0.023*SL$
	tF	0.27	$0.24 + 0.015*SL$	$0.25 + 0.012*SL$	$0.29 + 0.010*SL$
RN to Q1	tPHL	0.71	$0.68 + 0.015*SL$	$0.69 + 0.010*SL$	$0.75 + 0.007*SL$
	tF	0.32	$0.29 + 0.015*SL$	$0.30 + 0.011*SL$	$0.33 + 0.009*SL$
CKN to Q2	tPLH	1.05	$1.02 + 0.016*SL$	$1.03 + 0.012*SL$	$1.06 + 0.011*SL$
	tPHL	1.00	$0.97 + 0.014*SL$	$0.98 + 0.010*SL$	$1.03 + 0.008*SL$
	tR	0.31	$0.27 + 0.020*SL$	$0.26 + 0.023*SL$	$0.24 + 0.024*SL$
	tF	0.27	$0.24 + 0.015*SL$	$0.25 + 0.012*SL$	$0.29 + 0.010*SL$
RN to Q2	tPHL	0.71	$0.68 + 0.015*SL$	$0.69 + 0.010*SL$	$0.75 + 0.007*SL$
	tF	0.32	$0.29 + 0.015*SL$	$0.31 + 0.011*SL$	$0.33 + 0.009*SL$
CKN to Q3	tPLH	1.06	$1.03 + 0.016*SL$	$1.04 + 0.012*SL$	$1.07 + 0.011*SL$
	tPHL	1.01	$0.98 + 0.014*SL$	$0.99 + 0.010*SL$	$1.04 + 0.008*SL$
	tR	0.31	$0.27 + 0.020*SL$	$0.26 + 0.021*SL$	$0.24 + 0.023*SL$
	tF	0.27	$0.24 + 0.015*SL$	$0.25 + 0.012*SL$	$0.29 + 0.010*SL$
RN to Q3	tPHL	0.72	$0.69 + 0.015*SL$	$0.70 + 0.010*SL$	$0.76 + 0.007*SL$
	tF	0.32	$0.29 + 0.013*SL$	$0.30 + 0.011*SL$	$0.33 + 0.009*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD6D4X4Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.998
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D0 to CKN)	tHD	0.616
Input Hold Time (D1 to CKN)	tHD	0.616
Input Hold Time (D2 to CKN)	tHD	0.616
Input Hold Time (D3 to CKN)	tHD	0.616
Input Setup Time (D0 to CKN)	tSU	0.000

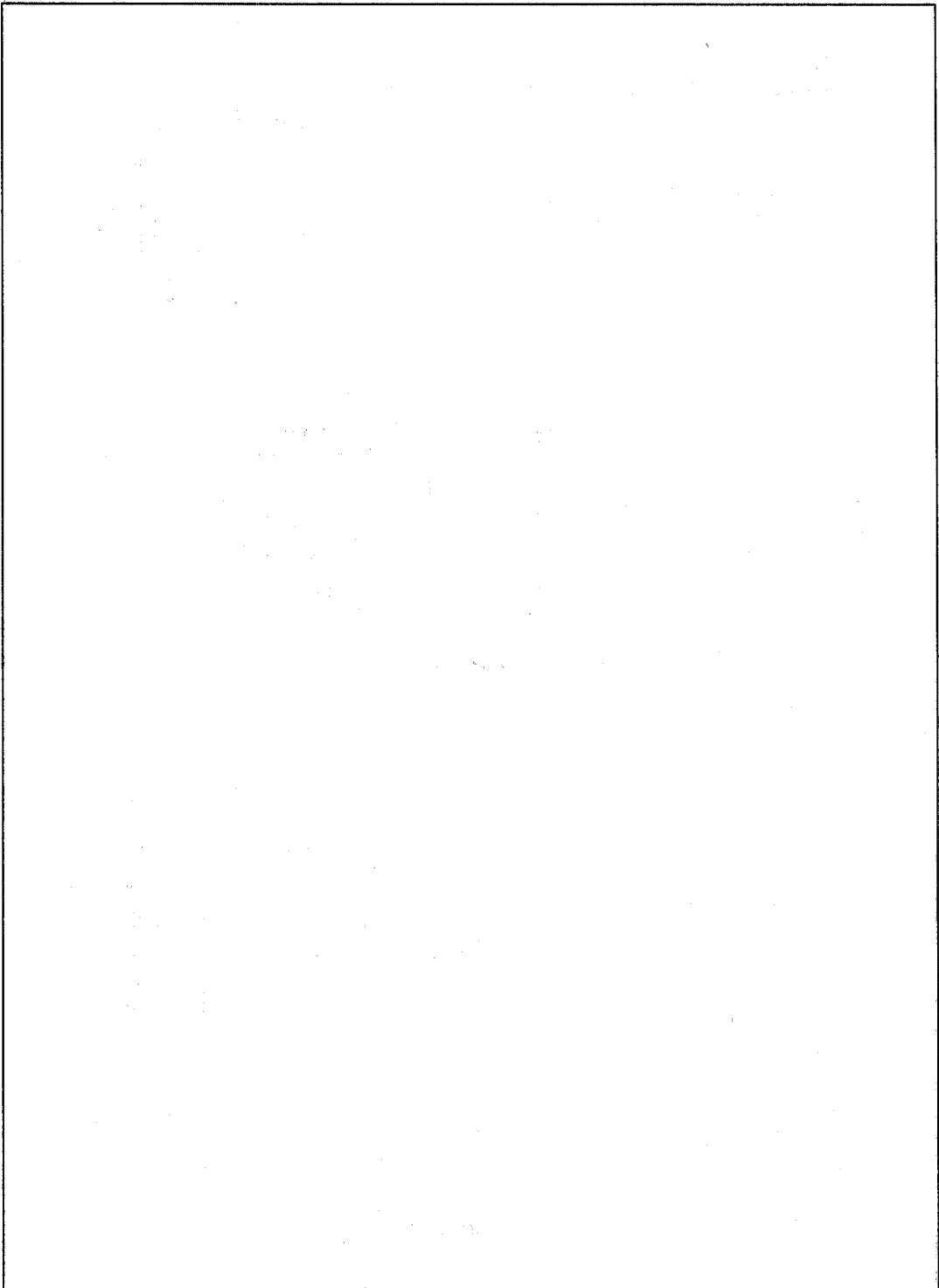
# FD6D4X4Q

4-Bit D Flip-Flop with Reset, Negative Edge Trigger, Q Output Only, 4X Drive

## FD6D4X4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Input Setup Time (D1 to CKN)	tSU	0.000
Input Setup Time (D2 to CKN)	tSU	0.000
Input Setup Time (D3 to CKN)	tSU	0.000
Recovery Time (RN)	tRC	0.139



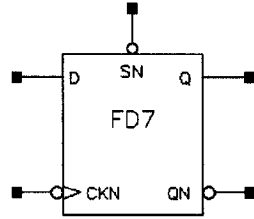
# FD7/FD7D2

D Flip-Flop with Set, Negative Edge Trigger, 1X Drive or 2X Drive

Inputs: D, CK, SN  
 Outputs: Q, QN  
 Input Loading (SL):  
 - D: 3  
 - CKN: 1  
 - SN: 2

Maximum Fanout (Rec. SL):  
 FD7: All : 28  
 FD7D2: All : 56

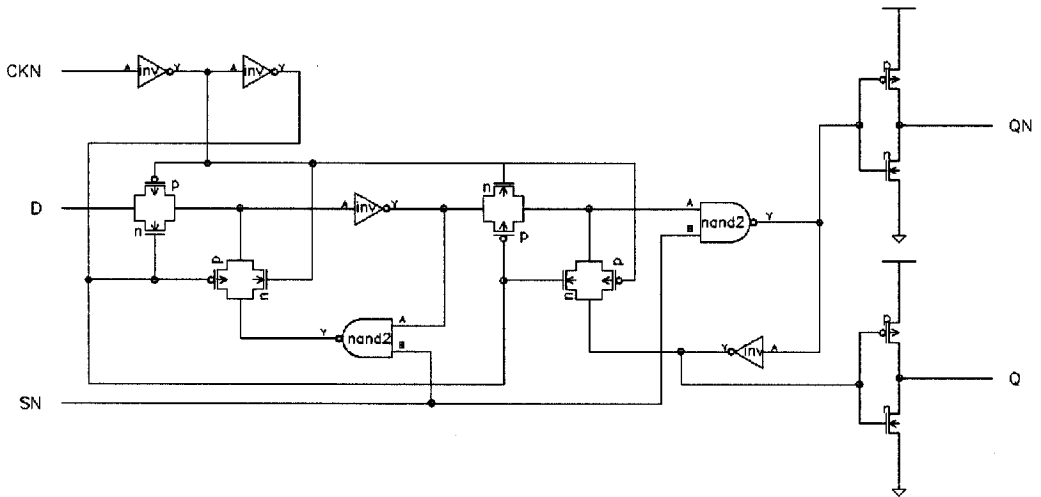
Gate Count:  
 FD7: 7  
 FD7D2: 8



**Symbol**

D	SN	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1		0	1
1	1		1	0
x	0	x	1	0
x	1		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FD7 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.61	$0.53 + 0.038*SL$	$0.53 + 0.039*SL$	$0.52 + 0.040*SL$
	tR	0.28	$0.10 + 0.086*SL$	$0.09 + 0.091*SL$	$0.08 + 0.092*SL$
CKN to Q	tPLH	0.88	$0.80 + 0.039*SL$	$0.80 + 0.039*SL$	$0.80 + 0.040*SL$
	tPHL	0.96	$0.90 + 0.026*SL$	$0.92 + 0.021*SL$	$0.94 + 0.020*SL$
	tR	0.27	$0.10 + 0.088*SL$	$0.09 + 0.091*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.10 + 0.033*SL$	$0.09 + 0.037*SL$	$0.07 + 0.038*SL$
SN to QN	tPHL	0.47	$0.40 + 0.032*SL$	$0.43 + 0.022*SL$	$0.47 + 0.020*SL$
	tF	0.23	$0.16 + 0.035*SL$	$0.16 + 0.035*SL$	$0.11 + 0.038*SL$
CKN to QN	tPLH	0.88	$0.79 + 0.042*SL$	$0.80 + 0.040*SL$	$0.81 + 0.040*SL$
	tPHL	0.74	$0.69 + 0.029*SL$	$0.71 + 0.021*SL$	$0.74 + 0.020*SL$
	tR	0.30	$0.13 + 0.088*SL$	$0.12 + 0.090*SL$	$0.10 + 0.091*SL$
	tF	0.18	$0.11 + 0.037*SL$	$0.11 + 0.037*SL$	$0.09 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD7 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.342
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (SN)	tRC	0.139



# FD7D2

## D Flip-Flop with Set and 2X Drive

### FD7D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{rj}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

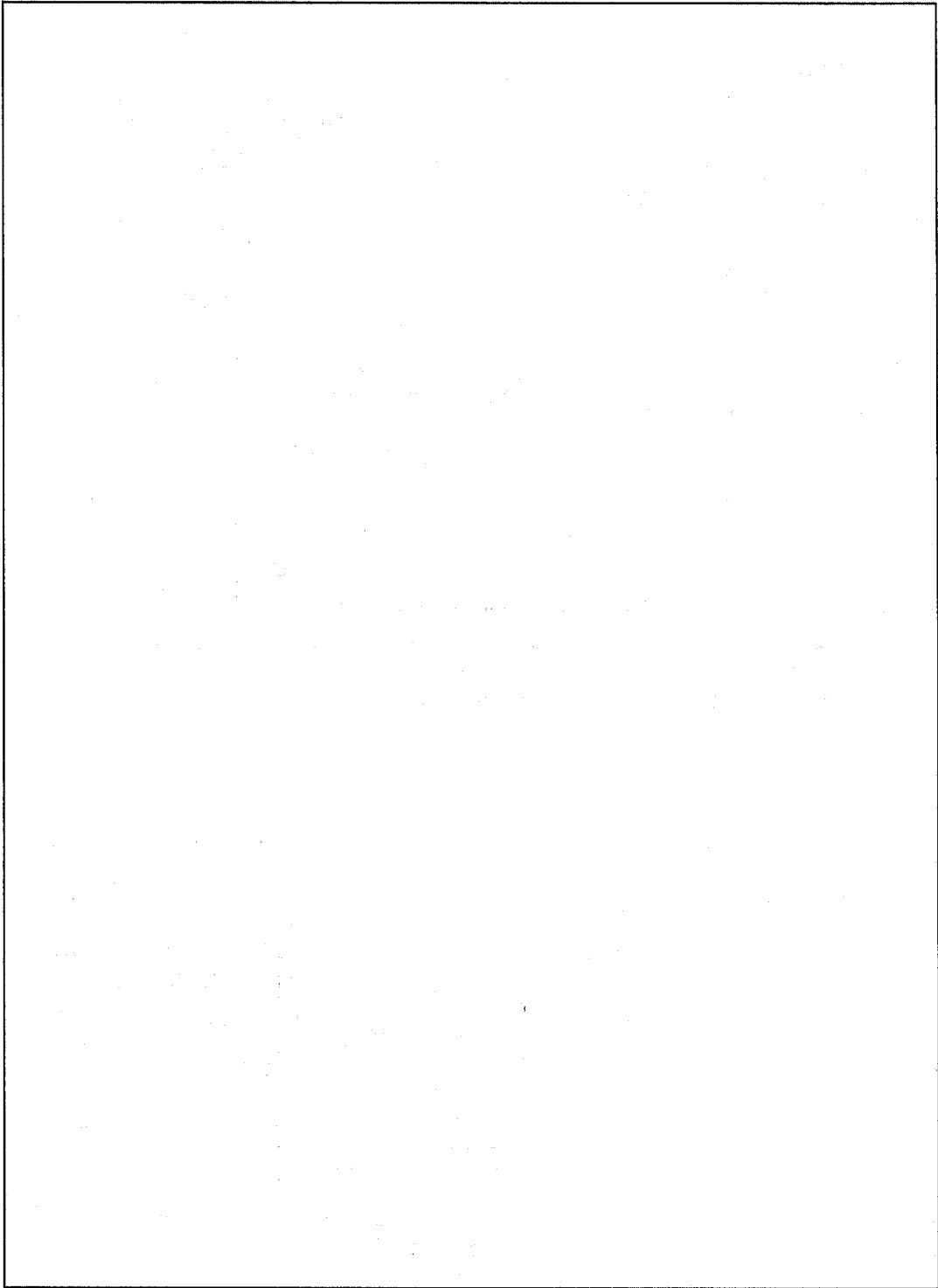
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.65	$0.61 + 0.018 * SL$	$0.61 + 0.019 * SL$	$0.60 + 0.020 * SL$
	tR	0.20	$0.11 + 0.043 * SL$	$0.11 + 0.045 * SL$	$0.08 + 0.046 * SL$
CKN to Q	tPLH	0.92	$0.88 + 0.018 * SL$	$0.88 + 0.019 * SL$	$0.87 + 0.020 * SL$
	tPHL	1.02	$0.99 + 0.015 * SL$	$1.00 + 0.012 * SL$	$1.03 + 0.010 * SL$
	tR	0.19	$0.11 + 0.042 * SL$	$0.10 + 0.045 * SL$	$0.08 + 0.046 * SL$
	tF	0.16	$0.12 + 0.018 * SL$	$0.12 + 0.018 * SL$	$0.11 + 0.019 * SL$
SN to QN	tPHL	0.47	$0.43 + 0.019 * SL$	$0.45 + 0.013 * SL$	$0.50 + 0.010 * SL$
	tF	0.21	$0.17 + 0.020 * SL$	$0.18 + 0.017 * SL$	$0.16 + 0.018 * SL$
CKN to QN	tPLH	0.88	$0.84 + 0.022 * SL$	$0.84 + 0.020 * SL$	$0.85 + 0.020 * SL$
	tPHL	0.75	$0.71 + 0.018 * SL$	$0.73 + 0.012 * SL$	$0.77 + 0.010 * SL$
	tR	0.23	$0.14 + 0.043 * SL$	$0.14 + 0.045 * SL$	$0.12 + 0.046 * SL$
	tF	0.17	$0.13 + 0.020 * SL$	$0.13 + 0.018 * SL$	$0.13 + 0.019 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### FD7D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.397
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (SN)	tRC	0.139



# FD8/FD8D2

## D Flip-Flop with Set, Reset, Negative Edge Trigger

Inputs: D, CKN, SN, RN

Outputs: Q, QN

Input Loading (SL):

- D: 3

- CKN: 1

- SN, RN: 2

Maximum Fanout (Rec. SL):

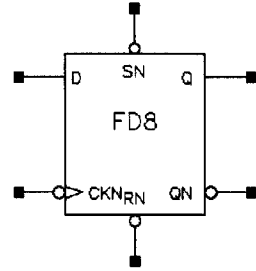
FD8: All : 28

FD8D2: All : 56

Gate Count:

FD8: 8

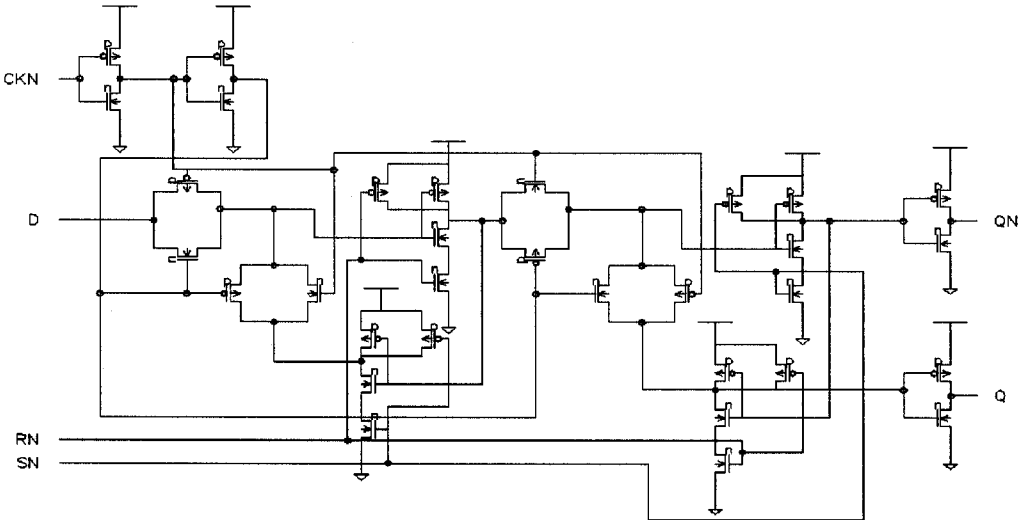
FD8D2 : 9



**Symbol**

D	SN	RN	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	1		0	1
1	1	1		1	0
x	0	1	x	1	0
x	1	0	x	0	1
x	0	0	x	0	0
x	1	1		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FD8 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	1.01	$0.93 + 0.041*SL$	$0.93 + 0.041*SL$	$0.93 + 0.041*SL$
	tPHL	0.95	$0.90 + 0.027*SL$	$0.91 + 0.021*SL$	$0.94 + 0.020*SL$
	tR	0.31	$0.13 + 0.092*SL$	$0.11 + 0.096*SL$	$0.09 + 0.097*SL$
	tF	0.18	$0.11 + 0.035*SL$	$0.10 + 0.036*SL$	$0.07 + 0.038*SL$
RN to Q	tPLH	0.32	$0.23 + 0.044*SL$	$0.24 + 0.041*SL$	$0.24 + 0.041*SL$
	tPHL	0.44	$0.38 + 0.031*SL$	$0.41 + 0.021*SL$	$0.44 + 0.020*SL$
	tR	0.32	$0.14 + 0.091*SL$	$0.13 + 0.095*SL$	$0.09 + 0.097*SL$
	tF	0.21	$0.15 + 0.033*SL$	$0.14 + 0.035*SL$	$0.09 + 0.038*SL$
SN to Q	tPLH	0.70	$0.62 + 0.041*SL$	$0.62 + 0.041*SL$	$0.61 + 0.041*SL$
	tR	0.31	$0.12 + 0.093*SL$	$0.12 + 0.096*SL$	$0.09 + 0.097*SL$
CKN to QN	tPLH	0.87	$0.78 + 0.045*SL$	$0.79 + 0.043*SL$	$0.79 + 0.043*SL$
	tPHL	0.78	$0.72 + 0.029*SL$	$0.74 + 0.022*SL$	$0.78 + 0.020*SL$
	tR	0.33	$0.13 + 0.098*SL$	$0.12 + 0.101*SL$	$0.10 + 0.102*SL$
	tF	0.19	$0.11 + 0.036*SL$	$0.11 + 0.037*SL$	$0.09 + 0.038*SL$
RN to QN	tPLH	0.86	$0.77 + 0.045*SL$	$0.78 + 0.042*SL$	$0.77 + 0.043*SL$
	tR	0.33	$0.13 + 0.097*SL$	$0.12 + 0.101*SL$	$0.10 + 0.102*SL$
SN to QN	tPLH	0.31	$0.22 + 0.045*SL$	$0.22 + 0.042*SL$	$0.22 + 0.043*SL$
	tPHL	0.46	$0.40 + 0.031*SL$	$0.42 + 0.022*SL$	$0.46 + 0.020*SL$
	tR	0.33	$0.14 + 0.097*SL$	$0.13 + 0.100*SL$	$0.10 + 0.102*SL$
	tF	0.22	$0.15 + 0.034*SL$	$0.15 + 0.035*SL$	$0.11 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD8 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.342
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

# FD8D2

## D Flip-Flop with Set, Reset and 2X Drive

### FD8D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

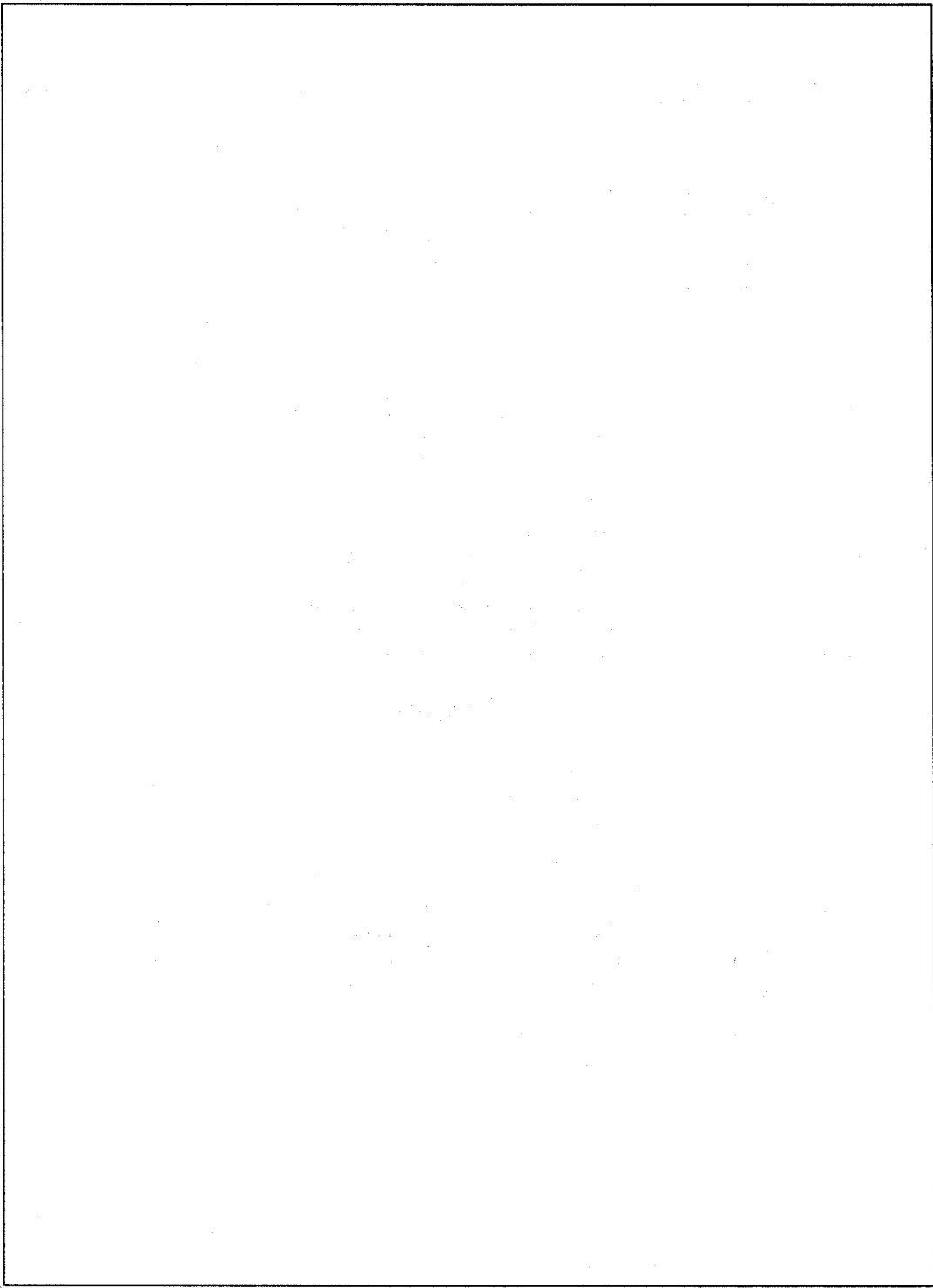
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	1.07	$1.03 + 0.020 \cdot SL$	$1.03 + 0.020 \cdot SL$	$1.02 + 0.020 \cdot SL$
	tPHL	1.01	$0.98 + 0.015 \cdot SL$	$0.99 + 0.012 \cdot SL$	$1.02 + 0.010 \cdot SL$
	tR	0.22	$0.14 + 0.044 \cdot SL$	$0.13 + 0.045 \cdot SL$	$0.11 + 0.047 \cdot SL$
	tF	0.16	$0.13 + 0.018 \cdot SL$	$0.13 + 0.018 \cdot SL$	$0.11 + 0.018 \cdot SL$
RN to Q	tPLH	0.32	$0.27 + 0.023 \cdot SL$	$0.28 + 0.020 \cdot SL$	$0.28 + 0.020 \cdot SL$
	tPHL	0.45	$0.42 + 0.019 \cdot SL$	$0.43 + 0.012 \cdot SL$	$0.48 + 0.010 \cdot SL$
	tR	0.23	$0.14 + 0.044 \cdot SL$	$0.14 + 0.045 \cdot SL$	$0.11 + 0.046 \cdot SL$
	tF	0.20	$0.16 + 0.018 \cdot SL$	$0.17 + 0.017 \cdot SL$	$0.14 + 0.018 \cdot SL$
SN to Q	tPLH	0.75	$0.71 + 0.020 \cdot SL$	$0.72 + 0.020 \cdot SL$	$0.71 + 0.020 \cdot SL$
	tR	0.22	$0.14 + 0.045 \cdot SL$	$0.13 + 0.045 \cdot SL$	$0.11 + 0.047 \cdot SL$
CKN to QN	tPLH	0.87	$0.83 + 0.023 \cdot SL$	$0.83 + 0.021 \cdot SL$	$0.84 + 0.021 \cdot SL$
	tPHL	0.79	$0.75 + 0.018 \cdot SL$	$0.77 + 0.012 \cdot SL$	$0.81 + 0.010 \cdot SL$
	tR	0.23	$0.14 + 0.048 \cdot SL$	$0.14 + 0.049 \cdot SL$	$0.11 + 0.050 \cdot SL$
	tF	0.17	$0.14 + 0.017 \cdot SL$	$0.14 + 0.018 \cdot SL$	$0.13 + 0.018 \cdot SL$
RN to QN	tPLH	0.86	$0.82 + 0.023 \cdot SL$	$0.82 + 0.021 \cdot SL$	$0.83 + 0.021 \cdot SL$
	tR	0.24	$0.15 + 0.045 \cdot SL$	$0.14 + 0.049 \cdot SL$	$0.11 + 0.050 \cdot SL$
SN to QN	tPLH	0.30	$0.25 + 0.023 \cdot SL$	$0.26 + 0.021 \cdot SL$	$0.27 + 0.021 \cdot SL$
	tPHL	0.46	$0.42 + 0.019 \cdot SL$	$0.44 + 0.013 \cdot SL$	$0.49 + 0.010 \cdot SL$
	tR	0.24	$0.14 + 0.048 \cdot SL$	$0.14 + 0.048 \cdot SL$	$0.11 + 0.050 \cdot SL$
	tF	0.21	$0.17 + 0.018 \cdot SL$	$0.18 + 0.017 \cdot SL$	$0.16 + 0.018 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### FD8D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.342
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



# FD8D2Q/FD8D4Q

D Flip-Flop with Set, Reset, Negative Edge Trigger, Q Output Only, 2X Drive or 4X Drive

Inputs: D, CKN, RN, SN

Output: Q

Input Loading (SL):

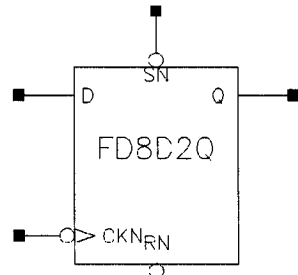
- FD8D2Q: D: 3, CKN: 1  
RN, SN: 2
- FD8D4Q: D: 3, CKN: 1  
RN, SN: 2

Maximum Fanout (Rec. SL):

- FD8D2Q: 56
- FD8D4Q: 112

Gate Count:

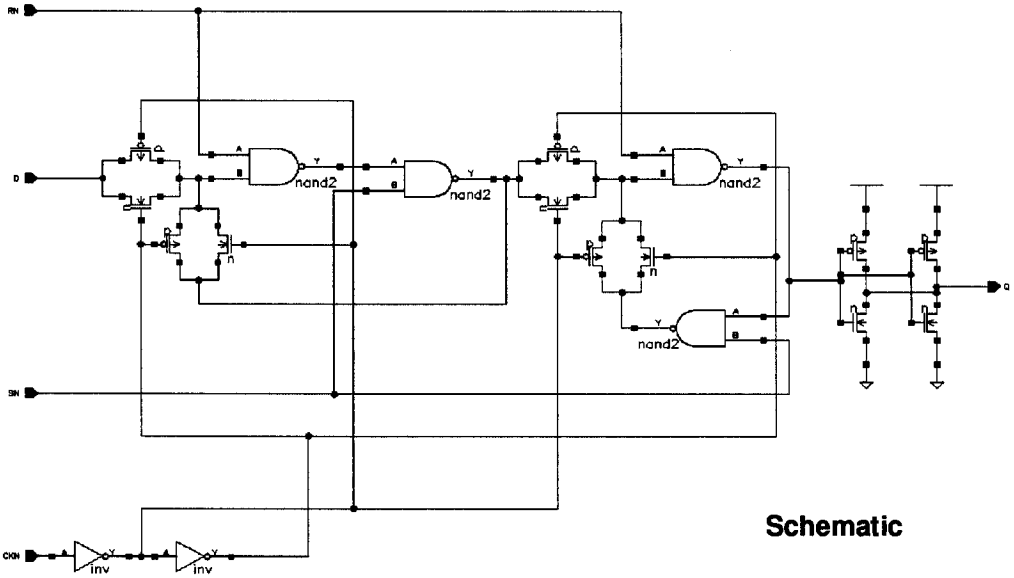
- FD8D2Q: 8
- FD8D4Q: 9



**Symbol**

D	SN	RN	CK	Q <sub>n+1</sub>
0	1	1		0
1	1	1		1
x	0	1	x	1
x	1	0	x	0
x	0	0	x	0
x	1	1		Q <sub>n</sub>

**Truth Table**



**Schematic**

**FD8D2Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.74	$0.69 + 0.027 \cdot SL$	$0.71 + 0.022 \cdot SL$	$0.74 + 0.021 \cdot SL$
	tPHL	0.65	$0.60 + 0.023 \cdot SL$	$0.62 + 0.016 \cdot SL$	$0.69 + 0.012 \cdot SL$
	tR	0.29	$0.20 + 0.045 \cdot SL$	$0.20 + 0.046 \cdot SL$	$0.17 + 0.047 \cdot SL$
	tF	0.21	$0.15 + 0.027 \cdot SL$	$0.17 + 0.021 \cdot SL$	$0.21 + 0.019 \cdot SL$
RN to Q	tPLH	0.53	$0.48 + 0.026 \cdot SL$	$0.49 + 0.021 \cdot SL$	$0.52 + 0.020 \cdot SL$
	tPHL	0.64	$0.59 + 0.025 \cdot SL$	$0.62 + 0.016 \cdot SL$	$0.71 + 0.012 \cdot SL$
	tR	0.29	$0.21 + 0.042 \cdot SL$	$0.20 + 0.045 \cdot SL$	$0.17 + 0.047 \cdot SL$
	tF	0.29	$0.24 + 0.025 \cdot SL$	$0.26 + 0.019 \cdot SL$	$0.28 + 0.018 \cdot SL$
SN to Q	tPLH	1.06	$1.01 + 0.026 \cdot SL$	$1.02 + 0.022 \cdot SL$	$1.05 + 0.020 \cdot SL$
	tR	0.29	$0.21 + 0.043 \cdot SL$	$0.20 + 0.045 \cdot SL$	$0.17 + 0.047 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FD8D2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.397
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



# FD8D4Q

D Flip-Flop with Set, Reset, Negative Edge Trigger, Q Output Only, 4X Drive

## FD8D4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

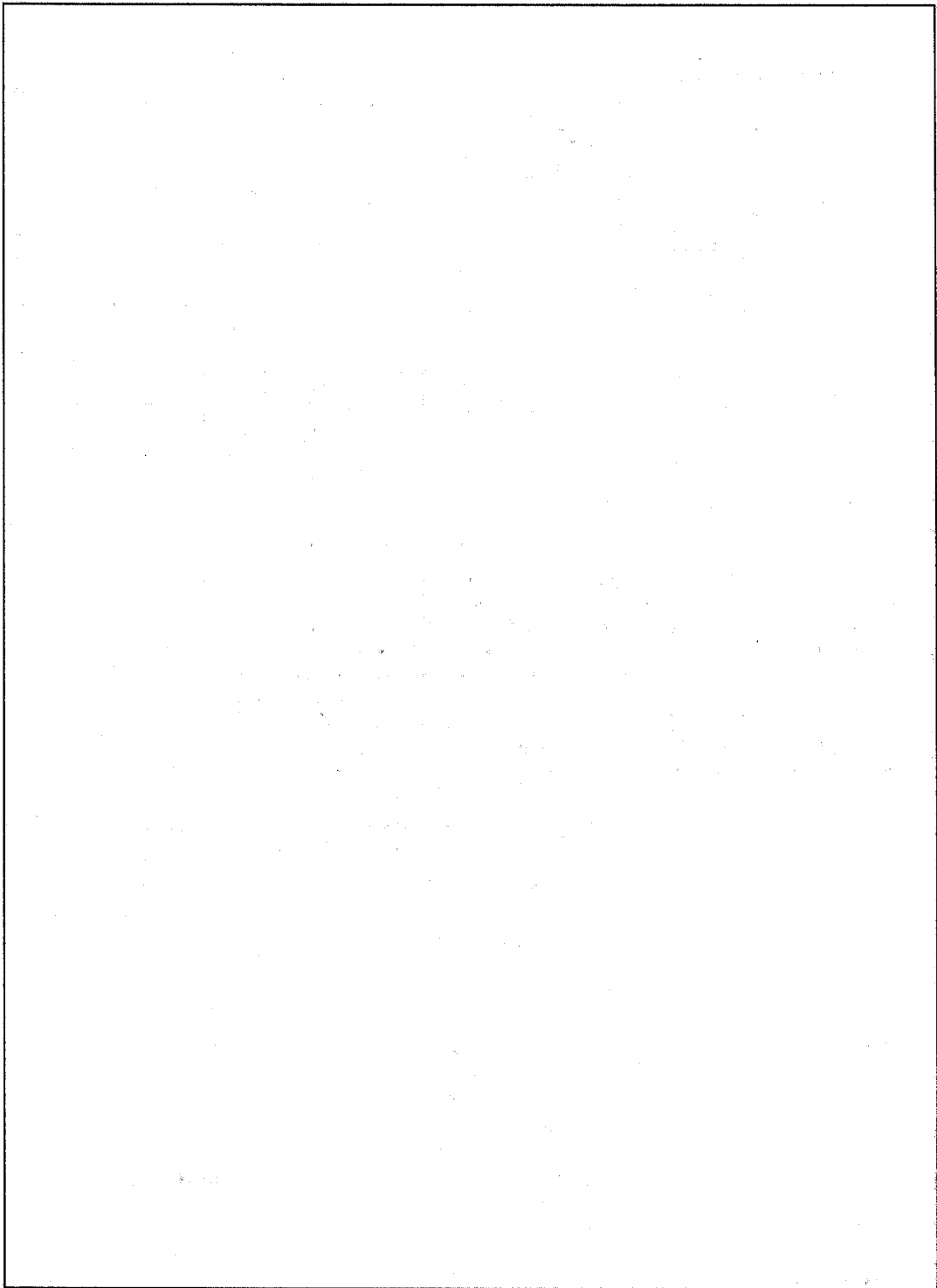
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q	tPLH	0.82	$0.79 + 0.016*SL$	$0.80 + 0.012*SL$	$0.82 + 0.011*SL$
	tPHL	0.68	$0.65 + 0.013*SL$	$0.66 + 0.010*SL$	$0.71 + 0.008*SL$
	tR	0.30	$0.26 + 0.020*SL$	$0.26 + 0.021*SL$	$0.24 + 0.022*SL$
	tF	0.23	$0.19 + 0.016*SL$	$0.20 + 0.012*SL$	$0.24 + 0.010*SL$
RN to Q	tPLH	0.60	$0.57 + 0.015*SL$	$0.58 + 0.012*SL$	$0.61 + 0.010*SL$
	tPHL	0.70	$0.67 + 0.015*SL$	$0.68 + 0.010*SL$	$0.73 + 0.008*SL$
	tR	0.30	$0.26 + 0.019*SL$	$0.25 + 0.021*SL$	$0.23 + 0.022*SL$
	tF	0.31	$0.28 + 0.013*SL$	$0.29 + 0.011*SL$	$0.32 + 0.009*SL$
SN to Q	tPLH	1.13	$1.10 + 0.016*SL$	$1.11 + 0.012*SL$	$1.14 + 0.010*SL$
	tR	0.30	$0.26 + 0.018*SL$	$0.25 + 0.021*SL$	$0.23 + 0.022*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD8D4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.397
Input Setup Time (D to CKN)	tSU	0.178
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



# FD8SD2Q/FD8SD4Q

D Flip-Flop with Set, Reset, Negative Edge Trigger, Scan, Q Output Only, 2X or 4X Drive

Inputs: D, TI, TE, CKN, RN, SN

Output: Q

Input Loading (SL):

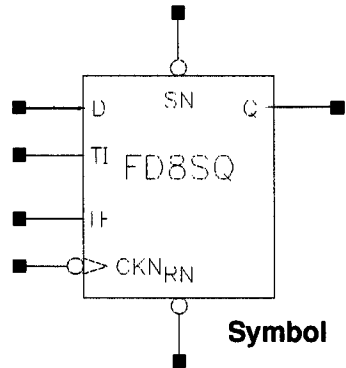
- FD8SD2Q: D, CKN, TI : 1  
RN, SN, TE : 2
- FD8SD4Q: D, CKN, TI : 1  
RN, SN, TE : 2

Maximum Fanout (Rec. SL):

- FD8SD2Q: 56
- FD8SD4Q: 112

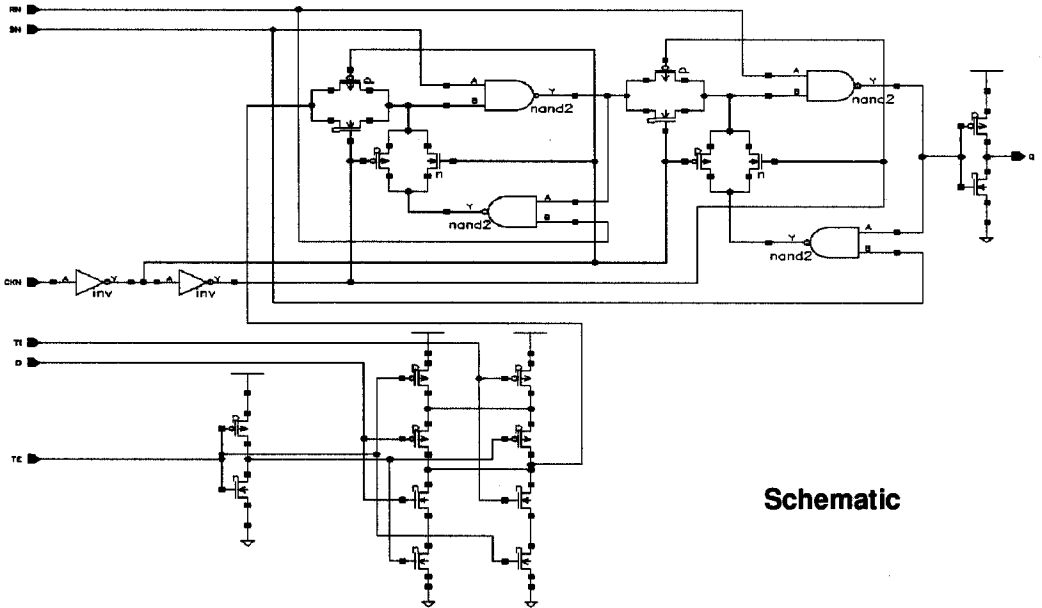
Gate Count:

- FD8SD2Q: 11
- FD8SD4Q: 12



Truth Table

D	SN	RN	TI	TE	CKN	Q <sub>n+1</sub>
0	1	1	X	0		0
1	1	1	X	0		1
x	1	1	0	1		0
x	1	1	1	1		1
x	0	1	x	x	x	1
x	1	0	x	x	x	0
x	0	0	x	x	x	0
x	1	1	x	x		Q <sub>n</sub>



**FD8SD2Q Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_r = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.86	$0.81 + 0.023 \cdot SL$	$0.82 + 0.020 \cdot SL$	$0.83 + 0.020 \cdot SL$
	tR	0.23	$0.15 + 0.042 \cdot SL$	$0.13 + 0.046 \cdot SL$	$0.11 + 0.047 \cdot SL$
RN to Q	tPLH	0.30	$0.25 + 0.023 \cdot SL$	$0.26 + 0.021 \cdot SL$	$0.27 + 0.020 \cdot SL$
	tPHL	0.45	$0.42 + 0.019 \cdot SL$	$0.43 + 0.013 \cdot SL$	$0.48 + 0.010 \cdot SL$
	tR	0.23	$0.14 + 0.044 \cdot SL$	$0.14 + 0.046 \cdot SL$	$0.11 + 0.047 \cdot SL$
	tF	0.20	$0.16 + 0.019 \cdot SL$	$0.17 + 0.017 \cdot SL$	$0.15 + 0.018 \cdot SL$
CKN to Q	tPLH	0.87	$0.82 + 0.023 \cdot SL$	$0.83 + 0.021 \cdot SL$	$0.84 + 0.020 \cdot SL$
	tPHL	0.78	$0.74 + 0.018 \cdot SL$	$0.76 + 0.012 \cdot SL$	$0.80 + 0.010 \cdot SL$
	tR	0.23	$0.14 + 0.046 \cdot SL$	$0.14 + 0.046 \cdot SL$	$0.11 + 0.047 \cdot SL$
	tF	0.17	$0.13 + 0.019 \cdot SL$	$0.13 + 0.018 \cdot SL$	$0.13 + 0.019 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FD8SD2Q Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.178
Input Hold Time (TE to CKN)	tHD	0.178
Input Hold Time (TI to CKN)	tHD	0.069
Input Setup Time (D to CKN)	tSU	0.561
Input Setup Time (TE to CKN)	tSU	0.780
Input Setup Time (TI to CKN)	tSU	0.616
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

# FD8SD4Q

D Flip-Flop with Set, Reset, Negative Edge Trigger, Scan, Q Output Only, 4X Drive

## FD8SD4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_r = 0.80ns$ ]

(SL: Standard Load)

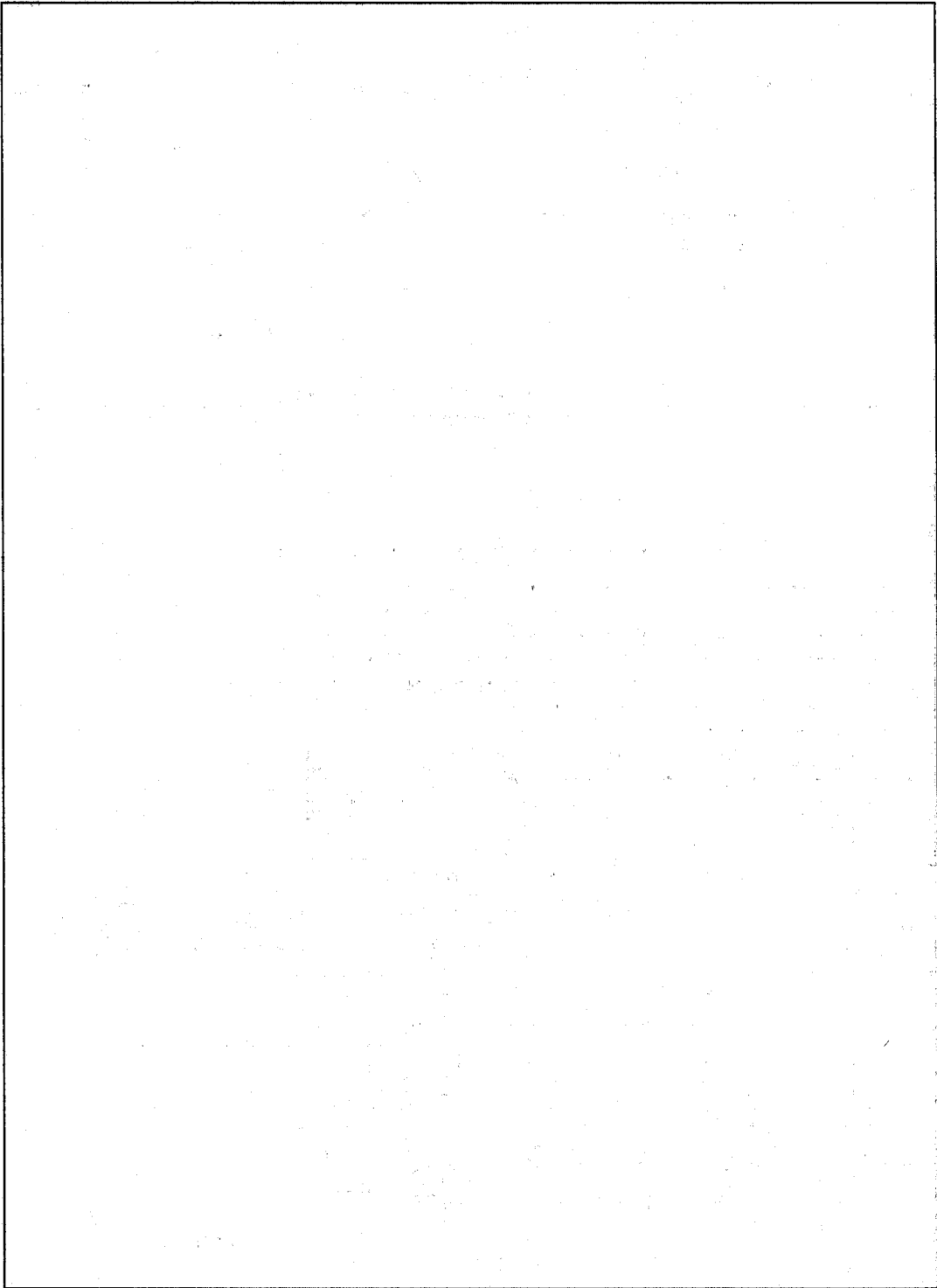
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.93	$0.90 + 0.012*SL$	$0.91 + 0.011*SL$	$0.92 + 0.010*SL$
	tR	0.21	$0.17 + 0.021*SL$	$0.17 + 0.022*SL$	$0.15 + 0.023*SL$
RN to Q	tPLH	0.36	$0.34 + 0.013*SL$	$0.34 + 0.011*SL$	$0.36 + 0.010*SL$
	tPHL	0.50	$0.48 + 0.011*SL$	$0.49 + 0.008*SL$	$0.53 + 0.006*SL$
	tR	0.22	$0.18 + 0.020*SL$	$0.17 + 0.022*SL$	$0.16 + 0.023*SL$
	tF	0.22	$0.20 + 0.010*SL$	$0.21 + 0.009*SL$	$0.21 + 0.009*SL$
CKN to Q	tPLH	0.94	$0.91 + 0.013*SL$	$0.92 + 0.011*SL$	$0.93 + 0.010*SL$
	tPHL	0.84	$0.81 + 0.011*SL$	$0.82 + 0.008*SL$	$0.86 + 0.006*SL$
	tR	0.22	$0.18 + 0.020*SL$	$0.17 + 0.022*SL$	$0.16 + 0.023*SL$
	tF	0.19	$0.17 + 0.010*SL$	$0.17 + 0.009*SL$	$0.18 + 0.009*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD8SD4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

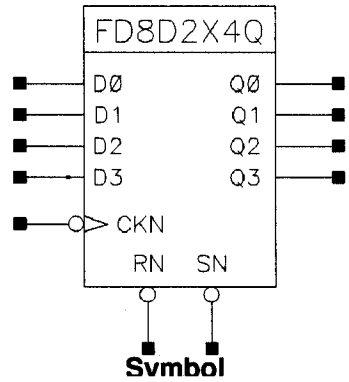
Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D to CKN)	tHD	0.178
Input Hold Time (TE to CKN)	tHD	0.178
Input Hold Time (TI to CKN)	tHD	0.069
Input Setup Time (D to CKN)	tSU	0.561
Input Setup Time (TE to CKN)	tSU	0.780
Input Setup Time (TI to CKN)	tSU	0.616
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



# FD8D2X4Q/FD8D4X4Q

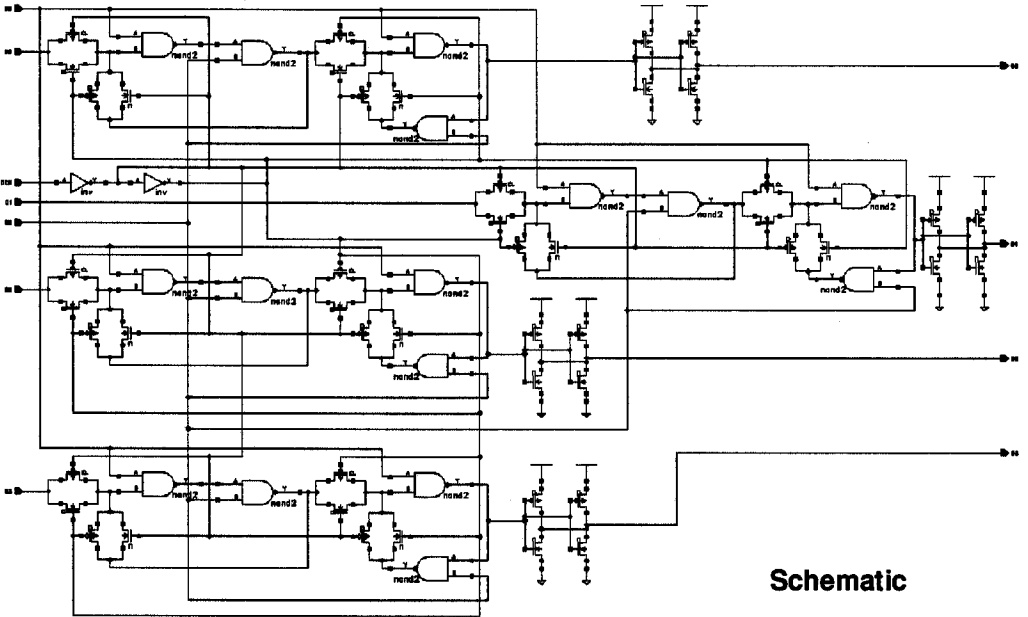
4-Bit D Flip-Flop with Set, Reset, Negative Edge Trigger, Q Output Only, 2X or 4X Drive

- Inputs: D0, D1, D2, D3, CKN, RN, SN  
 Output: Q0, Q1, Q2, Q3  
 Input Loading (SL): All: D0, D1, D2, D3: 3  
 CKN: 1, RN, SN: 8  
 Maximum Fanout (Rec. SL):  
 - FD8D2X4Q: 56  
 - FD8D4X4Q: 112  
 Gate Count:  
 - FD8D2X4Q: 29  
 - FD8D4X4Q: 33



D	SN	RN	CK	Q <sub>n+1</sub>
0	1	1		0
1	1	1		1
x	0	1	x	1
x	1	0	x	0
x	0	0	x	0
x	1	1		Q <sub>n</sub>

Truth Table



## FD8D2X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	1.00	$0.95 + 0.026 \cdot SL$	$0.96 + 0.022 \cdot SL$	$0.99 + 0.021 \cdot SL$
	tPHL	1.01	$0.96 + 0.024 \cdot SL$	$0.98 + 0.016 \cdot SL$	$1.06 + 0.012 \cdot SL$
	tR	0.28	$0.19 + 0.046 \cdot SL$	$0.19 + 0.046 \cdot SL$	$0.17 + 0.047 \cdot SL$
	tF	0.25	$0.20 + 0.024 \cdot SL$	$0.21 + 0.020 \cdot SL$	$0.25 + 0.019 \cdot SL$
RN to Q0	tPLH	0.53	$0.48 + 0.026 \cdot SL$	$0.50 + 0.022 \cdot SL$	$0.52 + 0.020 \cdot SL$
	tPHL	0.64	$0.59 + 0.025 \cdot SL$	$0.61 + 0.016 \cdot SL$	$0.70 + 0.012 \cdot SL$
	tR	0.29	$0.21 + 0.042 \cdot SL$	$0.20 + 0.045 \cdot SL$	$0.17 + 0.047 \cdot SL$
	tF	0.29	$0.24 + 0.025 \cdot SL$	$0.26 + 0.019 \cdot SL$	$0.28 + 0.018 \cdot SL$
SN to Q0	tPLH	1.06	$1.01 + 0.026 \cdot SL$	$1.02 + 0.022 \cdot SL$	$1.05 + 0.020 \cdot SL$
	tR	0.29	$0.21 + 0.043 \cdot SL$	$0.20 + 0.045 \cdot SL$	$0.17 + 0.047 \cdot SL$
CKN to Q1	tPLH	1.00	$0.95 + 0.027 \cdot SL$	$0.96 + 0.023 \cdot SL$	$0.99 + 0.022 \cdot SL$
	tPHL	1.00	$0.95 + 0.024 \cdot SL$	$0.98 + 0.016 \cdot SL$	$1.06 + 0.012 \cdot SL$
	tR	0.29	$0.20 + 0.049 \cdot SL$	$0.19 + 0.051 \cdot SL$	$0.17 + 0.051 \cdot SL$
	tF	0.25	$0.21 + 0.024 \cdot SL$	$0.22 + 0.021 \cdot SL$	$0.24 + 0.019 \cdot SL$
RN to Q1	tPLH	0.54	$0.48 + 0.027 \cdot SL$	$0.50 + 0.023 \cdot SL$	$0.52 + 0.022 \cdot SL$
	tPHL	0.63	$0.58 + 0.025 \cdot SL$	$0.61 + 0.016 \cdot SL$	$0.70 + 0.012 \cdot SL$
	tR	0.31	$0.21 + 0.046 \cdot SL$	$0.20 + 0.050 \cdot SL$	$0.17 + 0.051 \cdot SL$
	tF	0.29	$0.24 + 0.024 \cdot SL$	$0.26 + 0.019 \cdot SL$	$0.28 + 0.018 \cdot SL$
SN to Q1	tPLH	1.07	$1.01 + 0.027 \cdot SL$	$1.02 + 0.023 \cdot SL$	$1.05 + 0.022 \cdot SL$
	tR	0.30	$0.21 + 0.046 \cdot SL$	$0.20 + 0.050 \cdot SL$	$0.17 + 0.051 \cdot SL$
CKN to Q2	tPLH	1.00	$0.95 + 0.027 \cdot SL$	$0.96 + 0.023 \cdot SL$	$0.99 + 0.022 \cdot SL$
	tPHL	1.01	$0.96 + 0.024 \cdot SL$	$0.98 + 0.016 \cdot SL$	$1.06 + 0.012 \cdot SL$
	tR	0.30	$0.20 + 0.049 \cdot SL$	$0.19 + 0.050 \cdot SL$	$0.17 + 0.051 \cdot SL$
	tF	0.26	$0.21 + 0.025 \cdot SL$	$0.22 + 0.022 \cdot SL$	$0.25 + 0.020 \cdot SL$
RN to Q2	tPLH	0.53	$0.48 + 0.027 \cdot SL$	$0.49 + 0.023 \cdot SL$	$0.52 + 0.022 \cdot SL$
	tPHL	0.64	$0.59 + 0.026 \cdot SL$	$0.61 + 0.017 \cdot SL$	$0.70 + 0.012 \cdot SL$
	tR	0.31	$0.22 + 0.046 \cdot SL$	$0.21 + 0.050 \cdot SL$	$0.17 + 0.051 \cdot SL$
	tF	0.30	$0.25 + 0.025 \cdot SL$	$0.26 + 0.020 \cdot SL$	$0.28 + 0.019 \cdot SL$
SN to Q2	tPLH	1.06	$1.01 + 0.027 \cdot SL$	$1.02 + 0.023 \cdot SL$	$1.04 + 0.022 \cdot SL$
	tR	0.31	$0.22 + 0.046 \cdot SL$	$0.20 + 0.050 \cdot SL$	$0.17 + 0.051 \cdot SL$
CKN to Q3	tPLH	1.00	$0.95 + 0.026 \cdot SL$	$0.96 + 0.022 \cdot SL$	$0.99 + 0.021 \cdot SL$
	tPHL	1.01	$0.96 + 0.024 \cdot SL$	$0.98 + 0.016 \cdot SL$	$1.06 + 0.012 \cdot SL$
	tR	0.28	$0.19 + 0.045 \cdot SL$	$0.19 + 0.046 \cdot SL$	$0.17 + 0.047 \cdot SL$
	tF	0.25	$0.20 + 0.024 \cdot SL$	$0.21 + 0.020 \cdot SL$	$0.24 + 0.019 \cdot SL$
RN to Q3	tPLH	0.53	$0.48 + 0.026 \cdot SL$	$0.50 + 0.022 \cdot SL$	$0.52 + 0.020 \cdot SL$
	tPHL	0.64	$0.59 + 0.025 \cdot SL$	$0.61 + 0.016 \cdot SL$	$0.70 + 0.012 \cdot SL$
	tR	0.29	$0.21 + 0.042 \cdot SL$	$0.20 + 0.045 \cdot SL$	$0.17 + 0.047 \cdot SL$
	tF	0.29	$0.24 + 0.025 \cdot SL$	$0.26 + 0.019 \cdot SL$	$0.28 + 0.018 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# FD8D2X4Q

4-Bit D Flip-Flop with Set, Reset, Negative Edge Trigger, Q Output Only, 2X Drive

## FD8D2X4Q Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q3	tPLH	1.06	$1.01 + 0.026*SL$	$1.02 + 0.022*SL$	$1.05 + 0.020*SL$
	tR	0.29	$0.21 + 0.043*SL$	$0.20 + 0.045*SL$	$0.17 + 0.047*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FD8D2X4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	0.998
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D0 to CKN)	tHD	0.616
Input Hold Time (D1 to CKN)	tHD	0.616
Input Hold Time (D2 to CKN)	tHD	0.616
Input Hold Time (D3 to CKN)	tHD	0.616
Input Setup Time (D0 to CKN)	tSU	0.000
Input Setup Time (D1 to CKN)	tSU	0.000
Input Setup Time (D2 to CKN)	tSU	0.000
Input Setup Time (D3 to CKN)	tSU	0.000
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

**FD8D4X4Q Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CKN to Q0	tPLH	1.10	$1.07 + 0.015 \cdot SL$	$1.08 + 0.012 \cdot SL$	$1.11 + 0.011 \cdot SL$
	tPHL	1.04	$1.02 + 0.014 \cdot SL$	$1.03 + 0.010 \cdot SL$	$1.07 + 0.008 \cdot SL$
	tR	0.30	$0.26 + 0.021 \cdot SL$	$0.26 + 0.021 \cdot SL$	$0.23 + 0.023 \cdot SL$
	tF	0.27	$0.23 + 0.016 \cdot SL$	$0.25 + 0.012 \cdot SL$	$0.28 + 0.010 \cdot SL$
RN to Q0	tPLH	0.61	$0.58 + 0.015 \cdot SL$	$0.59 + 0.012 \cdot SL$	$0.62 + 0.010 \cdot SL$
	tPHL	0.70	$0.67 + 0.015 \cdot SL$	$0.68 + 0.010 \cdot SL$	$0.73 + 0.008 \cdot SL$
	tR	0.31	$0.27 + 0.020 \cdot SL$	$0.27 + 0.021 \cdot SL$	$0.24 + 0.022 \cdot SL$
	tF	0.32	$0.29 + 0.013 \cdot SL$	$0.30 + 0.012 \cdot SL$	$0.33 + 0.010 \cdot SL$
SN to Q0	tPLH	1.13	$1.10 + 0.016 \cdot SL$	$1.11 + 0.012 \cdot SL$	$1.14 + 0.010 \cdot SL$
	tR	0.30	$0.26 + 0.018 \cdot SL$	$0.25 + 0.021 \cdot SL$	$0.24 + 0.022 \cdot SL$
CKN to Q1	tPLH	1.10	$1.07 + 0.015 \cdot SL$	$1.07 + 0.012 \cdot SL$	$1.10 + 0.011 \cdot SL$
	tPHL	1.04	$1.01 + 0.014 \cdot SL$	$1.03 + 0.010 \cdot SL$	$1.07 + 0.008 \cdot SL$
	tR	0.31	$0.26 + 0.021 \cdot SL$	$0.26 + 0.022 \cdot SL$	$0.23 + 0.023 \cdot SL$
	tF	0.27	$0.24 + 0.016 \cdot SL$	$0.25 + 0.012 \cdot SL$	$0.28 + 0.010 \cdot SL$
RN to Q1	tPLH	0.61	$0.58 + 0.016 \cdot SL$	$0.59 + 0.012 \cdot SL$	$0.61 + 0.011 \cdot SL$
	tPHL	0.70	$0.67 + 0.015 \cdot SL$	$0.68 + 0.011 \cdot SL$	$0.73 + 0.008 \cdot SL$
	tR	0.32	$0.28 + 0.019 \cdot SL$	$0.27 + 0.022 \cdot SL$	$0.25 + 0.023 \cdot SL$
	tF	0.32	$0.30 + 0.013 \cdot SL$	$0.30 + 0.012 \cdot SL$	$0.33 + 0.010 \cdot SL$
SN to Q1	tPLH	1.13	$1.10 + 0.015 \cdot SL$	$1.11 + 0.012 \cdot SL$	$1.14 + 0.011 \cdot SL$
	tR	0.30	$0.26 + 0.019 \cdot SL$	$0.26 + 0.022 \cdot SL$	$0.23 + 0.023 \cdot SL$
CKN to Q2	tPLH	1.10	$1.07 + 0.015 \cdot SL$	$1.08 + 0.012 \cdot SL$	$1.10 + 0.011 \cdot SL$
	tPHL	1.04	$1.02 + 0.014 \cdot SL$	$1.03 + 0.010 \cdot SL$	$1.07 + 0.008 \cdot SL$
	tR	0.31	$0.27 + 0.020 \cdot SL$	$0.26 + 0.022 \cdot SL$	$0.23 + 0.023 \cdot SL$
	tF	0.27	$0.24 + 0.015 \cdot SL$	$0.25 + 0.012 \cdot SL$	$0.28 + 0.010 \cdot SL$
RN to Q2	tPLH	0.61	$0.58 + 0.016 \cdot SL$	$0.59 + 0.012 \cdot SL$	$0.61 + 0.011 \cdot SL$
	tPHL	0.70	$0.67 + 0.015 \cdot SL$	$0.68 + 0.011 \cdot SL$	$0.73 + 0.008 \cdot SL$
	tR	0.32	$0.28 + 0.019 \cdot SL$	$0.27 + 0.022 \cdot SL$	$0.25 + 0.023 \cdot SL$
	tF	0.32	$0.30 + 0.013 \cdot SL$	$0.30 + 0.012 \cdot SL$	$0.33 + 0.010 \cdot SL$
SN to Q2	tPLH	1.13	$1.10 + 0.016 \cdot SL$	$1.11 + 0.012 \cdot SL$	$1.14 + 0.011 \cdot SL$
	tR	0.30	$0.26 + 0.020 \cdot SL$	$0.26 + 0.022 \cdot SL$	$0.23 + 0.023 \cdot SL$
CKN to Q3	tPLH	1.10	$1.07 + 0.015 \cdot SL$	$1.08 + 0.012 \cdot SL$	$1.11 + 0.011 \cdot SL$
	tPHL	1.04	$1.02 + 0.014 \cdot SL$	$1.03 + 0.010 \cdot SL$	$1.07 + 0.008 \cdot SL$
	tR	0.30	$0.26 + 0.020 \cdot SL$	$0.26 + 0.021 \cdot SL$	$0.24 + 0.023 \cdot SL$
	tF	0.27	$0.23 + 0.016 \cdot SL$	$0.25 + 0.012 \cdot SL$	$0.28 + 0.010 \cdot SL$
RN to Q3	tPLH	0.61	$0.58 + 0.015 \cdot SL$	$0.59 + 0.012 \cdot SL$	$0.62 + 0.010 \cdot SL$
	tPHL	0.70	$0.67 + 0.015 \cdot SL$	$0.68 + 0.010 \cdot SL$	$0.73 + 0.008 \cdot SL$
	tR	0.31	$0.27 + 0.020 \cdot SL$	$0.27 + 0.021 \cdot SL$	$0.24 + 0.022 \cdot SL$
	tF	0.32	$0.29 + 0.013 \cdot SL$	$0.30 + 0.012 \cdot SL$	$0.33 + 0.010 \cdot SL$
SN to Q3	tPLH	1.13	$1.10 + 0.016 \cdot SL$	$1.11 + 0.012 \cdot SL$	$1.14 + 0.010 \cdot SL$
	tR	0.30	$0.26 + 0.018 \cdot SL$	$0.25 + 0.021 \cdot SL$	$0.24 + 0.022 \cdot SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

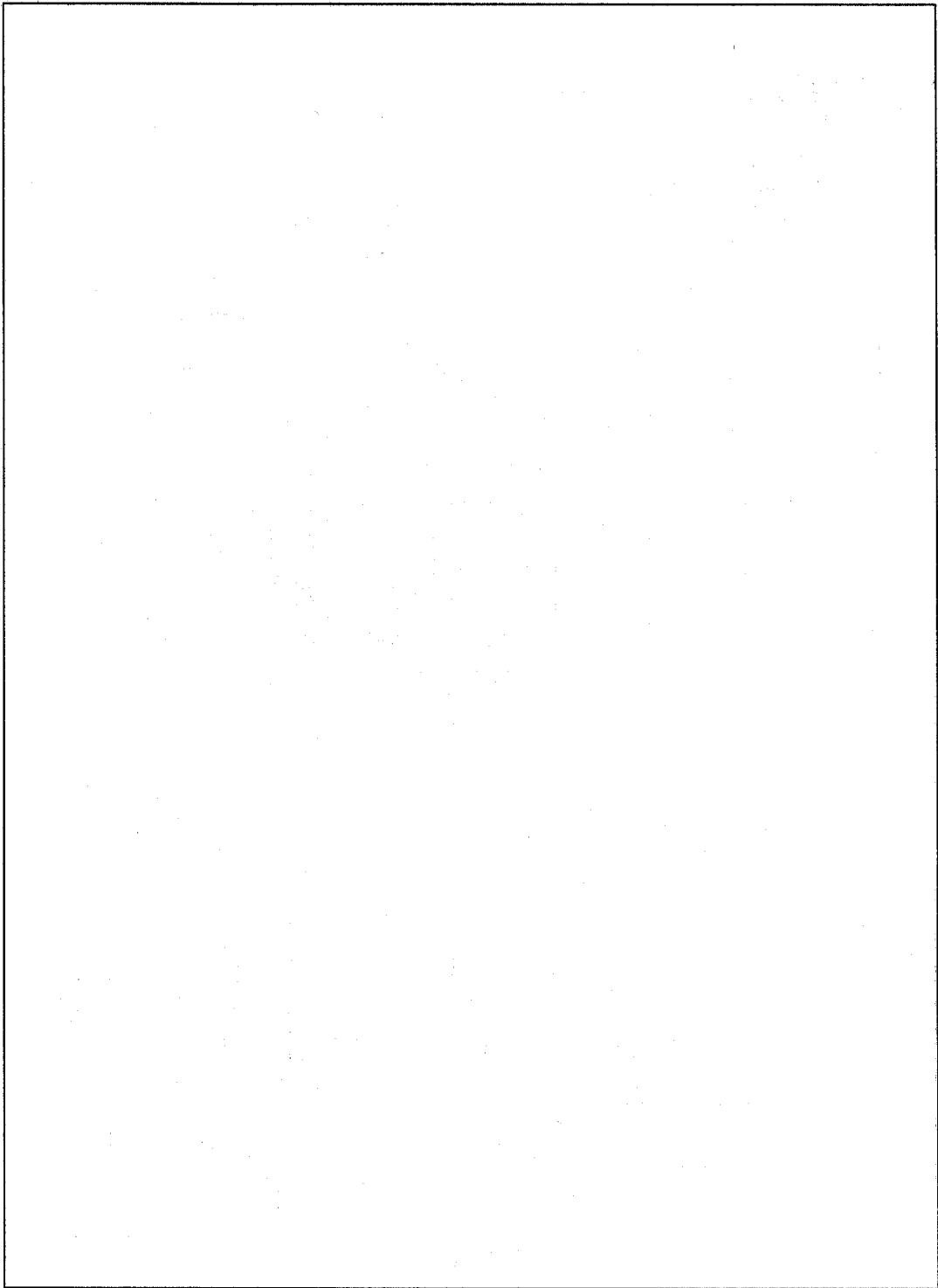
## FD8D4X4Q

4-Bit D Flip-Flop with Set, Reset, Negative Edge Trigger, Q Output Only, 4X Drive

### FD8D4X4Q Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CKN)	tPWL	1.077
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CKN)	tPWH	0.920
Input Hold Time (D0 to CKN)	tHD	0.616
Input Hold Time (D1 to CKN)	tHD	0.616
Input Hold Time (D2 to CKN)	tHD	0.616
Input Hold Time (D3 to CKN)	tHD	0.616
Input Setup Time (D0 to CKN)	tSU	0.000
Input Setup Time (D1 to CKN)	tSU	0.000
Input Setup Time (D2 to CKN)	tSU	0.000
Input Setup Time (D3 to CKN)	tSU	0.000
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



# FG1

## D Flip-Flop with CK Enable, Positive Edge Trigger

Inputs: D, E, CK

Outputs: Q, QN

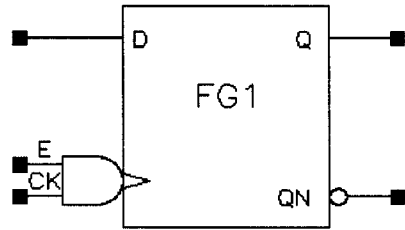
Input Loading (SL):

- D: 3

- E, CK: 1

Maximum Fanout (Rec. SL): All : 28

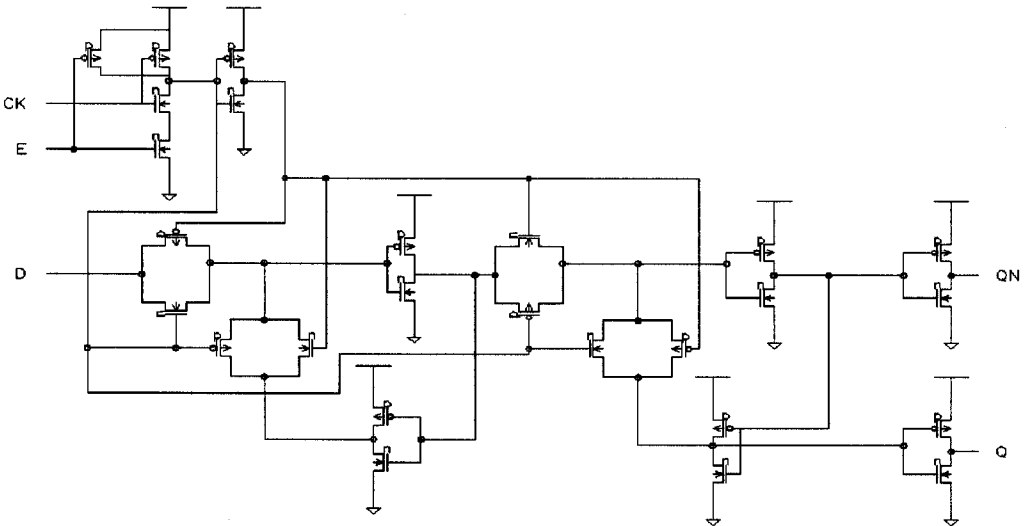
Gate Count: 7



**Symbol**

D	E	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1		0	1
1	1		1	0
x	0	x	Q <sub>n</sub>	Q <sub>Nn</sub>
x	x		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FG1 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.81	$0.73 + 0.040 * SL$	$0.73 + 0.041 * SL$	$0.73 + 0.041 * SL$
	tPHL	0.75	$0.70 + 0.026 * SL$	$0.72 + 0.021 * SL$	$0.73 + 0.020 * SL$
	tR	0.29	$0.10 + 0.094 * SL$	$0.09 + 0.097 * SL$	$0.08 + 0.097 * SL$
	tF	0.17	$0.09 + 0.035 * SL$	$0.09 + 0.037 * SL$	$0.06 + 0.038 * SL$
E to Q	tPLH	0.78	$0.70 + 0.040 * SL$	$0.69 + 0.041 * SL$	$0.69 + 0.041 * SL$
	tPHL	0.72	$0.66 + 0.027 * SL$	$0.68 + 0.021 * SL$	$0.70 + 0.020 * SL$
	tR	0.29	$0.10 + 0.093 * SL$	$0.09 + 0.097 * SL$	$0.08 + 0.097 * SL$
	tF	0.17	$0.10 + 0.035 * SL$	$0.09 + 0.037 * SL$	$0.06 + 0.038 * SL$
CK to QN	tPLH	0.69	$0.60 + 0.044 * SL$	$0.61 + 0.043 * SL$	$0.61 + 0.043 * SL$
	tPHL	0.66	$0.61 + 0.028 * SL$	$0.63 + 0.021 * SL$	$0.65 + 0.020 * SL$
	tR	0.31	$0.11 + 0.099 * SL$	$0.10 + 0.101 * SL$	$0.09 + 0.102 * SL$
	tF	0.17	$0.10 + 0.037 * SL$	$0.10 + 0.037 * SL$	$0.07 + 0.039 * SL$
E to QN	tPLH	0.65	$0.56 + 0.044 * SL$	$0.57 + 0.043 * SL$	$0.57 + 0.043 * SL$
	tPHL	0.63	$0.57 + 0.027 * SL$	$0.59 + 0.021 * SL$	$0.62 + 0.020 * SL$
	tR	0.31	$0.11 + 0.100 * SL$	$0.10 + 0.101 * SL$	$0.09 + 0.102 * SL$
	tF	0.17	$0.10 + 0.037 * SL$	$0.10 + 0.037 * SL$	$0.07 + 0.039 * SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FG1 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (E)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Pulse Width High (E)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.287
Input Hold Time (D to E)	tHD	0.287
Input Setup Time (D to CK)	tSU	0.233
Input Setup Time (D to E)	tSU	0.287

# FG1X4

## 4-Bit D Flip-Flop with CK Enable

Inputs: D0, D1, D2, D3, E, CK  
 Outputs: Q0, Q1, Q2, Q3

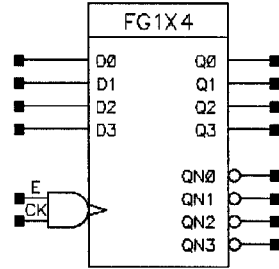
QN0, QN1, QN2, QN3

Input Loading (SL):

- D0, D1, D2, D3: 3
- E, CK: 1

Maximum Fanout (Rec. SL): All : 28

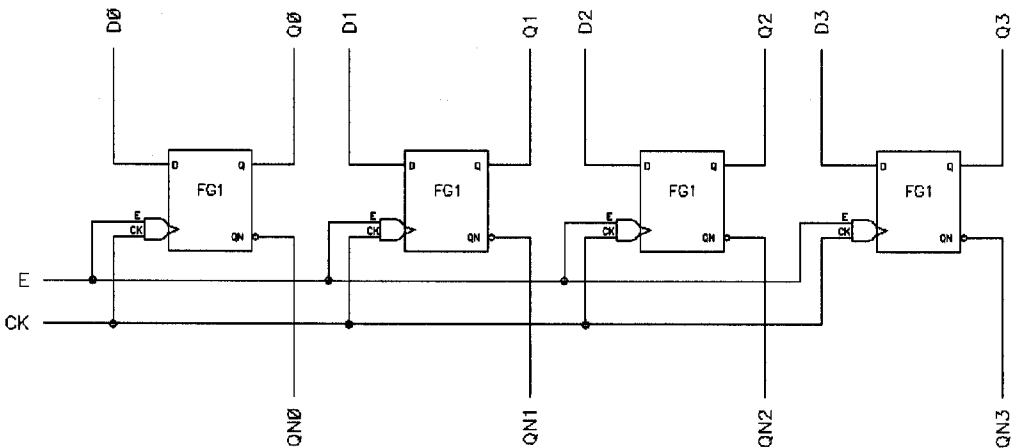
Gate Count: 22



**Symbol**

D	E	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1		0	1
1	1		1	0
x	0	x	Q <sub>n</sub>	Q <sub>Nn</sub>
x	x		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FG1X4 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q0	tPLH	1.20	$1.12 + 0.040 * SL$	$1.12 + 0.041 * SL$	$1.11 + 0.041 * SL$
	tPHL	1.00	$0.95 + 0.027 * SL$	$0.97 + 0.021 * SL$	$0.98 + 0.020 * SL$
	tR	0.29	$0.10 + 0.094 * SL$	$0.09 + 0.097 * SL$	$0.08 + 0.097 * SL$
	tF	0.17	$0.10 + 0.035 * SL$	$0.09 + 0.038 * SL$	$0.06 + 0.039 * SL$
E to Q0	tPLH	1.15	$1.07 + 0.041 * SL$	$1.06 + 0.041 * SL$	$1.06 + 0.041 * SL$
	tPHL	0.95	$0.89 + 0.027 * SL$	$0.91 + 0.021 * SL$	$0.93 + 0.020 * SL$
	tR	0.29	$0.10 + 0.093 * SL$	$0.09 + 0.097 * SL$	$0.08 + 0.097 * SL$
	tF	0.17	$0.10 + 0.036 * SL$	$0.09 + 0.038 * SL$	$0.06 + 0.039 * SL$
CK to Q1	tPLH	1.20	$1.12 + 0.042 * SL$	$1.12 + 0.043 * SL$	$1.11 + 0.043 * SL$
	tPHL	1.01	$0.95 + 0.028 * SL$	$0.97 + 0.021 * SL$	$0.99 + 0.020 * SL$
	tR	0.30	$0.10 + 0.099 * SL$	$0.10 + 0.102 * SL$	$0.08 + 0.102 * SL$
	tF	0.18	$0.10 + 0.038 * SL$	$0.09 + 0.040 * SL$	$0.07 + 0.041 * SL$
E to Q1	tPLH	1.15	$1.06 + 0.042 * SL$	$1.06 + 0.042 * SL$	$1.06 + 0.043 * SL$
	tPHL	0.95	$0.90 + 0.028 * SL$	$0.92 + 0.021 * SL$	$0.94 + 0.020 * SL$
	tR	0.30	$0.10 + 0.099 * SL$	$0.10 + 0.102 * SL$	$0.08 + 0.102 * SL$
	tF	0.18	$0.10 + 0.038 * SL$	$0.10 + 0.040 * SL$	$0.07 + 0.041 * SL$
CK to Q2	tPLH	1.20	$1.12 + 0.042 * SL$	$1.12 + 0.043 * SL$	$1.11 + 0.043 * SL$
	tPHL	1.01	$0.95 + 0.028 * SL$	$0.97 + 0.021 * SL$	$0.99 + 0.020 * SL$
	tR	0.30	$0.10 + 0.099 * SL$	$0.10 + 0.102 * SL$	$0.08 + 0.102 * SL$
	tF	0.18	$0.10 + 0.038 * SL$	$0.09 + 0.040 * SL$	$0.07 + 0.041 * SL$
E to Q2	tPLH	1.15	$1.06 + 0.042 * SL$	$1.06 + 0.042 * SL$	$1.06 + 0.043 * SL$
	tPHL	0.95	$0.90 + 0.028 * SL$	$0.92 + 0.021 * SL$	$0.94 + 0.020 * SL$
	tR	0.30	$0.10 + 0.099 * SL$	$0.10 + 0.102 * SL$	$0.08 + 0.102 * SL$
	tF	0.18	$0.10 + 0.038 * SL$	$0.10 + 0.040 * SL$	$0.07 + 0.041 * SL$
CK to Q3	tPLH	1.20	$1.12 + 0.040 * SL$	$1.12 + 0.041 * SL$	$1.11 + 0.041 * SL$
	tPHL	1.00	$0.95 + 0.027 * SL$	$0.97 + 0.021 * SL$	$0.98 + 0.020 * SL$
	tR	0.29	$0.10 + 0.094 * SL$	$0.09 + 0.097 * SL$	$0.08 + 0.097 * SL$
	tF	0.17	$0.10 + 0.035 * SL$	$0.09 + 0.038 * SL$	$0.06 + 0.039 * SL$
E to Q3	tPLH	1.15	$1.07 + 0.040 * SL$	$1.06 + 0.041 * SL$	$1.06 + 0.041 * SL$
	tPHL	0.95	$0.89 + 0.027 * SL$	$0.91 + 0.021 * SL$	$0.93 + 0.020 * SL$
	tR	0.29	$0.10 + 0.093 * SL$	$0.09 + 0.097 * SL$	$0.08 + 0.097 * SL$
	tF	0.17	$0.10 + 0.036 * SL$	$0.09 + 0.038 * SL$	$0.06 + 0.039 * SL$
CK to QN0	tPLH	0.94	$0.85 + 0.044 * SL$	$0.85 + 0.043 * SL$	$0.85 + 0.043 * SL$
	tPHL	1.06	$1.00 + 0.028 * SL$	$1.02 + 0.022 * SL$	$1.05 + 0.020 * SL$
	tR	0.31	$0.11 + 0.099 * SL$	$0.10 + 0.101 * SL$	$0.09 + 0.102 * SL$
	tF	0.18	$0.11 + 0.038 * SL$	$0.10 + 0.039 * SL$	$0.08 + 0.041 * SL$
E to QN0	tPLH	0.88	$0.80 + 0.043 * SL$	$0.80 + 0.043 * SL$	$0.80 + 0.043 * SL$
	tPHL	1.01	$0.95 + 0.028 * SL$	$0.97 + 0.022 * SL$	$0.99 + 0.020 * SL$
	tR	0.31	$0.11 + 0.099 * SL$	$0.10 + 0.101 * SL$	$0.09 + 0.102 * SL$
	tF	0.18	$0.11 + 0.039 * SL$	$0.10 + 0.039 * SL$	$0.08 + 0.041 * SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$



# FG1X4

## 4-Bit D Flip-Flop with CK Enable

### FG1X4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

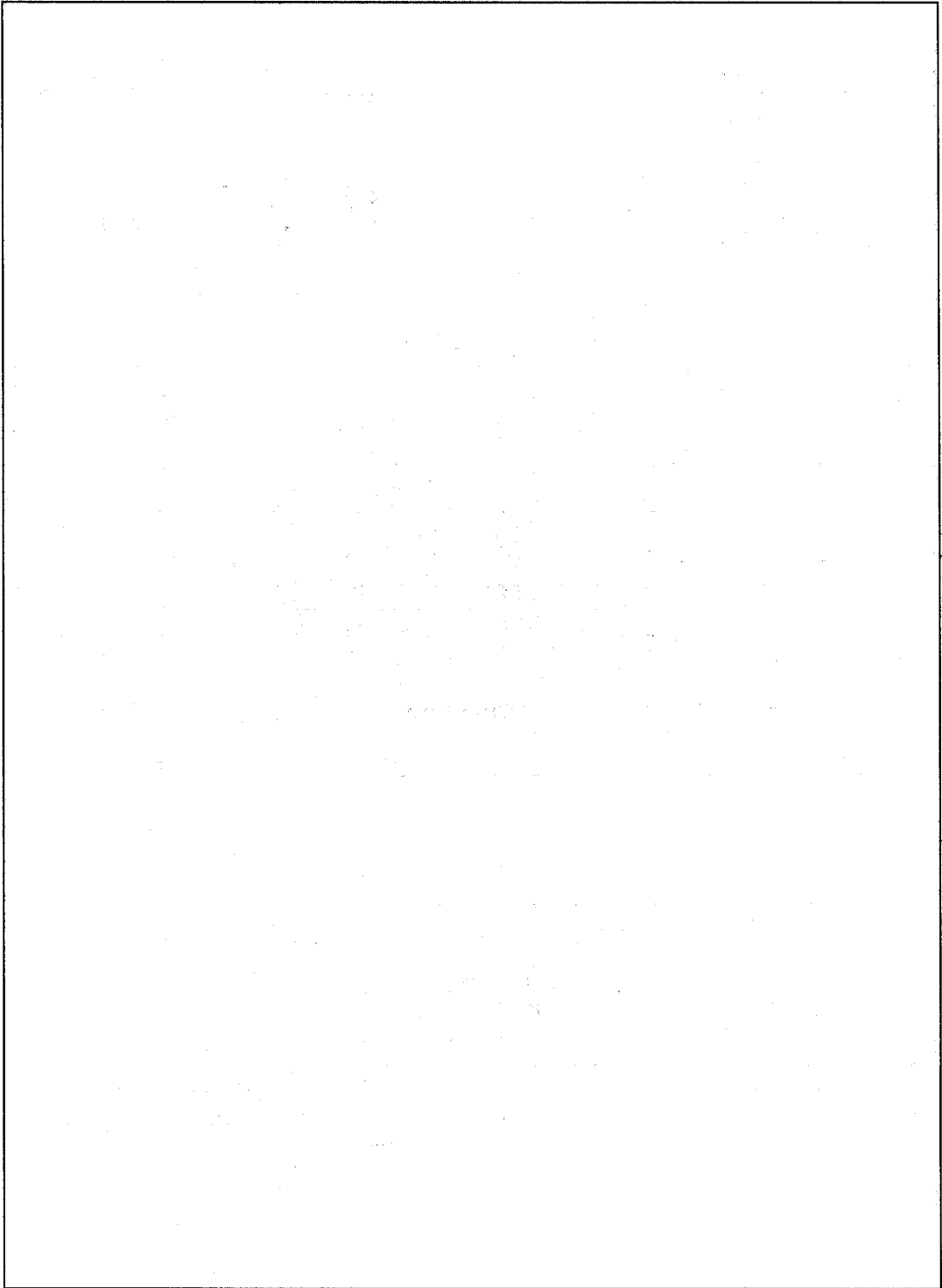
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to QN1	tPLH	0.94	$0.85 + 0.044*SL$	$0.85 + 0.043*SL$	$0.85 + 0.043*SL$
	tPHL	1.06	$1.00 + 0.028*SL$	$1.02 + 0.022*SL$	$1.05 + 0.020*SL$
	tR	0.31	$0.11 + 0.098*SL$	$0.10 + 0.102*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.040*SL$	$0.10 + 0.039*SL$	$0.08 + 0.041*SL$
E to QN1	tPLH	0.88	$0.80 + 0.044*SL$	$0.80 + 0.043*SL$	$0.80 + 0.043*SL$
	tPHL	1.00	$0.95 + 0.029*SL$	$0.97 + 0.022*SL$	$0.99 + 0.020*SL$
	tR	0.31	$0.11 + 0.098*SL$	$0.10 + 0.102*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.040*SL$	$0.10 + 0.040*SL$	$0.08 + 0.041*SL$
CK to QN2	tPLH	0.94	$0.85 + 0.044*SL$	$0.85 + 0.043*SL$	$0.85 + 0.043*SL$
	tPHL	1.06	$1.00 + 0.028*SL$	$1.02 + 0.022*SL$	$1.05 + 0.020*SL$
	tR	0.31	$0.11 + 0.098*SL$	$0.10 + 0.102*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.040*SL$	$0.10 + 0.039*SL$	$0.08 + 0.041*SL$
E to QN2	tPLH	0.88	$0.80 + 0.044*SL$	$0.80 + 0.043*SL$	$0.80 + 0.043*SL$
	tPHL	1.00	$0.95 + 0.029*SL$	$0.97 + 0.022*SL$	$0.99 + 0.020*SL$
	tR	0.31	$0.11 + 0.098*SL$	$0.10 + 0.102*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.040*SL$	$0.10 + 0.040*SL$	$0.08 + 0.041*SL$
CK to QN3	tPLH	0.94	$0.85 + 0.044*SL$	$0.85 + 0.043*SL$	$0.85 + 0.043*SL$
	tPHL	1.06	$1.00 + 0.028*SL$	$1.02 + 0.022*SL$	$1.05 + 0.020*SL$
	tR	0.31	$0.11 + 0.099*SL$	$0.10 + 0.101*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.11 + 0.038*SL$	$0.10 + 0.039*SL$	$0.08 + 0.041*SL$
E to QN3	tPLH	0.88	$0.80 + 0.043*SL$	$0.80 + 0.043*SL$	$0.80 + 0.043*SL$
	tPHL	1.01	$0.95 + 0.028*SL$	$0.97 + 0.022*SL$	$0.99 + 0.020*SL$
	tR	0.31	$0.11 + 0.099*SL$	$0.10 + 0.101*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.11 + 0.038*SL$	$0.10 + 0.039*SL$	$0.08 + 0.041*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### FG1X4 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.998
Pulse Width Low (E)	tPWL	1.077
Pulse Width High (CK)	tPWH	0.920
Pulse Width High (E)	tPWH	0.920
Input Hold Time (D0 to CK)	tHD	0.561
Input Hold Time (D0 to E)	tHD	0.506
Input Hold Time (D1 to CK)	tHD	0.561
Input Hold Time (D1 to E)	tHD	0.506



# FG2

## D Flip-Flop with Reset, CK Enable, Positive Edge Trigger, 1X Drive

Inputs: D, E, CK, RN

Outputs: Q, QN

Input Loading (SL):

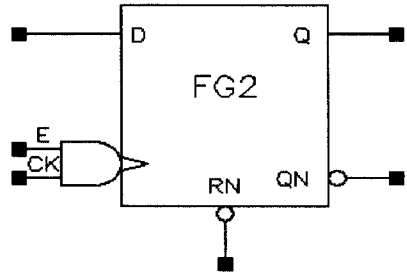
- D: 3

- E, CK: 1

- RN: 2

Maximum Fanout (Rec. SL): All : 28

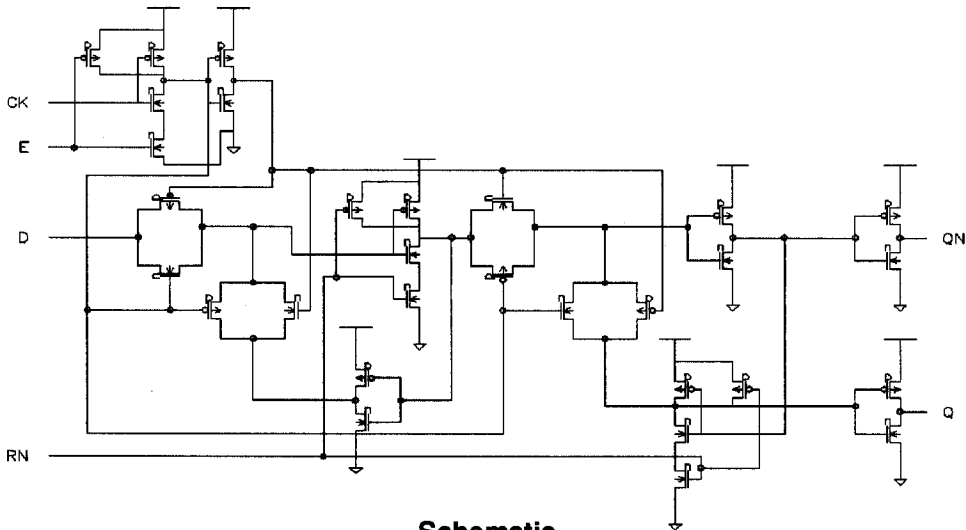
Gate Count: 8



**Symbol**

D	RN	E	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	1		0	1
1	1	1		1	0
x	1	0	x	Q <sub>n</sub>	Q <sub>Nn</sub>
x	0	x	x	0	1
x	1	x		Q <sub>n</sub>	Q <sub>Nn</sub>

**Truth Table**



**Schematic**

**FG2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q	tPHL	0.45	$0.39 + 0.030*SL$	$0.42 + 0.021*SL$	$0.45 + 0.020*SL$
	tF	0.21	$0.15 + 0.033*SL$	$0.14 + 0.035*SL$	$0.09 + 0.038*SL$
CK to Q	tPLH	0.93	$0.86 + 0.039*SL$	$0.85 + 0.040*SL$	$0.85 + 0.040*SL$
	tPHL	0.78	$0.73 + 0.027*SL$	$0.74 + 0.021*SL$	$0.77 + 0.020*SL$
	tR	0.30	$0.12 + 0.088*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.18	$0.11 + 0.034*SL$	$0.10 + 0.036*SL$	$0.07 + 0.038*SL$
E to Q	tPLH	0.90	$0.82 + 0.039*SL$	$0.82 + 0.040*SL$	$0.81 + 0.040*SL$
	tPHL	0.74	$0.68 + 0.027*SL$	$0.70 + 0.021*SL$	$0.73 + 0.020*SL$
	tR	0.30	$0.12 + 0.088*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
RN to QN	tF	0.18	$0.11 + 0.034*SL$	$0.10 + 0.036*SL$	$0.07 + 0.038*SL$
	tPLH	0.77	$0.69 + 0.040*SL$	$0.69 + 0.040*SL$	$0.69 + 0.040*SL$
	tR	0.29	$0.11 + 0.088*SL$	$0.10 + 0.092*SL$	$0.08 + 0.092*SL$
CK to QN	tPLH	0.69	$0.60 + 0.041*SL$	$0.61 + 0.040*SL$	$0.61 + 0.040*SL$
	tPHL	0.72	$0.66 + 0.028*SL$	$0.68 + 0.021*SL$	$0.71 + 0.020*SL$
	tR	0.28	$0.11 + 0.088*SL$	$0.10 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.18	$0.11 + 0.034*SL$	$0.11 + 0.036*SL$	$0.08 + 0.038*SL$
E to QN	tPLH	0.65	$0.56 + 0.041*SL$	$0.57 + 0.040*SL$	$0.57 + 0.040*SL$
	tPHL	0.68	$0.63 + 0.028*SL$	$0.64 + 0.021*SL$	$0.68 + 0.020*SL$
	tR	0.28	$0.11 + 0.088*SL$	$0.10 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.18	$0.11 + 0.035*SL$	$0.11 + 0.036*SL$	$0.08 + 0.038*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FG2 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (E)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Pulse Width High (E)	tPWH	0.920
Input Hold Time (D to CK)	tHD	0.287
Input Hold Time (D to E)	tHD	0.233
Input Setup Time (D to CK)	tSU	0.233
Input Setup Time (D to E)	tSU	0.287
Recovery Time (RN)	tRC	0.139
Recovery Time (RN)	tRC	0.139

# FG2X4

4-Bit D Flip-Flop with Reset, CK Enable, Positive Edge Trigger, 1X Drive

Inputs: D0, D1, D2, D3, E, CK, RN

Outputs: Q0, Q1, Q2, Q3,  
QN0, QN1, QN2, QN3

Input Loading (SL):

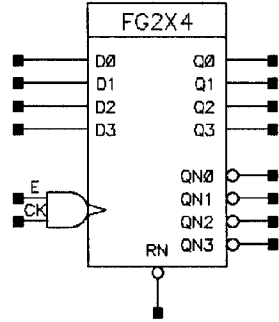
- D0, D1, D2, D3: 3

- E, CK: 1

- RN: 8

Maximum Fanout (Rec. SL): All : 28

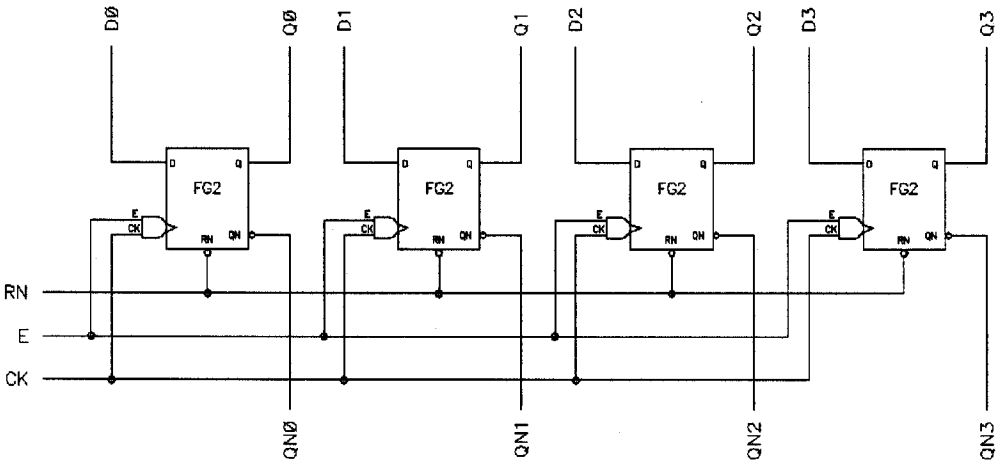
Gate Count: 26



Symbol

D	RN	E	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	1		0	1
1	1	1		1	0
x	1	0	x	Q <sub>n</sub>	Q <sub>Nn</sub>
x	0	x	x	0	1
x	1	x		Q <sub>n</sub>	Q <sub>Nn</sub>

Truth Table



Schematic

**FG2X4 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to Q0	tPHL	0.45	$0.39 + 0.030*SL$	$0.42 + 0.021*SL$	$0.45 + 0.020*SL$
	tF	0.22	$0.15 + 0.033*SL$	$0.14 + 0.035*SL$	$0.09 + 0.038*SL$
CK to Q0	tPLH	1.36	$1.28 + 0.039*SL$	$1.28 + 0.040*SL$	$1.27 + 0.040*SL$
	tPHL	1.03	$0.97 + 0.027*SL$	$0.99 + 0.021*SL$	$1.01 + 0.020*SL$
	tR	0.30	$0.12 + 0.088*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.17	$0.10 + 0.036*SL$	$0.10 + 0.037*SL$	$0.07 + 0.038*SL$
	tR	0.30	$0.12 + 0.088*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
E to Q0	tPLH	1.30	$1.22 + 0.039*SL$	$1.22 + 0.040*SL$	$1.22 + 0.040*SL$
	tPHL	0.97	$0.92 + 0.027*SL$	$0.93 + 0.021*SL$	$0.96 + 0.020*SL$
	tR	0.30	$0.12 + 0.088*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
RN to Q1	tPHL	0.45	$0.39 + 0.031*SL$	$0.42 + 0.022*SL$	$0.45 + 0.020*SL$
	tF	0.22	$0.16 + 0.035*SL$	$0.15 + 0.038*SL$	$0.09 + 0.041*SL$
	tR	0.32	$0.13 + 0.099*SL$	$0.12 + 0.101*SL$	$0.09 + 0.102*SL$
CK to Q1	tPLH	1.36	$1.28 + 0.041*SL$	$1.28 + 0.042*SL$	$1.27 + 0.043*SL$
	tPHL	1.03	$0.97 + 0.028*SL$	$0.99 + 0.022*SL$	$1.01 + 0.020*SL$
	tR	0.32	$0.13 + 0.099*SL$	$0.12 + 0.101*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.039*SL$	$0.10 + 0.040*SL$	$0.07 + 0.041*SL$
E to Q1	tPLH	1.31	$1.23 + 0.041*SL$	$1.22 + 0.042*SL$	$1.21 + 0.043*SL$
	tPHL	0.97	$0.91 + 0.027*SL$	$0.93 + 0.022*SL$	$0.95 + 0.021*SL$
	tR	0.32	$0.13 + 0.099*SL$	$0.12 + 0.101*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.039*SL$	$0.10 + 0.040*SL$	$0.07 + 0.041*SL$
RN to Q2	tPHL	0.45	$0.39 + 0.031*SL$	$0.42 + 0.022*SL$	$0.45 + 0.020*SL$
	tF	0.22	$0.16 + 0.035*SL$	$0.15 + 0.038*SL$	$0.09 + 0.041*SL$
CK to Q2	tPLH	1.36	$1.28 + 0.041*SL$	$1.28 + 0.042*SL$	$1.27 + 0.043*SL$
	tPHL	1.03	$0.97 + 0.028*SL$	$0.99 + 0.022*SL$	$1.01 + 0.020*SL$
	tR	0.32	$0.13 + 0.098*SL$	$0.12 + 0.101*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.039*SL$	$0.10 + 0.040*SL$	$0.07 + 0.041*SL$
E to Q2	tPLH	1.31	$1.23 + 0.041*SL$	$1.22 + 0.042*SL$	$1.22 + 0.043*SL$
	tPHL	0.97	$0.91 + 0.027*SL$	$0.93 + 0.022*SL$	$0.95 + 0.020*SL$
	tR	0.32	$0.13 + 0.099*SL$	$0.12 + 0.101*SL$	$0.09 + 0.102*SL$
	tF	0.18	$0.10 + 0.039*SL$	$0.10 + 0.040*SL$	$0.07 + 0.041*SL$
RN to Q3	tPHL	0.45	$0.39 + 0.030*SL$	$0.42 + 0.021*SL$	$0.45 + 0.020*SL$
	tF	0.22	$0.15 + 0.033*SL$	$0.14 + 0.035*SL$	$0.09 + 0.038*SL$
CK to Q3	tPLH	1.36	$1.28 + 0.039*SL$	$1.28 + 0.040*SL$	$1.27 + 0.040*SL$
	tPHL	1.03	$0.97 + 0.027*SL$	$0.99 + 0.021*SL$	$1.01 + 0.020*SL$
	tR	0.30	$0.12 + 0.088*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.17	$0.10 + 0.036*SL$	$0.10 + 0.037*SL$	$0.07 + 0.038*SL$
E to Q3	tPLH	1.30	$1.22 + 0.039*SL$	$1.22 + 0.040*SL$	$1.22 + 0.040*SL$
	tPHL	0.97	$0.92 + 0.027*SL$	$0.93 + 0.021*SL$	$0.96 + 0.020*SL$
	tR	0.30	$0.12 + 0.088*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.17	$0.10 + 0.036*SL$	$0.10 + 0.037*SL$	$0.07 + 0.038*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

# FG2X4

4-Bit D Flip-Flop with Reset, CK Enable, Positive Edge Trigger, 1X Drive

## FG2X4 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
RN to QN0	tPLH	0.77	$0.69 + 0.040 \cdot \text{SL}$	$0.69 + 0.040 \cdot \text{SL}$	$0.68 + 0.040 \cdot \text{SL}$
	tR	0.29	$0.11 + 0.088 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
CK to QN0	tPLH	0.93	$0.85 + 0.040 \cdot \text{SL}$	$0.85 + 0.040 \cdot \text{SL}$	$0.85 + 0.040 \cdot \text{SL}$
	tPHL	1.14	$1.09 + 0.028 \cdot \text{SL}$	$1.10 + 0.021 \cdot \text{SL}$	$1.14 + 0.020 \cdot \text{SL}$
	tR	0.28	$0.11 + 0.088 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
	tF	0.18	$0.11 + 0.036 \cdot \text{SL}$	$0.11 + 0.036 \cdot \text{SL}$	$0.08 + 0.038 \cdot \text{SL}$
E to QN0	tPLH	0.88	$0.80 + 0.040 \cdot \text{SL}$	$0.80 + 0.040 \cdot \text{SL}$	$0.80 + 0.040 \cdot \text{SL}$
	tPHL	1.09	$1.03 + 0.027 \cdot \text{SL}$	$1.05 + 0.021 \cdot \text{SL}$	$1.08 + 0.020 \cdot \text{SL}$
	tR	0.28	$0.11 + 0.088 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
	tF	0.18	$0.11 + 0.036 \cdot \text{SL}$	$0.11 + 0.036 \cdot \text{SL}$	$0.08 + 0.038 \cdot \text{SL}$
RN to QN1	tPLH	0.78	$0.69 + 0.043 \cdot \text{SL}$	$0.69 + 0.042 \cdot \text{SL}$	$0.68 + 0.042 \cdot \text{SL}$
	tR	0.31	$0.12 + 0.098 \cdot \text{SL}$	$0.10 + 0.101 \cdot \text{SL}$	$0.09 + 0.102 \cdot \text{SL}$
CK to QN1	tPLH	0.94	$0.85 + 0.044 \cdot \text{SL}$	$0.86 + 0.043 \cdot \text{SL}$	$0.86 + 0.043 \cdot \text{SL}$
	tPHL	1.14	$1.08 + 0.028 \cdot \text{SL}$	$1.10 + 0.022 \cdot \text{SL}$	$1.13 + 0.020 \cdot \text{SL}$
	tR	0.31	$0.11 + 0.099 \cdot \text{SL}$	$0.10 + 0.102 \cdot \text{SL}$	$0.09 + 0.102 \cdot \text{SL}$
	tF	0.19	$0.11 + 0.037 \cdot \text{SL}$	$0.11 + 0.038 \cdot \text{SL}$	$0.08 + 0.039 \cdot \text{SL}$
E to QN1	tPLH	0.88	$0.80 + 0.043 \cdot \text{SL}$	$0.80 + 0.043 \cdot \text{SL}$	$0.80 + 0.043 \cdot \text{SL}$
	tPHL	1.08	$1.03 + 0.028 \cdot \text{SL}$	$1.05 + 0.022 \cdot \text{SL}$	$1.08 + 0.020 \cdot \text{SL}$
	tR	0.31	$0.11 + 0.099 \cdot \text{SL}$	$0.10 + 0.102 \cdot \text{SL}$	$0.09 + 0.102 \cdot \text{SL}$
	tF	0.19	$0.11 + 0.037 \cdot \text{SL}$	$0.11 + 0.038 \cdot \text{SL}$	$0.08 + 0.039 \cdot \text{SL}$
RN to QN2	tPLH	0.78	$0.69 + 0.043 \cdot \text{SL}$	$0.69 + 0.042 \cdot \text{SL}$	$0.68 + 0.042 \cdot \text{SL}$
	tR	0.31	$0.12 + 0.098 \cdot \text{SL}$	$0.10 + 0.101 \cdot \text{SL}$	$0.09 + 0.102 \cdot \text{SL}$
CK to QN2	tPLH	0.94	$0.85 + 0.044 \cdot \text{SL}$	$0.86 + 0.043 \cdot \text{SL}$	$0.86 + 0.043 \cdot \text{SL}$
	tPHL	1.14	$1.08 + 0.028 \cdot \text{SL}$	$1.10 + 0.022 \cdot \text{SL}$	$1.13 + 0.020 \cdot \text{SL}$
	tR	0.31	$0.11 + 0.099 \cdot \text{SL}$	$0.10 + 0.102 \cdot \text{SL}$	$0.09 + 0.102 \cdot \text{SL}$
	tF	0.19	$0.11 + 0.037 \cdot \text{SL}$	$0.11 + 0.038 \cdot \text{SL}$	$0.08 + 0.039 \cdot \text{SL}$
E to QN2	tPLH	0.88	$0.80 + 0.043 \cdot \text{SL}$	$0.80 + 0.043 \cdot \text{SL}$	$0.80 + 0.043 \cdot \text{SL}$
	tPHL	1.08	$1.03 + 0.028 \cdot \text{SL}$	$1.05 + 0.022 \cdot \text{SL}$	$1.08 + 0.020 \cdot \text{SL}$
	tR	0.31	$0.11 + 0.099 \cdot \text{SL}$	$0.10 + 0.102 \cdot \text{SL}$	$0.09 + 0.102 \cdot \text{SL}$
	tF	0.19	$0.11 + 0.037 \cdot \text{SL}$	$0.11 + 0.038 \cdot \text{SL}$	$0.08 + 0.039 \cdot \text{SL}$
RN to QN3	tPLH	0.77	$0.69 + 0.040 \cdot \text{SL}$	$0.69 + 0.040 \cdot \text{SL}$	$0.68 + 0.040 \cdot \text{SL}$
	tR	0.29	$0.11 + 0.088 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
CK to QN3	tPLH	0.93	$0.85 + 0.040 \cdot \text{SL}$	$0.85 + 0.040 \cdot \text{SL}$	$0.85 + 0.040 \cdot \text{SL}$
	tPHL	1.14	$1.09 + 0.028 \cdot \text{SL}$	$1.11 + 0.021 \cdot \text{SL}$	$1.14 + 0.020 \cdot \text{SL}$
	tR	0.28	$0.11 + 0.088 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
	tF	0.18	$0.11 + 0.036 \cdot \text{SL}$	$0.11 + 0.036 \cdot \text{SL}$	$0.08 + 0.038 \cdot \text{SL}$
E to QN3	tPLH	0.88	$0.80 + 0.040 \cdot \text{SL}$	$0.80 + 0.040 \cdot \text{SL}$	$0.80 + 0.040 \cdot \text{SL}$
	tPHL	1.09	$1.03 + 0.027 \cdot \text{SL}$	$1.05 + 0.021 \cdot \text{SL}$	$1.08 + 0.020 \cdot \text{SL}$
	tR	0.28	$0.11 + 0.088 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
	tF	0.18	$0.11 + 0.036 \cdot \text{SL}$	$0.11 + 0.036 \cdot \text{SL}$	$0.08 + 0.038 \cdot \text{SL}$

\*Range1:  $\text{SL} < 3.00$ , \*Range2:  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3:  $20.00 < \text{SL}$

**FG2X4 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

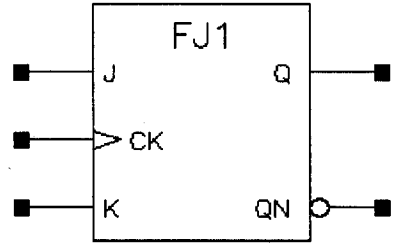
Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.998
Pulse Width Low (E)	tPWL	1.077
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Pulse Width High (E)	tPWH	0.920
Input Hold Time (D0 to CK)	tHD	0.561
Input Hold Time (D0 to E)	tHD	0.506
Input Hold Time (D1 to CK)	tHD	0.561
Input Hold Time (D1 to E)	tHD	0.506
Input Hold Time (D2 to CK)	tHD	0.561
Input Hold Time (D2 to E)	tHD	0.506
Input Hold Time (D3 to CK)	tHD	0.561
Input Hold Time (D3 to E)	tHD	0.506
Input Setup Time (D0 to CK)	tSU	0.069
Input Setup Time (D0 to E)	tSU	0.123
Input Setup Time (D1 to CK)	tSU	0.069
Input Setup Time (D1 to E)	tSU	0.123
Input Setup Time (D2 to CK)	tSU	0.069
Input Setup Time (D2 to E)	tSU	0.123
Input Setup Time (D3 to CK)	tSU	0.069
Input Setup Time (D3 to E)	tSU	0.123
Recovery Time (RN)	tRC	0.139
Recovery Time (RN)	tRC	0.139



# FJ1/FJ1D2

JK Flip-Flop with Positive Edge Trigger, 1X Drive or 2X Drive

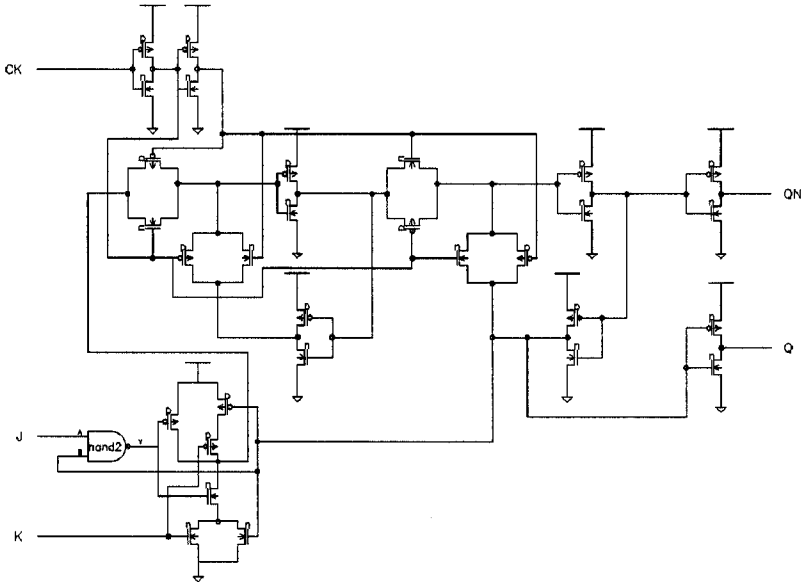
Inputs: J, K, CK  
 Outputs: Q, QN  
 Input Loading (SL): All : 1  
 Maximum Fanout (Rec. SL): All :  
     FJ1: 28  
     FJ1D2: 56  
 Gate Count:  
     FJ1: 9  
     FJ1D2: 10



**Symbol**

J	K	CK	Qn+1	QNn+1
0	1		0	1
1	0		1	0
0	0		Qn	QNn
1	1		QNn	Qn
x	x		Qn	QNn

**Truth Table**



**Schematic**

**FJ1 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.77	$0.69 + 0.039 \cdot \text{SL}$	$0.69 + 0.040 \cdot \text{SL}$	$0.68 + 0.040 \cdot \text{SL}$
	tPHL	0.72	$0.66 + 0.030 \cdot \text{SL}$	$0.69 + 0.022 \cdot \text{SL}$	$0.73 + 0.020 \cdot \text{SL}$
	tR	0.29	$0.11 + 0.088 \cdot \text{SL}$	$0.11 + 0.091 \cdot \text{SL}$	$0.08 + 0.092 \cdot \text{SL}$
	tF	0.21	$0.13 + 0.039 \cdot \text{SL}$	$0.14 + 0.036 \cdot \text{SL}$	$0.11 + 0.037 \cdot \text{SL}$
CK to QN	tPLH	0.56	$0.48 + 0.040 \cdot \text{SL}$	$0.48 + 0.040 \cdot \text{SL}$	$0.48 + 0.040 \cdot \text{SL}$
	tPHL	0.56	$0.50 + 0.027 \cdot \text{SL}$	$0.52 + 0.021 \cdot \text{SL}$	$0.55 + 0.020 \cdot \text{SL}$
	tR	0.28	$0.10 + 0.089 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$	$0.08 + 0.093 \cdot \text{SL}$
	tF	0.17	$0.10 + 0.035 \cdot \text{SL}$	$0.10 + 0.037 \cdot \text{SL}$	$0.07 + 0.038 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **FJ1 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.506
Input Setup Time (K to CK)	tSU	0.452

# FJ1D2

## JK Flip-Flop with Positive Edge Trigger, 2X Drive

### FJ1D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

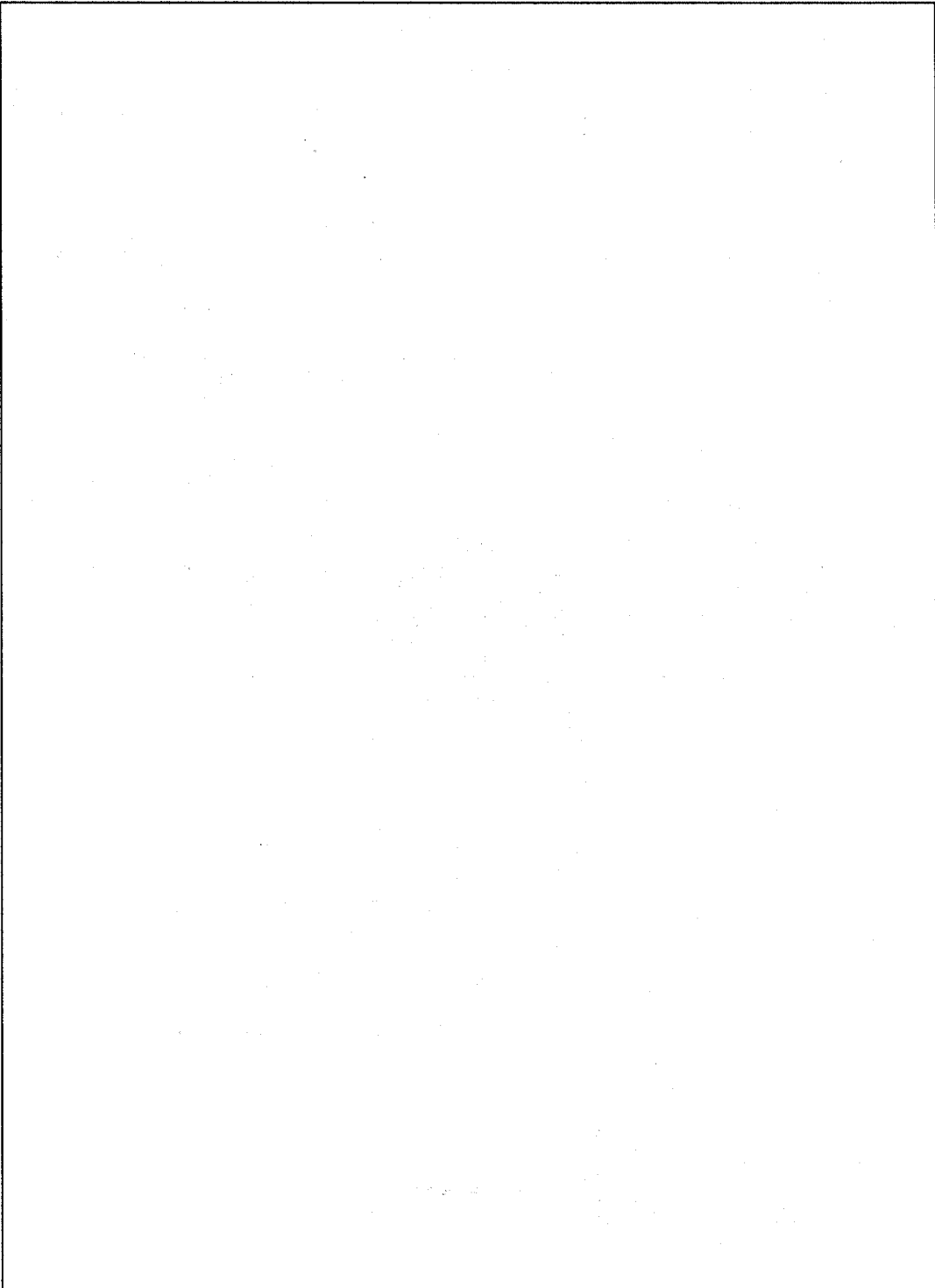
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.81	$0.77 + 0.020 \cdot \text{SL}$	$0.77 + 0.020 \cdot \text{SL}$	$0.76 + 0.020 \cdot \text{SL}$
	tPHL	0.76	$0.73 + 0.019 \cdot \text{SL}$	$0.74 + 0.013 \cdot \text{SL}$	$0.79 + 0.011 \cdot \text{SL}$
	tR	0.21	$0.12 + 0.044 \cdot \text{SL}$	$0.12 + 0.046 \cdot \text{SL}$	$0.09 + 0.047 \cdot \text{SL}$
	tF	0.20	$0.15 + 0.022 \cdot \text{SL}$	$0.16 + 0.018 \cdot \text{SL}$	$0.16 + 0.018 \cdot \text{SL}$
CK to QN	tPLH	0.56	$0.51 + 0.021 \cdot \text{SL}$	$0.52 + 0.020 \cdot \text{SL}$	$0.52 + 0.020 \cdot \text{SL}$
	tPHL	0.57	$0.53 + 0.017 \cdot \text{SL}$	$0.55 + 0.012 \cdot \text{SL}$	$0.58 + 0.010 \cdot \text{SL}$
	tR	0.20	$0.12 + 0.042 \cdot \text{SL}$	$0.11 + 0.046 \cdot \text{SL}$	$0.09 + 0.047 \cdot \text{SL}$
	tF	0.16	$0.13 + 0.016 \cdot \text{SL}$	$0.12 + 0.018 \cdot \text{SL}$	$0.11 + 0.019 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$

### FJ1D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.506
Input Setup Time (K to CK)	tSU	0.452



# FJ1S/FJ1SD2

JK Flip-Flop with Scan, Positive Edge Trigger, 1X Drive or 2X Drive

Inputs: J, K, CK, TI, TE

Outputs: Q, QN

Input Loading (SL):

- J, K, CK, TI: 1

- TE: 2

Maximum Fanout (Rec. SL): All :

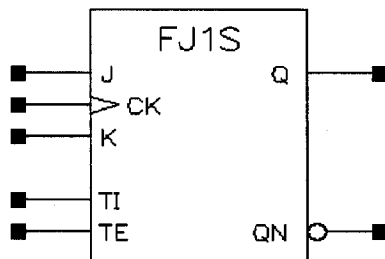
FJ1S: 28

FJ1SD2:56

Gate Count:

FJ1S: 11

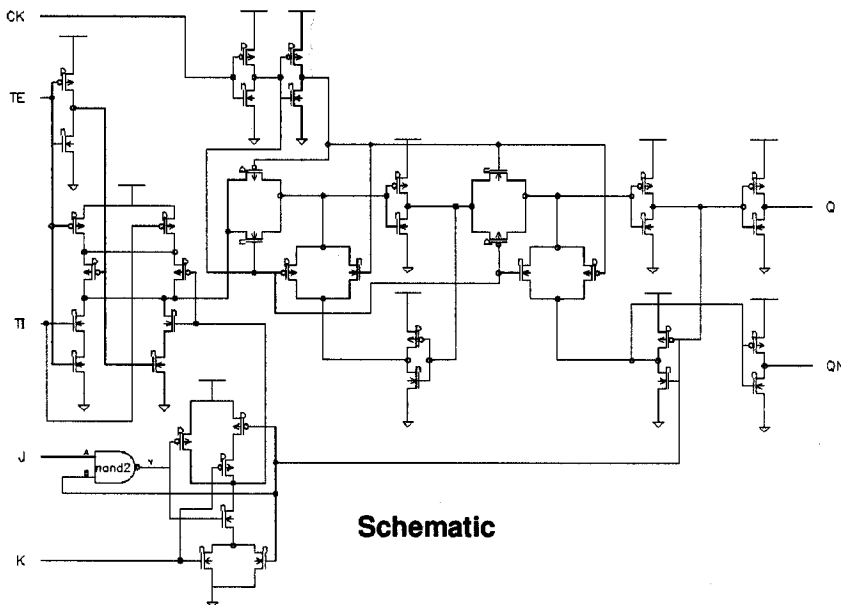
FJ1SD2:12



**Symbol**

J	K	TI	TE	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	x	0	⌄	0	1
1	0	x	0	⌄	1	0
0	0	x	0	⌄	Q <sub>n</sub>	Q <sub>Nn</sub>
1	1	x	0	⌄	Q <sub>Nn</sub>	Q <sub>n</sub>
x	x	x	x	⌄	Q <sub>n</sub>	Q <sub>Nn</sub>
x	x	0	1	⌄	0	1
x	x	1	1	⌄	1	0

**Truth Table**



**Schematic**

**FJ1S Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.64	$0.55 + 0.042*SL$	$0.56 + 0.040*SL$	$0.56 + 0.040*SL$
	tPHL	0.64	$0.57 + 0.033*SL$	$0.60 + 0.023*SL$	$0.66 + 0.020*SL$
	tR	0.30	$0.13 + 0.087*SL$	$0.11 + 0.092*SL$	$0.09 + 0.093*SL$
	tF	0.22	$0.14 + 0.040*SL$	$0.15 + 0.036*SL$	$0.13 + 0.037*SL$
CK to QN	tPLH	0.78	$0.70 + 0.039*SL$	$0.70 + 0.040*SL$	$0.70 + 0.040*SL$
	tPHL	0.71	$0.66 + 0.026*SL$	$0.68 + 0.021*SL$	$0.69 + 0.020*SL$
	tR	0.28	$0.11 + 0.088*SL$	$0.09 + 0.092*SL$	$0.08 + 0.092*SL$
	tF	0.17	$0.10 + 0.035*SL$	$0.09 + 0.037*SL$	$0.06 + 0.038*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FJ1S Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.725
Input Setup Time (K to CK)	tSU	0.670
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.889

# FJ1SD2

JK Flip-Flop with Scan, Positive Edge Trigger, 2X Drive

## FJ1SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

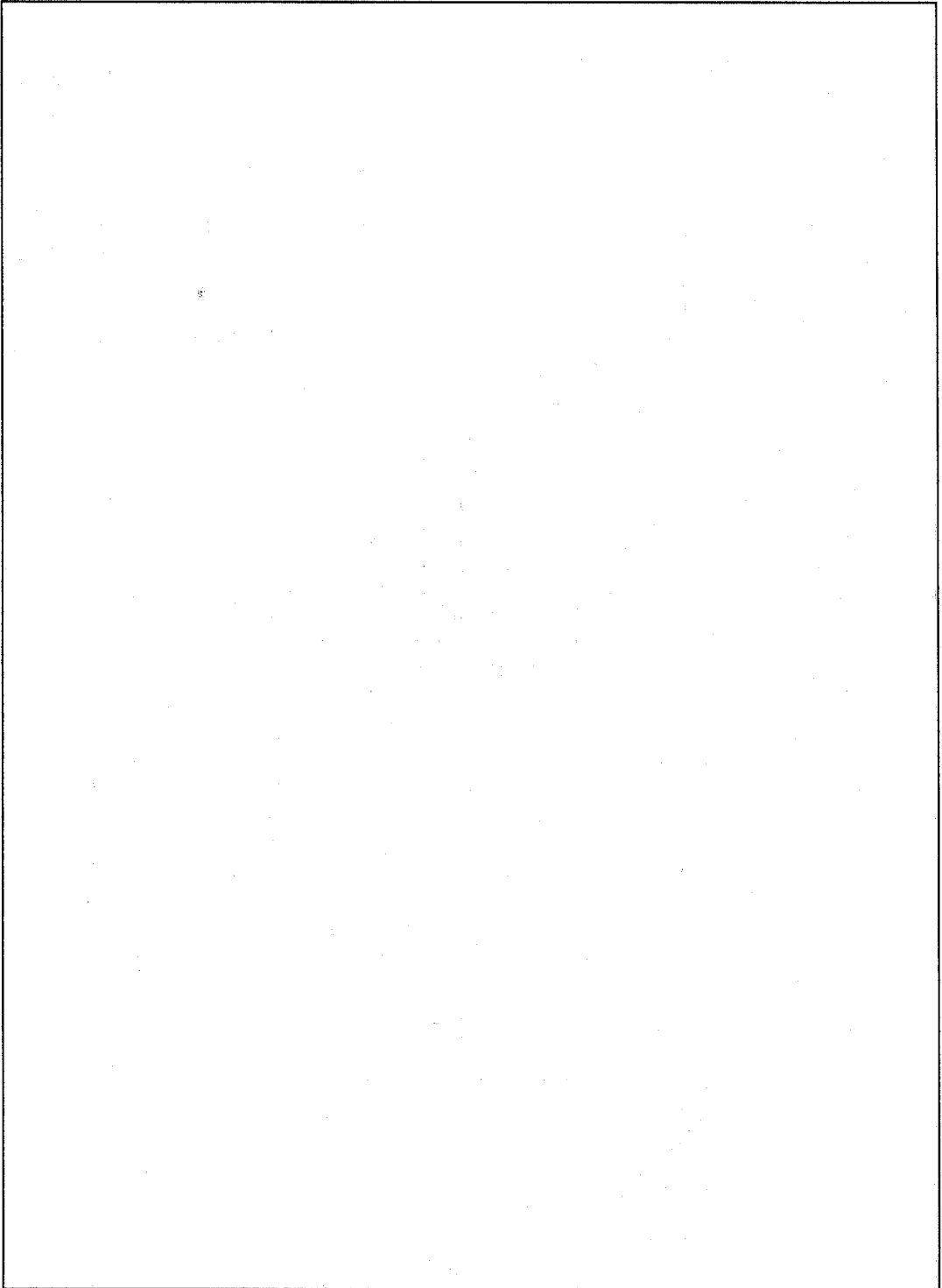
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.63	$0.59 + 0.022*SL$	$0.60 + 0.020*SL$	$0.60 + 0.020*SL$
	tPHL	0.64	$0.60 + 0.021*SL$	$0.62 + 0.014*SL$	$0.68 + 0.011*SL$
	tR	0.22	$0.14 + 0.042*SL$	$0.13 + 0.046*SL$	$0.10 + 0.047*SL$
	tF	0.20	$0.16 + 0.021*SL$	$0.17 + 0.018*SL$	$0.17 + 0.018*SL$
CK to QN	tPLH	0.83	$0.79 + 0.018*SL$	$0.79 + 0.019*SL$	$0.78 + 0.020*SL$
	tPHL	0.76	$0.73 + 0.016*SL$	$0.75 + 0.012*SL$	$0.78 + 0.010*SL$
	tR	0.20	$0.12 + 0.043*SL$	$0.11 + 0.046*SL$	$0.08 + 0.047*SL$
	tF	0.15	$0.12 + 0.019*SL$	$0.12 + 0.018*SL$	$0.10 + 0.019*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FJ1SD2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.725
Input Setup Time (K to CK)	tSU	0.670
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.889





# FJ2/FJ2D2

JK Flip-Flop with Reset, Positive Edge Trigger, 1X Drive or 2X Drive

Inputs: J, K, CK, RN

Outputs: Q, QN

Input Loading (SL):

- J, K, CK: 1

- RN: 2

Maximum Fanout (Rec. SL): All :

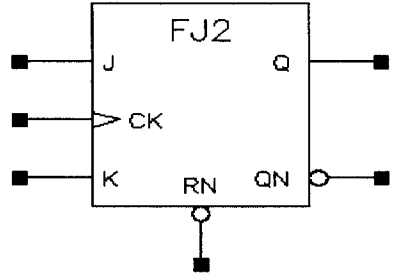
FJ2: 28

FJ2D2: 56

Gate Count:

FJ2: 10

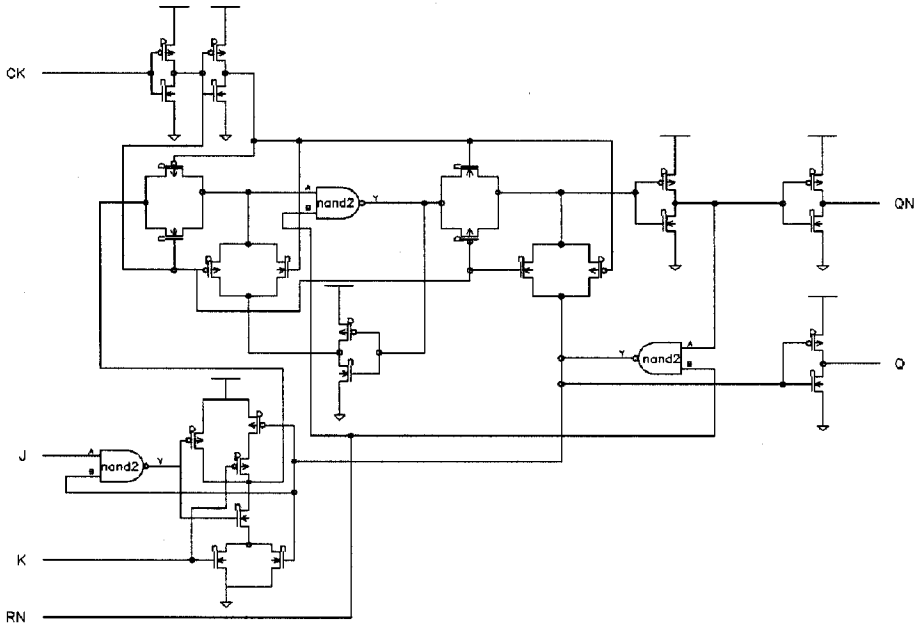
FJ2D2: 11



**Symbol**

J	K	RN	CK	Qn+1	QNn+1
0	1	1		0	1
1	0	1		1	0
0	0	1		Qn	QNn
1	1	1		QNn	Qn
x	x	1		Qn	QNn
x	x	0	x	0	1

**Truth Table**



**Schematic**

**FJ2 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{PR}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t <sub>PLH</sub>	0.93	$0.85 + 0.042 \cdot SL$	$0.85 + 0.040 \cdot SL$	$0.85 + 0.040 \cdot SL$
	t <sub>PHL</sub>	0.74	$0.68 + 0.031 \cdot SL$	$0.71 + 0.022 \cdot SL$	$0.76 + 0.020 \cdot SL$
	t <sub>R</sub>	0.32	$0.15 + 0.089 \cdot SL$	$0.14 + 0.090 \cdot SL$	$0.11 + 0.092 \cdot SL$
	t <sub>F</sub>	0.22	$0.14 + 0.038 \cdot SL$	$0.15 + 0.036 \cdot SL$	$0.12 + 0.037 \cdot SL$
RN to Q	t <sub>PHL</sub>	0.53	$0.46 + 0.034 \cdot SL$	$0.50 + 0.022 \cdot SL$	$0.54 + 0.020 \cdot SL$
	t <sub>F</sub>	0.25	$0.19 + 0.033 \cdot SL$	$0.19 + 0.034 \cdot SL$	$0.12 + 0.037 \cdot SL$
CK to QN	t <sub>PLH</sub>	0.57	$0.49 + 0.040 \cdot SL$	$0.49 + 0.040 \cdot SL$	$0.49 + 0.040 \cdot SL$
	t <sub>PHL</sub>	0.61	$0.55 + 0.028 \cdot SL$	$0.57 + 0.021 \cdot SL$	$0.60 + 0.020 \cdot SL$
	t <sub>R</sub>	0.28	$0.11 + 0.090 \cdot SL$	$0.10 + 0.092 \cdot SL$	$0.08 + 0.093 \cdot SL$
	t <sub>F</sub>	0.18	$0.11 + 0.035 \cdot SL$	$0.10 + 0.038 \cdot SL$	$0.08 + 0.039 \cdot SL$
RN to QN	t <sub>PLH</sub>	0.77	$0.69 + 0.041 \cdot SL$	$0.70 + 0.040 \cdot SL$	$0.69 + 0.040 \cdot SL$
	t <sub>R</sub>	0.29	$0.11 + 0.089 \cdot SL$	$0.10 + 0.092 \cdot SL$	$0.08 + 0.093 \cdot SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ **FJ2 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t <sub>PWL</sub>	0.920
Pulse Width Low (RN)	t <sub>PWL</sub>	0.920
Pulse Width High (CK)	t <sub>PWH</sub>	0.920
Input Hold Time (J to CK)	t <sub>HD</sub>	0.000
Input Hold Time (K to CK)	t <sub>HD</sub>	0.000
Input Setup Time (J to CK)	t <sub>SU</sub>	0.616
Input Setup Time (K to CK)	t <sub>SU</sub>	0.452
Recovery Time (RN)	t <sub>RC</sub>	0.139

# FJ2D2

JK Flip-Flop with Reset, Positive Edge Trigger, 2X Drive

## FJ2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

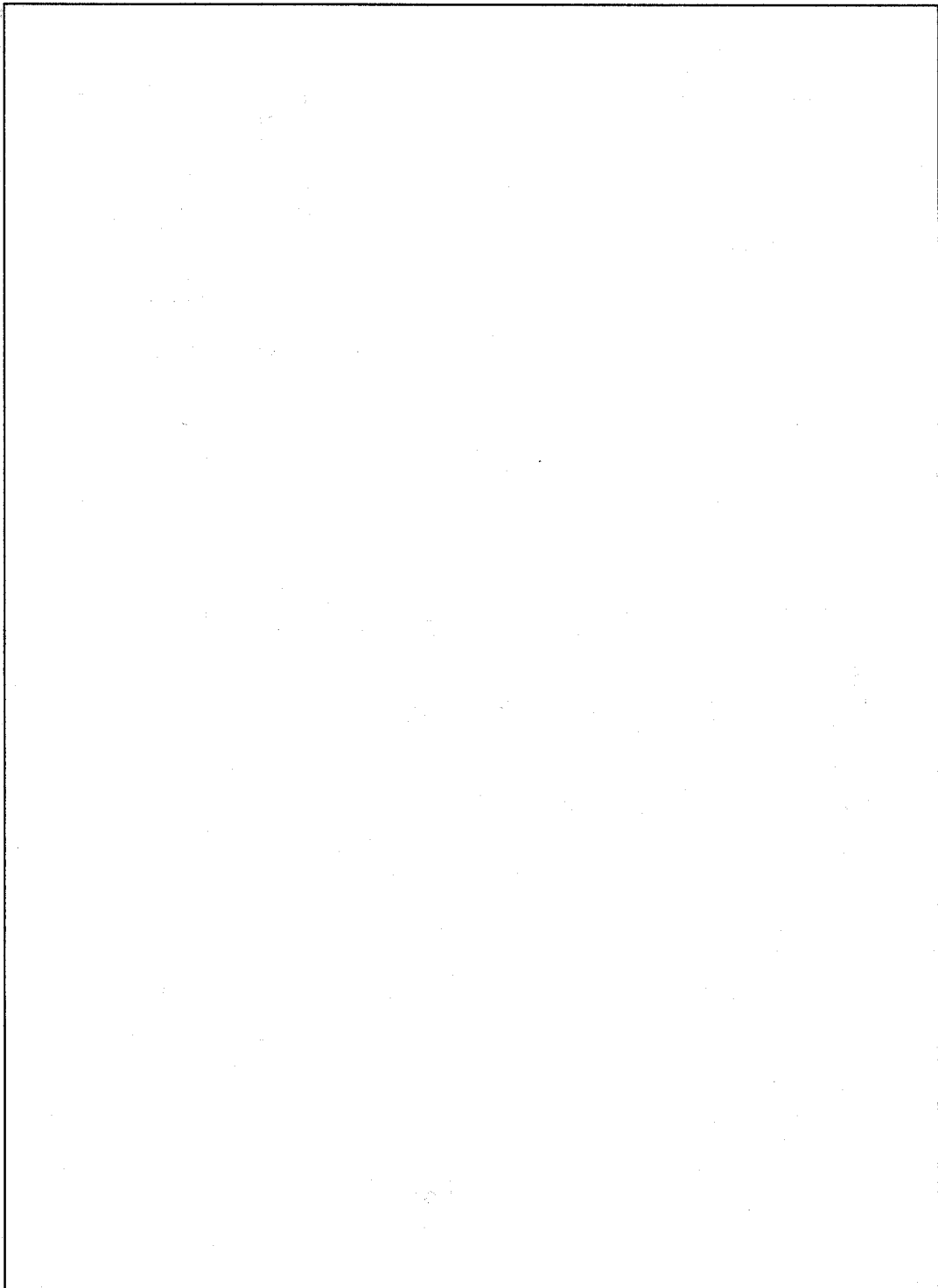
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.99	$0.94 + 0.023*SL$	$0.95 + 0.020*SL$	$0.95 + 0.020*SL$
	tPHL	0.78	$0.75 + 0.019*SL$	$0.76 + 0.013*SL$	$0.81 + 0.011*SL$
	tR	0.25	$0.16 + 0.045*SL$	$0.16 + 0.046*SL$	$0.14 + 0.047*SL$
	tF	0.20	$0.17 + 0.018*SL$	$0.17 + 0.018*SL$	$0.16 + 0.018*SL$
RN to Q	tPHL	0.53	$0.48 + 0.022*SL$	$0.51 + 0.013*SL$	$0.57 + 0.010*SL$
	tF	0.23	$0.20 + 0.019*SL$	$0.21 + 0.016*SL$	$0.18 + 0.017*SL$
CK to QN	tPLH	0.56	$0.52 + 0.021*SL$	$0.52 + 0.020*SL$	$0.52 + 0.020*SL$
	tPHL	0.62	$0.58 + 0.017*SL$	$0.60 + 0.012*SL$	$0.63 + 0.010*SL$
	tR	0.20	$0.12 + 0.043*SL$	$0.11 + 0.046*SL$	$0.09 + 0.047*SL$
	tF	0.17	$0.13 + 0.018*SL$	$0.13 + 0.018*SL$	$0.12 + 0.019*SL$
RN to QN	tPLH	0.77	$0.73 + 0.021*SL$	$0.73 + 0.020*SL$	$0.73 + 0.020*SL$
	tR	0.21	$0.12 + 0.044*SL$	$0.12 + 0.046*SL$	$0.09 + 0.047*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FJ2D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.616
Input Setup Time (K to CK)	tSU	0.452
Recovery Time (RN)	tRC	0.139



# FJ2S/FJ2SD2

JK Flip-Flop with Reset, Scan, Positive Edge Trigger, 1X Drive or 2X Drive

Inputs: J, K, CK, TI, TE, RN

Outputs: Q, QN

Input Loading (SL):

- J, K, CK, TI: 1

- TE, RN: 2

Maximum Fanout (Rec. SL): All :

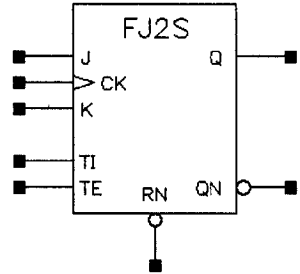
FJ2S: 28

FJ2SD2: 56

Gate Count:

FJ2S: 12

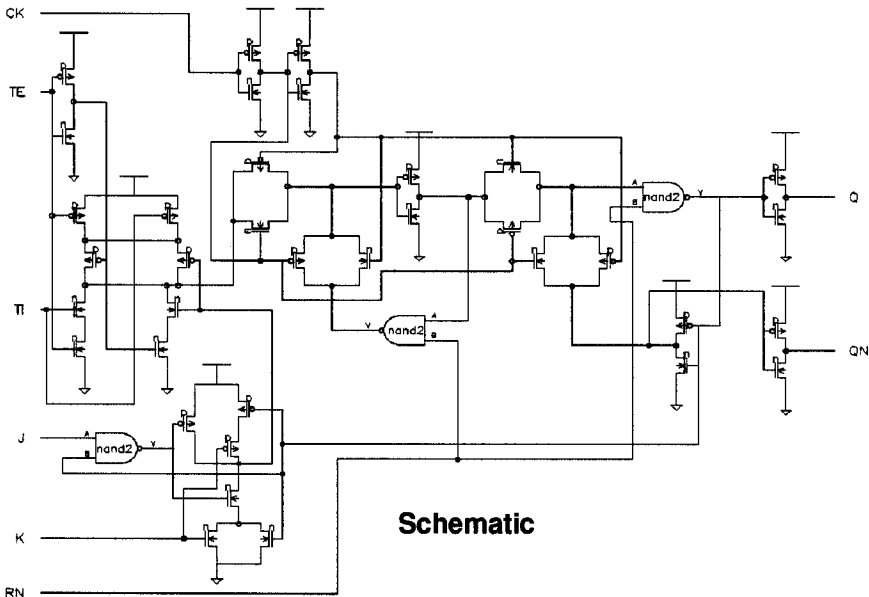
FJ2SD2: 13



**Symbol**

J	K	RN	TI	TE	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	1	x	0		0	1
1	0	1	x	0		1	0
0	0	1	x	0		Q <sub>n</sub>	Q <sub>Nn</sub>
1	1	1	x	0		Q <sub>Nn</sub>	Q <sub>n</sub>
x	x	1	x	0		Q <sub>n</sub>	Q <sub>Nn</sub>
x	x	0	x	x	x	0	1
x	x	1	0	1		0	1
x	x	1	1	1		1	0

**Truth Table**



**Schematic**

**FJ2S Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{q}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.77	$0.68 + 0.047 \cdot \text{SL}$	$0.69 + 0.043 \cdot \text{SL}$	$0.70 + 0.043 \cdot \text{SL}$
	tPHL	0.67	$0.60 + 0.035 \cdot \text{SL}$	$0.64 + 0.023 \cdot \text{SL}$	$0.70 + 0.020 \cdot \text{SL}$
	tR	0.36	$0.16 + 0.099 \cdot \text{SL}$	$0.16 + 0.100 \cdot \text{SL}$	$0.12 + 0.101 \cdot \text{SL}$
	tF	0.24	$0.16 + 0.040 \cdot \text{SL}$	$0.17 + 0.037 \cdot \text{SL}$	$0.15 + 0.038 \cdot \text{SL}$
RN to Q	tPHL	0.55	$0.48 + 0.037 \cdot \text{SL}$	$0.52 + 0.023 \cdot \text{SL}$	$0.58 + 0.020 \cdot \text{SL}$
	tF	0.27	$0.19 + 0.038 \cdot \text{SL}$	$0.20 + 0.035 \cdot \text{SL}$	$0.15 + 0.037 \cdot \text{SL}$
CK to QN	tPLH	0.84	$0.76 + 0.041 \cdot \text{SL}$	$0.76 + 0.041 \cdot \text{SL}$	$0.75 + 0.041 \cdot \text{SL}$
	tPHL	0.85	$0.80 + 0.027 \cdot \text{SL}$	$0.82 + 0.021 \cdot \text{SL}$	$0.84 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.11 + 0.093 \cdot \text{SL}$	$0.10 + 0.096 \cdot \text{SL}$	$0.08 + 0.097 \cdot \text{SL}$
	tF	0.18	$0.11 + 0.035 \cdot \text{SL}$	$0.11 + 0.036 \cdot \text{SL}$	$0.08 + 0.038 \cdot \text{SL}$
RN to QN	tPLH	0.73	$0.64 + 0.040 \cdot \text{SL}$	$0.64 + 0.041 \cdot \text{SL}$	$0.64 + 0.041 \cdot \text{SL}$
	tR	0.30	$0.11 + 0.093 \cdot \text{SL}$	$0.10 + 0.096 \cdot \text{SL}$	$0.09 + 0.097 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **FJ2S Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.725
Input Setup Time (K to CK)	tSU	0.670
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.889
Recovery Time (RN)	tRC	0.139

# FJ2SD2

JK Flip-Flop with Reset, Scan, Positive Edge Trigger, 2X Drive

## FJ2SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

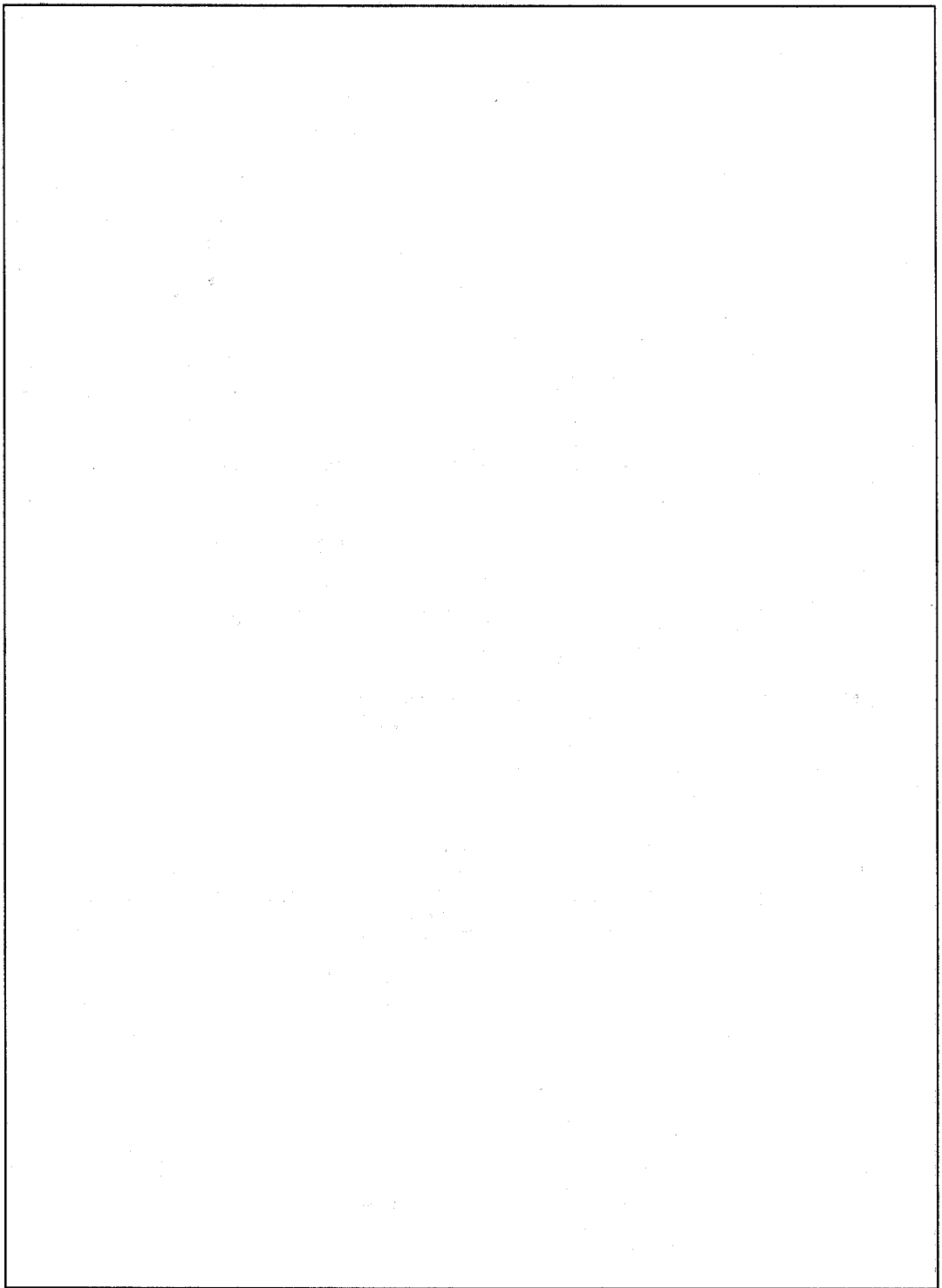
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.76	$0.71 + 0.025*SL$	$0.72 + 0.022*SL$	$0.74 + 0.021*SL$
	tPHL	0.67	$0.63 + 0.022*SL$	$0.65 + 0.014*SL$	$0.72 + 0.011*SL$
	tR	0.27	$0.18 + 0.045*SL$	$0.17 + 0.048*SL$	$0.14 + 0.050*SL$
	tF	0.22	$0.17 + 0.023*SL$	$0.18 + 0.019*SL$	$0.19 + 0.019*SL$
RN to Q	tPHL	0.55	$0.50 + 0.023*SL$	$0.53 + 0.014*SL$	$0.60 + 0.011*SL$
	tF	0.25	$0.21 + 0.022*SL$	$0.22 + 0.018*SL$	$0.21 + 0.018*SL$
CK to QN	tPLH	0.88	$0.84 + 0.018*SL$	$0.84 + 0.019*SL$	$0.83 + 0.020*SL$
	tPHL	0.91	$0.88 + 0.016*SL$	$0.89 + 0.012*SL$	$0.93 + 0.010*SL$
	tR	0.21	$0.12 + 0.042*SL$	$0.11 + 0.046*SL$	$0.09 + 0.047*SL$
	tF	0.17	$0.13 + 0.019*SL$	$0.14 + 0.018*SL$	$0.12 + 0.018*SL$
RN to QN	tPLH	0.76	$0.73 + 0.018*SL$	$0.72 + 0.019*SL$	$0.71 + 0.020*SL$
	tR	0.21	$0.12 + 0.043*SL$	$0.11 + 0.046*SL$	$0.09 + 0.047*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FJ2SD2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.725
Input Setup Time (K to CK)	tSU	0.670
Input Setup Time (TE to CK)	tSU	0.834
Input Setup Time (TI to CK)	tSU	0.889
Recovery Time (RN)	tRC	0.139





# FJ4/FJ4D2

JK Flip-Flop with Reset, Set, Posistive Edge Trigger, 1X Drive or 2X Drive

Inputs: J, K, CK, SN, RN

Outputs: Q, QN

Input Loading (SL):

- J, K, CK: 1

- SN, RN: 2

Maximum Fanout (Rec. SL): All :

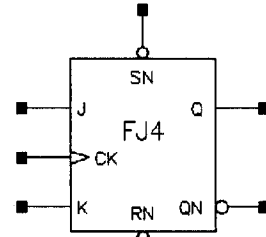
FJ4: 28

FJ4D2: 56

Gate Count:

FJ4: 11

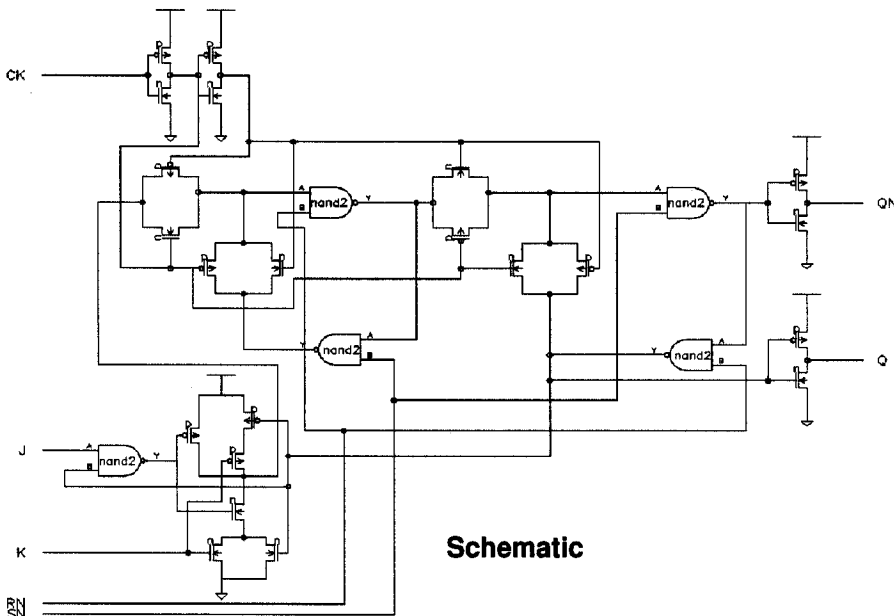
FJ4D2: 12



**Symbol**

J	K	RN	SN	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	1	1		0	1
1	0	1	1		1	0
0	0	1	1		Q <sub>n</sub>	Q <sub>Nn</sub>
1	1	1	1		Q <sub>Nn</sub>	Q <sub>n</sub>
x	x	1	1		Q <sub>n</sub>	Q <sub>Nn</sub>
x	x	0	1	x	0	1
x	x	1	0	x	1	0
x	x	0	0	x	0	0

**Truth Table**



**Schematic**

**FJ4 Switching Characteristics**[Delays for typical process, 25.00°C, 5.00V, when  $t_{\text{tr}}$  and  $t_{\text{f}} = 0.80\text{ns}$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.80	$0.72 + 0.042 \cdot \text{SL}$	$0.73 + 0.039 \cdot \text{SL}$	$0.72 + 0.040 \cdot \text{SL}$
	tR	0.33	$0.15 + 0.087 \cdot \text{SL}$	$0.14 + 0.090 \cdot \text{SL}$	$0.10 + 0.092 \cdot \text{SL}$
CK to Q	tPLH	0.94	$0.86 + 0.042 \cdot \text{SL}$	$0.86 + 0.040 \cdot \text{SL}$	$0.86 + 0.040 \cdot \text{SL}$
	tPHL	0.82	$0.76 + 0.031 \cdot \text{SL}$	$0.79 + 0.022 \cdot \text{SL}$	$0.84 + 0.020 \cdot \text{SL}$
	tR	0.33	$0.15 + 0.088 \cdot \text{SL}$	$0.14 + 0.090 \cdot \text{SL}$	$0.11 + 0.092 \cdot \text{SL}$
	tF	0.22	$0.16 + 0.034 \cdot \text{SL}$	$0.15 + 0.036 \cdot \text{SL}$	$0.12 + 0.037 \cdot \text{SL}$
RN to Q	tPLH	0.42	$0.34 + 0.044 \cdot \text{SL}$	$0.35 + 0.040 \cdot \text{SL}$	$0.35 + 0.040 \cdot \text{SL}$
	tPHL	0.54	$0.47 + 0.035 \cdot \text{SL}$	$0.51 + 0.022 \cdot \text{SL}$	$0.56 + 0.020 \cdot \text{SL}$
	tR	0.33	$0.16 + 0.085 \cdot \text{SL}$	$0.15 + 0.090 \cdot \text{SL}$	$0.11 + 0.092 \cdot \text{SL}$
	tF	0.26	$0.19 + 0.036 \cdot \text{SL}$	$0.19 + 0.034 \cdot \text{SL}$	$0.13 + 0.037 \cdot \text{SL}$
SN to QN	tPLH	0.30	$0.22 + 0.042 \cdot \text{SL}$	$0.22 + 0.040 \cdot \text{SL}$	$0.22 + 0.040 \cdot \text{SL}$
	tPHL	0.46	$0.39 + 0.031 \cdot \text{SL}$	$0.42 + 0.022 \cdot \text{SL}$	$0.46 + 0.020 \cdot \text{SL}$
	tR	0.31	$0.14 + 0.087 \cdot \text{SL}$	$0.13 + 0.091 \cdot \text{SL}$	$0.09 + 0.093 \cdot \text{SL}$
	tF	0.22	$0.15 + 0.035 \cdot \text{SL}$	$0.15 + 0.036 \cdot \text{SL}$	$0.10 + 0.038 \cdot \text{SL}$
CK to QN	tPLH	0.65	$0.56 + 0.042 \cdot \text{SL}$	$0.57 + 0.040 \cdot \text{SL}$	$0.57 + 0.040 \cdot \text{SL}$
	tPHL	0.61	$0.55 + 0.029 \cdot \text{SL}$	$0.57 + 0.021 \cdot \text{SL}$	$0.60 + 0.020 \cdot \text{SL}$
	tR	0.30	$0.13 + 0.088 \cdot \text{SL}$	$0.12 + 0.092 \cdot \text{SL}$	$0.10 + 0.093 \cdot \text{SL}$
	tF	0.19	$0.12 + 0.034 \cdot \text{SL}$	$0.11 + 0.037 \cdot \text{SL}$	$0.08 + 0.039 \cdot \text{SL}$
RN to QN	tPLH	0.85	$0.77 + 0.042 \cdot \text{SL}$	$0.78 + 0.040 \cdot \text{SL}$	$0.77 + 0.040 \cdot \text{SL}$
	tR	0.31	$0.13 + 0.087 \cdot \text{SL}$	$0.12 + 0.091 \cdot \text{SL}$	$0.09 + 0.093 \cdot \text{SL}$

\*Range1 :  $\text{SL} < 3.00$ , \*Range2 :  $3.00 \leq \text{SL} \leq 20.00$ , \*Range3 :  $20.00 < \text{SL}$ **FJ4 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.616
Input Setup Time (K to CK)	tSU	0.452
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

# FJ4D2

JK Flip-Flop with Reset, Set, Positive Edge Trigger, 2X Drive

## FJ4D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

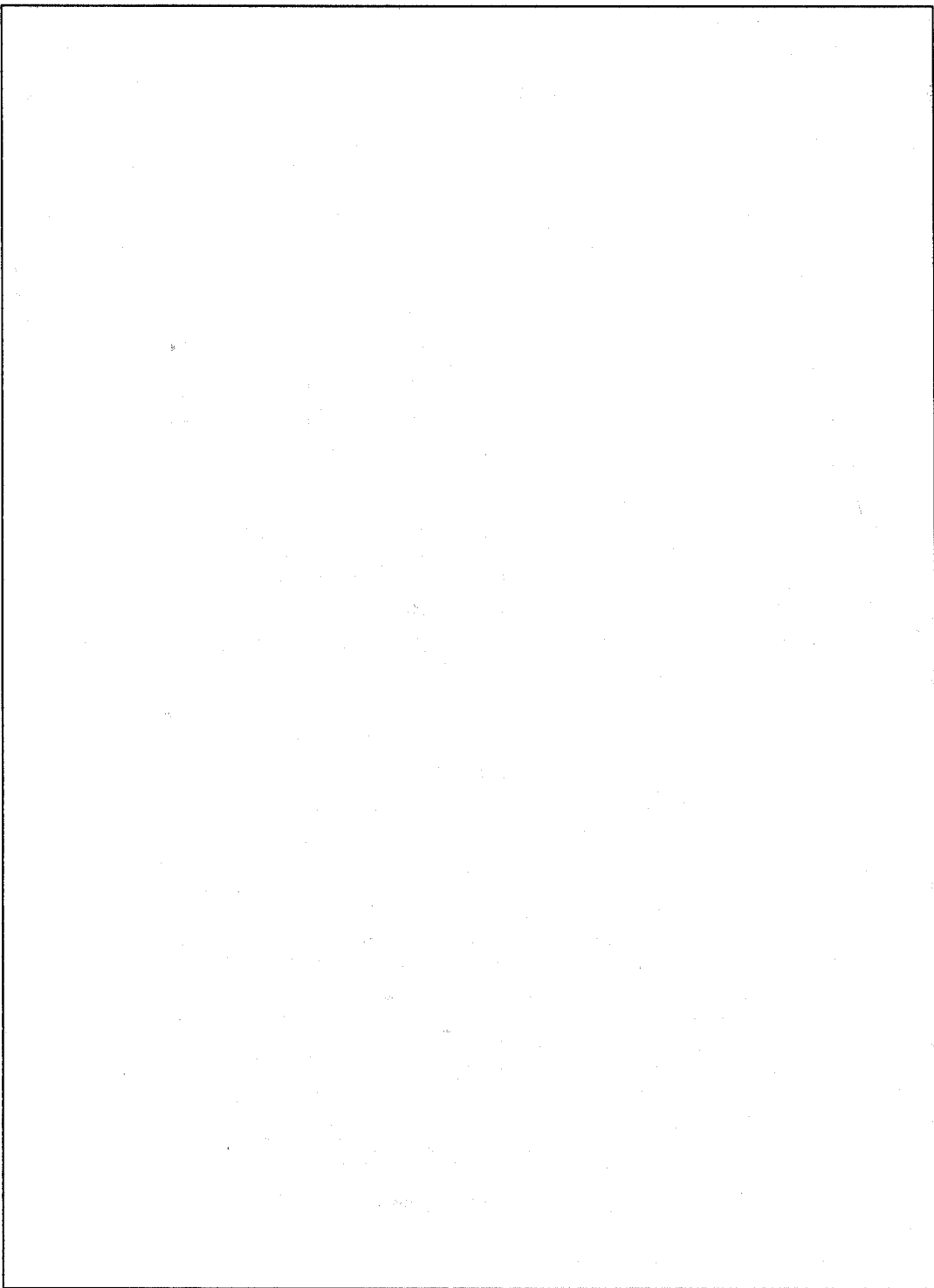
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.86	$0.81 + 0.023*SL$	$0.82 + 0.020*SL$	$0.82 + 0.020*SL$
	tR	0.25	$0.17 + 0.044*SL$	$0.16 + 0.046*SL$	$0.13 + 0.047*SL$
CK to Q	tPLH	1.00	$0.96 + 0.023*SL$	$0.96 + 0.020*SL$	$0.97 + 0.020*SL$
	tPHL	0.87	$0.84 + 0.019*SL$	$0.85 + 0.013*SL$	$0.90 + 0.011*SL$
	tR	0.25	$0.17 + 0.044*SL$	$0.16 + 0.046*SL$	$0.14 + 0.047*SL$
	tF	0.21	$0.16 + 0.021*SL$	$0.17 + 0.018*SL$	$0.17 + 0.018*SL$
RN to Q	tPLH	0.42	$0.37 + 0.025*SL$	$0.38 + 0.021*SL$	$0.40 + 0.020*SL$
	tPHL	0.53	$0.49 + 0.022*SL$	$0.52 + 0.014*SL$	$0.58 + 0.010*SL$
	tR	0.26	$0.18 + 0.043*SL$	$0.17 + 0.045*SL$	$0.14 + 0.047*SL$
SN to QN	tF	0.24	$0.20 + 0.021*SL$	$0.21 + 0.017*SL$	$0.20 + 0.017*SL$
	tPLH	0.30	$0.26 + 0.023*SL$	$0.26 + 0.020*SL$	$0.27 + 0.020*SL$
	tPHL	0.46	$0.42 + 0.019*SL$	$0.44 + 0.013*SL$	$0.49 + 0.010*SL$
	tR	0.23	$0.15 + 0.044*SL$	$0.14 + 0.045*SL$	$0.12 + 0.046*SL$
CK to QN	tF	0.21	$0.17 + 0.018*SL$	$0.17 + 0.017*SL$	$0.15 + 0.018*SL$
	tPLH	0.65	$0.60 + 0.023*SL$	$0.61 + 0.020*SL$	$0.62 + 0.020*SL$
	tPHL	0.62	$0.59 + 0.018*SL$	$0.60 + 0.012*SL$	$0.64 + 0.010*SL$
	tR	0.23	$0.14 + 0.043*SL$	$0.13 + 0.045*SL$	$0.11 + 0.047*SL$
RN to QN	tF	0.17	$0.13 + 0.018*SL$	$0.13 + 0.018*SL$	$0.12 + 0.019*SL$
	tPLH	0.86	$0.82 + 0.022*SL$	$0.82 + 0.020*SL$	$0.83 + 0.020*SL$
	tR	0.23	$0.14 + 0.044*SL$	$0.14 + 0.045*SL$	$0.11 + 0.047*SL$

\*Range1 :  $SL < 3.00$ , \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

## FJ4D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.616
Input Setup Time (K to CK)	tSU	0.452
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139



# FJ4S/FJ4SD2

JK Flip-Flop with Reset, Set, Scan, Positive Edge Trigger, 1X Drive or 2X Drive

Inputs: J, K, CK, TI, TE, SN, RN

Outputs: Q, QN

Input Loading (SL):

- J, K, CK, TI: 1

- TE, SN, RN: 2

Maximum Fanout (Rec. SL): All :

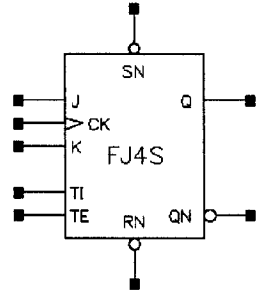
FJ4S: 28

FJ4SD2: 56

Gate Count:

FJ4S: 13

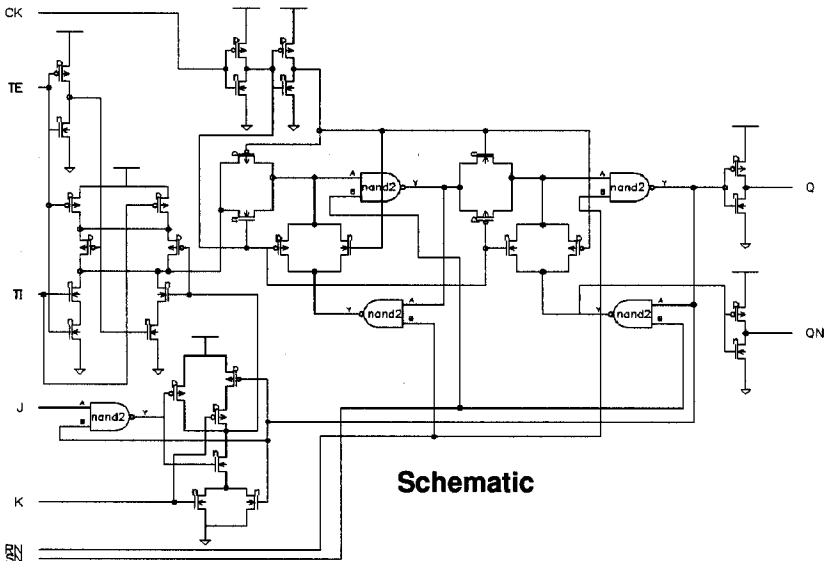
FJ4SD2: 14



Symbol

J	K	RN	SN	TI	TE	CK	Q <sub>n+1</sub>	Q <sub>Nn+1</sub>
0	1	1	1	x	0		0	1
1	0	1	1	x	0		1	0
0	0	1	1	x	0		Q <sub>n</sub>	Q <sub>Nn</sub>
1	1	1	1	x	0		Q <sub>Nn</sub>	Q <sub>n</sub>
x	x	1	1	x	0		Q <sub>n</sub>	Q <sub>Nn</sub>
x	x	0	1	x	x	x	0	1
x	x	1	0	x	x	x	1	0
x	x	0	0	x	x	x	0	0
x	x	1	1	0	1		0	1
x	x	1	1	1	1		1	0

Truth Table



Schematic

**FJ4S Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{tr}$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.98	$0.89 + 0.044*SL$	$0.91 + 0.040*SL$	$0.90 + 0.040*SL$
	tR	0.33	$0.16 + 0.087*SL$	$0.15 + 0.090*SL$	$0.11 + 0.092*SL$
CK to Q	tPLH	0.77	$0.68 + 0.044*SL$	$0.69 + 0.040*SL$	$0.70 + 0.040*SL$
	tPHL	0.70	$0.63 + 0.034*SL$	$0.67 + 0.023*SL$	$0.73 + 0.020*SL$
	tR	0.34	$0.16 + 0.089*SL$	$0.15 + 0.090*SL$	$0.12 + 0.092*SL$
	tF	0.23	$0.16 + 0.038*SL$	$0.16 + 0.037*SL$	$0.14 + 0.038*SL$
RN to Q	tPLH	0.42	$0.33 + 0.044*SL$	$0.34 + 0.040*SL$	$0.34 + 0.040*SL$
	tPHL	0.54	$0.46 + 0.035*SL$	$0.50 + 0.023*SL$	$0.57 + 0.020*SL$
	tR	0.34	$0.17 + 0.086*SL$	$0.15 + 0.090*SL$	$0.11 + 0.092*SL$
	tF	0.26	$0.18 + 0.039*SL$	$0.19 + 0.035*SL$	$0.15 + 0.037*SL$
SN to QN	tPLH	0.32	$0.23 + 0.043*SL$	$0.24 + 0.040*SL$	$0.24 + 0.040*SL$
	tPHL	0.44	$0.38 + 0.031*SL$	$0.41 + 0.021*SL$	$0.44 + 0.020*SL$
	tR	0.31	$0.14 + 0.087*SL$	$0.13 + 0.091*SL$	$0.09 + 0.092*SL$
	tF	0.21	$0.15 + 0.033*SL$	$0.14 + 0.035*SL$	$0.09 + 0.038*SL$
CK to QN	tPLH	0.95	$0.87 + 0.039*SL$	$0.87 + 0.039*SL$	$0.87 + 0.040*SL$
	tPHL	0.85	$0.80 + 0.027*SL$	$0.81 + 0.021*SL$	$0.84 + 0.020*SL$
	tR	0.30	$0.13 + 0.088*SL$	$0.12 + 0.091*SL$	$0.09 + 0.092*SL$
	tF	0.18	$0.11 + 0.036*SL$	$0.11 + 0.036*SL$	$0.07 + 0.038*SL$
RN to QN	tPLH	0.79	$0.71 + 0.039*SL$	$0.71 + 0.039*SL$	$0.71 + 0.040*SL$
	tR	0.30	$0.13 + 0.087*SL$	$0.12 + 0.091*SL$	$0.09 + 0.092*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

**FJ4S Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.725
Input Setup Time (K to CK)	tSU	0.780

# FJ4S

JK Flip-Flop with Reset, Set, Scan, Positive Edge Trigger, 1X Drive

## FJ4S Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Input Setup Time (TE to CK)	tSU	0.998
Input Setup Time (TI to CK)	tSU	0.998
Recovery Time (RN)	tRC	0.139
Recovery Time (SN)	tRC	0.139

## FJ4SD2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_p$  and  $t_f = 0.80ns$ ]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
SN to Q	tPLH	0.98	$0.93 + 0.024*SL$	$0.94 + 0.021*SL$	$0.96 + 0.020*SL$
	tR	0.26	$0.17 + 0.043*SL$	$0.17 + 0.045*SL$	$0.14 + 0.046*SL$
CK to Q	tPLH	0.76	$0.71 + 0.025*SL$	$0.72 + 0.021*SL$	$0.74 + 0.020*SL$
	tPHL	0.70	$0.66 + 0.021*SL$	$0.68 + 0.014*SL$	$0.74 + 0.011*SL$
	tR	0.26	$0.17 + 0.045*SL$	$0.17 + 0.045*SL$	$0.14 + 0.046*SL$
	tF	0.21	$0.17 + 0.020*SL$	$0.18 + 0.019*SL$	$0.18 + 0.018*SL$
RN to Q	tPLH	0.41	$0.36 + 0.025*SL$	$0.37 + 0.021*SL$	$0.39 + 0.020*SL$
	tPHL	0.53	$0.49 + 0.021*SL$	$0.51 + 0.014*SL$	$0.58 + 0.011*SL$
	tR	0.26	$0.18 + 0.043*SL$	$0.17 + 0.045*SL$	$0.14 + 0.046*SL$
	tF	0.24	$0.19 + 0.022*SL$	$0.21 + 0.018*SL$	$0.20 + 0.018*SL$
SN to QN	tPLH	0.32	$0.27 + 0.023*SL$	$0.28 + 0.020*SL$	$0.29 + 0.020*SL$
	tPHL	0.45	$0.41 + 0.019*SL$	$0.43 + 0.012*SL$	$0.47 + 0.010*SL$
	tR	0.23	$0.15 + 0.042*SL$	$0.14 + 0.045*SL$	$0.11 + 0.046*SL$
	tF	0.20	$0.17 + 0.015*SL$	$0.16 + 0.017*SL$	$0.14 + 0.018*SL$
CK to QN	tPLH	1.01	$0.97 + 0.020*SL$	$0.97 + 0.020*SL$	$0.97 + 0.020*SL$
	tPHL	0.91	$0.87 + 0.016*SL$	$0.89 + 0.012*SL$	$0.92 + 0.010*SL$
	tR	0.23	$0.14 + 0.044*SL$	$0.14 + 0.045*SL$	$0.11 + 0.047*SL$
	tF	0.17	$0.14 + 0.017*SL$	$0.13 + 0.018*SL$	$0.12 + 0.018*SL$
RN to QN	tPLH	0.85	$0.80 + 0.020*SL$	$0.81 + 0.020*SL$	$0.80 + 0.020*SL$
	tR	0.23	$0.14 + 0.044*SL$	$0.14 + 0.045*SL$	$0.11 + 0.046*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$ 

## FJ4SD2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width Low (SN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Input Hold Time (J to CK)	tHD	0.000
Input Hold Time (K to CK)	tHD	0.000
Input Hold Time (TE to CK)	tHD	0.000
Input Hold Time (TI to CK)	tHD	0.000
Input Setup Time (J to CK)	tSU	0.725
Input Setup Time (K to CK)	tSU	0.780
Input Setup Time (TE to CK)	tSU	0.998
Input Setup Time (TI to CK)	tSU	0.998



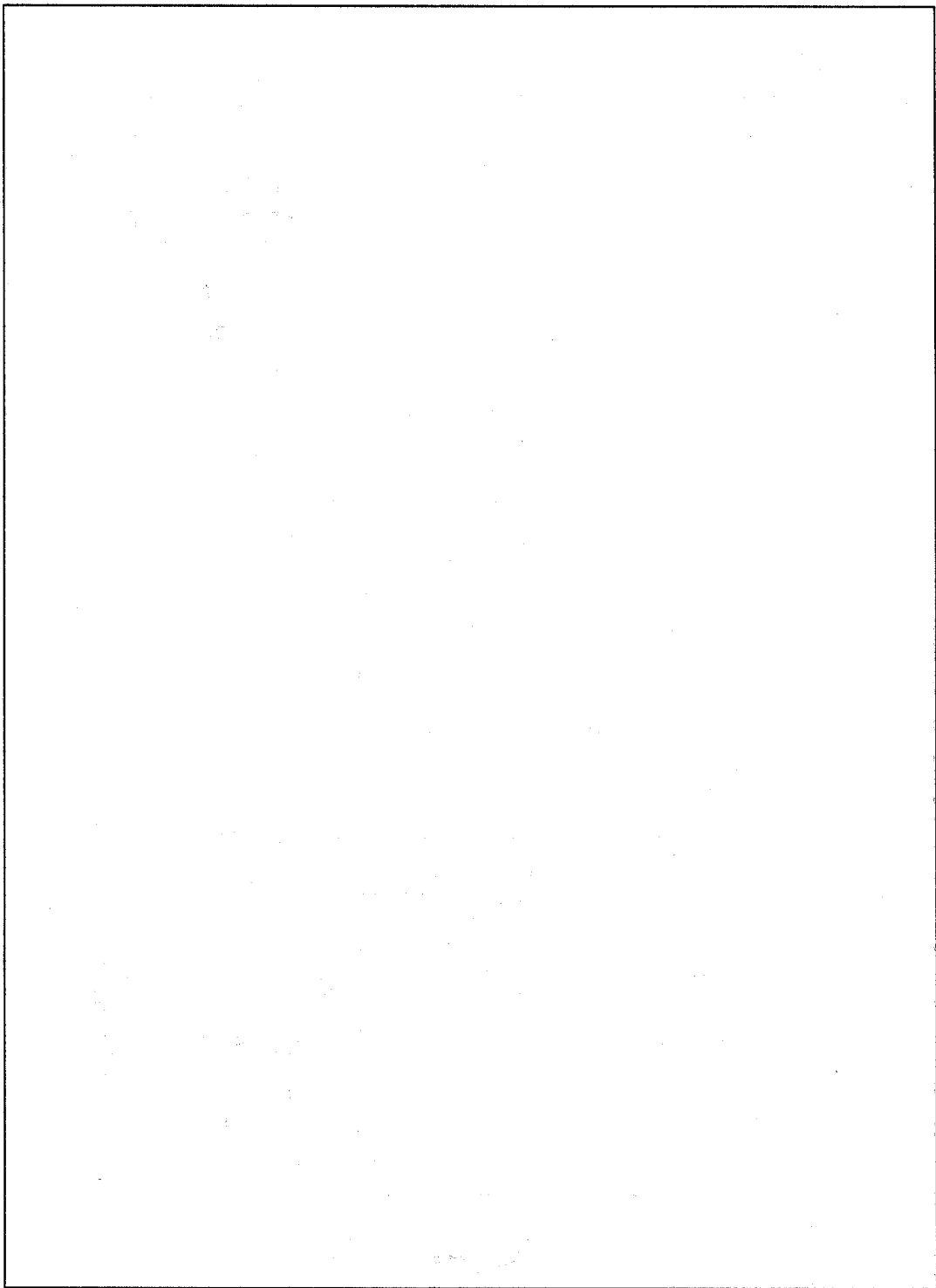
# FJ4SD2

JK Flip-Flop with Reset, Set, Scan, Positive Edge Trigger, 2X Drive

## FJ4SD2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Recovery Time (RN)	t <sub>RC</sub>	0.139
Recovery Time (SN)	t <sub>RC</sub>	0.139



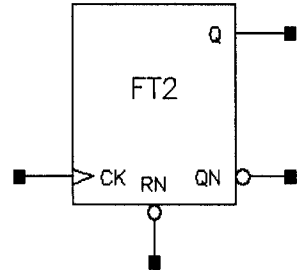
# FT2/FT2D2

Toggle Flip-Flop with Reset, Positive Edge Trigger, 1X Drive or 2X Drive


Inputs: CK, RN  
 Outputs: Q, QN  
 Input Loading (SL):  
 - CK: 1  
 - RN: 2

Maximum Fanout (Rec. SL): All :  
 FT2: 28  
 FT2D2: 56

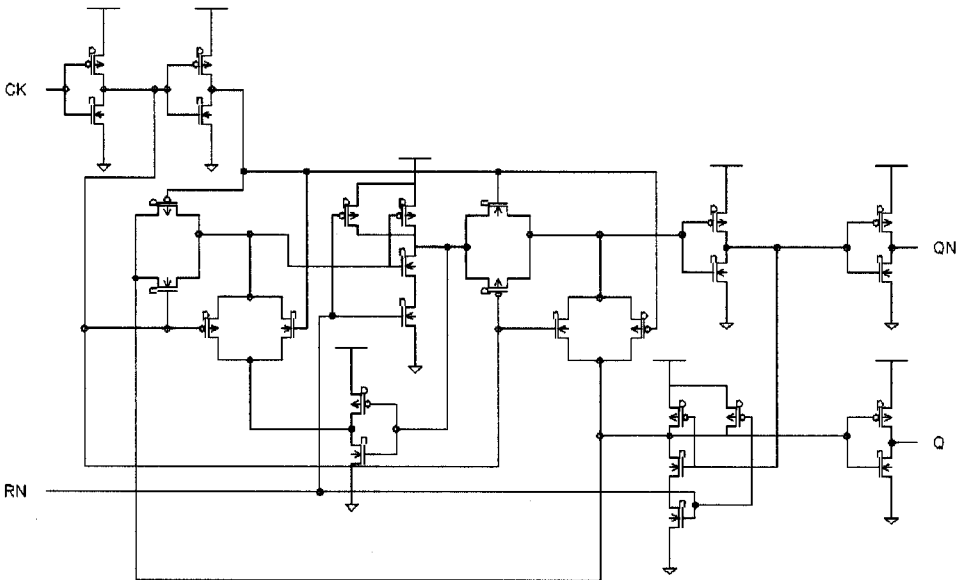
Gate Count:  
 FT2: 7  
 FT2D2: 8



**Symbol**

RN	CK	Qn+1	QNn+1
1		QNn	Qn
0	x	0	1

**Truth Table**



**Schematic**

**FT2 Switching Characteristics**

[Delays for typical process, 25.00°C, 5.00V, when  $t_{R}$  and  $t_{F}$  = 0.80ns]

(SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	t <sub>PLH</sub>	0.87	$0.79 + 0.040 \cdot SL$	$0.80 + 0.040 \cdot SL$	$0.79 + 0.040 \cdot SL$
	t <sub>PHL</sub>	0.69	$0.64 + 0.028 \cdot SL$	$0.66 + 0.021 \cdot SL$	$0.69 + 0.020 \cdot SL$
	t <sub>R</sub>	0.31	$0.13 + 0.087 \cdot SL$	$0.12 + 0.091 \cdot SL$	$0.09 + 0.092 \cdot SL$
	t <sub>F</sub>	0.19	$0.12 + 0.034 \cdot SL$	$0.12 + 0.036 \cdot SL$	$0.09 + 0.038 \cdot SL$
RN to Q	t <sub>PHL</sub>	0.48	$0.42 + 0.032 \cdot SL$	$0.45 + 0.021 \cdot SL$	$0.48 + 0.020 \cdot SL$
	t <sub>F</sub>	0.23	$0.16 + 0.035 \cdot SL$	$0.16 + 0.034 \cdot SL$	$0.10 + 0.037 \cdot SL$
CK to QN	t <sub>PLH</sub>	0.57	$0.49 + 0.041 \cdot SL$	$0.49 + 0.040 \cdot SL$	$0.49 + 0.040 \cdot SL$
	t <sub>PHL</sub>	0.60	$0.55 + 0.028 \cdot SL$	$0.57 + 0.021 \cdot SL$	$0.59 + 0.020 \cdot SL$
	t <sub>R</sub>	0.29	$0.11 + 0.088 \cdot SL$	$0.10 + 0.092 \cdot SL$	$0.08 + 0.093 \cdot SL$
	t <sub>F</sub>	0.18	$0.11 + 0.037 \cdot SL$	$0.11 + 0.037 \cdot SL$	$0.08 + 0.039 \cdot SL$
RN to QN	t <sub>PLH</sub>	0.77	$0.69 + 0.040 \cdot SL$	$0.70 + 0.040 \cdot SL$	$0.69 + 0.040 \cdot SL$
	t <sub>R</sub>	0.29	$0.11 + 0.090 \cdot SL$	$0.11 + 0.092 \cdot SL$	$0.08 + 0.093 \cdot SL$

\*Range1 : SL < 3.00, \*Range2 : 3.00 ≤ SL ≤ 20.00, \*Range3 : 20.00 < SL

**FT2 Timing Requirements**

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	t <sub>PWL</sub>	0.920
Pulse Width Low (RN)	t <sub>PWL</sub>	0.920
Pulse Width High (CK)	t <sub>PWH</sub>	0.920
Recovery Time (RN)	t <sub>RC</sub>	0.139

# FT2D2

## Toggle Flip-Flop with Reset, Positive Edge Trigger, 2X Drive

### FT2D2 Switching Characteristics

[Delays for typical process, 25.00°C, 5.00V, when  $t_R$  and  $t_F = 0.80ns$ ]

(SL: Standard Load)

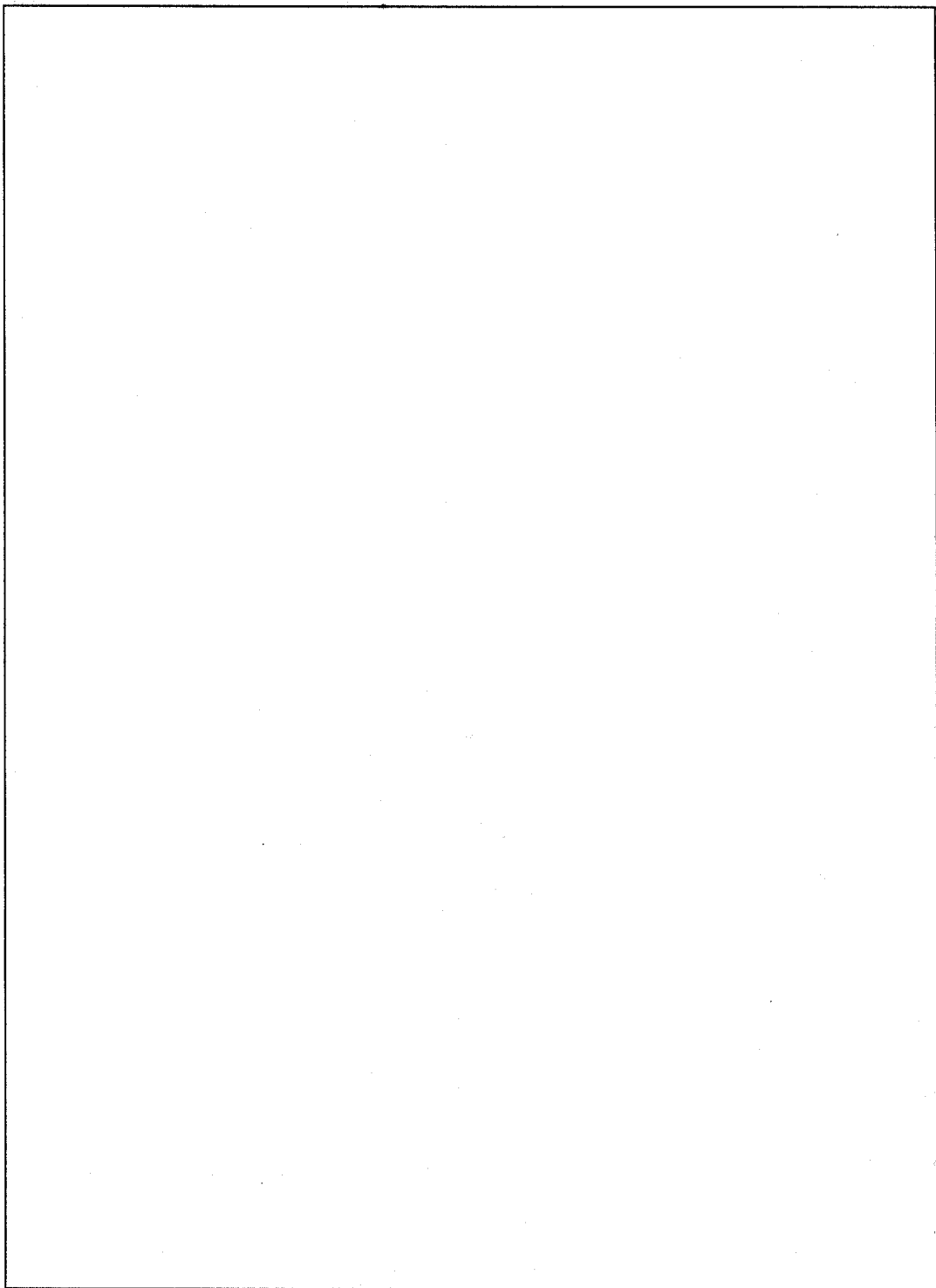
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
CK to Q	tPLH	0.94	$0.89 + 0.021*SL$	$0.90 + 0.020*SL$	$0.89 + 0.020*SL$
	tPHL	0.74	$0.71 + 0.017*SL$	$0.72 + 0.012*SL$	$0.76 + 0.010*SL$
	tR	0.24	$0.15 + 0.046*SL$	$0.15 + 0.046*SL$	$0.12 + 0.047*SL$
	tF	0.17	$0.13 + 0.019*SL$	$0.14 + 0.018*SL$	$0.13 + 0.018*SL$
RN to Q	tPHL	0.48	$0.44 + 0.020*SL$	$0.46 + 0.013*SL$	$0.51 + 0.010*SL$
	tF	0.21	$0.18 + 0.017*SL$	$0.18 + 0.017*SL$	$0.16 + 0.018*SL$
CK to QN	tPLH	0.56	$0.52 + 0.021*SL$	$0.53 + 0.020*SL$	$0.53 + 0.020*SL$
	tPHL	0.61	$0.58 + 0.018*SL$	$0.60 + 0.012*SL$	$0.63 + 0.010*SL$
	tR	0.20	$0.12 + 0.044*SL$	$0.11 + 0.046*SL$	$0.09 + 0.047*SL$
	tF	0.17	$0.13 + 0.019*SL$	$0.13 + 0.018*SL$	$0.12 + 0.019*SL$
RN to QN	tPLH	0.77	$0.73 + 0.021*SL$	$0.73 + 0.020*SL$	$0.73 + 0.020*SL$
	tR	0.21	$0.12 + 0.042*SL$	$0.11 + 0.046*SL$	$0.09 + 0.047*SL$

\*Range1 : SL < 3.00, \*Range2 :  $3.00 \leq SL \leq 20.00$ , \*Range3 :  $20.00 < SL$

### FT2D2 Timing Requirements

[Values for typical process, 25.00°C, 5.00V]

Parameter	Symbol	Value [ns]
Pulse Width Low (CK)	tPWL	0.920
Pulse Width Low (RN)	tPWL	0.920
Pulse Width High (CK)	tPWH	0.920
Recovery Time (RN)	tRC	0.139

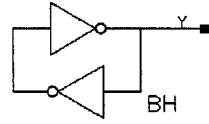


# Busholder

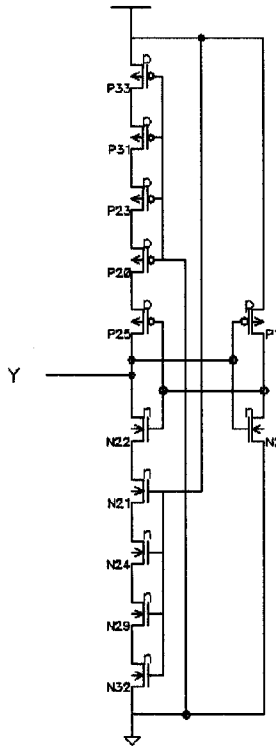
Inputs: Y  
Outputs: Y

Input Loading (SL): 2

Gate Count: 2



**Symbol**



**Schematic**