ASPEC
TECHNOLOGY

ASPEC Technology, Inc.

0.5 Micron

HDA/C 9000

(TSMC Polycide 5.0V Process)

3.3V

I/OCELL Databook

75 Micron Pitch (Type 1)

December 1996

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Chapter 1: Introduction to the 5.0V Process 3.3V 0.5μm Products

This databook provides basic technical information on the 5.0V process 3.3V HDA/C9000 product line, including input and output DC characteristics, cell name conventions and Application Notes on Power and Ground rules and Clock Skew Management.

1.1 Product Description

HDA/C9000, based on a patented architecture, supports a triple layer metal HCMOS process. The high gate-density of this architecture results in lower on-chip noise, higher chip level performance, and lower component cost. HDA/C9000 is well-suited for cost-sensitive applications that also demand high circuit performance.

HDA/C9000 libraries support over 300 different combinations of I/O buffers are supported, including Input Buffers with CMOS, TTL and Schmitt Trigger threshold voltages, and Output Buffers with varied slew-rate control for VSS/VDD bus noise management. Buffers that provide an interface between a 5.0V environment in the chip core and a 3.3V environment external to the the chip are also available.

1.2 CAE Support

HDA/C9000 supports popular design platforms and environments such as Verilog, Viewlogic, Mentor, and Synopsys for front-end logic design capture and simulation, and Cadence Cell3, Avant! Arc-CellXO, and SVR Sonic for back-end place-and-route. For higher simulation accuracy, HDA/C9000 uses the ADVER™ delay calculator. Signal interconnect delay is based on RC Tree analysis.

1.3 I/O (Input/Output) Buffers

There are more than 300 I/O buffers. Each I/O cell is implemented solely on the basic I/O cell architecture which forms the periphery of the masterslice. Test logic is provided to enable efficient parametric (threshold voltage) testing on input buffers, including CMOS and TTL level converters, Schmitt Trigger Input buffers, Clock drivers and Oscillator buffers. Pull-up and pull-down resistors are optional features. The I/O structure has been fully characterized for ESD protection and latch-up resistance.

Three basic types of single voltage output buffers, non-inverting, 3-state and open drain, are available in a range of driving capabilities from 1 mA to 24 mA. Slew-rate control buffers are provided for each output buffer type (except 1mA and 2mA buffers) to reduce power/ground bus noise and signal ringing, especially for simultaneous switching outputs.

Also available are two basic types of 5.0V Tolerant output buffers, 3-state and open-drain, in a range of driving capabilities from 1mA to 6mA.

Bi-directional buffers are combinations of input buffers and output 3-state buffers (or open drain buffers) in a single unit.

1.4 VDD and VSS Rules and Guidelines

There are three types of VDD and VSS in this product family, each with its related bus and pad cells.

1. Core Logic

   IVSS, IVDD

2. Input Buffers

   RVSS, RVDD

3. Output Buffers

   OVSS, OVDD

The number of VSS and VDD pads required for a specific design depends on the following factors:

Number of input and output buffers

Number of simultaneous switching inputs

Number of simultaneous switching outputs

Number of used gates and number of simultaneous switching gates

Operating frequency of the design

1.4.1 Core Logic VSS Bus and IVSS Pad Allocation Guidelines

The purpose of these guidelines is to ensure that VDD/VSS bounce due to simultaneous gate switching is kept to a minimum. Voltage bounce on the power bus could have a negative impact on gate switching speed, and in an extreme case could even affect the functionality of the macrocells, e.g., flip-flops and latches. Because of variations in package inductance, the number of VDD/VSS pads required for a specific design is a function of the operating frequency of the chip, i.e., designs operating at high frequency should use more VDD/VSS pads.

- VDD Bus width and pad requirement is half that of VSS.
- VDD/VSS Bus and Pads should be distributed evenly in the core and on all sides of the chip.
- At least one (1) IVSS pad should be used on each side of the chip.
- The total number of IVDD pads required is half that of IVSS.

The number of IVSS pads required for a design can be calculated from the following expression:

Number of IVSS pads = G x S x F x 2.72 x (10^ - 5)

where G = Total number of used gates (k)

S = % of simultaneous switching gates

F = Switching frequency in Mhz

1.4.2 Input Buffer RVDD Bus and RVSS Pad Allocation Guidelines

These guidelines ensure that adequate Input Threshold voltage margin is maintained during switching.

- One RVSS is required to support 32 input buffers, and one RVDD can support up to 64 inputs.
- For simultaneous switching inputs, one RVSS pad is required for every 20 inputs and one RVDD pad for every 40 inputs.
- RVSS/RVDD pads should be placed in such a way that they equally divide the input buffers on either side.

1.4.3 Output Buffer OVDD Bus and OVSS Pad Allocation Guidelines

The number of OVSS pads required for a device can be calculated from the following expression:

$\Sigma\,(IOL_{\text{Simultaneous Switching Outputs}})/40 \;+\; \Sigma\,(IOL_{\text{Normal Outputs}})/64$

- The total number of OVDD pads required is half that of OVSS.
- OVSS/OVDD pads should be placed in such a way that the output buffers are equally divided on either side.

1.5 Propagation Delays

Interconnect wire-length, temperature and supply voltage are the chief factors affecting propagation delay.

1.5.1 Wire Length Loading Estimation

Loading due to interconnect wire-length can be estimated with the following expression. The result is given in terms of number of equivalent standard loads.

$$C_{WL} = C_{fo} \times (0.049 \times \sqrt{A} + 0.48) + 0.079 \times \sqrt{A} + 0.33$$

where C_{fo} = number of fan-outs in standard load
A = area of block size in mm^2
C_{WL} = number of equivalent standard loads due to interconnect

e.g., C_{fo} = 7 (standard loads)
A = 25 mm^2
C_{WL} = 5.8 (standard load)

1.5.2 Temperature and Supply Voltage

Fig. 1.1 describes propagation delay correction factor (K_T) as a function of on-chip junction temperature (T_j), and voltage delay correction factor (K_V) as a function of supply voltage (V_{DD}). As a result of increasing CMOS power dissipation, ambient and junction temperature are generally not the same. The temperature of the die inside the package (junction temperature, T_j), is calculated using chip power dissipation and the Thermal Resistance to Ambient (θ_{ja}) temperature of the package. Information on package thermal performance can be obtained from ASPEC Application Engineers.

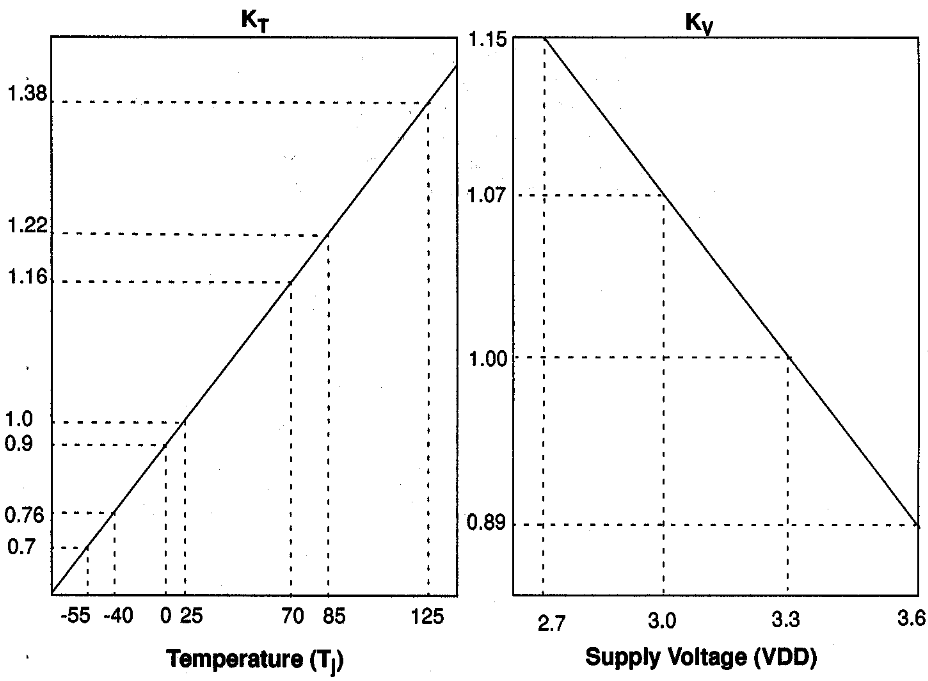


Figure 1.1: Effect of Temperature and Supply Voltage on Propagation Delay

1.5.3 Propagation Delay

A circuit should be designed to operate properly within a given specification level, either commercial, industrial or military. It is recommended that circuits be simulated for Best Case, Nominal Case and Worst Case conditions at each specification level. The following expressions also allow for the effect of process variation on circuit performance.

Worst Case:

$$T_{WC} = K_{PWC} \times K_T \times K_V \times t_{nom} = K_{WC} \times t_{nom}$$

Best Case:

$$T_{BC} = K_{PBC} \times K_T \times K_V \times t_{nom} = K_{BC} \times t_{nom}$$

T_{WC} = Worst case propagation delay
T_{BC} = Best case propagation delay
t_{nom} = nominal propagation delay (T_J = 25°C, V_{DD} = 5V and typical process parameters)
K_{PWC} = Worst case process correction factor
K_{PBC} = Best case process correction factor

Chapter 2.0 DC Characteristics

2.1 VDD = 5V ± 10%, junction temperature range -55 to +125°C.

Table 2.1: DC CHARACTERISTICS AT VDD = 5v

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage					
	CMOS				$0.3V_{DD}$	V
	CMOS Schmitt Trigger				1.0	V
	TTL				0.8	V
	TTL Schmitt Trigger				0.8	V
V_{IH}	Input High Voltage					
	CMOS		$0.7V_{DD}$			V
	CMOS Schmitt Trigger		4.0			V
	TTL		2.0			V
	TTL Schmitt Trigger		2.0			V
I_{IH}	Input High Current	$V_{IN}=V_{DD}$	-10		10	µA
	Input with pull-down	$V_{IN}=V_{DD}$	10		180	µA
I_{IL}	Input Low Current	$V_{IN}=V_{SS}$	-10		10	µA
	Input with pull-up	$V_{IN}=V_{SS}$	-180		-10	µA
V_{OH}	Output High Voltage					
	Type B1	I_{OH}= -1mA	2.4			V
	Type B2	I_{OH}= -2mA	2.4			V
	Type B4	I_{OH}= -4mA	2.4			V
	Type B8	I_{OH}= -8mA	2.4			V
	Type B12	I_{OH}= -12mA	2.4			V
	Type B16	I_{OH}= -16mA	2.4			V
	Type B20	I_{OH}= -20mA	2.4			V
	Type B24	I_{OH}= -24mA	2.4			V
V_{OL}	Output Low Voltage					
	Type B1	I_{OL}= 1mA			0.4	V
	Type B2	I_{OL}= 2mA			0.4	V
	Type B4	I_{OL}= 4mA			0.4	V
	Type B8	I_{OL}= 8mA			0.4	V
	Type B12	I_{OL}= 12mA			0.4	V
	Type B16	I_{OL}= 16mA			0.4	V
	Type B20	I_{OL}= 20mA			0.4	V
	Type B24	I_{OL}= 24mA			0.4	V
I_{OZ}	3-State Output Leakage Current	$V_{OH}=V_{SS}$ or V_{DD}	-10		10	µA
I_{DD}	Quiescent Supply Current	$V_{IN}=V_{SS}$ or V_{DD}			100[1]	µA

1. Depends on customer design

2.2 Absolute Maximum Ratings

Table 2.2: Maximum Ratings

	Symbol	Parameter	Rating	Unit
Absolute Maximum Ratings	V_{DD}	DC Supply Voltage	-0.3 to 7.0	V
	V_{IN}	DC Input Voltage	-0.3 to VDD +0.3	V
	I_{IN}	DC Input Current	± 10	mA
	T_{STG}	Storage Temperature	-40 to +125	°C
Recommended Operating Conditions	V_{DD}	DC Supply Voltage	4.5 to 5.5	V
	T_A	Commercial Temperature	0 to 70	°C
	T_A	Industrial Temperature	-40 to 85	°C
	T_A	Military Temperature	-55 to 125	°C

2.3 PRELIMINARY VDD = 3.3V ± 10%, junction temperature range -55 to +125°C.

Table 2.3: DC CHARACTERISTICS AT VDD = 3.3v

Symbol	Parameter	Condition	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage					
	CMOS				$0.3V_{DD}$	V
	CMOS Schmitt Trigger				$0.3V_{DD}$	V
	TTL				0.8	V
	TTL Schmitt Trigger				0.8	V
V_{IH}	Input High Voltage					
	CMOS		$0.7V_{DD}$			V
	CMOS Schmitt Trigger		$0.7V_{DD}$			V
	TTL		2.0			V
	TTL Schmitt Trigger		2.0			V
I_{IH}	Input High Current	$V_{IN}=V_{DD}$	-10		10	μA
	Input with pull-down	$V_{IN}=V_{DD}$	4		100	μA
I_{IL}	Input Low Current	$V_{IN}=V_{SS}$	-10		10	μA
	Input with pull-up	$V_{IN}=V_{SS}$	-100		-4	μA
V_{OH}	Output High Voltage					
	Type B1	I_{OH}= -1mA	2.4			V
	Type B2	I_{OH}= -2mA	2.4			V
	Type B4	I_{OH}= -4mA	2.4			V
	Type B6	I_{OH}= -6mA	2.4			V
	Type B8	I_{OH}= -8mA	2.4			V
	Type B10	I_{OH}= -10mA	2.4			V
	Type B12	I_{OH}= -12mA	2.4			V
V_{OL}	Output Low Voltage					
	Type B1	I_{OH}= 1mA			0.4	V
	Type B2	I_{OH}= 2mA			0.4	V
	Type B4	I_{OH}= 4mA			0.4	V
	Type B6	I_{OH}= 6mA			0.4	V
	Type B8	I_{OH}= 8mA			0.4	V
	Type B10	I_{OH}= 10mA			0.4	V
	Type B12	I_{OH}= 12mA			0.4	V
I_{OZ}	3-State Output Leakage Current	$V_{OH}=V_{SS}$ or V_{DD}	-10		10	μA
I_{DD}	Quiescent Supply Current	$V_{IN}=V_{SS}$ or V_{DD}			80[1]	μA

1. Depends on customer design

2.4 Absolute Maximum Ratings

Table 2.4: Maximum Ratings

	Symbol	Parameter	Rating	Unit
Absolute Maximum Ratings	V_{DD}	DC Supply Voltage	-0.3 to 7.0	V
	V_{IN}	DC Input Voltage	-0.3 to VDD +0.3	V
	I_{IN}	DC Input Current	$\pm$ 10	mA
	T_{STG}	Storage Temperature	-40 to +125	°C
Recommended Operating Conditions	V_{DD}	DC Supply Voltage	3.0 - 3.6V	V
	T_A	Commercial Temperature	0 to 70	°C
	T_A	Industrial Temperature	-40 to 85	°C
	T_A	Military Temperature	-55 to 125	°C

Chapter 3.0 5.0V Process, 3.3V I/O Buffers and Clock Drivers

3.1 Overview

This chapter describes the AC characteristics of 3.3V Input and Output Buffers and Clock Drivers.. The AC characteristics of Bidirectional Buffers can be derived from different combinations of Input and Output Buffers.

As there are over 300 possible combinations of I/O Buffers in the library, naming conventions have been adopted to help designers to memorize and use the cell library more efficiently. Naming conventions are described at the beginning of each sub-section.

3.2 Summary Tables

Table 3.3: 3.3V Input Buffers

Cell Name	Description	Page
PIC/PICU/PICD	CMOS Level Non-Inverting Input Buffers	3-8
PIS/PISU/PISD	CMOS Schmitt Trigger Level Non-Inverting Input Buffers	3-10

Table 3.4: 3.3V Output Buffers

Cell Name	Description	Page
POB(1/2/4/6/8/10/12/16)SM	Non-Inverting Output Buffers with medium slew-rate control.	3-13
POT(1/2/4/6/8/10/12/16)SM	Tristate Non-Inverting Output Buffers with medium slew-rate control.	3-17
POD(1/2/4/6/8/10/12/16)SM	Open Drain Output Buffers with medium slew-rate control.	3-25

Table 3.5: 3.3V Bidirectional Buffers

Cell Name	Description	Page
PBxUTvw	Bidirectional Buffer with Pull-Up, Non-Inverting Input	3-31
PBxDTvw	BdDirectional Buffer with Pull-Down, Non-Inverting Input	3-31
PBxTvw	Bidirectional Buffer with Non-Inverting Input	3-31
PBxUDvw	Bidirectional Open Drain Buffer with Pull-Up, Non-Inverting Input	3-32
PBxDDvw	Bidirectional Open Drain Buffer with Pull-Down, Non-Inverting Input	3-32
PBxDvw	Bidirectional Open Drain Buffer with Non-Inverting Input	3-32

Table 3.6: 3.3V Input Clock Drivers

Cell Name	Description	Page
CK2/4/6/8	Internal Clock Driver CMOS Level	3-35
PSCKDC2/4/6/8	CMOS Level Clock Driver	3-36
PSCKDCD2/4/6/8	CMOS Level Clock Driver with Pull-Down Input	3-38
PSCKDCU2/4/6/8	CMOS Level Clock Driver with Pull-Up Input	3-40
PSCKDS2/4/6/8	CMOS Schmitt Trigger Level Clock Driver	3-42
PSCKDSD2/4/6/8	CMOS Schmitt Trigger Level Clock Driver with Pull-Down Input	3-44
PSCKDSU2/4/6/8	CMOS Schmitt Trigger Level Clock Driver with Pull-Up Input	3-46

3.3 Input Buffers

3V Input Buffer Naming Conventions:

PI x z

where x = C -- CMOS levels
S -- CMOS Schmitt Trigger levels

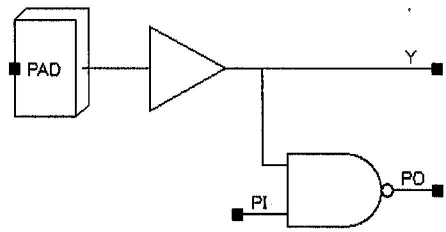
z = (optional)
U -- pull-up resistor
D -- pull-down resistor

e.g. PISD - CMOS Schmitt Trigger input buffer with pull-down

Input: PAD, PI
Output Y, PO

Input Loading (SL): All
- PI: 2.6106

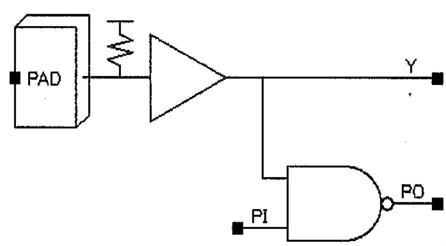
I/O Slots: 1



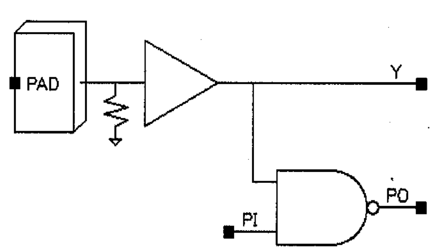
PIC Symbol

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Truth Table



PICU Symbol



PICD Symbol

PIC Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.27	0.21 + 0.031*SL	0.23 + 0.023*SL	0.26 + 0.022*SL
	tPHL	0.08	0.03 + 0.027*SL	0.06 + 0.017*SL	0.14 + 0.013*SL
	tR	0.33	0.25 + 0.044*SL	0.24 + 0.045*SL	0.18 + 0.048*SL
	tF	0.29	0.22 + 0.032*SL	0.25 + 0.023*SL	0.24 + 0.023*SL
PI to PO	tPLH	0.35	0.30 + 0.026*SL	0.31 + 0.022*SL	0.32 + 0.022*SL
	tPHL	0.07	0.02 + 0.022*SL	0.04 + 0.015*SL	0.10 + 0.013*SL
	tR	0.40	0.31 + 0.044*SL	0.31 + 0.045*SL	0.25 + 0.048*SL
	tF	0.27	0.22 + 0.024*SL	0.23 + 0.022*SL	0.20 + 0.024*SL
PAD to Y	tPLH	0.25	0.24 + 0.009*SL	0.24 + 0.008*SL	0.25 + 0.007*SL
	tPHL	0.31	0.29 + 0.009*SL	0.29 + 0.008*SL	0.30 + 0.008*SL
	tR	0.18	0.14 + 0.016*SL	0.15 + 0.015*SL	0.13 + 0.016*SL
	tF	0.15	0.13 + 0.012*SL	0.13 + 0.014*SL	0.12 + 0.014*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

PICU Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.27	0.21 + 0.031*SL	0.23 + 0.023*SL	0.26 + 0.022*SL
	tPHL	0.08	0.03 + 0.027*SL	0.06 + 0.017*SL	0.14 + 0.013*SL
	tR	0.33	0.25 + 0.044*SL	0.24 + 0.045*SL	0.18 + 0.048*SL
	tF	0.29	0.22 + 0.032*SL	0.25 + 0.023*SL	0.24 + 0.023*SL
PI to PO	tPLH	0.35	0.30 + 0.026*SL	0.31 + 0.022*SL	0.32 + 0.022*SL
	tPHL	0.07	0.02 + 0.022*SL	0.04 + 0.015*SL	0.10 + 0.013*SL
	tR	0.40	0.31 + 0.044*SL	0.31 + 0.045*SL	0.25 + 0.048*SL
	tF	0.27	0.22 + 0.024*SL	0.23 + 0.022*SL	0.20 + 0.024*SL
PAD to Y	tPLH	0.26	0.24 + 0.009*SL	0.24 + 0.008*SL	0.25 + 0.007*SL
	tPHL	0.31	0.30 + 0.009*SL	0.30 + 0.008*SL	0.31 + 0.008*SL
	tR	0.17	0.14 + 0.017*SL	0.15 + 0.015*SL	0.13 + 0.016*SL
	tF	0.15	0.13 + 0.014*SL	0.13 + 0.014*SL	0.12 + 0.014*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

PICD Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

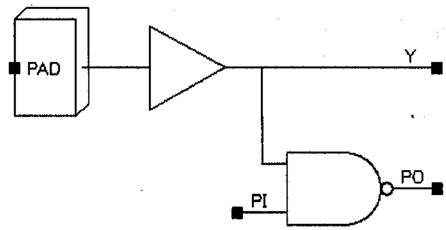
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.27	0.21 + 0.031*SL	0.23 + 0.023*SL	0.26 + 0.022*SL
	tPHL	0.08	0.03 + 0.027*SL	0.06 + 0.017*SL	0.14 + 0.013*SL
	tR	0.33	0.25 + 0.044*SL	0.24 + 0.045*SL	0.18 + 0.048*SL
	tF	0.29	0.22 + 0.032*SL	0.25 + 0.023*SL	0.24 + 0.023*SL
PI to PO	tPLH	0.35	0.30 + 0.026*SL	0.31 + 0.022*SL	0.32 + 0.022*SL
	tPHL	0.07	0.02 + 0.022*SL	0.04 + 0.015*SL	0.10 + 0.013*SL
	tR	0.40	0.31 + 0.044*SL	0.31 + 0.045*SL	0.25 + 0.048*SL
	tF	0.27	0.22 + 0.024*SL	0.23 + 0.022*SL	0.20 + 0.024*SL
PAD to Y	tPLH	0.27	0.25 + 0.009*SL	0.25 + 0.008*SL	0.27 + 0.007*SL
	tPHL	0.32	0.30 + 0.009*SL	0.30 + 0.008*SL	0.31 + 0.008*SL
	tR	0.18	0.14 + 0.021*SL	0.16 + 0.014*SL	0.13 + 0.016*SL
	tF	0.15	0.13 + 0.014*SL	0.13 + 0.014*SL	0.12 + 0.014*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Input: PAD, PI
Output Y, PO

Input Loading (SL): All:
- PI: 2.6106

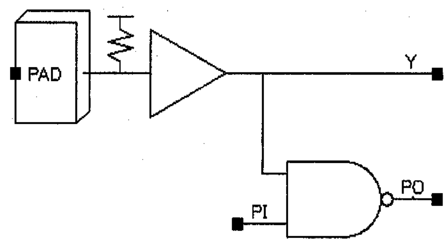
I/O Slots: 1



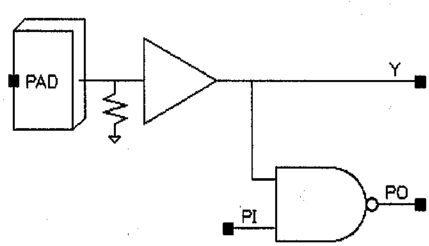
PIS Symbol

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Truth Table



PISU Symbol



PISD Symbol

PIS Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.27	0.21 + 0.031*SL	0.23 + 0.023*SL	0.26 + 0.022*SL
	tPHL	0.08	0.03 + 0.027*SL	0.06 + 0.017*SL	0.14 + 0.013*SL
	tR	0.33	0.25 + 0.044*SL	0.24 + 0.045*SL	0.18 + 0.048*SL
	tF	0.29	0.22 + 0.032*SL	0.25 + 0.023*SL	0.24 + 0.023*SL
PI to PO	tPLH	0.35	0.30 + 0.026*SL	0.31 + 0.022*SL	0.32 + 0.022*SL
	tPHL	0.07	0.02 + 0.022*SL	0.04 + 0.015*SL	0.10 + 0.013*SL
	tR	0.40	0.31 + 0.044*SL	0.31 + 0.045*SL	0.25 + 0.048*SL
	tF	0.27	0.22 + 0.024*SL	0.23 + 0.022*SL	0.20 + 0.024*SL
PAD to Y	tPLH	0.64	0.63 + 0.008*SL	0.63 + 0.006*SL	0.65 + 0.005*SL
	tPHL	1.30	1.28 + 0.009*SL	1.29 + 0.007*SL	1.32 + 0.006*SL
	tR	0.19	0.18 + 0.009*SL	0.17 + 0.010*SL	0.18 + 0.009*SL
	tF	0.28	0.26 + 0.010*SL	0.26 + 0.008*SL	0.28 + 0.007*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

PISU Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.27	0.21 + 0.031*SL	0.23 + 0.023*SL	0.26 + 0.022*SL
	tPHL	0.08	0.03 + 0.027*SL	0.06 + 0.017*SL	0.14 + 0.013*SL
	tR	0.33	0.25 + 0.044*SL	0.24 + 0.045*SL	0.18 + 0.048*SL
	tF	0.29	0.22 + 0.032*SL	0.25 + 0.023*SL	0.24 + 0.023*SL
PI to PO	tPLH	0.35	0.30 + 0.026*SL	0.31 + 0.022*SL	0.32 + 0.022*SL
	tPHL	0.07	0.02 + 0.022*SL	0.04 + 0.015*SL	0.10 + 0.013*SL
	tR	0.40	0.31 + 0.044*SL	0.31 + 0.045*SL	0.25 + 0.048*SL
	tF	0.27	0.22 + 0.024*SL	0.23 + 0.022*SL	0.20 + 0.024*SL
PAD to Y	tPLH	0.65	0.63 + 0.008*SL	0.64 + 0.006*SL	0.66 + 0.005*SL
	tPHL	1.32	1.30 + 0.009*SL	1.30 + 0.007*SL	1.33 + 0.006*SL
	tR	0.19	0.18 + 0.007*SL	0.17 + 0.010*SL	0.18 + 0.009*SL
	tF	0.28	0.26 + 0.009*SL	0.26 + 0.008*SL	0.28 + 0.007*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

PISD Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(SL: Standard Load)**

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.27	0.21 + 0.031*SL	0.23 + 0.023*SL	0.26 + 0.022*SL
	tPHL	0.08	0.03 + 0.027*SL	0.06 + 0.017*SL	0.14 + 0.013*SL
	tR	0.33	0.25 + 0.044*SL	0.24 + 0.045*SL	0.18 + 0.048*SL
	tF	0.29	0.22 + 0.032*SL	0.25 + 0.023*SL	0.24 + 0.023*SL
PI to PO	tPLH	0.35	0.30 + 0.026*SL	0.31 + 0.022*SL	0.32 + 0.022*SL
	tPHL	0.07	0.02 + 0.022*SL	0.04 + 0.015*SL	0.10 + 0.013*SL
	tR	0.40	0.31 + 0.044*SL	0.31 + 0.045*SL	0.25 + 0.048*SL
	tF	0.27	0.22 + 0.024*SL	0.23 + 0.022*SL	0.20 + 0.024*SL
PAD to Y	tPLH	0.65	0.63 + 0.008*SL	0.64 + 0.006*SL	0.66 + 0.005*SL
	tPHL	1.34	1.32 + 0.009*SL	1.32 + 0.007*SL	1.35 + 0.006*SL
	tR	0.19	0.18 + 0.007*SL	0.17 + 0.010*SL	0.18 + 0.009*SL
	tF	0.28	0.26 + 0.009*SL	0.26 + 0.008*SL	0.28 + 0.007*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

3.4 Output Buffers

3.3V Output Buffer Naming Conventions:

PO u v w

where u = B -- Normal non-inverting buffer
T -- Tristate non-inverting buffer
D -- Open-drain output

v = 1 -- 1mA drive
2 -- 2mA drive
4 -- 4mA drive
6 -- 6mA drive
8 -- 8mA drive
10 -- 10mA drive
12 -- 12mA drive
16 -- 16mA drive

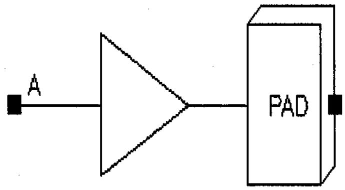
w = (optional)
none -- no slew-rate control
SM -- medium slew-rate control

e.g., POT12SM - 3-state output buffer with 12mA drive and medium slew-rate control

Input: A
Output: PAD

Input Loading (SL): A:
- POB1/2/12/16: 8.7019
- POB4/6/8: 6.3779
- POB10: 7.5312
- POB(4/6/810/12/16)SM: 19.1337

I/O Slots: 1



Symbol

A	PAD
0	0
1	1

Truth Table

POB1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	19.20	1.36 + 0.357*CL	1.36 + 0.357*CL	1.36 + 0.357*CL
	tPHL	12.48	1.12 + 0.227*CL	1.12 + 0.227*CL	1.12 + 0.227*CL
	tR	43.49	2.90 + 0.812*CL	2.90 + 0.812*CL	2.90 + 0.812*CL
	tF	24.65	1.59 + 0.461*CL	1.58 + 0.461*CL	1.58 + 0.461*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	9.76	0.84 + 0.178*CL	0.84 + 0.178*CL	0.84 + 0.178*CL
	tPHL	6.44	0.76 + 0.114*CL	0.76 + 0.114*CL	0.76 + 0.114*CL
	tR	21.76	1.47 + 0.406*CL	1.47 + 0.406*CL	1.47 + 0.406*CL
	tF	12.34	0.81 + 0.231*CL	0.81 + 0.231*CL	0.81 + 0.231*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	5.08	0.62 + 0.089*CL	0.62 + 0.089*CL	0.62 + 0.089*CL
	tPHL	3.51	0.69 + 0.056*CL	0.68 + 0.057*CL	0.68 + 0.057*CL
	tR	10.91	0.76 + 0.203*CL	0.76 + 0.203*CL	0.76 + 0.203*CL
	tF	6.20	0.45 + 0.115*CL	0.43 + 0.115*CL	0.43 + 0.115*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB4SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	5.28	0.82 + 0.089*CL	0.82 + 0.089*CL	0.82 + 0.089*CL
	tPHL	3.84	1.00 + 0.057*CL	1.00 + 0.057*CL	1.00 + 0.057*CL
	tR	10.93	0.79 + 0.203*CL	0.78 + 0.203*CL	0.78 + 0.203*CL
	tF	6.27	0.59 + 0.114*CL	0.54 + 0.115*CL	0.50 + 0.115*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.60	0.63 + 0.059*CL	0.63 + 0.059*CL	0.63 + 0.059*CL
	tPHL	2.63	0.78 + 0.037*CL	0.75 + 0.037*CL	0.74 + 0.038*CL
	tR	7.30	0.54 + 0.135*CL	0.53 + 0.135*CL	0.53 + 0.135*CL
	tF	4.18	0.42 + 0.075*CL	0.37 + 0.076*CL	0.33 + 0.077*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB6SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.93	0.95 + 0.060*CL	0.95 + 0.060*CL	0.95 + 0.060*CL
	tPHL	3.20	1.24 + 0.039*CL	1.29 + 0.038*CL	1.30 + 0.038*CL
	tR	7.36	0.66 + 0.134*CL	0.62 + 0.135*CL	0.59 + 0.135*CL
	tF	4.38	0.69 + 0.074*CL	0.63 + 0.075*CL	0.57 + 0.076*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.91	0.68 + 0.045*CL	0.68 + 0.045*CL	0.68 + 0.045*CL
	tPHL	2.26	0.91 + 0.027*CL	0.88 + 0.028*CL	0.85 + 0.028*CL
	tR	5.50	0.45 + 0.101*CL	0.43 + 0.101*CL	0.43 + 0.101*CL
	tF	3.23	0.49 + 0.055*CL	0.42 + 0.056*CL	0.37 + 0.057*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB8SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.35	1.10 + 0.045*CL	1.11 + 0.045*CL	1.12 + 0.045*CL
	tPHL	3.01	1.43 + 0.032*CL	1.53 + 0.030*CL	1.59 + 0.029*CL
	tR	5.63	0.67 + 0.099*CL	0.61 + 0.100*CL	0.57 + 0.101*CL
	tF	3.54	0.81 + 0.055*CL	0.78 + 0.055*CL	0.73 + 0.056*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB10 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.54	0.75 + 0.036*CL	0.76 + 0.036*CL	0.76 + 0.036*CL
	tPHL	1.98	0.85 + 0.023*CL	0.85 + 0.023*CL	0.85 + 0.023*CL
	tR	4.43	0.41 + 0.080*CL	0.39 + 0.081*CL	0.37 + 0.081*CL
	tF	2.59	0.37 + 0.044*CL	0.33 + 0.045*CL	0.29 + 0.046*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB10SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.90	1.07 + 0.037*CL	1.10 + 0.036*CL	1.11 + 0.036*CL
	tPHL	2.69	1.33 + 0.027*CL	1.45 + 0.025*CL	1.53 + 0.024*CL
	tR	4.60	0.69 + 0.078*CL	0.63 + 0.079*CL	0.58 + 0.080*CL
	tF	3.07	0.91 + 0.043*CL	0.91 + 0.043*CL	0.87 + 0.044*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.33	0.84 + 0.030*CL	0.84 + 0.030*CL	0.84 + 0.030*CL
	tPHL	1.86	0.88 + 0.020*CL	0.90 + 0.019*CL	0.91 + 0.019*CL
	tR	3.74	0.41 + 0.067*CL	0.38 + 0.067*CL	0.36 + 0.067*CL
	tF	2.22	0.36 + 0.037*CL	0.34 + 0.038*CL	0.31 + 0.038*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB12SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.78	1.19 + 0.032*CL	1.26 + 0.030*CL	1.29 + 0.030*CL
	tPHL	2.74	1.47 + 0.025*CL	1.62 + 0.022*CL	1.74 + 0.021*CL
	tR	3.99	0.77 + 0.064*CL	0.72 + 0.065*CL	0.66 + 0.066*CL
	tF	2.85	1.01 + 0.037*CL	1.05 + 0.036*CL	1.04 + 0.036*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB16 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.11	0.97 + 0.023*CL	0.99 + 0.022*CL	0.99 + 0.022*CL
	tPHL	1.78	1.00 + 0.015*CL	1.04 + 0.015*CL	1.06 + 0.014*CL
	tR	2.89	0.42 + 0.049*CL	0.40 + 0.050*CL	0.37 + 0.050*CL
	tF	1.79	0.42 + 0.028*CL	0.40 + 0.028*CL	0.38 + 0.028*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POB16SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

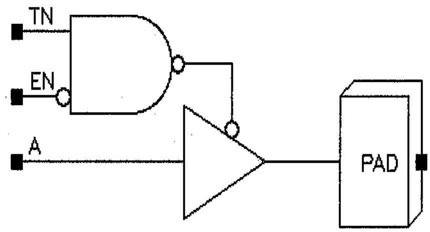
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.73	1.41 + 0.026*CL	1.52 + 0.024*CL	1.60 + 0.023*CL
	tPHL	2.91	1.73 + 0.024*CL	1.92 + 0.020*CL	2.07 + 0.018*CL
	tR	3.31	0.90 + 0.048*CL	0.89 + 0.048*CL	0.86 + 0.049*CL
	tF	2.65	1.14 + 0.030*CL	1.24 + 0.028*CL	1.30 + 0.027*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

Input: TN, EN, A
Output: PAD

Input Loading (SL): All:
- TN: 2.6036
- EN: 2.6036
- A: 3.7743

I/O Slots: 1



Symbol

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

Truth Table

POT1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	19.50	1.67 + 0.357*CL	1.66 + 0.357*CL	1.67 + 0.357*CL
	tPHL	12.77	1.41 + 0.227*CL	1.41 + 0.227*CL	1.41 + 0.227*CL
	tR	43.49	2.90 + 0.812*CL	2.90 + 0.812*CL	2.90 + 0.812*CL
	tF	24.65	1.59 + 0.461*CL	1.58 + 0.461*CL	1.58 + 0.461*CL
EN to PAD	tPLH	19.65	1.81 + 0.357*CL	1.81 + 0.357*CL	1.87 + 0.356*CL
	tPHL	12.99	1.63 + 0.227*CL	1.66 + 0.227*CL	1.63 + 0.227*CL
	tR	43.49	2.90 + 0.812*CL	2.90 + 0.812*CL	2.90 + 0.812*CL
	tF	24.78	1.58 + 0.464*CL	1.78 + 0.460*CL	1.71 + 0.461*CL
	tPLZ	0.64	0.64 + -0.000*CL	0.64 + -0.000*CL	0.64 + -0.000*CL
	tPHZ	0.61	0.61 + -0.000*CL	0.61 + -0.000*CL	0.61 + -0.000*CL
TN to PAD	tPLH	19.41	1.57 + 0.357*CL	1.58 + 0.357*CL	1.63 + 0.356*CL
	tPHL	12.72	1.37 + 0.227*CL	1.38 + 0.227*CL	1.39 + 0.227*CL
	tR	43.49	2.90 + 0.812*CL	2.90 + 0.812*CL	2.90 + 0.812*CL
	tF	24.73	1.76 + 0.459*CL	1.65 + 0.462*CL	1.69 + 0.461*CL
	tPLZ	0.86	0.86 + 0.000*CL	0.86 + 0.000*CL	0.86 + -0.000*CL
	tPHZ	0.84	0.84 + -0.000*CL	0.84 + -0.000*CL	0.84 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	10.05	1.13 + 0.178*CL	1.13 + 0.178*CL	1.13 + 0.178*CL
	tPHL	6.72	1.04 + 0.114*CL	1.04 + 0.114*CL	1.04 + 0.114*CL
	tR	21.76	1.47 + 0.406*CL	1.47 + 0.406*CL	1.47 + 0.406*CL
	tF	12.34	0.81 + 0.231*CL	0.81 + 0.231*CL	0.81 + 0.231*CL
EN to PAD	tPLH	10.20	1.28 + 0.178*CL	1.28 + 0.178*CL	1.28 + 0.178*CL
	tPHL	6.97	1.38 + 0.112*CL	1.33 + 0.113*CL	1.37 + 0.112*CL
	tR	21.76	1.47 + 0.406*CL	1.47 + 0.406*CL	1.47 + 0.406*CL
	tF	12.58	0.75 + 0.237*CL	1.29 + 0.226*CL	0.87 + 0.231*CL
	tPLZ	0.69	0.69 + -0.000*CL	0.69 + -0.000*CL	0.69 + -0.000*CL
	tPHZ	0.68	0.68 + -0.000*CL	0.68 + -0.000*CL	0.68 + -0.000*CL
TN to PAD	tPLH	9.96	1.04 + 0.178*CL	1.04 + 0.178*CL	1.04 + 0.178*CL
	tPHL	6.70	1.06 + 0.113*CL	1.07 + 0.113*CL	1.07 + 0.113*CL
	tR	21.76	1.47 + 0.406*CL	1.47 + 0.406*CL	1.47 + 0.406*CL
	tF	12.55	0.87 + 0.234*CL	1.15 + 0.228*CL	1.20 + 0.227*CL
	tPLZ	0.94	0.94 + 0.000*CL	0.94 + 0.000*CL	0.94 + -0.000*CL
	tPHZ	0.90	0.90 + -0.000*CL	0.90 + -0.000*CL	0.90 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	5.33	0.86 + 0.089*CL	0.86 + 0.089*CL	0.87 + 0.089*CL
	tPHL	3.78	0.95 + 0.057*CL	0.94 + 0.057*CL	0.94 + 0.057*CL
	tR	10.91	0.76 + 0.203*CL	0.76 + 0.203*CL	0.76 + 0.203*CL
	tF	6.20	0.45 + 0.115*CL	0.43 + 0.115*CL	0.43 + 0.115*CL
EN to PAD	tPLH	5.47	1.01 + 0.089*CL	1.01 + 0.089*CL	1.01 + 0.089*CL
	tPHL	4.02	1.10 + 0.058*CL	1.15 + 0.057*CL	1.27 + 0.056*CL
	tR	10.91	0.76 + 0.203*CL	0.76 + 0.203*CL	0.76 + 0.203*CL
	tF	6.37	1.44 + 0.099*CL	0.46 + 0.118*CL	1.18 + 0.109*CL
	tPLZ	0.84	0.84 + 0.000*CL	0.84 + 0.000*CL	0.84 + 0.000*CL
	tPHZ	1.62	1.62 + -0.000*CL	1.62 + -0.000*CL	1.62 + 0.000*CL
TN to PAD	tPLH	5.23	0.77 + 0.089*CL	0.77 + 0.089*CL	0.77 + 0.089*CL
	tPHL	3.77	0.80 + 0.060*CL	1.04 + 0.055*CL	0.71 + 0.059*CL
	tR	10.91	0.76 + 0.203*CL	0.76 + 0.203*CL	0.76 + 0.203*CL
	tF	6.67	0.60 + 0.121*CL	1.35 + 0.106*CL	0.40 + 0.118*CL
	tPLZ	1.04	1.04 + 0.000*CL	1.04 + 0.000*CL	1.04 + 0.000*CL
	tPHZ	1.75	1.75 + -0.000*CL	1.75 + 0.000*CL	1.76 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT4SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	5.64	1.18 + 0.089*CL	1.18 + 0.089*CL	1.18 + 0.089*CL
	tPHL	4.18	1.33 + 0.057*CL	1.34 + 0.057*CL	1.34 + 0.057*CL
	tR	10.93	0.79 + 0.203*CL	0.78 + 0.203*CL	0.78 + 0.203*CL
	tF	6.26	0.59 + 0.114*CL	0.53 + 0.115*CL	0.50 + 0.115*CL
EN to PAD	tPLH	5.77	1.30 + 0.089*CL	1.31 + 0.089*CL	1.31 + 0.089*CL
	tPHL	4.42	1.62 + 0.056*CL	1.56 + 0.057*CL	1.54 + 0.058*CL
	tR	10.93	0.79 + 0.203*CL	0.78 + 0.203*CL	0.78 + 0.203*CL
	tF	6.59	0.56 + 0.121*CL	1.18 + 0.108*CL	0.47 + 0.117*CL
	tPLZ	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + -0.000*CL
	tPHZ	0.72	0.72 + 0.000*CL	0.72 + 0.000*CL	0.72 + -0.000*CL
TN to PAD	tPLH	5.54	1.08 + 0.089*CL	1.08 + 0.089*CL	1.08 + 0.089*CL
	tPHL	4.16	1.27 + 0.058*CL	1.35 + 0.056*CL	1.22 + 0.058*CL
	tR	10.93	0.79 + 0.203*CL	0.78 + 0.203*CL	0.78 + 0.203*CL
	tF	6.78	0.86 + 0.118*CL	1.50 + 0.106*CL	0.60 + 0.117*CL
	tPLZ	0.99	0.99 + 0.000*CL	0.99 + -0.000*CL	0.99 + 0.000*CL
	tPHZ	0.95	0.95 + 0.000*CL	0.95 + 0.000*CL	0.95 + 0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.83	0.86 + 0.060*CL	0.86 + 0.059*CL	0.86 + 0.059*CL
	tPHL	2.88	1.03 + 0.037*CL	1.01 + 0.037*CL	1.00 + 0.038*CL
	tR	7.30	0.54 + 0.135*CL	0.53 + 0.135*CL	0.53 + 0.135*CL
	tF	4.18	0.42 + 0.075*CL	0.37 + 0.076*CL	0.33 + 0.077*CL
EN to PAD	tPLH	3.98	1.00 + 0.060*CL	1.00 + 0.059*CL	1.00 + 0.059*CL
	tPHL	3.06	1.15 + 0.038*CL	1.06 + 0.040*CL	1.37 + 0.036*CL
	tR	7.30	0.54 + 0.135*CL	0.53 + 0.135*CL	0.53 + 0.135*CL
	tF	4.29	1.29 + 0.060*CL	0.29 + 0.080*CL	-0.17 + 0.086*CL
	tPLZ	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL
	tPHZ	1.97	1.97 + -0.000*CL	1.97 + -0.000*CL	1.97 + -0.000*CL
TN to PAD	tPLH	3.74	0.76 + 0.060*CL	0.76 + 0.059*CL	0.76 + 0.059*CL
	tPHL	2.79	0.89 + 0.038*CL	0.77 + 0.040*CL	1.09 + 0.036*CL
	tR	7.30	0.54 + 0.135*CL	0.53 + 0.135*CL	0.53 + 0.135*CL
	tF	4.38	1.26 + 0.062*CL	0.29 + 0.082*CL	0.79 + 0.076*CL
	tPLZ	1.17	1.17 + 0.000*CL	1.17 + -0.000*CL	1.17 + -0.000*CL
	tPHZ	2.27	2.31 + -0.001*CL	2.27 + 0.000*CL	2.27 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT6SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	4.31	1.32 + 0.060*CL	1.33 + 0.060*CL	1.33 + 0.060*CL
	tPHL	3.51	1.56 + 0.039*CL	1.60 + 0.038*CL	1.62 + 0.038*CL
	tR	7.36	0.66 + 0.134*CL	0.62 + 0.135*CL	0.59 + 0.135*CL
	tF	4.38	0.68 + 0.074*CL	0.62 + 0.075*CL	0.57 + 0.076*CL
EN to PAD	tPLH	4.43	1.45 + 0.060*CL	1.46 + 0.060*CL	1.46 + 0.060*CL
	tPHL	3.81	1.88 + 0.038*CL	1.82 + 0.040*CL	2.07 + 0.037*CL
	tR	7.36	0.66 + 0.134*CL	0.62 + 0.135*CL	0.59 + 0.135*CL
	tF	4.72	1.44 + 0.066*CL	0.76 + 0.079*CL	2.20 + 0.061*CL
	tPLZ	0.70	0.70 + -0.000*CL	0.70 + 0.000*CL	0.70 + -0.000*CL
	tPHZ	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.68 + -0.000*CL
TN to PAD	tPLH	4.21	1.22 + 0.060*CL	1.23 + 0.060*CL	1.23 + 0.060*CL
	tPHL	3.55	1.46 + 0.042*CL	1.65 + 0.038*CL	1.91 + 0.035*CL
	tR	7.36	0.66 + 0.134*CL	0.62 + 0.135*CL	0.59 + 0.135*CL
	tF	4.74	1.78 + 0.059*CL	1.24 + 0.070*CL	0.22 + 0.083*CL
	tPLZ	0.95	0.95 + -0.000*CL	0.95 + -0.000*CL	0.95 + -0.000*CL
	tPHZ	0.91	0.91 + -0.000*CL	0.91 + 0.000*CL	0.91 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.13	0.90 + 0.045*CL	0.90 + 0.045*CL	0.90 + 0.045*CL
	tPHL	2.51	1.17 + 0.027*CL	1.13 + 0.028*CL	1.11 + 0.028*CL
	tR	5.50	0.44 + 0.101*CL	0.43 + 0.101*CL	0.43 + 0.101*CL
	tF	3.23	0.49 + 0.055*CL	0.42 + 0.056*CL	0.37 + 0.057*CL
EN to PAD	tPLH	3.27	1.04 + 0.045*CL	1.04 + 0.045*CL	1.04 + 0.045*CL
	tPHL	2.65	1.25 + 0.028*CL	1.16 + 0.030*CL	1.24 + 0.029*CL
	tR	5.50	0.44 + 0.101*CL	0.43 + 0.101*CL	0.43 + 0.101*CL
	tF	3.49	0.29 + 0.064*CL	0.29 + 0.064*CL	1.90 + 0.044*CL
	tPLZ	1.06	1.06 + -0.000*CL	1.06 + 0.000*CL	1.06 + -0.000*CL
	tPHZ	2.50	2.50 + 0.000*CL	2.50 + 0.000*CL	2.50 + 0.000*CL
TN to PAD	tPLH	3.03	0.80 + 0.045*CL	0.80 + 0.045*CL	0.80 + 0.045*CL
	tPHL	2.40	0.86 + 0.031*CL	1.04 + 0.027*CL	0.60 + 0.033*CL
	tR	5.50	0.44 + 0.101*CL	0.43 + 0.101*CL	0.43 + 0.101*CL
	tF	3.72	-0.23 + 0.079*CL	1.15 + 0.051*CL	0.26 + 0.063*CL
	tPLZ	1.30	1.30 + 0.000*CL	1.30 + 0.000*CL	1.30 + -0.000*CL
	tPHZ	2.68	2.68 + -0.000*CL	2.68 + -0.000*CL	2.68 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT8SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.73	1.47 + 0.045*CL	1.49 + 0.045*CL	1.50 + 0.045*CL
	tPHL	3.33	1.75 + 0.032*CL	1.85 + 0.030*CL	1.90 + 0.029*CL
	tR	5.63	0.67 + 0.099*CL	0.62 + 0.100*CL	0.57 + 0.101*CL
	tF	3.54	0.80 + 0.055*CL	0.78 + 0.055*CL	0.73 + 0.056*CL
EN to PAD	tPLH	3.86	1.60 + 0.045*CL	1.62 + 0.045*CL	1.62 + 0.045*CL
	tPHL	3.62	1.98 + 0.033*CL	2.20 + 0.028*CL	1.86 + 0.033*CL
	tR	5.63	0.67 + 0.099*CL	0.62 + 0.100*CL	0.57 + 0.101*CL
	tF	3.89	1.51 + 0.047*CL	1.45 + 0.049*CL	-0.96 + 0.079*CL
	tPLZ	0.70	0.70 + 0.000*CL	0.70 + 0.000*CL	0.70 + -0.000*CL
	tPHZ	0.68	0.68 + 0.000*CL	0.68 + -0.000*CL	0.68 + 0.000*CL
TN to PAD	tPLH	3.63	1.37 + 0.045*CL	1.39 + 0.045*CL	1.40 + 0.045*CL
	tPHL	3.29	1.78 + 0.030*CL	1.81 + 0.030*CL	1.83 + 0.029*CL
	tR	5.63	0.67 + 0.099*CL	0.62 + 0.100*CL	0.57 + 0.101*CL
	tF	3.81	2.41 + 0.028*CL	1.41 + 0.048*CL	-1.11 + 0.080*CL
	tPLZ	0.95	0.95 + 0.000*CL	0.95 + -0.000*CL	0.95 + -0.000*CL
	tPHZ	0.91	0.91 + -0.000*CL	0.91 + -0.000*CL	0.91 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT10 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.78	0.99 + 0.036*CL	1.00 + 0.036*CL	1.00 + 0.036*CL
	tPHL	2.24	1.11 + 0.023*CL	1.11 + 0.023*CL	1.10 + 0.023*CL
	tR	4.43	0.41 + 0.080*CL	0.39 + 0.081*CL	0.37 + 0.081*CL
	tF	2.59	0.37 + 0.044*CL	0.33 + 0.045*CL	0.29 + 0.046*CL
EN to PAD	tPLH	2.92	1.13 + 0.036*CL	1.13 + 0.036*CL	1.14 + 0.036*CL
	tPHL	2.43	1.28 + 0.023*CL	1.28 + 0.023*CL	1.23 + 0.024*CL
	tR	4.43	0.41 + 0.080*CL	0.39 + 0.081*CL	0.37 + 0.081*CL
	tF	2.91	0.32 + 0.052*CL	0.88 + 0.041*CL	-0.53 + 0.058*CL
	tPLZ	1.16	1.16 + -0.000*CL	1.16 + 0.000*CL	1.16 + -0.000*CL
	tPHZ	1.77	1.77 + -0.000*CL	1.77 + -0.000*CL	1.77 + -0.000*CL
TN to PAD	tPLH	2.69	0.89 + 0.036*CL	0.90 + 0.036*CL	0.90 + 0.036*CL
	tPHL	2.16	1.00 + 0.023*CL	1.00 + 0.023*CL	1.10 + 0.022*CL
	tR	4.43	0.41 + 0.080*CL	0.39 + 0.081*CL	0.37 + 0.081*CL
	tF	2.71	0.69 + 0.040*CL	0.01 + 0.054*CL	1.52 + 0.035*CL
	tPLZ	1.37	1.37 + 0.000*CL	1.37 + -0.000*CL	1.37 + 0.000*CL
	tPHZ	1.97	1.97 + -0.000*CL	1.97 + 0.000*CL	1.97 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT10SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.25	1.42 + 0.037*CL	1.46 + 0.036*CL	1.47 + 0.036*CL
	tPHL	3.03	1.67 + 0.027*CL	1.79 + 0.025*CL	1.87 + 0.024*CL
	tR	4.60	0.70 + 0.078*CL	0.63 + 0.079*CL	0.58 + 0.080*CL
	tF	3.07	0.90 + 0.043*CL	0.90 + 0.043*CL	0.86 + 0.044*CL
EN to PAD	tPLH	3.38	1.54 + 0.037*CL	1.58 + 0.036*CL	1.59 + 0.036*CL
	tPHL	3.27	1.84 + 0.028*CL	1.87 + 0.028*CL	2.28 + 0.023*CL
	tR	4.60	0.70 + 0.078*CL	0.63 + 0.079*CL	0.58 + 0.080*CL
	tF	3.51	2.13 + 0.028*CL	1.29 + 0.044*CL	1.40 + 0.043*CL
	tPLZ	0.84	0.84 + -0.000*CL	0.84 + -0.000*CL	0.84 + -0.000*CL
	tPHZ	0.84	0.84 + -0.000*CL	0.84 + -0.000*CL	0.84 + -0.000*CL
TN to PAD	tPLH	3.15	1.32 + 0.037*CL	1.35 + 0.036*CL	1.37 + 0.036*CL
	tPHL	2.98	1.67 + 0.026*CL	1.49 + 0.030*CL	1.97 + 0.024*CL
	tR	4.61	0.70 + 0.078*CL	0.63 + 0.079*CL	0.58 + 0.080*CL
	tF	3.74	1.76 + 0.039*CL	1.64 + 0.042*CL	2.04 + 0.037*CL
	tPLZ	1.05	1.05 + -0.000*CL	1.05 + -0.000*CL	1.05 + -0.000*CL
	tPHZ	1.08	1.08 + 0.000*CL	1.08 + -0.000*CL	1.08 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.59	1.09 + 0.030*CL	1.10 + 0.030*CL	1.10 + 0.030*CL
	tPHL	2.11	1.14 + 0.019*CL	1.16 + 0.019*CL	1.16 + 0.019*CL
	tR	3.74	0.41 + 0.067*CL	0.38 + 0.067*CL	0.36 + 0.067*CL
	tF	2.22	0.36 + 0.037*CL	0.33 + 0.038*CL	0.31 + 0.038*CL
EN to PAD	tPLH	2.73	1.22 + 0.030*CL	1.23 + 0.030*CL	1.24 + 0.030*CL
	tPHL	2.36	1.34 + 0.020*CL	1.43 + 0.018*CL	1.21 + 0.021*CL
	tR	3.74	0.41 + 0.066*CL	0.38 + 0.067*CL	0.36 + 0.067*CL
	tF	2.38	0.57 + 0.036*CL	0.41 + 0.039*CL	0.06 + 0.044*CL
	tPLZ	1.31	1.31 + 0.000*CL	1.31 + 0.000*CL	1.31 + 0.000*CL
	tPHZ	1.55	1.55 + -0.000*CL	1.55 + -0.000*CL	1.55 + -0.000*CL
TN to PAD	tPLH	2.50	0.99 + 0.030*CL	1.00 + 0.030*CL	1.01 + 0.030*CL
	tPHL	2.04	1.07 + 0.019*CL	1.07 + 0.020*CL	1.09 + 0.019*CL
	tR	3.74	0.41 + 0.066*CL	0.38 + 0.067*CL	0.36 + 0.067*CL
	tF	2.38	0.48 + 0.038*CL	-0.10 + 0.050*CL	1.72 + 0.027*CL
	tPLZ	1.59	1.59 + 0.000*CL	1.59 + 0.000*CL	1.59 + 0.000*CL
	tPHZ	1.78	1.78 + -0.000*CL	1.78 + -0.000*CL	1.78 + 0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT12SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.13	1.54 + 0.032*CL	1.61 + 0.030*CL	1.64 + 0.030*CL
	tPHL	3.08	1.81 + 0.025*CL	1.96 + 0.022*CL	2.08 + 0.021*CL
	tR	3.99	0.78 + 0.064*CL	0.72 + 0.065*CL	0.67 + 0.066*CL
	tF	2.85	1.00 + 0.037*CL	1.04 + 0.036*CL	1.04 + 0.036*CL
EN to PAD	tPLH	3.25	1.66 + 0.032*CL	1.73 + 0.030*CL	1.76 + 0.030*CL
	tPHL	3.37	1.79 + 0.032*CL	2.19 + 0.024*CL	2.41 + 0.021*CL
	tR	4.00	0.79 + 0.064*CL	0.73 + 0.065*CL	0.67 + 0.066*CL
	tF	3.49	1.94 + 0.031*CL	1.44 + 0.041*CL	2.26 + 0.031*CL
	tPLZ	0.84	0.84 + -0.000*CL	0.84 + -0.000*CL	0.84 + -0.000*CL
	tPHZ	0.83	0.83 + -0.000*CL	0.83 + -0.000*CL	0.83 + -0.000*CL
TN to PAD	tPLH	3.03	1.43 + 0.032*CL	1.50 + 0.030*CL	1.54 + 0.030*CL
	tPHL	3.00	1.75 + 0.025*CL	1.61 + 0.028*CL	2.06 + 0.022*CL
	tR	4.00	0.79 + 0.064*CL	0.73 + 0.065*CL	0.67 + 0.066*CL
	tF	3.64	2.18 + 0.029*CL	2.24 + 0.028*CL	0.95 + 0.044*CL
	tPLZ	1.05	1.05 + -0.000*CL	1.05 + -0.000*CL	1.05 + -0.000*CL
	tPHZ	1.08	1.08 + 0.000*CL	1.08 + 0.000*CL	1.08 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT16 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.36	1.22 + 0.023*CL	1.24 + 0.022*CL	1.25 + 0.022*CL
	tPHL	2.03	1.26 + 0.015*CL	1.30 + 0.015*CL	1.32 + 0.014*CL
	tR	2.90	0.43 + 0.049*CL	0.40 + 0.050*CL	0.38 + 0.050*CL
	tF	1.79	0.42 + 0.027*CL	0.41 + 0.028*CL	0.38 + 0.028*CL
EN to PAD	tPLH	2.50	1.35 + 0.023*CL	1.37 + 0.023*CL	1.38 + 0.022*CL
	tPHL	2.28	1.40 + 0.018*CL	1.58 + 0.014*CL	1.47 + 0.016*CL
	tR	2.90	0.44 + 0.049*CL	0.41 + 0.050*CL	0.38 + 0.050*CL
	tF	2.28	0.39 + 0.038*CL	1.12 + 0.023*CL	1.06 + 0.024*CL
	tPLZ	1.51	1.51 + 0.000*CL	1.51 + 0.000*CL	1.51 + 0.000*CL
	tPHZ	1.81	2.00 + -0.004*CL	1.81 + -0.000*CL	1.81 + -0.000*CL
TN to PAD	tPLH	2.27	1.11 + 0.023*CL	1.14 + 0.023*CL	1.15 + 0.022*CL
	tPHL	1.99	1.09 + 0.018*CL	1.21 + 0.016*CL	1.40 + 0.013*CL
	tR	2.90	0.45 + 0.049*CL	0.41 + 0.050*CL	0.38 + 0.050*CL
	tF	1.95	1.12 + 0.017*CL	-0.09 + 0.041*CL	1.07 + 0.026*CL
	tPLZ	1.78	1.78 + 0.000*CL	1.78 + 0.000*CL	1.78 + 0.000*CL
	tPHZ	2.06	2.06 + -0.000*CL	2.06 + -0.000*CL	2.06 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POT16SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

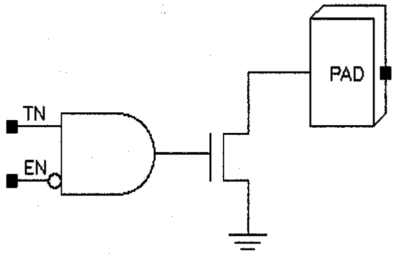
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.08	1.75 + 0.027*CL	1.87 + 0.024*CL	1.95 + 0.023*CL
	tPHL	3.26	2.08 + 0.024*CL	2.26 + 0.020*CL	2.42 + 0.018*CL
	tR	3.32	0.92 + 0.048*CL	0.91 + 0.048*CL	0.87 + 0.049*CL
	tF	2.64	1.14 + 0.030*CL	1.23 + 0.028*CL	1.29 + 0.027*CL
EN to PAD	tPLH	3.20	1.85 + 0.027*CL	1.98 + 0.024*CL	2.06 + 0.023*CL
	tPHL	3.47	1.91 + 0.031*CL	2.32 + 0.023*CL	2.82 + 0.017*CL
	tR	3.33	0.96 + 0.047*CL	0.93 + 0.048*CL	0.88 + 0.049*CL
	tF	3.43	1.68 + 0.035*CL	1.64 + 0.036*CL	2.52 + 0.025*CL
	tPLZ	0.84	0.84 + -0.000*CL	0.84 + -0.000*CL	0.84 + -0.000*CL
	tPHZ	0.83	0.83 + -0.000*CL	0.83 + -0.000*CL	0.83 + -0.000*CL
TN to PAD	tPLH	2.97	1.63 + 0.027*CL	1.75 + 0.024*CL	1.84 + 0.023*CL
	tPHL	3.12	1.84 + 0.026*CL	1.79 + 0.027*CL	2.37 + 0.019*CL
	tR	3.33	0.96 + 0.047*CL	0.93 + 0.048*CL	0.88 + 0.049*CL
	tF	3.64	1.14 + 0.050*CL	2.59 + 0.021*CL	1.39 + 0.036*CL
	tPLZ	1.05	1.05 + -0.000*CL	1.05 + 0.000*CL	1.05 + -0.000*CL
	tPHZ	1.08	1.08 + -0.000*CL	1.08 + -0.000*CL	1.08 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

Input: TN, EN
Output: PAD

Input Loading (SL): All:
- TN: 2.6036
- EN: 2.6036

I/O Slots: 1



Symbol

EN	TN	PAD
0	1	0
x	0	Hi-Z
1	x	Hi-Z

Truth Table

POD1 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	12.87	1.50 + 0.227*CL	1.50 + 0.227*CL	1.51 + 0.227*CL
	tF	24.65	1.59 + 0.461*CL	1.58 + 0.461*CL	1.58 + 0.461*CL
	tPLZ	0.47	0.47 + -0.000*CL	0.47 + -0.000*CL	0.47 + -0.000*CL
TN to PAD	tPHL	12.59	1.23 + 0.227*CL	1.23 + 0.227*CL	1.23 + 0.227*CL
	tF	24.65	1.59 + 0.461*CL	1.58 + 0.461*CL	1.58 + 0.461*CL
	tPLZ	0.69	0.69 + -0.000*CL	0.69 + -0.000*CL	0.69 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

POD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	6.81	1.13 + 0.114*CL	1.13 + 0.114*CL	1.13 + 0.114*CL
	tF	12.34	0.81 + 0.231*CL	0.81 + 0.231*CL	0.81 + 0.231*CL
	tPLZ	0.52	0.52 + -0.000*CL	0.52 + -0.000*CL	0.52 + -0.000*CL
TN to PAD	tPHL	6.54	0.85 + 0.114*CL	0.85 + 0.114*CL	0.85 + 0.114*CL
	tF	12.34	0.81 + 0.231*CL	0.81 + 0.231*CL	0.81 + 0.231*CL
	tPLZ	0.74	0.74 + -0.000*CL	0.74 + -0.000*CL	0.74 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

POD4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	3.85	1.01 + 0.057*CL	1.01 + 0.057*CL	1.01 + 0.057*CL
	tF	6.20	0.43 + 0.115*CL	0.43 + 0.115*CL	0.43 + 0.115*CL
	tPLZ	0.62	0.62 + -0.000*CL	0.62 + -0.000*CL	0.62 + -0.000*CL
TN to PAD	tPHL	3.58	0.74 + 0.057*CL	0.74 + 0.057*CL	0.74 + 0.057*CL
	tF	6.20	0.43 + 0.115*CL	0.43 + 0.115*CL	0.43 + 0.115*CL
	tPLZ	0.85	0.85 + -0.000*CL	0.85 + -0.000*CL	0.85 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

POD4SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	4.34	1.49 + 0.057*CL	1.50 + 0.057*CL	1.50 + 0.057*CL
	tF	6.27	0.60 + 0.113*CL	0.54 + 0.115*CL	0.51 + 0.115*CL
	tPLZ	0.55	0.55 + -0.000*CL	0.55 + -0.000*CL	0.55 + -0.000*CL
TN to PAD	tPHL	4.08	1.23 + 0.057*CL	1.23 + 0.057*CL	1.23 + 0.057*CL
	tF	6.27	0.60 + 0.113*CL	0.54 + 0.115*CL	0.51 + 0.115*CL
	tPLZ	0.76	0.76 + -0.000*CL	0.76 + -0.000*CL	0.76 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

POD6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.93	1.03 + 0.038*CL	1.04 + 0.038*CL	1.04 + 0.038*CL
	tF	4.16	0.34 + 0.076*CL	0.32 + 0.077*CL	0.32 + 0.077*CL
	tPLZ	0.73	0.73 + -0.000*CL	0.73 + -0.000*CL	0.73 + 0.000*CL
TN to PAD	tPHL	2.66	0.76 + 0.038*CL	0.76 + 0.038*CL	0.76 + 0.038*CL
	tF	4.16	0.34 + 0.076*CL	0.33 + 0.077*CL	0.32 + 0.077*CL
	tPLZ	0.95	0.95 + -0.000*CL	0.95 + -0.000*CL	0.95 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

POD6SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	3.70	1.74 + 0.039*CL	1.78 + 0.038*CL	1.80 + 0.038*CL
	tF	4.39	0.73 + 0.073*CL	0.65 + 0.075*CL	0.59 + 0.076*CL
	tPLZ	0.55	0.55 + -0.000*CL	0.55 + -0.000*CL	0.55 + -0.000*CL
TN to PAD	tPHL	3.43	1.47 + 0.039*CL	1.51 + 0.038*CL	1.53 + 0.038*CL
	tF	4.39	0.72 + 0.073*CL	0.65 + 0.075*CL	0.59 + 0.076*CL
	tPLZ	0.76	0.76 + -0.000*CL	0.76 + -0.000*CL	0.76 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.52	1.09 + 0.029*CL	1.09 + 0.028*CL	1.10 + 0.028*CL
	tF	3.17	0.33 + 0.057*CL	0.30 + 0.057*CL	0.29 + 0.057*CL
	tPLZ	0.83	0.83 + -0.000*CL	0.83 + -0.000*CL	0.83 + -0.000*CL
TN to PAD	tPHL	2.24	0.82 + 0.029*CL	0.82 + 0.028*CL	0.82 + 0.028*CL
	tF	3.17	0.33 + 0.057*CL	0.30 + 0.057*CL	0.29 + 0.057*CL
	tPLZ	1.06	1.06 + -0.000*CL	1.06 + -0.000*CL	1.06 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD8SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	3.52	1.93 + 0.032*CL	2.03 + 0.030*CL	2.09 + 0.029*CL
	tF	3.57	0.88 + 0.054*CL	0.82 + 0.055*CL	0.76 + 0.056*CL
	tPLZ	0.55	0.55 + -0.000*CL	0.55 + -0.000*CL	0.55 + -0.000*CL
TN to PAD	tPHL	3.25	1.66 + 0.032*CL	1.76 + 0.030*CL	1.82 + 0.029*CL
	tF	3.57	0.88 + 0.054*CL	0.82 + 0.055*CL	0.76 + 0.056*CL
	tPLZ	0.76	0.76 + -0.000*CL	0.76 + -0.000*CL	0.76 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD10 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.30	1.15 + 0.023*CL	1.16 + 0.023*CL	1.17 + 0.023*CL
	tF	2.59	0.34 + 0.045*CL	0.32 + 0.045*CL	0.29 + 0.046*CL
	tPLZ	0.94	0.94 + -0.000*CL	0.94 + -0.000*CL	0.94 + -0.000*CL
TN to PAD	tPHL	2.03	0.87 + 0.023*CL	0.89 + 0.023*CL	0.89 + 0.023*CL
	tF	2.59	0.35 + 0.045*CL	0.32 + 0.045*CL	0.29 + 0.046*CL
	tPLZ	1.16	1.16 + -0.000*CL	1.16 + -0.000*CL	1.16 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD10SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	3.19	1.80 + 0.028*CL	1.94 + 0.025*CL	2.04 + 0.024*CL
	tF	3.11	1.03 + 0.042*CL	0.97 + 0.043*CL	0.91 + 0.044*CL
	tPLZ	0.61	0.61 + -0.000*CL	0.61 + -0.000*CL	0.61 + -0.000*CL
TN to PAD	tPHL	2.93	1.53 + 0.028*CL	1.67 + 0.025*CL	1.77 + 0.024*CL
	tF	3.11	1.03 + 0.042*CL	0.97 + 0.043*CL	0.91 + 0.044*CL
	tPLZ	0.83	0.83 + 0.000*CL	0.83 + -0.000*CL	0.83 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD12 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.19	1.20 + 0.020*CL	1.23 + 0.019*CL	1.24 + 0.019*CL
	tF	2.22	0.37 + 0.037*CL	0.35 + 0.038*CL	0.32 + 0.038*CL
	tPLZ	1.04	1.04 + -0.000*CL	1.04 + -0.000*CL	1.04 + -0.000*CL
TN to PAD	tPHL	1.92	0.93 + 0.020*CL	0.96 + 0.019*CL	0.97 + 0.019*CL
	tF	2.22	0.37 + 0.037*CL	0.35 + 0.038*CL	0.32 + 0.038*CL
	tPLZ	1.26	1.26 + -0.000*CL	1.26 + -0.000*CL	1.26 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD12SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	3.24	1.92 + 0.026*CL	2.10 + 0.023*CL	2.23 + 0.021*CL
	tF	2.92	1.20 + 0.034*CL	1.16 + 0.035*CL	1.12 + 0.036*CL
	tPLZ	0.61	0.61 + -0.000*CL	0.61 + -0.000*CL	0.61 + -0.000*CL
TN to PAD	tPHL	2.97	1.65 + 0.026*CL	1.83 + 0.023*CL	1.96 + 0.021*CL
	tF	2.92	1.20 + 0.034*CL	1.16 + 0.035*CL	1.12 + 0.036*CL
	tPLZ	0.83	0.83 + -0.000*CL	0.83 + -0.000*CL	0.83 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD16 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.10	1.30 + 0.016*CL	1.35 + 0.015*CL	1.38 + 0.015*CL
	tF	1.80	0.42 + 0.028*CL	0.41 + 0.028*CL	0.40 + 0.028*CL
	tPLZ	1.25	1.25 + -0.000*CL	1.25 + -0.000*CL	1.25 + -0.000*CL
TN to PAD	tPHL	1.82	1.02 + 0.016*CL	1.08 + 0.015*CL	1.11 + 0.015*CL
	tF	1.80	0.42 + 0.028*CL	0.42 + 0.028*CL	0.40 + 0.028*CL
	tPLZ	1.47	1.47 + -0.000*CL	1.47 + -0.000*CL	1.47 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

POD16SM Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	3.38	2.10 + 0.026*CL	2.35 + 0.021*CL	2.54 + 0.018*CL
	tF	2.79	1.51 + 0.026*CL	1.49 + 0.026*CL	1.46 + 0.026*CL
	tPLZ	0.61	0.61 + -0.000*CL	0.61 + -0.000*CL	0.61 + -0.000*CL
TN to PAD	tPHL	3.11	1.84 + 0.026*CL	2.08 + 0.021*CL	2.27 + 0.018*CL
	tF	2.79	1.51 + 0.026*CL	1.49 + 0.026*CL	1.46 + 0.026*CL
	tPLZ	0.83	0.83 + -0.000*CL	0.83 + -0.000*CL	0.83 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

3.5 Bidirectional I/O Buffers

3.3V Bidirectional Buffer Naming Conventions:

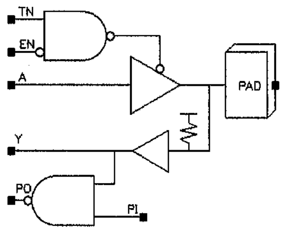
P B xz u v w

where x, and z define the input buffer characteristics, and u, v, and w define the output buffer characteristics, as described previously.

e.g. PBSIUT16SM - Schmitt Trigger input buffer and tristate output buffer with 16mA drive and medium slew-rate control

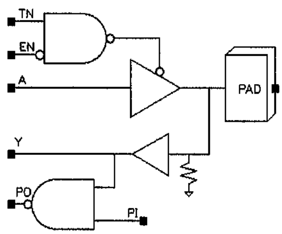
x v w

Pull-up



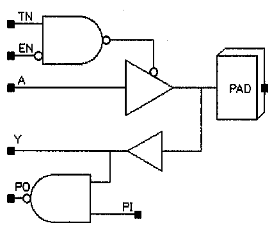
PBxUTvw

Bidirectional Tristate Buffer with Pull-Up, Non-Inverting Input



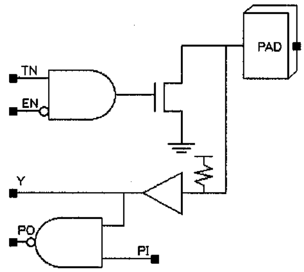
PBxDTvw

Bidirectional Tristate Buffer with Pull-Down, Non-Inverting Input



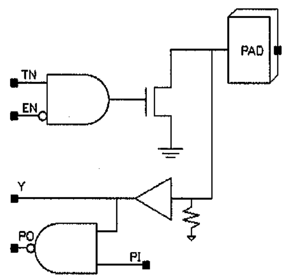
PBxTvw

Bidirectional Tristate Buffer with Non-Inverting Input



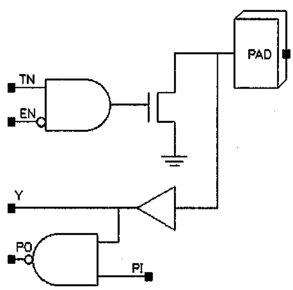
PBxUDvw

Bidirectional Open Drain Buffer with Pull-Up, Non-Inverting Input



PBxDDvw

Bidirectional Open Drain Buffer with Pull-Down, Non-Inverting Input



PBxDvw

Bidirectional Open Drain Buffer with Non-Inverting Input

3.6 Clock Drivers

Clock Driver Naming Convention:

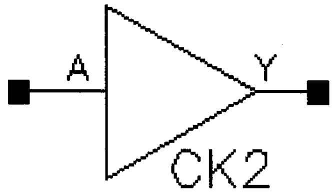
CKz

PSCKD x y z

where	x =	C -- CMOS level
		S -- CMOS Schmitt Trigger level
	y = (optional)	
		U -- pull-up resistor
		D -- pull-down resistor
	z =	2 -- 2mA drive
		4 -- 4mA drive
		6 -- 6mA drive
		8 -- 8mA drive

Inputs: A
Outputs: Y
Input Loading (SL):
- CK2/4: 4.9276
- CK6/8: 8.7019

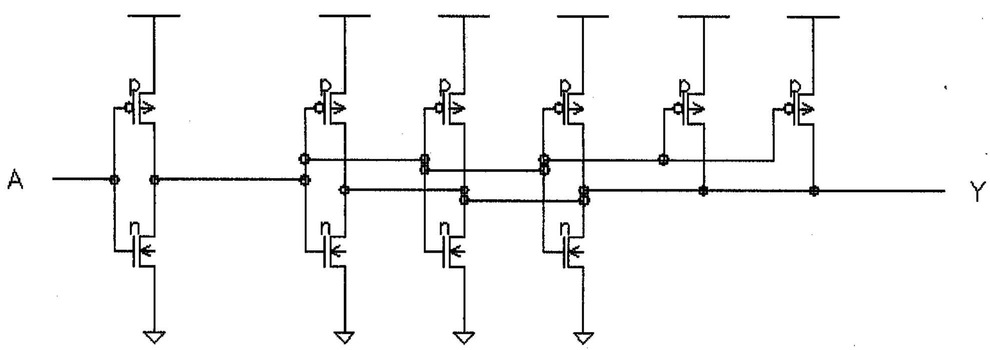
I/O Slots: All : 1



Symbol

A	Y
0	0
1	1

Truth Table



Schematic

CK2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

Path	Parameter	Delay [ns] SL = 50.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.46	0.27 + 0.004*SL	0.27 + 0.004*SL	0.27 + 0.004*SL
	tPHL	0.44	0.30 + 0.003*SL	0.30 + 0.003*SL	0.30 + 0.003*SL
	tR	0.51	0.13 + 0.008*SL	0.13 + 0.008*SL	0.12 + 0.008*SL
	tF	0.33	0.11 + 0.005*SL	0.11 + 0.005*SL	0.11 + 0.005*SL

*Range1 : SL < 2.00, *Range2 : 2.00 ≦ SL ≦ 3.00, *Range3 : 3.00 < SL

CK4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	5.18	0.39 + 0.098*CL	0.40 + 0.096*CL	0.40 + 0.096*CL
	tPHL	3.73	0.41 + 0.073*CL	0.43 + 0.067*CL	0.44 + 0.066*CL
	tR	10.80	0.15 + 0.203*CL	0.12 + 0.211*CL	0.10 + 0.214*CL
	tF	6.42	0.14 + 0.116*CL	0.12 + 0.124*CL	0.10 + 0.126*CL

*Range1 : CL < 3.00, *Range2 : 3.00 ≦ CL ≦ 7.00, *Range3 : 7.00 < CL

CK6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	3.52	0.33 + 0.064*CL	0.33 + 0.064*CL	0.33 + 0.064*CL
	tPHL	2.61	0.41 + 0.047*CL	0.42 + 0.044*CL	0.43 + 0.044*CL
	tR	7.23	0.13 + 0.138*CL	0.10 + 0.142*CL	0.10 + 0.143*CL
	tF	4.30	0.13 + 0.080*CL	0.10 + 0.084*CL	0.10 + 0.084*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

CK8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

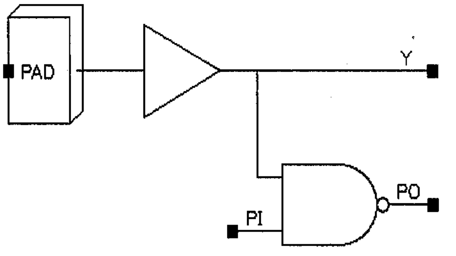
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	2.78	0.38 + 0.049*CL	0.39 + 0.048*CL	0.39 + 0.048*CL
	tPHL	2.14	0.46 + 0.037*CL	0.48 + 0.034*CL	0.49 + 0.033*CL
	tR	5.44	0.14 + 0.103*CL	0.12 + 0.106*CL	0.11 + 0.107*CL
	tF	3.24	0.15 + 0.059*CL	0.13 + 0.061*CL	0.12 + 0.062*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

Inputs: PAD, PI
Outputs: Y, PO

Input Loading (SL): All:
- PI: 2.6106

I/O Slots: 1



PSCKDC2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	9.93	0.41 + 0.191*CL	0.42 + 0.190*CL	0.42 + 0.190*CL
	tPHL	7.23	0.52 + 0.136*CL	0.53 + 0.134*CL	0.53 + 0.134*CL
	tR	21.20	0.16 + 0.417*CL	0.13 + 0.421*CL	0.13 + 0.421*CL
	tF	12.34	0.15 + 0.241*CL	0.13 + 0.244*CL	0.13 + 0.244*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDC4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	5.34	0.56 + 0.097*CL	0.57 + 0.095*CL	0.57 + 0.095*CL
	tPHL	3.98	0.66 + 0.070*CL	0.69 + 0.066*CL	0.69 + 0.066*CL
	tR	10.75	0.18 + 0.206*CL	0.13 + 0.212*CL	0.13 + 0.212*CL
	tF	6.36	0.19 + 0.118*CL	0.14 + 0.124*CL	0.14 + 0.124*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDC6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	3.69	0.50 + 0.065*CL	0.51 + 0.064*CL	0.51 + 0.064*CL
	tPHL	2.92	0.68 + 0.048*CL	0.71 + 0.044*CL	0.71 + 0.044*CL
	tR	7.20	0.17 + 0.135*CL	0.13 + 0.141*CL	0.12 + 0.142*CL
	tF	4.27	0.18 + 0.078*CL	0.14 + 0.082*CL	0.14 + 0.083*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDC8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

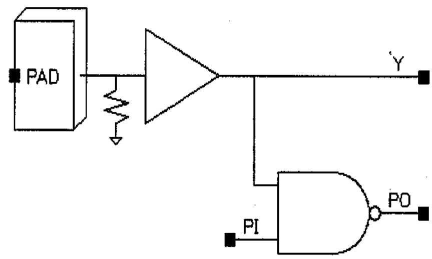
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	2.96	0.57 + 0.049*CL	0.58 + 0.048*CL	0.58 + 0.048*CL
	tPHL	2.45	0.75 + 0.038*CL	0.78 + 0.034*CL	0.79 + 0.033*CL
	tR	5.42	0.18 + 0.100*CL	0.15 + 0.104*CL	0.14 + 0.106*CL
	tF	3.23	0.20 + 0.058*CL	0.18 + 0.060*CL	0.16 + 0.061*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

Inputs: PAD, PI
Outputs: Y, PO

Input Loading (SL): All:
- PI: 2.6106

I/O Slots: 1



Symbol

PSCKDCD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	10.00	0.43 + 0.192*CL	0.44 + 0.191*CL	0.44 + 0.191*CL
	tPHL	7.24	0.52 + 0.136*CL	0.54 + 0.134*CL	0.54 + 0.134*CL
	tR	21.15	0.16 + 0.417*CL	0.13 + 0.420*CL	0.13 + 0.420*CL
	tF	12.45	0.16 + 0.242*CL	0.13 + 0.246*CL	0.13 + 0.246*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDCD4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	5.36	0.58 + 0.097*CL	0.59 + 0.096*CL	0.59 + 0.096*CL
	tPHL	3.99	0.67 + 0.070*CL	0.70 + 0.066*CL	0.70 + 0.066*CL
	tR	10.75	0.18 + 0.206*CL	0.13 + 0.212*CL	0.13 + 0.212*CL
	tF	6.36	0.19 + 0.118*CL	0.15 + 0.124*CL	0.15 + 0.124*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDCD6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	3.71	0.52 + 0.065*CL	0.52 + 0.064*CL	0.52 + 0.064*CL
	tPHL	2.92	0.69 + 0.048*CL	0.72 + 0.044*CL	0.72 + 0.044*CL
	tR	7.20	0.17 + 0.135*CL	0.13 + 0.141*CL	0.12 + 0.142*CL
	tF	4.27	0.18 + 0.078*CL	0.15 + 0.082*CL	0.14 + 0.083*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDCD8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

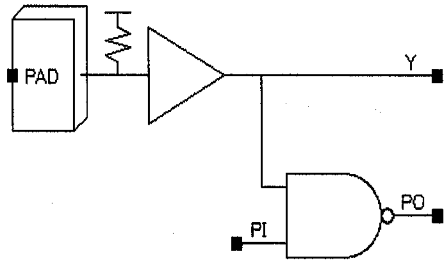
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	2.99	0.59 + 0.049*CL	0.60 + 0.048*CL	0.60 + 0.048*CL
	tPHL	2.46	0.76 + 0.038*CL	0.79 + 0.034*CL	0.80 + 0.033*CL
	tR	5.42	0.18 + 0.101*CL	0.15 + 0.104*CL	0.14 + 0.106*CL
	tF	3.23	0.20 + 0.058*CL	0.18 + 0.060*CL	0.17 + 0.061*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

Inputs: PAD, PI
Outputs: Y, PO

Input Loading (SL): All:
-PI: 2.6106

I/O Slots: 1



Symbol

PSCKDCU2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	10.00	0.41 + 0.192*CL	0.42 + 0.192*CL	0.42 + 0.192*CL
	tPHL	7.24	0.53 + 0.136*CL	0.54 + 0.134*CL	0.54 + 0.134*CL
	tR	21.12	0.16 + 0.416*CL	0.13 + 0.420*CL	0.13 + 0.420*CL
	tF	12.34	0.16 + 0.241*CL	0.13 + 0.244*CL	0.13 + 0.244*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDCU4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	5.34	0.56 + 0.097*CL	0.57 + 0.095*CL	0.57 + 0.095*CL
	tPHL	3.99	0.67 + 0.070*CL	0.70 + 0.066*CL	0.70 + 0.066*CL
	tR	10.75	0.18 + 0.206*CL	0.13 + 0.212*CL	0.13 + 0.212*CL
	tF	6.36	0.18 + 0.119*CL	0.14 + 0.124*CL	0.14 + 0.124*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDCU6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	3.69	0.50 + 0.065*CL	0.51 + 0.064*CL	0.51 + 0.064*CL
	tPHL	2.93	0.69 + 0.048*CL	0.72 + 0.044*CL	0.73 + 0.044*CL
	tR	7.21	0.17 + 0.135*CL	0.13 + 0.141*CL	0.12 + 0.142*CL
	tF	4.27	0.17 + 0.078*CL	0.14 + 0.082*CL	0.14 + 0.083*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDCU8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

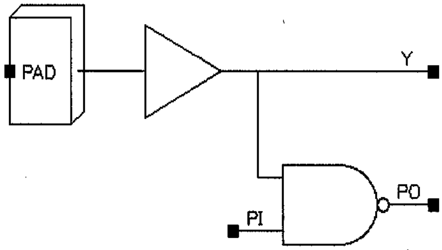
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	2.96	0.57 + 0.049*CL	0.58 + 0.048*CL	0.58 + 0.048*CL
	tPHL	2.47	0.76 + 0.038*CL	0.79 + 0.034*CL	0.80 + 0.033*CL
	tR	5.42	0.18 + 0.100*CL	0.15 + 0.104*CL	0.14 + 0.106*CL
	tF	3.22	0.19 + 0.058*CL	0.18 + 0.060*CL	0.17 + 0.061*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

Inputs: PAD, PI
Outputs: Y, PO

Input Loading (SL): All:
- PI: 2.6106

I/O Slots: 1



PSCKDS2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	10.96	1.05 + 0.200*CL	1.07 + 0.198*CL	1.07 + 0.198*CL
	tPHL	10.10	1.99 + 0.167*CL	2.03 + 0.162*CL	2.03 + 0.162*CL
	tR	20.99	0.20 + 0.415*CL	0.20 + 0.416*CL	0.20 + 0.416*CL
	tF	12.26	0.33 + 0.240*CL	0.34 + 0.238*CL	0.34 + 0.238*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDS4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	6.27	1.30 + 0.106*CL	1.36 + 0.098*CL	1.36 + 0.098*CL
	tPHL	6.69	2.56 + 0.097*CL	2.68 + 0.080*CL	2.68 + 0.080*CL
	tR	10.70	0.26 + 0.208*CL	0.26 + 0.209*CL	0.26 + 0.209*CL
	tF	6.50	0.52 + 0.124*CL	0.55 + 0.119*CL	0.55 + 0.119*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDS6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	4.46	1.17 + 0.071*CL	1.20 + 0.065*CL	1.21 + 0.065*CL
	tPHL	4.94	2.25 + 0.065*CL	2.34 + 0.053*CL	2.35 + 0.052*CL
	tR	7.19	0.22 + 0.138*CL	0.21 + 0.139*CL	0.21 + 0.140*CL
	tF	4.42	0.40 + 0.083*CL	0.43 + 0.080*CL	0.43 + 0.080*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDS8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

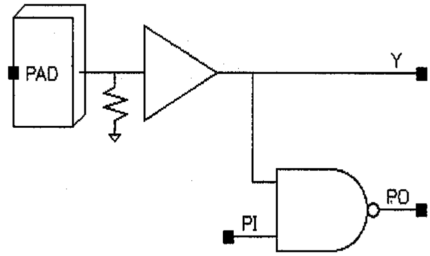
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	3.82	1.29 + 0.056*CL	1.32 + 0.051*CL	1.34 + 0.049*CL
	tPHL	4.72	2.53 + 0.055*CL	2.60 + 0.045*CL	2.65 + 0.042*CL
	tR	5.45	0.26 + 0.104*CL	0.26 + 0.104*CL	0.26 + 0.104*CL
	tF	3.53	0.50 + 0.065*CL	0.52 + 0.061*CL	0.54 + 0.060*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

Inputs: PAD, PI
Outputs: Y, PO

Input Loading (SL): All:
- PI: 2.6106

I/O Slots: 1



Symbol

PSCKDSD2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	10.97	1.06 + 0.200*CL	1.08 + 0.198*CL	1.08 + 0.198*CL
	tPHL	10.13	2.01 + 0.168*CL	2.05 + 0.162*CL	2.05 + 0.162*CL
	tR	20.95	0.20 + 0.414*CL	0.20 + 0.415*CL	0.20 + 0.415*CL
	tF	12.19	0.33 + 0.239*CL	0.34 + 0.237*CL	0.34 + 0.237*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDSD4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	6.28	1.32 + 0.106*CL	1.37 + 0.098*CL	1.37 + 0.098*CL
	tPHL	6.72	2.59 + 0.097*CL	2.71 + 0.080*CL	2.71 + 0.080*CL
	tR	10.70	0.26 + 0.208*CL	0.26 + 0.209*CL	0.26 + 0.209*CL
	tF	6.50	0.52 + 0.124*CL	0.55 + 0.119*CL	0.55 + 0.119*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDSD6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	4.47	1.18 + 0.071*CL	1.22 + 0.065*CL	1.22 + 0.065*CL
	tPHL	4.97	2.28 + 0.066*CL	2.37 + 0.053*CL	2.38 + 0.052*CL
	tR	7.19	0.23 + 0.138*CL	0.21 + 0.139*CL	0.21 + 0.140*CL
	tF	4.42	0.40 + 0.083*CL	0.43 + 0.080*CL	0.43 + 0.080*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDSD8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

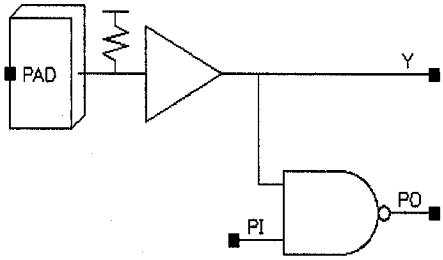
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.51	0.43 + 1.219*CL	0.57 + 1.199*CL	0.57 + 1.199*CL
	tPHL	44.18	-0.03 + 0.908*CL	0.16 + 0.880*CL	0.16 + 0.880*CL
	tR	118.75	0.42 + 2.371*CL	0.46 + 2.366*CL	0.46 + 2.366*CL
	tF	62.25	0.44 + 1.247*CL	0.53 + 1.234*CL	0.53 + 1.234*CL
PI to PO	tPLH	59.23	0.56 + 1.184*CL	0.65 + 1.172*CL	0.65 + 1.172*CL
	tPHL	39.63	-0.07 + 0.812*CL	0.07 + 0.791*CL	0.07 + 0.791*CL
	tR	119.16	0.51 + 2.374*CL	0.52 + 2.373*CL	0.52 + 2.373*CL
	tF	60.83	0.43 + 1.211*CL	0.45 + 1.208*CL	0.45 + 1.208*CL
PAD to Y	tPLH	3.84	1.31 + 0.056*CL	1.35 + 0.051*CL	1.37 + 0.049*CL
	tPHL	4.77	2.57 + 0.055*CL	2.63 + 0.045*CL	2.68 + 0.042*CL
	tR	5.46	0.28 + 0.101*CL	0.26 + 0.104*CL	0.26 + 0.104*CL
	tF	3.52	0.51 + 0.064*CL	0.53 + 0.061*CL	0.55 + 0.059*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

Inputs: PAD, PI
Outputs: Y, PO

Input Loading (SL): All:
- PI: 2.6106

I/O Slots: 1



Symbol

PSCKDSU2 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	10.96	1.05 + 0.200*CL	1.07 + 0.198*CL	1.07 + 0.198*CL
	tPHL	10.12	2.00 + 0.168*CL	2.04 + 0.162*CL	2.04 + 0.162*CL
	tR	20.97	0.20 + 0.415*CL	0.20 + 0.415*CL	0.20 + 0.415*CL
	tF	12.24	0.33 + 0.240*CL	0.34 + 0.238*CL	0.34 + 0.238*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDSU4 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	6.27	1.31 + 0.106*CL	1.37 + 0.098*CL	1.37 + 0.098*CL
	tPHL	6.71	2.58 + 0.097*CL	2.70 + 0.080*CL	2.70 + 0.080*CL
	tR	10.69	0.26 + 0.208*CL	0.26 + 0.209*CL	0.26 + 0.209*CL
	tF	6.50	0.52 + 0.124*CL	0.56 + 0.119*CL	0.56 + 0.119*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDSU6 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	4.46	1.17 + 0.071*CL	1.21 + 0.065*CL	1.21 + 0.065*CL
	tPHL	4.96	2.27 + 0.066*CL	2.36 + 0.053*CL	2.37 + 0.052*CL
	tR	7.19	0.23 + 0.138*CL	0.22 + 0.139*CL	0.21 + 0.140*CL
	tF	4.42	0.40 + 0.084*CL	0.43 + 0.080*CL	0.43 + 0.080*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PSCKDSU8 Switching Characteristics

[Delays for typical process, 25.00°C, 3.30V, when t_R and t_F = 2.00ns] **(CL: Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	60.42	0.41 + 1.217*CL	0.55 + 1.197*CL	0.55 + 1.197*CL
	tPHL	44.05	-0.04 + 0.904*CL	0.14 + 0.878*CL	0.14 + 0.878*CL
	tR	118.90	0.41 + 2.375*CL	0.45 + 2.369*CL	0.45 + 2.369*CL
	tF	61.79	0.43 + 1.241*CL	0.54 + 1.225*CL	0.54 + 1.225*CL
PI to PO	tPLH	59.14	0.55 + 1.182*CL	0.63 + 1.170*CL	0.63 + 1.170*CL
	tPHL	39.50	-0.08 + 0.808*CL	0.06 + 0.789*CL	0.06 + 0.789*CL
	tR	119.49	0.50 + 2.381*CL	0.51 + 2.380*CL	0.51 + 2.380*CL
	tF	59.96	0.43 + 1.196*CL	0.47 + 1.190*CL	0.47 + 1.190*CL
PAD to Y	tPLH	3.82	1.29 + 0.056*CL	1.33 + 0.051*CL	1.35 + 0.050*CL
	tPHL	4.75	2.55 + 0.054*CL	2.62 + 0.045*CL	2.67 + 0.042*CL
	tR	5.45	0.26 + 0.104*CL	0.26 + 0.104*CL	0.26 + 0.104*CL
	tF	3.53	0.50 + 0.065*CL	0.53 + 0.061*CL	0.54 + 0.060*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

Chapter 4.0 5.0V Interface I/O Buffers

4.1 Overview

This chapter describes the AC characteristics of 5.0V Interface Input and Output Buffers. The AC characteristics of Bidirectional Buffers can be derived from different combinations of Input and Output Buffers.

As there are over 450 possible combinations of I/O Buffers in the library, naming conventions have been adopted. Naming conventions are described at the beginning of each sub-section.

4.2 Summary Tables

Table 4.1: 5.0V Interface Input Buffers

Cell Name	Description	Page
PHIC/PHICU/PHICD	CMOS Level Non-Inverting Input Buffers	4-8
PHIT/PHITU/PHITD	TTL Level Non-Inverting Input Buffers	4-10
PHIS/PHISU/PHISD	CMOS Schmitt Trigger Level Non-Inverting Input Buffers	4-12
PHIL/PHILU/PHILD	TTL Schmitt Trigger Level Non-Inverting Input Buffers	4-14

Table 4.2: 5.0V Interface Output Buffers

Cell Name	Description	Page
PHOB1/2/4/8/12/16/20/24 and PHOB(4/8/12/16/20/24)SM and PHOB(12/16/20/24)SH	Non-Inverting Output Buffers with no slew-rate control, medium slew-rate control and high slew-rate control.	4-18
PHOT1/2/4/8/12/16/20/24 and PHOT(4/8/12/16/20/24)SM and PHOT(12/16/20/24)SH	Tristate Non-Inverting Output Buffers s with no slew-rate control, medium slew-rate control and high slew-rate control.	4-24
PHOD1/2/4/8/12/16/20/24 and PHOD(4/8/12/16/20/24)SM and PHOD(12/16/20/24)SH	Open Drain Output Buffers s with no slew-rate control, medium slew-rate control and high slew-rate control.	4-34

Table 4.3: 5.0V Interface Bidirectional Buffers

Cell Name	Description	Page
PHBxUTvw	Bidirectional Buffer with Pull-Up, Non-Inverting Input	4-42
PHBxDTvw	Bidirectional Buffer with Pull-Down, Non-Inverting Input	4-42
PHBxTvw	Bidirectional Buffer with Non-Inverting Input	4-42
PHBxUDvw	Bidirectional Open Drain Buffer with Pull-Up, Non-Inverting Input	4-43
PHBxDDvw	Bidirectional Open Drain Buffer with Pull-Down, Non-Inverting Input	4-43
PHBxDvw	Bidirectional Open Drain Buffer with Non-Inverting Input	4-43

4.3 Input Buffers

5.0V Interface Input Buffer Naming Conventions:

PH x z

where x = C -- CMOS levels

T -- TTL levels

S -- CMOS Schmitt Trigger levels

L -- TTL Schmitt Trigger levels

z = (optional)

U -- pull-up resistor

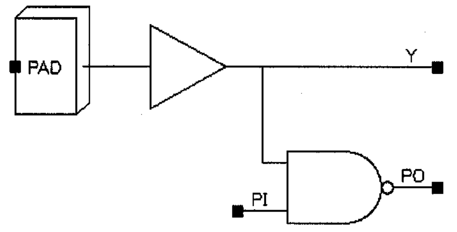
D -- pull-down resistor

e.g. PHISD - 5.0V interface CMOS Schmitt Trigger input buffer with pull-down

Input: PAD, PI
Output Y, PO

Input Loading (SL): All :
- PI : 1.7474

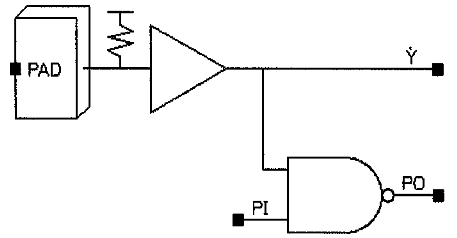
I/O Slots: 1



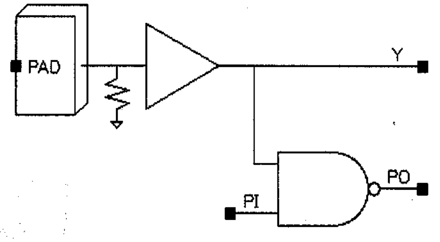
PHIC Symbol

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Truth Table



PHICU Symbol



PHICD Symbol

PHIC Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.39	0.32 + 0.036*SL	0.34 + 0.029*SL	0.35 + 0.029*SL
	tPHL	-0.05	-0.12 + 0.031*SL	-0.08 + 0.019*SL	0.03 + 0.013*SL
	tR	0.31	0.20 + 0.054*SL	0.18 + 0.062*SL	0.12 + 0.065*SL
	tF	0.26	0.18 + 0.043*SL	0.22 + 0.030*SL	0.25 + 0.028*SL
PI to PO	tPLH	0.45	0.39 + 0.032*SL	0.39 + 0.029*SL	0.39 + 0.029*SL
	tPHL	-0.05	-0.10 + 0.023*SL	-0.07 + 0.016*SL	-0.01 + 0.013*SL
	tR	0.41	0.30 + 0.055*SL	0.27 + 0.062*SL	0.22 + 0.065*SL
	tF	0.27	0.21 + 0.033*SL	0.22 + 0.028*SL	0.22 + 0.028*SL
PAD to Y	tPLH	0.32	0.30 + 0.009*SL	0.30 + 0.008*SL	0.31 + 0.007*SL
	tPHL	0.66	0.64 + 0.011*SL	0.65 + 0.008*SL	0.68 + 0.007*SL
	tR	0.14	0.10 + 0.017*SL	0.11 + 0.015*SL	0.09 + 0.016*SL
	tF	0.16	0.13 + 0.014*SL	0.14 + 0.011*SL	0.14 + 0.012*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

PHICU Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.39	0.32 + 0.036*SL	0.34 + 0.029*SL	0.35 + 0.029*SL
	tPHL	-0.05	-0.12 + 0.031*SL	-0.08 + 0.019*SL	0.03 + 0.013*SL
	tR	0.31	0.20 + 0.054*SL	0.18 + 0.062*SL	0.12 + 0.065*SL
	tF	0.26	0.18 + 0.043*SL	0.22 + 0.030*SL	0.25 + 0.028*SL
PI to PO	tPLH	0.45	0.39 + 0.032*SL	0.39 + 0.029*SL	0.39 + 0.029*SL
	tPHL	-0.05	-0.10 + 0.023*SL	-0.07 + 0.016*SL	-0.01 + 0.013*SL
	tR	0.41	0.30 + 0.055*SL	0.27 + 0.062*SL	0.22 + 0.065*SL
	tF	0.27	0.21 + 0.033*SL	0.22 + 0.028*SL	0.22 + 0.028*SL
PAD to Y	tPLH	0.32	0.30 + 0.009*SL	0.30 + 0.008*SL	0.31 + 0.007*SL
	tPHL	0.68	0.66 + 0.011*SL	0.66 + 0.008*SL	0.69 + 0.007*SL
	tR	0.14	0.10 + 0.016*SL	0.11 + 0.015*SL	0.09 + 0.016*SL
	tF	0.16	0.13 + 0.013*SL	0.14 + 0.011*SL	0.14 + 0.012*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

PHICD Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

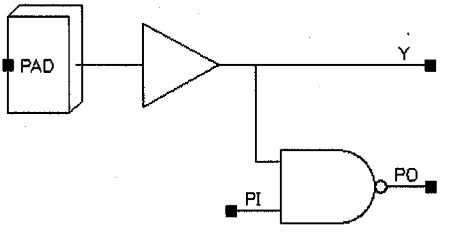
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.39	0.32 + 0.036*SL	0.34 + 0.029*SL	0.35 + 0.029*SL
	tPHL	-0.05	-0.12 + 0.031*SL	-0.08 + 0.019*SL	0.03 + 0.013*SL
	tR	0.31	0.20 + 0.054*SL	0.18 + 0.062*SL	0.12 + 0.065*SL
	tF	0.26	0.18 + 0.043*SL	0.22 + 0.030*SL	0.25 + 0.028*SL
PI to PO	tPLH	0.45	0.39 + 0.032*SL	0.39 + 0.029*SL	0.39 + 0.029*SL
	tPHL	-0.05	-0.10 + 0.023*SL	-0.07 + 0.016*SL	-0.01 + 0.013*SL
	tR	0.41	0.30 + 0.055*SL	0.27 + 0.062*SL	0.22 + 0.065*SL
	tF	0.27	0.21 + 0.033*SL	0.22 + 0.028*SL	0.22 + 0.028*SL
PAD to Y	tPLH	0.34	0.32 + 0.009*SL	0.33 + 0.008*SL	0.33 + 0.007*SL
	tPHL	0.67	0.65 + 0.011*SL	0.66 + 0.008*SL	0.69 + 0.007*SL
	tR	0.14	0.11 + 0.014*SL	0.10 + 0.016*SL	0.09 + 0.016*SL
	tF	0.16	0.14 + 0.013*SL	0.14 + 0.011*SL	0.14 + 0.012*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Input: PAD, PI
Output Y, PO

Input Loading (SL): All :
- PI: 1.7474

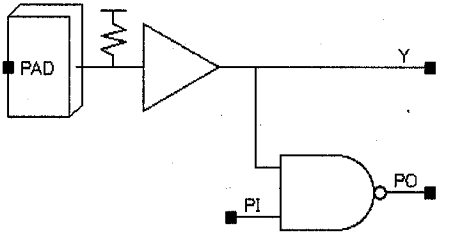
I/O Slots: 1



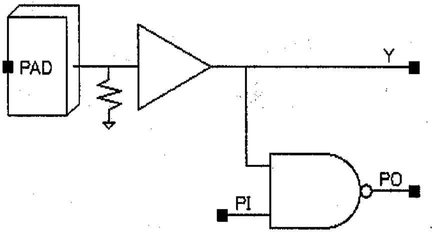
PHIT Symbol

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Truth Table



PHITU Symbol



PHITD Symbol

PHIT Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 2.00ns](CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	76.95	0.16 + 1.548*CL	0.27 + 1.534*CL	0.27 + 1.534*CL
	tPHL	47.39	0.17 + 0.969*CL	0.38 + 0.940*CL	0.38 + 0.940*CL
	tR	164.88	0.33 + 3.286*CL	0.28 + 3.292*CL	0.28 + 3.292*CL
	tF	75.74	0.33 + 1.527*CL	0.48 + 1.505*CL	0.48 + 1.505*CL
PI to PO	tPLH	76.27	0.26 + 1.528*CL	0.32 + 1.519*CL	0.32 + 1.519*CL
	tPHL	41.55	0.18 + 0.844*CL	0.32 + 0.825*CL	0.32 + 0.825*CL
	tR	165.29	0.44 + 3.290*CL	0.38 + 3.298*CL	0.38 + 3.298*CL
	tF	73.80	0.35 + 1.479*CL	0.43 + 1.467*CL	0.43 + 1.467*CL
PAD to Y	tPLH	19.72	0.41 + 0.388*CL	0.42 + 0.386*CL	0.42 + 0.386*CL
	tPHL	18.51	0.84 + 0.358*CL	0.88 + 0.353*CL	0.88 + 0.353*CL
	tR	42.55	0.10 + 0.847*CL	0.09 + 0.849*CL	0.09 + 0.849*CL
	tF	30.50	0.14 + 0.607*CL	0.14 + 0.607*CL	0.14 + 0.607*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PHITU Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 2.00ns](CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	76.95	0.16 + 1.548*CL	0.27 + 1.534*CL	0.27 + 1.534*CL
	tPHL	47.39	0.17 + 0.969*CL	0.38 + 0.940*CL	0.38 + 0.940*CL
	tR	164.88	0.33 + 3.286*CL	0.28 + 3.292*CL	0.28 + 3.292*CL
	tF	75.74	0.33 + 1.527*CL	0.48 + 1.505*CL	0.48 + 1.505*CL
PI to PO	tPLH	76.27	0.26 + 1.528*CL	0.32 + 1.519*CL	0.32 + 1.519*CL
	tPHL	41.55	0.18 + 0.844*CL	0.32 + 0.825*CL	0.32 + 0.825*CL
	tR	165.29	0.44 + 3.290*CL	0.38 + 3.298*CL	0.38 + 3.298*CL
	tF	73.80	0.35 + 1.479*CL	0.43 + 1.467*CL	0.43 + 1.467*CL
PAD to Y	tPLH	19.66	0.39 + 0.387*CL	0.40 + 0.385*CL	0.40 + 0.385*CL
	tPHL	18.52	0.86 + 0.358*CL	0.89 + 0.353*CL	0.89 + 0.353*CL
	tR	42.57	0.11 + 0.848*CL	0.09 + 0.850*CL	0.09 + 0.850*CL
	tF	30.38	0.14 + 0.605*CL	0.14 + 0.605*CL	0.14 + 0.605*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PHITD Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 2.00ns](CL: Capacitive Load [pF])

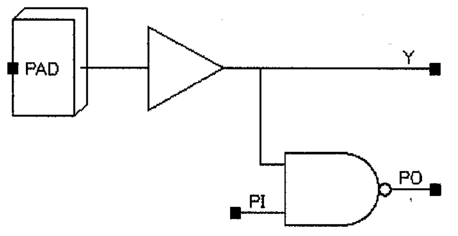
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	76.95	0.16 + 1.548*CL	0.27 + 1.534*CL	0.27 + 1.534*CL
	tPHL	47.39	0.17 + 0.969*CL	0.38 + 0.940*CL	0.38 + 0.940*CL
	tR	164.88	0.33 + 3.286*CL	0.28 + 3.292*CL	0.28 + 3.292*CL
	tF	75.74	0.33 + 1.527*CL	0.48 + 1.505*CL	0.48 + 1.505*CL
PI to PO	tPLH	76.27	0.26 + 1.528*CL	0.32 + 1.519*CL	0.32 + 1.519*CL
	tPHL	41.55	0.18 + 0.844*CL	0.32 + 0.825*CL	0.32 + 0.825*CL
	tR	165.29	0.44 + 3.290*CL	0.38 + 3.298*CL	0.38 + 3.298*CL
	tF	73.80	0.35 + 1.479*CL	0.43 + 1.467*CL	0.43 + 1.467*CL
PAD to Y	tPLH	19.70	0.44 + 0.387*CL	0.45 + 0.385*CL	0.45 + 0.385*CL
	tPHL	18.53	0.86 + 0.358*CL	0.90 + 0.353*CL	0.90 + 0.353*CL
	tR	42.59	0.10 + 0.848*CL	0.09 + 0.850*CL	0.09 + 0.850*CL
	tF	30.55	0.14 + 0.608*CL	0.14 + 0.608*CL	0.14 + 0.608*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

Input: PAD, PI
Output Y, PO

Input Loading (SL): All :
- PI: 1.7474

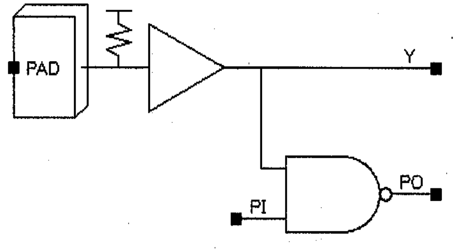
I/O Slots: 1



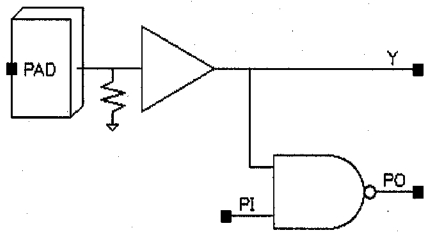
PHIS Symbol

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Truth Table



PHISU Symbol



PHISD Symbol

PHIS Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.39	0.32 + 0.036*SL	0.34 + 0.029*SL	0.35 + 0.029*SL
	tPHL	-0.05	-0.12 + 0.031*SL	-0.08 + 0.019*SL	0.03 + 0.013*SL
	tR	0.31	0.20 + 0.054*SL	0.18 + 0.062*SL	0.12 + 0.065*SL
	tF	0.26	0.18 + 0.043*SL	0.22 + 0.030*SL	0.25 + 0.028*SL
PI to PO	tPLH	0.45	0.39 + 0.032*SL	0.39 + 0.029*SL	0.39 + 0.029*SL
	tPHL	-0.05	-0.10 + 0.023*SL	-0.07 + 0.016*SL	-0.01 + 0.013*SL
	tR	0.41	0.30 + 0.055*SL	0.27 + 0.062*SL	0.22 + 0.065*SL
	tF	0.27	0.21 + 0.033*SL	0.22 + 0.028*SL	0.22 + 0.028*SL
PAD to Y	tPLH	0.63	0.61 + 0.009*SL	0.61 + 0.008*SL	0.62 + 0.007*SL
	tPHL	1.13	1.11 + 0.011*SL	1.12 + 0.008*SL	1.15 + 0.007*SL
	tR	0.13	0.11 + 0.012*SL	0.10 + 0.016*SL	0.09 + 0.016*SL
	tF	0.16	0.14 + 0.011*SL	0.14 + 0.012*SL	0.14 + 0.012*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

PHISU Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.39	0.32 + 0.036*SL	0.34 + 0.029*SL	0.35 + 0.029*SL
	tPHL	-0.05	-0.12 + 0.031*SL	-0.08 + 0.019*SL	0.03 + 0.013*SL
	tR	0.31	0.20 + 0.054*SL	0.18 + 0.062*SL	0.12 + 0.065*SL
	tF	0.26	0.18 + 0.043*SL	0.22 + 0.030*SL	0.25 + 0.028*SL
PI to PO	tPLH	0.45	0.39 + 0.032*SL	0.39 + 0.029*SL	0.39 + 0.029*SL
	tPHL	-0.05	-0.10 + 0.023*SL	-0.07 + 0.016*SL	-0.01 + 0.013*SL
	tR	0.41	0.30 + 0.055*SL	0.27 + 0.062*SL	0.22 + 0.065*SL
	tF	0.27	0.21 + 0.033*SL	0.22 + 0.028*SL	0.22 + 0.028*SL
PAD to Y	tPLH	0.64	0.62 + 0.009*SL	0.62 + 0.008*SL	0.63 + 0.007*SL
	tPHL	1.14	1.12 + 0.011*SL	1.13 + 0.008*SL	1.16 + 0.007*SL
	tR	0.14	0.11 + 0.012*SL	0.10 + 0.016*SL	0.09 + 0.016*SL
	tF	0.16	0.14 + 0.011*SL	0.14 + 0.012*SL	0.14 + 0.012*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

PHISD Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 0.80ns] (SL: Standard Load)

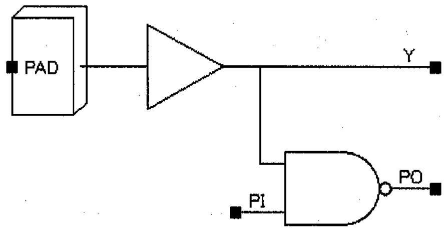
Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	0.39	0.32 + 0.036*SL	0.34 + 0.029*SL	0.35 + 0.029*SL
	tPHL	-0.05	-0.12 + 0.031*SL	-0.08 + 0.019*SL	0.03 + 0.013*SL
	tR	0.31	0.20 + 0.054*SL	0.18 + 0.062*SL	0.12 + 0.065*SL
	tF	0.26	0.18 + 0.043*SL	0.22 + 0.030*SL	0.25 + 0.028*SL
PI to PO	tPLH	0.45	0.39 + 0.032*SL	0.39 + 0.029*SL	0.39 + 0.029*SL
	tPHL	-0.05	-0.10 + 0.023*SL	-0.07 + 0.016*SL	-0.01 + 0.013*SL
	tR	0.41	0.30 + 0.055*SL	0.27 + 0.062*SL	0.22 + 0.065*SL
	tF	0.27	0.21 + 0.033*SL	0.22 + 0.028*SL	0.22 + 0.028*SL
PAD to Y	tPLH	0.64	0.62 + 0.009*SL	0.62 + 0.008*SL	0.63 + 0.007*SL
	tPHL	1.15	1.13 + 0.011*SL	1.14 + 0.008*SL	1.17 + 0.007*SL
	tR	0.13	0.11 + 0.013*SL	0.10 + 0.016*SL	0.09 + 0.016*SL
	tF	0.16	0.14 + 0.011*SL	0.14 + 0.012*SL	0.14 + 0.012*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≦ SL ≦ 20.00, *Range3 : 20.00 < SL

Input: PAD, PI
Output Y, PO

Input Loading (SL): All :
- PI: 1.7474

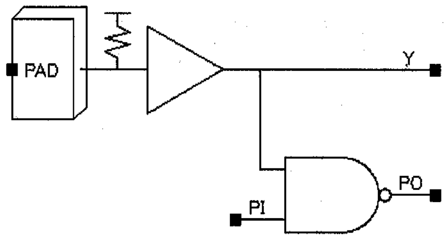
I/O Slots: 1



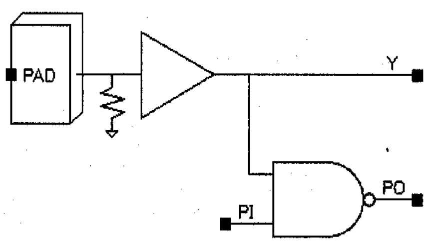
PHIL Symbol

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Truth Table



PHILU Symbol



PHILD Symbol

PHIL Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 2.00ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	76.95	0.16 + 1.548*CL	0.27 + 1.534*CL	0.27 + 1.534*CL
	tPHL	47.39	0.17 + 0.969*CL	0.38 + 0.940*CL	0.38 + 0.940*CL
	tR	164.88	0.33 + 3.286*CL	0.28 + 3.292*CL	0.28 + 3.292*CL
	tF	75.74	0.33 + 1.527*CL	0.48 + 1.505*CL	0.48 + 1.505*CL
PI to PO	tPLH	76.27	0.26 + 1.528*CL	0.32 + 1.519*CL	0.32 + 1.519*CL
	tPHL	41.55	0.18 + 0.844*CL	0.32 + 0.825*CL	0.32 + 0.825*CL
	tR	165.29	0.44 + 3.290*CL	0.38 + 3.298*CL	0.38 + 3.298*CL
	tF	73.80	0.35 + 1.479*CL	0.43 + 1.467*CL	0.43 + 1.467*CL
PAD to Y	tPLH	20.28	1.05 + 0.386*CL	1.06 + 0.384*CL	1.06 + 0.384*CL
	tPHL	20.01	2.33 + 0.358*CL	2.36 + 0.353*CL	2.36 + 0.353*CL
	tR	42.33	0.11 + 0.843*CL	0.10 + 0.845*CL	0.10 + 0.845*CL
	tF	30.51	0.14 + 0.608*CL	0.14 + 0.608*CL	0.14 + 0.608*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PHILU Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 2.00ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	76.95	0.16 + 1.548*CL	0.27 + 1.534*CL	0.27 + 1.534*CL
	tPHL	47.39	0.17 + 0.969*CL	0.38 + 0.940*CL	0.38 + 0.940*CL
	tR	164.88	0.33 + 3.286*CL	0.28 + 3.292*CL	0.28 + 3.292*CL
	tF	75.74	0.33 + 1.527*CL	0.48 + 1.505*CL	0.48 + 1.505*CL
PI to PO	tPLH	76.27	0.26 + 1.528*CL	0.32 + 1.519*CL	0.32 + 1.519*CL
	tPHL	41.55	0.18 + 0.844*CL	0.32 + 0.825*CL	0.32 + 0.825*CL
	tR	165.29	0.44 + 3.290*CL	0.38 + 3.298*CL	0.38 + 3.298*CL
	tF	73.80	0.35 + 1.479*CL	0.43 + 1.467*CL	0.43 + 1.467*CL
PAD to Y	tPLH	20.28	1.04 + 0.386*CL	1.05 + 0.385*CL	1.05 + 0.385*CL
	tPHL	20.03	2.36 + 0.358*CL	2.40 + 0.353*CL	2.40 + 0.353*CL
	tR	42.36	0.11 + 0.843*CL	0.10 + 0.845*CL	0.10 + 0.845*CL
	tF	30.44	0.14 + 0.606*CL	0.14 + 0.606*CL	0.14 + 0.606*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

PHILD Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=5.00V, ovdd=3.30V, when t_R and t_F = 2.00ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
Y to PO	tPLH	76.95	0.16 + 1.548*CL	0.27 + 1.534*CL	0.27 + 1.534*CL
	tPHL	47.39	0.17 + 0.969*CL	0.38 + 0.940*CL	0.38 + 0.940*CL
	tR	164.88	0.33 + 3.286*CL	0.28 + 3.292*CL	0.28 + 3.292*CL
	tF	75.74	0.33 + 1.527*CL	0.48 + 1.505*CL	0.48 + 1.505*CL
PI to PO	tPLH	76.27	0.26 + 1.528*CL	0.32 + 1.519*CL	0.32 + 1.519*CL
	tPHL	41.55	0.18 + 0.844*CL	0.32 + 0.825*CL	0.32 + 0.825*CL
	tR	165.29	0.44 + 3.290*CL	0.38 + 3.298*CL	0.38 + 3.298*CL
	tF	73.80	0.35 + 1.479*CL	0.43 + 1.467*CL	0.43 + 1.467*CL
PAD to Y	tPLH	20.31	1.07 + 0.386*CL	1.08 + 0.385*CL	1.08 + 0.385*CL
	tPHL	20.04	2.36 + 0.358*CL	2.39 + 0.353*CL	2.39 + 0.353*CL
	tR	42.30	0.11 + 0.842*CL	0.10 + 0.844*CL	0.10 + 0.844*CL
	tF	30.41	0.14 + 0.606*CL	0.14 + 0.605*CL	0.14 + 0.605*CL

*Range1 : CL < 7.00, *Range2 : 7.00 ≦ CL ≦ 14.00, *Range3 : 14.00 < CL

4.4 Output Buffers

5.0V Interface Output Buffer Naming Conventions:

PH O u v w

where u = B -- Normal non-inverting buffer

T -- Tristate non-inverting buffer

D -- Open-drain output

v = 1 -- 1mA drive

2 -- 2mA drive

4 -- 4mA drive

8 -- 8mA drive

12 -- 12mA drive

16 -- 16mA drive

20 -- 206mA drive

24 -- 24mA drive

w = (optional)

none -- no slew-rate control

SM -- medium slew-rate control

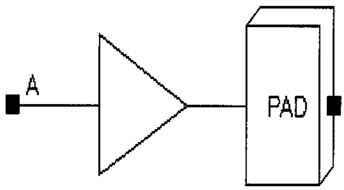
SH -- high slew-rate control

e.g., PHOT12SM is a 5.0V Interface tristate output buffer with 12mA drive and medium slew-rate control

Input: A
Output: PAD

Input Loading (SL): All:
- A: 3.4947

I/O Slots: 1



Symbol

A	PAD
0	0
1	1

Truth Table

PHOB1 Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	14.28	1.32 + 0.259*CL	1.32 + 0.259*CL	1.32 + 0.259*CL
	tPHL	10.80	1.19 + 0.192*CL	1.19 + 0.192*CL	1.19 + 0.192*CL
	tR	32.51	1.97 + 0.611*CL	1.97 + 0.611*CL	1.97 + 0.611*CL
	tF	20.35	1.18 + 0.383*CL	1.18 + 0.383*CL	1.18 + 0.383*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB2 Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	7.46	0.98 + 0.130*CL	0.98 + 0.130*CL	0.98 + 0.130*CL
	tPHL	5.70	0.89 + 0.096*CL	0.89 + 0.096*CL	0.89 + 0.096*CL
	tR	16.27	1.00 + 0.305*CL	0.99 + 0.305*CL	1.00 + 0.305*CL
	tF	10.19	0.60 + 0.192*CL	0.60 + 0.192*CL	0.60 + 0.192*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB4 Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	5.21	0.89 + 0.086*CL	0.89 + 0.086*CL	0.89 + 0.086*CL
	tPHL	4.02	0.81 + 0.064*CL	0.81 + 0.064*CL	0.81 + 0.064*CL
	tR	10.86	0.67 + 0.204*CL	0.67 + 0.204*CL	0.67 + 0.204*CL
	tF	6.80	0.41 + 0.128*CL	0.41 + 0.128*CL	0.41 + 0.128*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB4SM Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	6.15	1.82 + 0.087*CL	1.83 + 0.086*CL	1.83 + 0.086*CL
	tPHL	5.19	1.93 + 0.065*CL	1.97 + 0.064*CL	1.99 + 0.064*CL
	tR	10.90	0.78 + 0.202*CL	0.74 + 0.203*CL	0.72 + 0.203*CL
	tF	7.02	0.79 + 0.125*CL	0.73 + 0.126*CL	0.67 + 0.127*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB8 Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.04	0.88 + 0.043*CL	0.88 + 0.043*CL	0.88 + 0.043*CL
	tPHL	2.41	0.80 + 0.032*CL	0.80 + 0.032*CL	0.80 + 0.032*CL
	tR	5.45	0.37 + 0.102*CL	0.36 + 0.102*CL	0.36 + 0.102*CL
	tF	3.43	0.25 + 0.064*CL	0.24 + 0.064*CL	0.23 + 0.064*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB8SM Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	4.31	2.08 + 0.045*CL	2.13 + 0.044*CL	2.15 + 0.043*CL
	tPHL	4.03	2.16 + 0.037*CL	2.30 + 0.035*CL	2.40 + 0.033*CL
	tR	5.68	0.76 + 0.098*CL	0.69 + 0.100*CL	0.63 + 0.101*CL
	tF	4.02	0.92 + 0.062*CL	0.95 + 0.062*CL	0.93 + 0.062*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB12 Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.54	0.92 + 0.032*CL	0.92 + 0.032*CL	0.92 + 0.032*CL
	tPHL	2.04	0.84 + 0.024*CL	0.84 + 0.024*CL	0.84 + 0.024*CL
	tR	4.11	0.31 + 0.076*CL	0.30 + 0.076*CL	0.29 + 0.076*CL
	tF	2.60	0.23 + 0.047*CL	0.22 + 0.048*CL	0.20 + 0.048*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB12SM Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.78	2.03 + 0.035*CL	2.11 + 0.033*CL	2.15 + 0.033*CL
	tPHL	3.60	2.05 + 0.031*CL	2.21 + 0.028*CL	2.33 + 0.026*CL
	tR	4.42	0.75 + 0.073*CL	0.72 + 0.074*CL	0.66 + 0.075*CL
	tF	3.30	0.88 + 0.048*CL	0.97 + 0.047*CL	1.00 + 0.046*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB12SH Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	4.02	2.24 + 0.036*CL	2.34 + 0.034*CL	2.39 + 0.033*CL
	tPHL	3.97	2.36 + 0.032*CL	2.54 + 0.029*CL	2.68 + 0.027*CL
	tR	4.50	0.86 + 0.073*CL	0.81 + 0.074*CL	0.75 + 0.075*CL
	tF	3.45	1.03 + 0.049*CL	1.12 + 0.047*CL	1.16 + 0.046*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB16 Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.19	1.01 + 0.024*CL	1.01 + 0.024*CL	1.01 + 0.024*CL
	tPHL	1.79	0.91 + 0.018*CL	0.92 + 0.017*CL	0.92 + 0.017*CL
	tR	3.03	0.30 + 0.055*CL	0.27 + 0.055*CL	0.26 + 0.055*CL
	tF	1.95	0.26 + 0.034*CL	0.23 + 0.034*CL	0.21 + 0.035*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB16SM Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.43	2.05 + 0.028*CL	2.16 + 0.026*CL	2.23 + 0.025*CL
	tPHL	3.18	1.99 + 0.024*CL	2.11 + 0.021*CL	2.22 + 0.020*CL
	tR	3.47	0.78 + 0.054*CL	0.79 + 0.054*CL	0.77 + 0.054*CL
	tF	2.58	0.78 + 0.036*CL	0.85 + 0.035*CL	0.89 + 0.034*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB16SH Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.86	2.39 + 0.029*CL	2.54 + 0.026*CL	2.64 + 0.025*CL
	tPHL	3.72	2.43 + 0.026*CL	2.58 + 0.023*CL	2.72 + 0.021*CL
	tR	3.63	0.98 + 0.053*CL	0.98 + 0.053*CL	0.95 + 0.053*CL
	tF	2.81	0.98 + 0.037*CL	1.06 + 0.035*CL	1.13 + 0.034*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB20 Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	1.94	1.01 + 0.019*CL	1.01 + 0.019*CL	1.01 + 0.019*CL
	tPHL	1.63	0.93 + 0.014*CL	0.94 + 0.014*CL	0.94 + 0.014*CL
	tR	2.37	0.22 + 0.043*CL	0.21 + 0.043*CL	0.19 + 0.044*CL
	tF	1.54	0.22 + 0.026*CL	0.19 + 0.027*CL	0.18 + 0.027*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB20SM Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.46	1.43 + 0.021*CL	1.49 + 0.019*CL	1.52 + 0.019*CL
	tPHL	2.19	1.31 + 0.018*CL	1.39 + 0.016*CL	1.46 + 0.015*CL
	tR	2.63	0.54 + 0.042*CL	0.53 + 0.042*CL	0.50 + 0.042*CL
	tF	1.94	0.61 + 0.027*CL	0.63 + 0.026*CL	0.63 + 0.026*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOB20SH Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns] [CL: Capacitive Load [pF]]

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.78	1.65 + 0.023*CL	1.75 + 0.021*CL	1.82 + 0.020*CL
	tPHL	2.63	1.81 + 0.016*CL	1.87 + 0.015*CL	1.90 + 0.015*CL
	tR	2.84	0.74 + 0.042*CL	0.75 + 0.042*CL	0.74 + 0.042*CL
	tF	2.13	0.91 + 0.024*CL	0.87 + 0.025*CL	0.84 + 0.026*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

PHOB24 Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns] [CL: Capacitive Load [pF]]

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	1.90	1.09 + 0.016*CL	1.09 + 0.016*CL	1.09 + 0.016*CL
	tPHL	1.58	0.96 + 0.012*CL	0.97 + 0.012*CL	0.98 + 0.012*CL
	tR	2.10	0.23 + 0.037*CL	0.21 + 0.038*CL	0.19 + 0.038*CL
	tF	1.38	0.22 + 0.023*CL	0.21 + 0.023*CL	0.20 + 0.024*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

PHOB24SM Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns] [CL: Capacitive Load [pF]]

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.45	1.50 + 0.019*CL	1.57 + 0.018*CL	1.62 + 0.017*CL
	tPHL	2.23	1.39 + 0.017*CL	1.49 + 0.015*CL	1.57 + 0.014*CL
	tR	2.42	0.59 + 0.037*CL	0.60 + 0.036*CL	0.58 + 0.037*CL
	tF	1.88	0.70 + 0.024*CL	0.73 + 0.023*CL	0.73 + 0.023*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

PHOB24SH Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns] [CL: Capacitive Load [pF]]

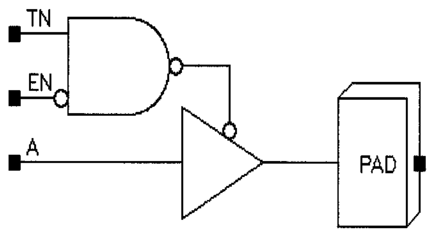
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.79	1.73 + 0.021*CL	1.84 + 0.019*CL	1.93 + 0.018*CL
	tPHL	2.73	1.97 + 0.015*CL	2.04 + 0.014*CL	2.08 + 0.013*CL
	tR	2.65	0.77 + 0.038*CL	0.82 + 0.037*CL	0.82 + 0.037*CL
	tF	2.09	1.07 + 0.020*CL	1.01 + 0.022*CL	0.97 + 0.022*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

Input: TN, EN, A
Output: PAD

Input Loading (SL): All:
- TN: 1.7474
- EN: 1.7474
- A: 3.4947

I/O Slots: 1



Symbol

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

Truth Table

PHOT1 Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	14.36	1.40 + 0.259*CL	1.40 + 0.259*CL	1.41 + 0.259*CL
	tPHL	10.94	1.33 + 0.192*CL	1.33 + 0.192*CL	1.33 + 0.192*CL
	tR	32.51	1.97 + 0.611*CL	1.97 + 0.611*CL	1.97 + 0.611*CL
	tF	20.35	1.18 + 0.383*CL	1.18 + 0.383*CL	1.18 + 0.383*CL
EN to PAD	tPLH	14.51	1.55 + 0.259*CL	1.55 + 0.259*CL	1.55 + 0.259*CL
	tPHL	11.20	1.64 + 0.191*CL	1.60 + 0.192*CL	1.60 + 0.192*CL
	tR	32.51	1.97 + 0.611*CL	1.97 + 0.611*CL	1.97 + 0.611*CL
	tF	20.53	1.37 + 0.383*CL	1.50 + 0.380*CL	1.22 + 0.384*CL
	tPLZ	0.81	0.81 + 0.000*CL	0.81 + -0.000*CL	0.81 + -0.000*CL
	tPHZ	0.79	0.79 + -0.000*CL	0.79 + -0.000*CL	0.79 + -0.000*CL
TN to PAD	tPLH	14.31	1.35 + 0.259*CL	1.35 + 0.259*CL	1.35 + 0.259*CL
	tPHL	10.96	1.43 + 0.191*CL	1.35 + 0.192*CL	1.38 + 0.192*CL
	tR	32.51	1.97 + 0.611*CL	1.97 + 0.611*CL	1.97 + 0.611*CL
	tF	20.47	1.16 + 0.386*CL	1.44 + 0.381*CL	0.99 + 0.386*CL
	tPLZ	1.02	1.02 + -0.000*CL	1.02 + -0.000*CL	1.02 + -0.000*CL
	tPHZ	0.99	0.99 + -0.000*CL	0.99 + -0.000*CL	0.99 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOT2 Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	7.55	1.06 + 0.130*CL	1.07 + 0.130*CL	1.07 + 0.130*CL
	tPHL	5.84	1.03 + 0.096*CL	1.03 + 0.096*CL	1.03 + 0.096*CL
	tR	16.27	1.00 + 0.305*CL	0.99 + 0.305*CL	1.00 + 0.305*CL
	tF	10.19	0.60 + 0.192*CL	0.60 + 0.192*CL	0.60 + 0.192*CL
EN to PAD	tPLH	7.69	1.20 + 0.130*CL	1.21 + 0.130*CL	1.20 + 0.130*CL
	tPHL	6.14	1.21 + 0.098*CL	1.37 + 0.095*CL	1.35 + 0.096*CL
	tR	16.27	1.00 + 0.305*CL	0.99 + 0.305*CL	1.00 + 0.305*CL
	tF	10.50	0.93 + 0.192*CL	1.14 + 0.187*CL	1.19 + 0.187*CL
	tPLZ	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL
	tPHZ	0.87	0.87 + 0.000*CL	0.87 + 0.000*CL	0.87 + -0.000*CL
TN to PAD	tPLH	7.49	1.01 + 0.130*CL	1.01 + 0.130*CL	1.01 + 0.130*CL
	tPHL	5.89	1.06 + 0.097*CL	1.11 + 0.096*CL	1.08 + 0.096*CL
	tR	16.27	1.00 + 0.305*CL	0.99 + 0.305*CL	1.00 + 0.305*CL
	tF	10.45	1.13 + 0.186*CL	0.98 + 0.189*CL	1.27 + 0.186*CL
	tPLZ	1.07	1.07 + -0.000*CL	1.07 + -0.000*CL	1.07 + -0.000*CL
	tPHZ	1.06	1.06 + -0.000*CL	1.06 + -0.000*CL	1.06 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOT4 Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	5.30	0.98 + 0.086*CL	0.98 + 0.086*CL	0.98 + 0.086*CL
	tPHL	4.16	0.96 + 0.064*CL	0.96 + 0.064*CL	0.96 + 0.064*CL
	tR	10.86	0.67 + 0.204*CL	0.67 + 0.204*CL	0.67 + 0.204*CL
	tF	6.80	0.41 + 0.128*CL	0.41 + 0.128*CL	0.41 + 0.128*CL
EN to PAD	tPLH	5.44	1.12 + 0.086*CL	1.12 + 0.086*CL	1.12 + 0.086*CL
	tPHL	4.48	1.18 + 0.066*CL	1.35 + 0.063*CL	1.19 + 0.065*CL
	tR	10.86	0.67 + 0.204*CL	0.67 + 0.204*CL	0.67 + 0.204*CL
	tF	7.25	1.10 + 0.123*CL	1.35 + 0.118*CL	0.45 + 0.129*CL
	tPLZ	0.93	0.93 + 0.000*CL	0.93 + -0.000*CL	0.93 + -0.000*CL
	tPHZ	0.95	0.93 + 0.000*CL	0.95 + 0.000*CL	0.95 + 0.000*CL
TN to PAD	tPLH	5.24	0.92 + 0.086*CL	0.92 + 0.086*CL	0.92 + 0.086*CL
	tPHL	4.22	0.97 + 0.065*CL	1.00 + 0.064*CL	1.12 + 0.063*CL
	tR	10.86	0.67 + 0.204*CL	0.67 + 0.204*CL	0.67 + 0.204*CL
	tF	7.04	0.71 + 0.127*CL	0.53 + 0.130*CL	1.01 + 0.124*CL
	tPLZ	1.13	1.13 + -0.000*CL	1.13 + 0.000*CL	1.13 + -0.000*CL
	tPHZ	1.14	1.14 + -0.000*CL	1.14 + -0.000*CL	1.14 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

PHOT4SM Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	5.70	1.37 + 0.086*CL	1.38 + 0.086*CL	1.38 + 0.086*CL
	tPHL	5.17	1.90 + 0.065*CL	1.95 + 0.064*CL	1.96 + 0.064*CL
	tR	10.89	0.75 + 0.203*CL	0.72 + 0.203*CL	0.70 + 0.204*CL
	tF	7.02	0.78 + 0.125*CL	0.73 + 0.126*CL	0.67 + 0.127*CL
EN to PAD	tPLH	5.81	1.48 + 0.087*CL	1.49 + 0.086*CL	1.49 + 0.086*CL
	tPHL	5.42	2.22 + 0.064*CL	2.16 + 0.065*CL	2.29 + 0.064*CL
	tR	10.89	0.75 + 0.203*CL	0.72 + 0.203*CL	0.70 + 0.204*CL
	tF	7.36	1.52 + 0.117*CL	1.19 + 0.123*CL	1.06 + 0.125*CL
	tPLZ	1.54	1.54 + -0.000*CL	1.54 + -0.000*CL	1.54 + -0.000*CL
	tPHZ	1.44	1.44 + -0.000*CL	1.44 + -0.000*CL	1.44 + -0.000*CL
TN to PAD	tPLH	5.62	1.29 + 0.087*CL	1.29 + 0.086*CL	1.30 + 0.086*CL
	tPHL	5.23	1.90 + 0.067*CL	2.05 + 0.064*CL	1.91 + 0.065*CL
	tR	10.89	0.75 + 0.203*CL	0.72 + 0.203*CL	0.70 + 0.204*CL
	tF	7.30	1.15 + 0.123*CL	1.17 + 0.123*CL	1.32 + 0.121*CL
	tPLZ	1.76	1.76 + -0.000*CL	1.76 + -0.000*CL	1.76 + -0.000*CL
	tPHZ	1.63	1.63 + -0.000*CL	1.63 + -0.000*CL	1.63 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

PHOT8 Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.12	0.96 + 0.043*CL	0.96 + 0.043*CL	0.96 + 0.043*CL
	tPHL	2.55	0.95 + 0.032*CL	0.95 + 0.032*CL	0.95 + 0.032*CL
	tR	5.45	0.37 + 0.102*CL	0.36 + 0.102*CL	0.36 + 0.102*CL
	tF	3.43	0.25 + 0.064*CL	0.24 + 0.064*CL	0.23 + 0.064*CL
EN to PAD	tPLH	3.26	1.10 + 0.043*CL	1.10 + 0.043*CL	1.10 + 0.043*CL
	tPHL	2.79	1.22 + 0.032*CL	1.16 + 0.033*CL	1.27 + 0.031*CL
	tR	5.45	0.37 + 0.102*CL	0.36 + 0.102*CL	0.36 + 0.102*CL
	tF	3.76	0.49 + 0.065*CL	0.76 + 0.060*CL	-0.19 + 0.072*CL
	tPLZ	1.13	1.13 + 0.000*CL	1.13 + 0.000*CL	1.13 + -0.000*CL
	tPHZ	1.17	1.17 + 0.000*CL	1.17 + 0.000*CL	1.17 + 0.000*CL
TN to PAD	tPLH	3.06	0.90 + 0.043*CL	0.90 + 0.043*CL	0.90 + 0.043*CL
	tPHL	2.58	0.94 + 0.033*CL	0.92 + 0.033*CL	1.00 + 0.032*CL
	tR	5.45	0.37 + 0.102*CL	0.36 + 0.102*CL	0.36 + 0.102*CL
	tF	3.69	0.44 + 0.065*CL	0.22 + 0.069*CL	1.64 + 0.052*CL
	tPLZ	1.27	1.27 + 0.000*CL	1.27 + 0.000*CL	1.27 + -0.000*CL
	tPHZ	1.35	1.35 + 0.000*CL	1.35 + 0.000*CL	1.35 + 0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOT8SM Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.84	1.61 + 0.044*CL	1.66 + 0.044*CL	1.67 + 0.043*CL
	tPHL	4.00	2.13 + 0.037*CL	2.27 + 0.035*CL	2.37 + 0.033*CL
	tR	5.65	0.69 + 0.099*CL	0.64 + 0.100*CL	0.59 + 0.101*CL
	tF	4.02	0.92 + 0.062*CL	0.95 + 0.062*CL	0.93 + 0.062*CL
EN to PAD	tPLH	3.94	1.72 + 0.044*CL	1.76 + 0.044*CL	1.78 + 0.043*CL
	tPHL	4.29	2.42 + 0.037*CL	2.60 + 0.034*CL	2.50 + 0.035*CL
	tR	5.65	0.69 + 0.099*CL	0.64 + 0.100*CL	0.59 + 0.101*CL
	tF	4.20	1.55 + 0.053*CL	1.09 + 0.062*CL	-0.07 + 0.077*CL
	tPLZ	1.52	1.52 + -0.000*CL	1.52 + -0.000*CL	1.52 + -0.000*CL
	tPHZ	1.47	1.47 + -0.000*CL	1.47 + -0.000*CL	1.47 + -0.000*CL
TN to PAD	tPLH	3.75	1.53 + 0.044*CL	1.57 + 0.044*CL	1.59 + 0.043*CL
	tPHL	4.12	2.00 + 0.042*CL	2.45 + 0.033*CL	2.53 + 0.032*CL
	tR	5.65	0.69 + 0.099*CL	0.64 + 0.100*CL	0.59 + 0.101*CL
	tF	4.50	1.49 + 0.060*CL	1.79 + 0.054*CL	0.36 + 0.072*CL
	tPLZ	1.72	1.72 + -0.000*CL	1.72 + -0.000*CL	1.72 + -0.000*CL
	tPHZ	1.66	1.66 + -0.000*CL	1.66 + -0.000*CL	1.66 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOT12 Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when tR and tF = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.62	1.00 + 0.032*CL	1.00 + 0.032*CL	1.00 + 0.032*CL
	tPHL	2.19	0.99 + 0.024*CL	0.99 + 0.024*CL	0.99 + 0.024*CL
	tR	4.11	0.31 + 0.076*CL	0.30 + 0.076*CL	0.29 + 0.076*CL
	tF	2.60	0.23 + 0.047*CL	0.22 + 0.048*CL	0.20 + 0.048*CL
EN to PAD	tPLH	2.76	1.13 + 0.033*CL	1.14 + 0.032*CL	1.14 + 0.032*CL
	tPHL	2.44	1.21 + 0.024*CL	1.24 + 0.024*CL	1.11 + 0.026*CL
	tR	4.11	0.31 + 0.076*CL	0.30 + 0.076*CL	0.29 + 0.076*CL
	tF	2.99	0.08 + 0.058*CL	0.84 + 0.043*CL	-0.49 + 0.060*CL
	tPLZ	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + -0.000*CL
	tPHZ	1.27	1.27 + -0.000*CL	1.27 + -0.000*CL	1.27 + -0.000*CL
TN to PAD	tPLH	2.56	0.94 + 0.033*CL	0.94 + 0.032*CL	0.94 + 0.032*CL
	tPHL	2.21	1.00 + 0.024*CL	1.00 + 0.024*CL	0.96 + 0.025*CL
	tR	4.11	0.31 + 0.076*CL	0.30 + 0.076*CL	0.29 + 0.076*CL
	tF	2.80	0.53 + 0.045*CL	0.44 + 0.047*CL	-0.03 + 0.053*CL
	tPLZ	1.39	1.39 + 0.000*CL	1.39 + 0.000*CL	1.39 + -0.000*CL
	tPHZ	1.48	1.48 + -0.000*CL	1.48 + -0.000*CL	1.48 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOT12SH Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when tR and tF = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.52	1.75 + 0.035*CL	1.84 + 0.034*CL	1.89 + 0.033*CL
	tPHL	3.95	2.33 + 0.032*CL	2.51 + 0.029*CL	2.66 + 0.027*CL
	tR	4.46	0.77 + 0.074*CL	0.74 + 0.074*CL	0.70 + 0.075*CL
	tF	3.45	1.03 + 0.049*CL	1.12 + 0.047*CL	1.16 + 0.046*CL
EN to PAD	tPLH	3.62	1.86 + 0.035*CL	1.95 + 0.034*CL	2.00 + 0.033*CL
	tPHL	4.22	2.66 + 0.031*CL	2.62 + 0.032*CL	2.81 + 0.030*CL
	tR	4.46	0.77 + 0.074*CL	0.74 + 0.074*CL	0.70 + 0.075*CL
	tF	4.39	1.58 + 0.056*CL	2.72 + 0.033*CL	0.64 + 0.059*CL
	tPLZ	1.52	1.52 + -0.000*CL	1.52 + -0.000*CL	1.52 + -0.000*CL
	tPHZ	1.47	1.47 + -0.000*CL	1.47 + -0.000*CL	1.47 + -0.000*CL
TN to PAD	tPLH	3.43	1.67 + 0.035*CL	1.75 + 0.034*CL	1.80 + 0.033*CL
	tPHL	4.02	2.22 + 0.036*CL	2.57 + 0.029*CL	2.79 + 0.026*CL
	tR	4.46	0.77 + 0.074*CL	0.74 + 0.074*CL	0.70 + 0.075*CL
	tF	4.01	1.87 + 0.043*CL	1.86 + 0.043*CL	1.74 + 0.045*CL
	tPLZ	1.72	1.72 + -0.000*CL	1.72 + -0.000*CL	1.72 + -0.000*CL
	tPHZ	1.66	1.66 + -0.000*CL	1.66 + -0.000*CL	1.66 + 0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOT12SM Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns] [CL: Capacitive Load [pF]]

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.32	1.59 + 0.035*CL	1.66 + 0.033*CL	1.69 + 0.033*CL
	tPHL	3.57	2.03 + 0.031*CL	2.18 + 0.028*CL	2.30 + 0.026*CL
	tR	4.38	0.67 + 0.074*CL	0.65 + 0.075*CL	0.61 + 0.075*CL
	tF	3.29	0.88 + 0.048*CL	0.96 + 0.047*CL	1.00 + 0.046*CL
EN to PAD	tPLH	3.42	1.69 + 0.035*CL	1.76 + 0.033*CL	1.80 + 0.033*CL
	tPHL	3.81	2.30 + 0.030*CL	2.25 + 0.031*CL	2.66 + 0.026*CL
	tR	4.38	0.68 + 0.074*CL	0.65 + 0.075*CL	0.61 + 0.075*CL
	tF	3.80	1.64 + 0.043*CL	1.39 + 0.048*CL	2.41 + 0.035*CL
	tPLZ	1.75	1.75 + -0.000*CL	1.75 + -0.000*CL	1.75 + -0.000*CL
	tPHZ	1.84	1.84 + 0.000*CL	1.84 + 0.000*CL	1.84 + -0.000*CL
TN to PAD	tPLH	3.23	1.50 + 0.035*CL	1.57 + 0.033*CL	1.61 + 0.033*CL
	tPHL	3.60	1.97 + 0.033*CL	2.16 + 0.029*CL	2.32 + 0.027*CL
	tR	4.38	0.68 + 0.074*CL	0.65 + 0.075*CL	0.61 + 0.075*CL
	tF	4.08	0.50 + 0.072*CL	2.03 + 0.041*CL	2.45 + 0.036*CL
	tPLZ	1.94	1.94 + -0.000*CL	1.94 + -0.000*CL	1.94 + -0.000*CL
	tPHZ	2.10	2.10 + 0.000*CL	2.10 + 0.000*CL	2.10 + 0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOT16 Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns] [CL: Capacitive Load [pF]]

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.26	1.08 + 0.024*CL	1.09 + 0.024*CL	1.09 + 0.024*CL
	tPHL	1.94	1.07 + 0.018*CL	1.07 + 0.017*CL	1.07 + 0.017*CL
	tR	3.03	0.30 + 0.055*CL	0.27 + 0.055*CL	0.26 + 0.055*CL
	tF	1.95	0.27 + 0.034*CL	0.24 + 0.034*CL	0.21 + 0.035*CL
EN to PAD	tPLH	2.39	1.20 + 0.024*CL	1.21 + 0.024*CL	1.21 + 0.024*CL
	tPHL	2.17	1.31 + 0.017*CL	1.24 + 0.019*CL	1.41 + 0.017*CL
	tR	3.03	0.31 + 0.054*CL	0.27 + 0.055*CL	0.26 + 0.055*CL
	tF	2.08	0.53 + 0.031*CL	-0.13 + 0.044*CL	1.64 + 0.022*CL
	tPLZ	1.37	1.37 + 0.000*CL	1.37 + 0.000*CL	1.37 + 0.000*CL
	tPHZ	1.54	1.54 + 0.000*CL	1.54 + 0.000*CL	1.54 + 0.000*CL
TN to PAD	tPLH	2.20	1.01 + 0.024*CL	1.02 + 0.024*CL	1.02 + 0.024*CL
	tPHL	1.94	1.08 + 0.017*CL	1.02 + 0.018*CL	1.10 + 0.017*CL
	tR	3.03	0.30 + 0.055*CL	0.28 + 0.055*CL	0.26 + 0.055*CL
	tF	2.06	0.38 + 0.034*CL	-0.13 + 0.044*CL	0.85 + 0.032*CL
	tPLZ	1.53	1.53 + 0.000*CL	1.53 + 0.000*CL	1.53 + -0.000*CL
	tPHZ	1.67	1.67 + -0.000*CL	1.60 + 0.002*CL	1.72 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOT16SH Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.37	1.92 + 0.029*CL	2.06 + 0.026*CL	2.15 + 0.025*CL
	tPHL	3.69	2.40 + 0.026*CL	2.56 + 0.023*CL	2.69 + 0.021*CL
	tR	3.58	0.89 + 0.054*CL	0.91 + 0.054*CL	0.89 + 0.054*CL
	tF	2.81	0.98 + 0.037*CL	1.06 + 0.035*CL	1.12 + 0.034*CL
EN to PAD	tPLH	3.47	2.02 + 0.029*CL	2.16 + 0.026*CL	2.25 + 0.025*CL
	tPHL	3.93	2.45 + 0.029*CL	2.78 + 0.023*CL	2.82 + 0.022*CL
	tR	3.59	0.89 + 0.054*CL	0.91 + 0.054*CL	0.89 + 0.054*CL
	tF	3.72	0.68 + 0.061*CL	2.27 + 0.029*CL	1.71 + 0.036*CL
	tPLZ	1.51	1.51 + -0.000*CL	1.51 + -0.000*CL	1.51 + -0.000*CL
	tPHZ	1.47	1.47 + -0.000*CL	1.47 + -0.000*CL	1.47 + -0.000*CL
TN to PAD	tPLH	3.28	1.83 + 0.029*CL	1.96 + 0.026*CL	2.06 + 0.025*CL
	tPHL	3.72	2.12 + 0.032*CL	2.59 + 0.023*CL	2.72 + 0.021*CL
	tR	3.59	0.89 + 0.054*CL	0.91 + 0.054*CL	0.89 + 0.054*CL
	tF	3.43	1.62 + 0.036*CL	1.39 + 0.041*CL	2.33 + 0.029*CL
	tPLZ	1.69	1.70 + -0.000*CL	1.69 + -0.000*CL	1.69 + -0.000*CL
	tPHZ	1.66	1.66 + -0.000*CL	1.66 + -0.000*CL	1.66 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

PHOT16SM Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	3.01	1.64 + 0.027*CL	1.74 + 0.025*CL	1.81 + 0.025*CL
	tPHL	3.15	1.96 + 0.024*CL	2.09 + 0.021*CL	2.19 + 0.020*CL
	tR	3.41	0.70 + 0.054*CL	0.72 + 0.054*CL	0.71 + 0.054*CL
	tF	2.57	0.77 + 0.036*CL	0.84 + 0.035*CL	0.89 + 0.034*CL
EN to PAD	tPLH	3.11	1.74 + 0.027*CL	1.84 + 0.025*CL	1.91 + 0.025*CL
	tPHL	3.37	2.09 + 0.025*CL	2.22 + 0.023*CL	2.40 + 0.021*CL
	tR	3.41	0.71 + 0.054*CL	0.72 + 0.054*CL	0.71 + 0.054*CL
	tF	3.01	1.19 + 0.036*CL	0.79 + 0.044*CL	2.16 + 0.027*CL
	tPLZ	1.95	1.95 + -0.000*CL	1.95 + -0.000*CL	1.95 + -0.000*CL
	tPHZ	2.25	2.25 + -0.000*CL	2.25 + -0.000*CL	2.25 + -0.000*CL
TN to PAD	tPLH	2.92	1.54 + 0.027*CL	1.65 + 0.025*CL	1.72 + 0.025*CL
	tPHL	3.17	1.79 + 0.028*CL	2.10 + 0.021*CL	2.21 + 0.020*CL
	tR	3.41	0.71 + 0.054*CL	0.72 + 0.054*CL	0.71 + 0.054*CL
	tF	3.07	1.05 + 0.040*CL	1.00 + 0.041*CL	2.46 + 0.023*CL
	tPLZ	2.15	2.15 + -0.000*CL	2.15 + -0.000*CL	2.15 + -0.000*CL
	tPHZ	2.40	2.40 + -0.000*CL	2.40 + -0.000*CL	2.40 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

PHOT20 Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	1.89	0.96 + 0.019*CL	0.96 + 0.019*CL	0.96 + 0.019*CL
	tPHL	1.72	1.03 + 0.014*CL	1.03 + 0.014*CL	1.04 + 0.014*CL
	tR	2.37	0.22 + 0.043*CL	0.20 + 0.043*CL	0.19 + 0.044*CL
	tF	1.54	0.22 + 0.026*CL	0.20 + 0.027*CL	0.18 + 0.027*CL
EN to PAD	tPLH	2.02	1.09 + 0.019*CL	1.10 + 0.019*CL	1.10 + 0.019*CL
	tPHL	1.96	1.25 + 0.014*CL	1.25 + 0.014*CL	1.33 + 0.013*CL
	tR	2.37	0.22 + 0.043*CL	0.20 + 0.043*CL	0.19 + 0.044*CL
	tF	1.66	0.43 + 0.025*CL	0.19 + 0.029*CL	0.57 + 0.025*CL
	tPLZ	1.24	1.24 + 0.000*CL	1.24 + 0.000*CL	1.24 + 0.000*CL
	tPHZ	1.36	1.36 + 0.000*CL	1.36 + 0.000*CL	1.36 + -0.000*CL
TN to PAD	tPLH	1.83	0.90 + 0.019*CL	0.90 + 0.019*CL	0.90 + 0.019*CL
	tPHL	1.73	1.00 + 0.015*CL	1.05 + 0.014*CL	1.05 + 0.014*CL
	tR	2.37	0.22 + 0.043*CL	0.20 + 0.043*CL	0.19 + 0.044*CL
	tF	1.64	0.42 + 0.024*CL	0.25 + 0.028*CL	0.28 + 0.028*CL
	tPLZ	1.46	1.46 + 0.000*CL	1.46 + 0.000*CL	1.46 + 0.000*CL
	tPHZ	1.58	1.58 + 0.000*CL	1.58 + 0.000*CL	1.58 + 0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOT20SH Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.68	1.55 + 0.023*CL	1.65 + 0.021*CL	1.73 + 0.020*CL
	tPHL	2.70	1.89 + 0.016*CL	1.95 + 0.015*CL	1.98 + 0.015*CL
	tR	2.82	0.72 + 0.042*CL	0.73 + 0.042*CL	0.72 + 0.042*CL
	tF	2.14	0.94 + 0.024*CL	0.89 + 0.025*CL	0.86 + 0.025*CL
EN to PAD	tPLH	2.80	1.65 + 0.023*CL	1.76 + 0.021*CL	1.84 + 0.020*CL
	tPHL	2.76	1.83 + 0.019*CL	1.70 + 0.021*CL	2.17 + 0.015*CL
	tR	2.83	0.74 + 0.042*CL	0.74 + 0.042*CL	0.72 + 0.042*CL
	tF	2.61	1.26 + 0.027*CL	1.26 + 0.027*CL	0.01 + 0.043*CL
	tPLZ	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
	tPHZ	1.24	1.24 + -0.000*CL	1.24 + -0.000*CL	1.24 + -0.000*CL
TN to PAD	tPLH	2.60	1.46 + 0.023*CL	1.57 + 0.021*CL	1.65 + 0.020*CL
	tPHL	2.55	1.55 + 0.020*CL	1.57 + 0.019*CL	1.94 + 0.015*CL
	tR	2.83	0.74 + 0.042*CL	0.74 + 0.042*CL	0.72 + 0.042*CL
	tF	2.67	1.03 + 0.033*CL	1.56 + 0.022*CL	-0.09 + 0.043*CL
	tPLZ	1.08	1.08 + -0.000*CL	1.08 + -0.000*CL	1.08 + -0.000*CL
	tPHZ	1.46	1.46 + 0.000*CL	1.46 + 0.000*CL	1.46 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOT24SH Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.69	1.63 + 0.021*CL	1.74 + 0.019*CL	1.83 + 0.018*CL
	tPHL	2.80	2.05 + 0.015*CL	2.12 + 0.014*CL	2.16 + 0.013*CL
	tR	2.63	0.76 + 0.038*CL	0.80 + 0.037*CL	0.80 + 0.037*CL
	tF	2.11	1.11 + 0.020*CL	1.03 + 0.022*CL	1.00 + 0.022*CL
EN to PAD	tPLH	2.80	1.72 + 0.022*CL	1.84 + 0.019*CL	1.94 + 0.018*CL
	tPHL	2.77	1.90 + 0.017*CL	1.77 + 0.020*CL	2.16 + 0.015*CL
	tR	2.65	0.81 + 0.037*CL	0.82 + 0.037*CL	0.82 + 0.037*CL
	tF	2.58	1.04 + 0.031*CL	1.63 + 0.019*CL	-0.56 + 0.046*CL
	tPLZ	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
	tPHZ	1.24	1.24 + -0.000*CL	1.24 + -0.000*CL	1.24 + -0.000*CL
TN to PAD	tPLH	2.60	1.52 + 0.022*CL	1.65 + 0.019*CL	1.74 + 0.018*CL
	tPHL	2.57	1.60 + 0.019*CL	1.66 + 0.018*CL	1.92 + 0.015*CL
	tR	2.65	0.81 + 0.037*CL	0.82 + 0.037*CL	0.82 + 0.037*CL
	tF	2.61	1.15 + 0.029*CL	1.51 + 0.022*CL	0.41 + 0.036*CL
	tPLZ	1.08	1.08 + -0.000*CL	1.08 + -0.000*CL	1.08 + -0.000*CL
	tPHZ	1.46	1.46 + 0.000*CL	1.46 + 0.000*CL	1.46 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

PHOT24SM Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

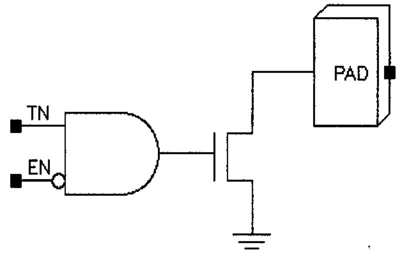
Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to PAD	tPLH	2.29	1.33 + 0.019*CL	1.41 + 0.018*CL	1.46 + 0.017*CL
	tPHL	2.30	1.47 + 0.017*CL	1.55 + 0.015*CL	1.63 + 0.014*CL
	tR	2.40	0.56 + 0.037*CL	0.57 + 0.037*CL	0.55 + 0.037*CL
	tF	1.88	0.71 + 0.023*CL	0.73 + 0.023*CL	0.74 + 0.023*CL
EN to PAD	tPLH	2.41	1.44 + 0.019*CL	1.52 + 0.018*CL	1.58 + 0.017*CL
	tPHL	2.50	1.60 + 0.018*CL	1.70 + 0.016*CL	1.51 + 0.018*CL
	tR	2.41	0.59 + 0.036*CL	0.58 + 0.037*CL	0.56 + 0.037*CL
	tF	2.50	0.28 + 0.044*CL	1.72 + 0.015*CL	0.26 + 0.034*CL
	tPLZ	1.06	1.06 + 0.000*CL	1.06 + 0.000*CL	1.06 + -0.000*CL
	tPHZ	1.06	1.06 + -0.000*CL	1.06 + -0.000*CL	1.06 + -0.000*CL
TN to PAD	tPLH	2.21	1.25 + 0.019*CL	1.33 + 0.018*CL	1.39 + 0.017*CL
	tPHL	2.26	1.35 + 0.018*CL	1.44 + 0.016*CL	1.44 + 0.016*CL
	tR	2.41	0.59 + 0.036*CL	0.58 + 0.036*CL	0.56 + 0.037*CL
	tF	2.36	1.07 + 0.026*CL	1.17 + 0.024*CL	1.05 + 0.025*CL
	tPLZ	1.26	1.26 + 0.000*CL	1.26 + 0.000*CL	1.26 + -0.000*CL
	tPHZ	1.28	1.28 + -0.000*CL	1.28 + -0.000*CL	1.28 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

Input: TN, EN
Output: PAD

Input Loading (SL): All:
- TN: 1.7474
- EN: 1.7474

I/O Slots: 1



Symbol

EN	TN	PAD
0	1	0
x	0	Hi-Z
1	x	Hi-Z

Truth Table

PHOD1 Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	11.10	1.49 + 0.192*CL	1.49 + 0.192*CL	1.49 + 0.192*CL
	tF	20.35	1.18 + 0.383*CL	1.18 + 0.383*CL	1.18 + 0.383*CL
	tPLZ	0.70	0.70 + -0.000*CL	0.70 + -0.000*CL	0.70 + -0.000*CL
TN to PAD	tPHL	10.87	1.25 + 0.192*CL	1.25 + 0.192*CL	1.25 + 0.192*CL
	tF	20.35	1.18 + 0.383*CL	1.18 + 0.383*CL	1.18 + 0.383*CL
	tPLZ	0.89	0.89 + 0.000*CL	0.89 + -0.000*CL	0.89 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

PHOD2 Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	5.99	1.18 + 0.096*CL	1.18 + 0.096*CL	1.18 + 0.096*CL
	tF	10.18	0.60 + 0.192*CL	0.60 + 0.192*CL	0.59 + 0.192*CL
	tPLZ	0.75	0.75 + -0.000*CL	0.75 + -0.000*CL	0.75 + -0.000*CL
TN to PAD	tPHL	5.76	0.95 + 0.096*CL	0.95 + 0.096*CL	0.95 + 0.096*CL
	tF	10.18	0.60 + 0.192*CL	0.60 + 0.192*CL	0.59 + 0.192*CL
	tPLZ	0.94	0.94 + -0.000*CL	0.94 + -0.000*CL	0.94 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD4 Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	4.33	1.12 + 0.064*CL	1.12 + 0.064*CL	1.12 + 0.064*CL
	tF	6.80	0.41 + 0.128*CL	0.41 + 0.128*CL	0.41 + 0.128*CL
	tPLZ	0.77	0.77 + -0.000*CL	0.77 + -0.000*CL	0.77 + -0.000*CL
TN to PAD	tPHL	4.10	0.89 + 0.064*CL	0.89 + 0.064*CL	0.89 + 0.064*CL
	tF	6.80	0.41 + 0.128*CL	0.41 + 0.128*CL	0.41 + 0.128*CL
	tPLZ	0.97	0.97 + -0.000*CL	0.97 + -0.000*CL	0.97 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD4SM Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns(CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	4.58	1.37 + 0.064*CL	1.37 + 0.064*CL	1.37 + 0.064*CL
	tF	6.82	0.45 + 0.127*CL	0.43 + 0.128*CL	0.42 + 0.128*CL
	tPLZ	0.78	0.78 + -0.000*CL	0.78 + -0.000*CL	0.78 + -0.000*CL
TN to PAD	tPHL	4.34	1.13 + 0.064*CL	1.14 + 0.064*CL	1.14 + 0.064*CL
	tF	6.82	0.45 + 0.127*CL	0.43 + 0.128*CL	0.42 + 0.128*CL
	tPLZ	0.98	0.98 + -0.000*CL	0.98 + -0.000*CL	0.98 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD8 Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.72	1.11 + 0.032*CL	1.11 + 0.032*CL	1.11 + 0.032*CL
	tF	3.43	0.25 + 0.064*CL	0.24 + 0.064*CL	0.23 + 0.064*CL
	tPLZ	0.92	0.92 + -0.000*CL	0.92 + -0.000*CL	0.92 + -0.000*CL
TN to PAD	tPHL	2.48	0.88 + 0.032*CL	0.88 + 0.032*CL	0.88 + 0.032*CL
	tF	3.43	0.25 + 0.064*CL	0.24 + 0.064*CL	0.23 + 0.064*CL
	tPLZ	1.11	1.11 + -0.000*CL	1.11 + -0.000*CL	1.11 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD8SM Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	3.24	1.60 + 0.033*CL	1.63 + 0.032*CL	1.64 + 0.032*CL
	tF	3.57	0.50 + 0.062*CL	0.45 + 0.063*CL	0.40 + 0.063*CL
	tPLZ	0.78	0.78 + 0.000*CL	0.78 + -0.000*CL	0.78 + -0.000*CL
TN to PAD	tPHL	3.01	1.36 + 0.033*CL	1.39 + 0.032*CL	1.40 + 0.032*CL
	tF	3.57	0.50 + 0.062*CL	0.45 + 0.063*CL	0.40 + 0.063*CL
	tPLZ	0.98	0.98 + -0.000*CL	0.98 + -0.000*CL	0.97 + 0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD12 Switching Characteristics

[Delays for typical process, 25.00°C, lvdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.35	1.14 + 0.024*CL	1.15 + 0.024*CL	1.15 + 0.024*CL
	tF	2.60	0.24 + 0.047*CL	0.22 + 0.048*CL	0.21 + 0.048*CL
	tPLZ	1.02	1.02 + -0.000*CL	1.02 + -0.000*CL	1.02 + -0.000*CL
TN to PAD	tPHL	2.12	0.91 + 0.024*CL	0.91 + 0.024*CL	0.91 + 0.024*CL
	tF	2.60	0.24 + 0.047*CL	0.22 + 0.048*CL	0.21 + 0.048*CL
	tPLZ	1.21	1.21 + -0.000*CL	1.21 + -0.000*CL	1.21 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD12SH Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns[CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	3.02	1.71 + 0.026*CL	1.78 + 0.025*CL	1.81 + 0.024*CL
	tF	2.86	0.59 + 0.045*CL	0.55 + 0.046*CL	0.52 + 0.047*CL
	tPLZ	0.73	0.73 + 0.000*CL	0.73 + -0.000*CL	0.73 + -0.000*CL
TN to PAD	tPHL	2.78	1.47 + 0.026*CL	1.54 + 0.025*CL	1.58 + 0.024*CL
	tF	2.86	0.59 + 0.045*CL	0.55 + 0.046*CL	0.51 + 0.047*CL
	tPLZ	0.92	0.92 + -0.000*CL	0.92 + -0.000*CL	0.92 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD12SM Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns[CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.82	1.53 + 0.026*CL	1.59 + 0.025*CL	1.62 + 0.024*CL
	tF	2.81	0.54 + 0.045*CL	0.50 + 0.046*CL	0.46 + 0.047*CL
	tPLZ	0.78	0.78 + -0.000*CL	0.78 + -0.000*CL	0.78 + -0.000*CL
TN to PAD	tPHL	2.59	1.30 + 0.026*CL	1.36 + 0.025*CL	1.39 + 0.024*CL
	tF	2.81	0.54 + 0.045*CL	0.50 + 0.046*CL	0.46 + 0.047*CL
	tPLZ	0.98	0.98 + -0.000*CL	0.98 + -0.000*CL	0.98 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD16 Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns[CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.10	1.20 + 0.018*CL	1.21 + 0.018*CL	1.22 + 0.018*CL
	tF	1.95	0.26 + 0.034*CL	0.24 + 0.034*CL	0.22 + 0.034*CL
	tPLZ	1.16	1.16 + -0.000*CL	1.16 + -0.000*CL	1.16 + -0.000*CL
TN to PAD	tPHL	1.86	0.97 + 0.018*CL	0.98 + 0.018*CL	0.98 + 0.018*CL
	tF	1.95	0.26 + 0.034*CL	0.24 + 0.034*CL	0.22 + 0.034*CL
	tPLZ	1.36	1.36 + -0.000*CL	1.36 + -0.000*CL	1.36 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD16SM Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.58	1.53 + 0.021*CL	1.63 + 0.019*CL	1.69 + 0.018*CL
	tF	2.27	0.63 + 0.033*CL	0.62 + 0.033*CL	0.60 + 0.033*CL
	tPLZ	0.83	0.84 + -0.000*CL	0.84 + -0.000*CL	0.83 + -0.000*CL
TN to PAD	tPHL	2.35	1.30 + 0.021*CL	1.39 + 0.019*CL	1.46 + 0.018*CL
	tF	2.27	0.63 + 0.033*CL	0.62 + 0.033*CL	0.60 + 0.033*CL
	tPLZ	1.03	1.03 + -0.000*CL	1.03 + -0.000*CL	1.03 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD16SH Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.94	1.84 + 0.022*CL	1.95 + 0.020*CL	2.03 + 0.019*CL
	tF	2.37	0.70 + 0.033*CL	0.71 + 0.033*CL	0.70 + 0.033*CL
	tPLZ	0.73	0.73 + -0.000*CL	0.73 + 0.000*CL	0.73 + -0.000*CL
TN to PAD	tPHL	2.70	1.61 + 0.022*CL	1.72 + 0.020*CL	1.80 + 0.019*CL
	tF	2.37	0.70 + 0.033*CL	0.71 + 0.033*CL	0.70 + 0.033*CL
	tPLZ	0.92	0.92 + -0.000*CL	0.92 + -0.000*CL	0.92 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD20 Switching Characteristics

[Delays for typical process, 25.00°C, Ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	1.98	1.25 + 0.015*CL	1.28 + 0.014*CL	1.29 + 0.014*CL
	tF	1.60	0.28 + 0.026*CL	0.27 + 0.027*CL	0.25 + 0.027*CL
	tPLZ	1.31	1.31 + -0.000*CL	1.31 + -0.000*CL	1.31 + -0.000*CL
TN to PAD	tPHL	1.75	1.01 + 0.015*CL	1.04 + 0.014*CL	1.06 + 0.014*CL
	tF	1.60	0.28 + 0.026*CL	0.27 + 0.027*CL	0.25 + 0.027*CL
	tPLZ	1.51	1.51 + -0.000*CL	1.51 + -0.000*CL	1.51 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD20SM Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.45	1.51 + 0.019*CL	1.63 + 0.016*CL	1.72 + 0.015*CL
	tF	2.01	0.67 + 0.027*CL	0.71 + 0.026*CL	0.72 + 0.026*CL
	tPLZ	0.89	0.89 + -0.000*CL	0.89 + -0.000*CL	0.89 + -0.000*CL
TN to PAD	tPHL	2.22	1.27 + 0.019*CL	1.40 + 0.016*CL	1.49 + 0.015*CL
	tF	2.01	0.67 + 0.027*CL	0.71 + 0.026*CL	0.72 + 0.026*CL
	tPLZ	1.08	1.08 + -0.000*CL	1.08 + -0.000*CL	1.08 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD20SH Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.76	1.77 + 0.020*CL	1.91 + 0.017*CL	2.01 + 0.016*CL
	tF	2.13	0.83 + 0.026*CL	0.84 + 0.026*CL	0.83 + 0.026*CL
	tPLZ	0.78	0.78 + -0.000*CL	0.78 + -0.000*CL	0.78 + -0.000*CL
TN to PAD	tPHL	2.53	1.54 + 0.020*CL	1.67 + 0.017*CL	1.78 + 0.016*CL
	tF	2.13	0.83 + 0.026*CL	0.84 + 0.026*CL	0.83 + 0.026*CL
	tPLZ	0.98	0.98 + -0.000*CL	0.98 + -0.000*CL	0.98 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD24 Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when t_R and t_F = 0.80ns, CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	1.94	1.28 + 0.013*CL	1.32 + 0.013*CL	1.34 + 0.012*CL
	tF	1.45	0.30 + 0.023*CL	0.30 + 0.023*CL	0.28 + 0.023*CL
	tPLZ	1.41	1.41 + -0.000*CL	1.41 + -0.000*CL	1.41 + -0.000*CL
TN to PAD	tPHL	1.71	1.04 + 0.013*CL	1.08 + 0.013*CL	1.10 + 0.012*CL
	tF	1.45	0.30 + 0.023*CL	0.30 + 0.023*CL	0.28 + 0.023*CL
	tPLZ	1.61	1.61 + -0.000*CL	1.61 + -0.000*CL	1.61 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≦ CL ≦ 80.00, *Range3 : 80.00 < CL

PHOD24SM Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when tR and tF = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.48	1.55 + 0.019*CL	1.70 + 0.016*CL	1.81 + 0.014*CL
	tF	1.96	0.75 + 0.024*CL	0.82 + 0.023*CL	0.84 + 0.023*CL
	tPLZ	0.89	0.89 + -0.000*CL	0.89 + -0.000*CL	0.89 + -0.000*CL
TN to PAD	tPHL	2.25	1.32 + 0.019*CL	1.46 + 0.016*CL	1.57 + 0.014*CL
	tF	1.95	0.75 + 0.024*CL	0.82 + 0.023*CL	0.84 + 0.023*CL
	tPLZ	1.08	1.08 + -0.000*CL	1.08 + -0.000*CL	1.08 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

PHOD24SH Switching Characteristics

[Delays for typical process, 25.00°C, ivdd=3.30V, ovdd=5.00V, when tR and tF = 0.80ns] (CL: Capacitive Load [pF])

Path	Parameter	Delay [ns] CL=50.00 pF	Delay Equations [ns]		
			Range1*	Range2*	Range3*
EN to PAD	tPHL	2.79	1.83 + 0.019*CL	1.98 + 0.016*CL	2.10 + 0.015*CL
	tF	2.06	0.91 + 0.023*CL	0.92 + 0.023*CL	0.93 + 0.023*CL
	tPLZ	0.78	0.78 + -0.000*CL	0.78 + -0.000*CL	0.78 + -0.000*CL
TN to PAD	tPHL	2.56	1.59 + 0.019*CL	1.75 + 0.016*CL	1.87 + 0.015*CL
	tF	2.06	0.91 + 0.023*CL	0.92 + 0.023*CL	0.93 + 0.023*CL
	tPLZ	0.98	0.98 + -0.000*CL	0.98 + -0.000*CL	0.98 + -0.000*CL

*Range1 : CL < 50.00, *Range2 : 50.00 ≤ CL ≤ 80.00, *Range3 : 80.00 < CL

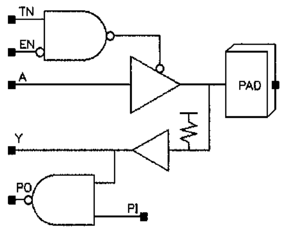
4.5 5.0V Interface Bidirectional I/O Buffers

5.0V Interface Bidirectional Buffer Naming Conventions

PHB w x z u v w

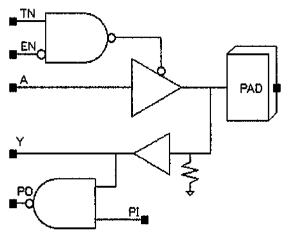
where x and z define the input buffer characteristics, and u, v, and w define the output buffer characteristics, as described previously.

e.g. PHBSUT12SM is a 5.0V Interface Schmitt Trigger input buffer and tristate output buffer with12 mA drive and medium slew-rate control



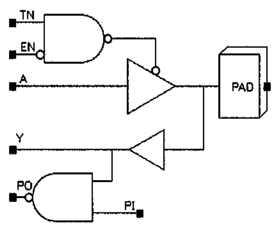
PHBxUTvw

Bidirectional Tri-state Buffer with Pull-Up, Non-Inverting Input



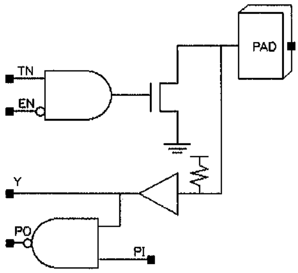
PHBxDTvw

Bidirectional Tri-state Buffer with Pull-Down, Non-Inverting Input



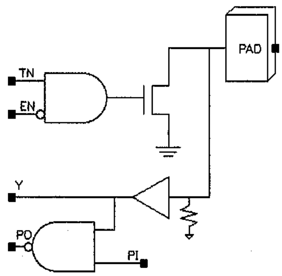
PHBxTvw

Bidirectional Tri-state Buffer with Non-Inverting Input



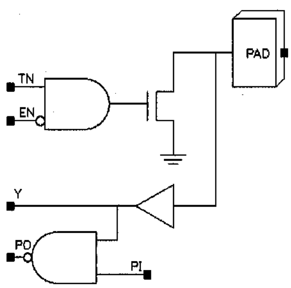
PHBxUDvw

Bidirectional Open Drain Buffer with Pull-Up, Non-Inverting Input



PHBxDDvw

Bidirectional Open Drain Buffer with Pull-Down, Non-Inverting Input



PHBxDvw

Bidirectional Open Drain Buffer with Non-Inverting Input