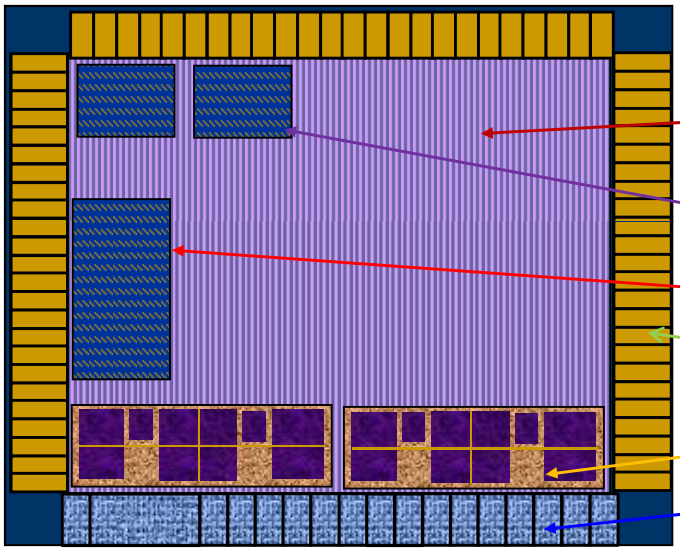
Embedded Array

- Structure ASIC architecture
- Split-the-Middle choice (ASIC/FPGA)
- Embedded Aspec logic IP
- Embedded Silicon IP
- Platform ASIC (CPU,high speed)
- Integration
  - -Clock domain
  - -Preconfigured DFT (Scan,BIST)
  - -Power distribution



- Metal Programmable
  - .Aspec Logic array
- Embedded Silicon IP
  - .Memory
  - .mProcessor
  - .Standard I/Os
  - .Special functions
  - .Special I/Os

Metal Programmmable

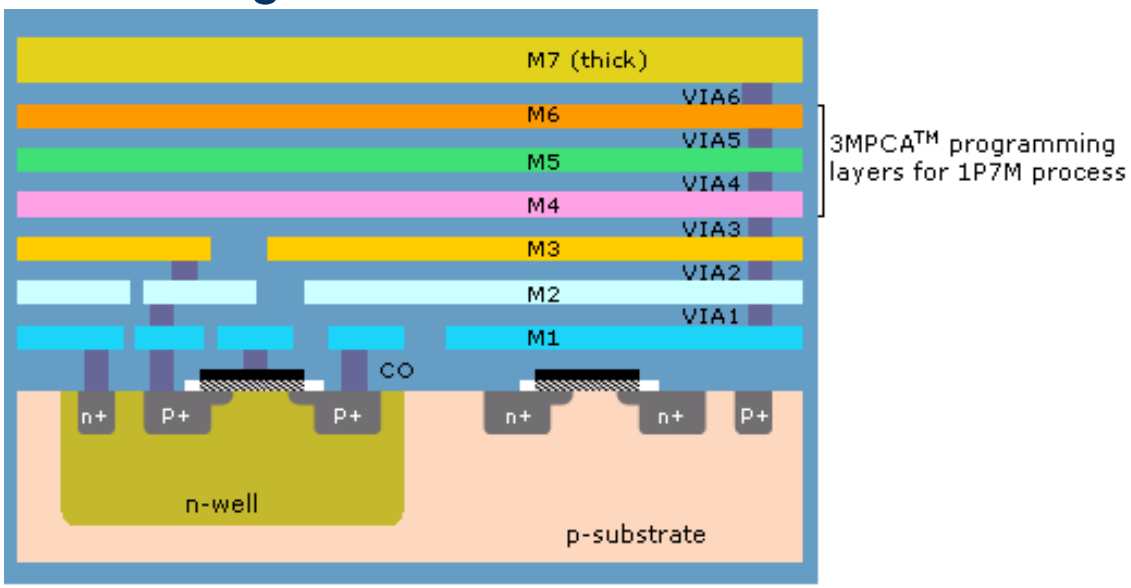


Figure 1: IC Fabrication Mask Layers