CONIO_3 Bi-directional I/O Cell

CONIO_3 : Non inverting CMOS buffer with a TTL receiver. The cell can be configured to be a four to twenty four milliamp output in four milliamp steps , a receiver with or without pull up or pull down devices or as a bi-directional buffer.

Supply voltages: The circuit requires two positive operating supplies. The first is VD5 which is nominally 5.0V but the circuit also functions when VD5 is 3.3V. The second supply is a 3.3V chip core supply. There are two return paths. VSSPST is the return for the output transistors while VSS is the return for the control circuits. Both VSSPST and VSS contact the substrate.

Signals:

1. **PAD:** Bond pad - driver output/ receiver input
2. **USER_IN:** receiver output to core
3. **PULLUP_CNTRL:** high enables a nominal 100K Ohm pull up circuit
4. **PULLDOWN_CNTRL:** high enables a nominal 100K Ohm pull down circuit
5. **USER_OUT:** data input to buffer
6. **SLEW_CNTRL:** high for high current slew rate, low for low current slew rate.
7. **CNTRL_4MA_1:** high enables the first 4mA buffer section.
8. **CNTRL_4MA_2:** high enables the second 4mA buffer section.
9. **CNTRL_8MA_1:** high enables the first 8mA buffer section.
10. **CNTRL_8MA_2:** high enables the second 8mA buffer section
11. **OUTPUT_ENABLE:** high enables all buffer outputs that are selected through the control signals.

PORTS: All are located with Y=364µm to Y=365µm. The ports are 2.5µm wide by 1.0µm tall

1. **USER_IN:** X=5.6µm to X=8.10µm
2. **PULLUP_CNTRL:** X=49.3µm to X=51.8µm
3. **PULLDOWN_CNTRL:** X=52.7µm to X=55.2µm
4. **USER_OUT:** X=33.0µm to X=35.5µm
5. **SLEW_CNTRL:** X=70.9µm to X=73.4µm
6. **CNTRL_4MA_1:** X=67.5µm to X=70.0µm
7. **CNTRL_4MA_2:** X=58.4µm to X=60.9µm
8. **CNTRL_8MA_1:** X=43.6µm to X=46.1µm
9. **CNTRL_8MA_2:** X=40.2µm to X=42.7µm
10. **OUTPUT_ENABLE:** X=61.8µm to X=64.3µm

CONIO_3 Bi-directional I/O Cell

BUFFER CONFIGURATION: The buffer can be configured as a single output with drive levels of 4mA, 8mA, 12mA, 16mA, 20mA, or 24mA. There is no preferred control signal configuration for any buffer type but timing data has been confirmed for only one control signal configuration for each buffer type. The table shows all the signal configurations that can be utilized to get any buffer drive level. No timing information has been generated for the shaded sections of the table. To utilize these configurations all timing figures given in the data sheets or models need to be multiplied by 1.1

	Buffer Drive Level in Milliamps														
Control Signal	4	4	8	8	8	12	12	12	12	16	16	16	20	20	24
CNTRL_4MA_1	H	L	L	L	H	H	H	L	L	L	H	H	H	L	H
CNTRL_4MA_2	L	H	L	L	H	L	L	H	H	L	H	H	L	H	H
CNTRL_8MA_1	L	H	H	L	L	H	L	H	L	H	H	L	H	H	H
CNTRL_8MA_2	L	H	L	H	L	L	H	L	H	H	L	H	H	H	H

Cell Size: 85µM by 365µM with bond pad

TRI-STATE Control

There are two methods that can be utilized to put this buffer in tristate. The first is the use of the OUTPUT_ENABLE input which puts all selected buffer stages into tristate when it is low. The second method is to hold OUTPUT_ENABLE high and to put the control signals for the individual stages low.

Truth Table: Not all states are shown in the table. Receiver operation with the pad driven from an outside source or with the pull up and pull down circuits is given. The two methods of putting the circuit into tri-state are detailed. The driver operation is shown only for the high slew 24mA buffer. All other buffer control signal configurations are given on the respective data sheet pages.

	Receiver Operation				Tri-state Operation		Typical Driver Operation	
Signals	Pad Driven		Pad Open		Output_ Enable	CNTRL Signals	24 mA High Slew	
PAD	1	0	0	1	Z	Z	1	0
USER_IN	1	0	0	1	X	X	1	0
PULLDOWN_CNTRL	0	0	1	0	0	0	0	0
PULLUP_CNTRL	0	0	0	1	0	0	0	0
USER_OUT	X	X	X	X	X	X	1	0
SLEW_CNTRL	X	X	X	X	X	X	1	1
OUTPUT_ENABLE	0	0	0	0	0	1	1	1
CNTRL_4MA_1	X	X	X	X	X	0	1	1
CNTRL_4MA_2	X	X	X	X	X	0	1	1
CNTRL_8MA_1	X	X	X	X	X	0	1	1
CNTRL_8MA_2	X	X	X	X	X	0	1	1

CONIO_3 Bi-directional I/O Cell

Operating Conditions:

	Parameter	Min.	Nom.	Max.	Comments
VD5	Driver 5V Supply	4.5V	5.0V	5.5V	5V Operation
VD5	Driver 5V Supply	3.0V	3.3V	3.6V	3V Operation
VD33	Core Supply Voltage	3.0V	3.3V	3.6V	
T_j	Junction Temperature	0^OC	25^OC	125^OC	
V_{il}	Input Low Voltage	-0.3V		0.8V	
V_{ih}	Input High Voltage	2.0V		5.5V	5V Operation
V_{ih}	Input High Voltage	2.0V		3.6V	3V Operation
V_t	Receiver Threshold	1.0V	1.4V	1.67V	
R_{pu}	Pull Up Resistor		100KΩ		
R_{pd}	Pull Down Resistor		100KΩ		
V_{ol}	Output Low Voltage			0.1V	@ 10µA
V_{oh}	Output High Voltage	VD5-0.1V			@ 10µA

Pin Capacitance:

Signals	Capacitance (Worst Case)
PAD	2.31 pF
PULLDOWN_CNTRL	8.27 fF
PULLUP_CNTRL	8.27 fF
USER_OUT	8.27 fF
SLEW_CNTRL	8.27 fF
OUTPUT_ENABLE	8.27 fF
CNTRL_4MA_1	8.27 fF
CNTRL_4MA_2	8.27 fF
CNTRL_8MA_1	8.27 fF
CNTRL_8MA_2	8.27 fF

Characterization Conditions:

This Data sheet shows TYPICAL data. The VHDL and Verilog Views contain BEST CASE, WORSE CASE and TYPICAL DATA

	Variables				
Case	VD5 5V / 3V operation	VD33	Junction Temp	PMOS	NMOS
Best (FPFN)	5.5V/3.6V	3.6V	0^0C	Fast	Fast
TYPICAL (TPTN)	5.0V/3.3V	3.3V	25^0C	Typical	Typical
Worst (SPSN)	4.5V/3.0V	3.0V	125^0C	Slow	Slow

The RECEIVER portion of the cell was also simulated at the FPSN and SPFN process windows. This data is not included in the models. The simulation was performed to verify this critical circuits operation at all variables. These results are reflected in the receiver threshold data in this document.

CONIO Bi-directional IO Cell
VD5 = 5.0V VD33=3.3V

Slew Control Timing

Note: Timing is delay from slew control to buffer internal control nodes switching

	Typical Case SPSN 25°C VD5=5.0V Vd33=3.3V
Low Slew To High Slew	2.303ns
High Slew To Low Slew	2.276ns

Output Enable Timing

Buffer section enabled, Input condition preset

Note: Timing is delay to output transistor turn on or off with 50pf loading. Turn on is defined as the 90% point of enable signal to the output transistors. Turn off is defined as the 10% point of the enable signal to the output transistors.

Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V					
Buffer Section		4mA_1	4mA_2	8mA_1	8mA_2
High Slew Rate	Pad Z to 1	1.989ns	1.995ns	2.121ns	2.140ns
	Pad 1 to Z	1.867ns	1.871ns	1.956ns	1.967ns
	Pad Z to 0	2.083ns	2.079ns	2.123ns	2.123ns
	Pad 0 to Z	1.724ns	1.721ns	1.824ns	1.825ns
Low Slew Rate	Pad Z to 1	2.492ns	2.496ns	2.958ns	2.971ns
	Pad 1 to Z	1.867ns	1.872ns	1.961ns	1.971ns
	Pad Z to 0	3.176ns	3.157ns	4.028ns	4.009ns
	Pad 0 to Z	1.626ns	1.625ns	1.725ns	1.725ns

Buffer Enable Timing

Output enable high, Input condition preset – See note on Output EnableTiming

Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V					
Buffer Section		4mA_1	4mA_2	8mA_1	8mA_2
High Slew Rate	Pad Z to 1	1.792ns	1.791ns	1.923ns	1.954ns
	Pad 1 to Z	1.594ns	1.596ns	1.683ns	1.705ns
	Pad Z to 0	1.868ns	1.863ns	1.923ns	1.931ns
	Pad 0 to Z	1.401ns	1.400ns	1.504ns	1.511ns
Low Slew Rate	Pad Z to 1	2.262ns	2.265ns	2.719ns	2.746ns
	Pad 1 to Z	1.602ns	1.604ns	1.694ns	1.694ns
	Pad Z to 0	2.948ns	2.944ns	3.785ns	3.776ns
	Pad 0 to Z	1.373ns	1.370ns	1.472ns	1.459ns

CONIO Bi-directional IO Cell
VD5 = 5.0V VD33=3.3V

Receiver Mode No Pull Up or Pull Down

Rise / Fall delay is 50% to 50% input to output
Time Rise/Time Fall is 10% to 90% of output signal

	Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V			
Fan out	1 = 50fF	2 = 100fF	5 = 250fF	10 = 500fF
Rise Delay	0.611ns	0.636ns	0.701ns	0.793ns
Fall Delay	0.400ns	0.428ns	0.509ns	0.630ns
Time Rise	0.181ns	0.214ns	0.310ns	0.481ns
Time Fall	0.128ns	0.174ns	0.302ns	0.506ns

Receiver Mode with Pull Up

	Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V			
Fan out	1 = 50fF	2 = 100fF	5 = 250fF	10 = 500fF
Rise Delay	0.609ns	0.636ns	0.702ns	0.776ns
Fall Delay	0.396ns	0.429ns	0.510ns	0.630ns
Time Rise	0.183ns	0.214ns	0.312ns	0.480ns
Time Fall	0.129ns	0.172ns	0.303ns	0.504ns

Receiver Mode with Pull Down

	Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V			
Fan out	1 = 50fF	2 = 100fF	5 = 250fF	10 = 500fF
Rise Delay	0.608ns	0.641ns	0.704ns	0.789ns
Fall Delay	0.397ns	0.431ns	0.512ns	0.632ns
Time Rise	0.186ns	0.212ns	0.310ns	0.479ns

CONIO Bi-directional IO Cell
VD5 = 5.0V VD33=3.3V

Time Fall	0.127ns	0.173ns	0.304ns	0.503ns

24 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	1	1	1	1
CNTRL_4MA_2	1	1	1	1
CNTRL_8MA_1	1	1	1	1
CNTRL_8MA_2	1	1	1	1

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Load	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.002ns	1.973ns	2.108ns	2.059ns	2.413ns	2.327ns	2.988ns	2.794ns
Low Slew	2.228ns	2.418ns	2.374ns	2.575ns	2.771ns	2.974ns	3.382ns	3.595ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Load	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	0.617ns	0.423ns	0.841ns	0.584ns	1.549ns	1.053ns	2.795ns	2.919ns
Low Slew	0.652ns	0.576ns	0.915ns	0.812ns	1.674ns	1.379ns	1.885ns	2.238ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	29.6mW	34.7mw	51.9mw	81.2mw
Low Slew	21.2mW	28.1mw	46.6mw	77.8mw

CONIO Bi-directional IO Cell
VD5 = 5.0V VD33=3.3V

20 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	1	1	1	1
CNTRL_4MA_2	0	0	0	0
CNTRL_8MA_1	1	1	1	1
CNTRL_8MA_2	1	1	1	1

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.634ns	2.618ns	1.562ns	ns	2.856ns	2.772ns	3.217ns	2.991ns
Low Slew	3.127ns	3.567ns	4.070ns	4.521ns	3.382ns	3.853ns	3.656ns	3.848ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	0.941ns	0.609ns	2.618ns	1.675ns	1.349ns	1.254ns	2.795ns	2.919ns
Low Slew	1.125ns	1.031ns	2.825ns	2.278ns	1.956ns	1.601ns	3.456ns	2.617ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	25.1mW	30.9mw	48.3mw	78.3mw
Low Slew	20.1mW	25.7mw	44.5mw	75.6mw

CONIO Bi-directional IO Cell
VD5 = 5.0V VD33=3.3V

16 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	0	0	0	0
CNTRL_4MA_2	0	0	0	0
CNTRL_8MA_1	1	1	1	1
CNTRL_8MA_2	1	1	1	1

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.085ns	2.027ns	2.240ns	2.154ns	2.735ns	2.575ns	3.601ns	3.293ns
Low Slew	2.385ns	2.589ns	2.604ns	2.843ns	3.196ns	3.446ns	4.064ns	4.243ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	0.803ns	0.547ns	1.146ns	0.786ns	2.241ns	1.515ns	4.158ns	2.084ns
Low Slew	0.891ns	0.814ns	1.271ns	1.120ns	2.384ns	1.920ns	4.064ns	4.243ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	21.8mW	27.3mw	44.7mw	75.1mw
Low Slew	17.3mW	23.5mw	42.3mw	73.3mw

CONIO Bi-directional IO Cell
VD5 = 5.0V VD33=3.3V

12 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	1	1	1	1
CNTRL_4MA_2	0	0	0	0
CNTRL_8MA_1	1	1	1	1
CNTRL_8MA_2	0	0	0	0

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.138ns	2.095ns	2.346ns	2.269ns	2.988ns	2.842ns	4.166ns	3.749ns
Low Slew	2.418ns	2.637ns	2.688ns	2.919ns	3.420ns	3.640ns	4.613ns	4.625ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	0.991ns	0.673ns	1.465ns	0.992ns	2.954ns	1.993ns	5.522ns	3.725ns
Low Slew	1.076ns	0.923ns	1.579ns	1.307ns	3.074ns	2.343ns	5.599ns	4.037ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	21.8mW	25.1mw	43.0mw	73.1mw
Low Slew	17.3mW	22.6mw	41.3mw	71.7mw

CONIO Bi-directional IO Cell
VD5 = 5.0V VD33=3.3V

8 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	0	0	0	0
CNTRL_4MA_2	0	0	0	0
CNTRL_8MA_1	1	1	1	1
CNTRL_8MA_2	0	0	0	0

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.314ns	2.223ns	2.650ns	2.506ns	3.676ns	3.360ns	5.388ns	4.412ns
Low Slew	2.700ns	2.864ns	3.083ns	3.330ns	4.148ns	4.341ns	5.869ns	5.356ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	1.364ns	0.922ns	2.103ns	1.411ns	4.397ns	2.959ns	8.258ns	5.590ns
Low Slew	1.494ns	1.282	2.241ns	1.814ns	4.499ns	3.329ns	8.322ns	6.115ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	15mW	25.1mw	39.8mw	66.4mw
Low Slew	14.1	22.6mw	39.0mw	64.7mw

CONIO Bi-directional IO Cell
VD5 = 5.0V VD33=3.3V

4 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	1	1	1	1
CNTRL_4MA_2	0	0	0	0
CNTRL_8MA_1	0	0	0	0
CNTRL_8MA_2	0	0	0	0

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.707ns	2.646ns	3.415ns	3.211ns	5.504ns	4.914ns	8.975ns	7.055ns
Low Slew	3.030ns	3.194ns	3.748ns	3.839ns	5.828ns	5.461ns	9.273ns	7.653ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.563ns	1.720ns	4.098ns	2.746ns	8.727ns	5.884ns	16.45ns	11.12ns
Low Slew	2.626ns	1.925ns	4.147ns	2.933ns	5.828ns	5.461ns	16.47ns	11.29ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	7.9mW	12.5mW	24.4mW	41.7mW
Low Slew	6.4mW	9.2mW	17.5mW	29.6mW

CONIO Bi-directional IO Cell
VD5=3.3V VD33=3.3V

Receiver Mode No Pull Up or Pull Down

Rise / Fall delay is 50% to 50% input to output
Time Rise/Time Fall is 10% to 90% of output signal

	Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V			
Fan out	1 = 50fF	2 = 100fF	5 = 250fF	10 = 500fF
Rise Delay	0.654ns	0.675ns	0.736ns	0.830ns
Fall Delay	0.350ns	0.381ns	0.461ns	0.568ns
Time Rise	0.184ns	0.213ns	0.311ns	0.482ns
Time Fall	0.131ns	0.175ns	0.305ns	0.504ns

Receiver Mode with Pull Up

	Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V			
Fan out	1 = 50fF	2 = 100fF	5 = 250fF	10 = 500fF
Rise Delay	0.646ns	0.677ns	0.736ns	0.828ns
Fall Delay	0.351ns	0.381ns	0.461ns	0.577ns
Time Rise	0.184ns	0.217ns	0.314ns	0.479ns
Time Fall	0.129ns	0.173ns	0.302ns	0.505ns

Receiver Mode with Pull Down

	Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V			
Fan out	1 = 50fF	2 = 100fF	5 = 250fF	10 = 500fF
Rise Delay	0.647ns	0.676ns	0.744ns	0.839ns
Fall Delay	0.348ns	0.379ns	0.460ns	0.579ns
Time Rise	0.182ns	0.218ns	0.314ns	0.485ns
Time Fall	0.131ns	0.177ns	0.304ns	0.510ns

CONIO Bi-directional IO Cell
VD5=3.3V VD33=3.3V

Output Enable Timing

Buffer section enabled, Input condition preset

Note: Timing is delay to output transistor turn on or off with 50pf loading. Turn on is defined as the 90% point of enable signal to the output transistors. Turn off is defined as the 10% point of the enable signal to the output transistors.

Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V					
Buffer Section		4mA_1	4mA_2	8mA_1	8mA_2
High Slew Rate	Pad Z to 1	2.595ns	2.601ns	2.763ns	2.790ns
	Pad 1 to Z	2.488ns	2.492ns	2.652ns	2.680ns
	Pad Z to 0	2.819ns	2.813ns	2.885ns	2.882ns
	Pad 0 to Z	2.187ns	2.186ns	2.320ns	2.325ns
Low Slew Rate	Pad Z to 1	3.283ns	3.307ns	3.828ns	3.853ns
	Pad 1 to Z	2.527ns	2.532ns	2.693ns	2.703ns
	Pad Z to 0	4.411ns	4.385ns	5.598ns	5.575ns
	Pad 0 to Z	2.183ns	2.181ns	2.303ns	2.303ns

Buffer Section Enable Timing

Output enable high, Input condition preset

Note: Timing is delay with 50pf loading no rise or fall time is included

Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V					
Buffer Section		4mA_1	4mA_2	8mA_1	8mA_2
High Slew Rate	Pad Z to 1	2.257ns	2.567ns	2.418ns	2.451ns
	Pad 1 to Z	2.153ns	2.156ns	2.305ns	2.334ns
	Pad Z to 0	2.509ns	2.492ns	2.550ns	2.536ns
	Pad 0 to Z	1.836ns	1.834ns	1.970ns	2.015ns
Low Slew Rate	Pad Z to 1	2.945ns	2.947ns	3.494ns	3.558ns
	Pad 1 to Z	2.142ns	2.144ns	2.292ns	2.355ns
	Pad Z to 0	4.054ns	4.007ns	5.225ns	5.220ns
	Pad 0 to Z	1.798ns	1.794ns	1.914ns	1.962ns

Slew Control Timing

Note: Timing is delay from slew control to buffer internal control nodes switching

	Typical Case SPSN 25°C VD5=3.3V Vd33=3.3V
Low Slew To High Slew	2.839ns
High Slew To Low Slew	2.919ns

CONIO Bi-directional IO Cell
VD5=3.3V VD33=3.3V

24 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	1	1	1	1
CNTRL_4MA_2	1	1	1	1
CNTRL_8MA_1	1	1	1	1
CNTRL_8MA_2	1	1	1	1

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.574ns	2.645ns	2.801ns	2.707ns	3.229ns	3.062ns	4.094ns	3.705ns
Low Slew	3.029ns	3.407ns	3.217ns	3.603ns	3.829ns	4.268ns	4.744ns	5.007ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	0.821ns	0.607ns	1.218ns	0.752ns	2.207ns	1.413ns	4.033ns	2.567ns
Low Slew	0.977ns	0.908ns	1.358ns	1.215ns	2.417ns	1.977ns	4.199ns	3.136ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=5.0V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	11.0mW	13.5mw	21.0mw	34.3mw
Low Slew	9.1mW	11.7mw	20.0mw	33.6mw

CONIO Bi-directional IO Cell
VD5=3.3V VD33=3.3V

20 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	1	1	1	1
CNTRL_4MA_2	0	0	0	0
CNTRL_8MA_1	1	1	1	1
CNTRL_8MA_2	1	1	1	1

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.085ns	2.027ns	2.240ns	2.215ns	2.735ns	2.575ns	3.601ns	3.293ns
Low Slew	2.385ns	2.590ns	3.604ns	2.843ns	3.196ns	3.446ns	4.064ns	4.243ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	0.803ns	0.548ns	1.146ns	0.786ns	2.241ns	1.515ns	4.158ns	2.804ns
Low Slew	0.892ns	0.814ns	1.271ns	1.120ns	2.384ns	1.920ns	4.266ns	3.176ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	9.8mW	12.1mw	20.0mw	33.4mw
Low Slew	8.2mW	11.0mw	19.2mw	32.7mw

CONIO Bi-directional IO Cell
VD5=3.3V VD33=3.3V

16 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	0	0	0	0
CNTRL_4MA_2	0	0	0	0
CNTRL_8MA_1	1	1	1	1
CNTRL_8MA_2	1	1	1	1

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.775ns	2.665ns	2.981ns	2.849ns	3.756ns	3.439ns	5.026ns	4.325ns
Low Slew	3.275ns	3.732ns	3.592ns	4.099ns	4.431ns	4.918ns	5.742ns	5.930ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	1.163ns	0.717ns	1.622ns	1.047ns	3.248ns	2.067ns	6.007ns	3.825ns
Low Slew	2.323ns	1.221ns	1.855ns	1.632ns	3.443ns	2.709ns	6.149ns	4.462ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	9.8mW	11.0mw	19.0mw	32.0mw
Low Slew	8.2mW	10.2mw	18.4mw	31.4mw

CONIO Bi-directional IO Cell
VD5=3.3V VD33=3.3V

12 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	1	1	1	1
CNTRL_4MA_2	0	0	0	0
CNTRL_8MA_1	1	1	1	1
CNTRL_8MA_2	0	0	0	0

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.826ns	2.783ns	3.153ns	3.009ns	4.189ns	3.776ns	5.904ns	4.748ns
Low Slew	3.362ns	3.797ns	3.715ns	4.174ns	4.816ns	5.127ns	6.493ns	6.137ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	1.403ns	0.931ns	2.109ns	1.338ns	4.292ns	2.727ns	7.982ns	5.095ns
Low Slew	1.596ns	1.394ns	2.311ns	1.899ns	4.443ns	3.289ns	8.086ns	5.843ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	7.8mW	10.4mw	18.4mw	30.4mw
Low Slew	7.0mW	9.8mw	18.0mw	29.5mw

CONIO Bi-directional IO Cell
VD5=3.3V VD33=3.3V

8 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	0	0	0	0
CNTRL_4MA_2	0	0	0	0
CNTRL_8MA_1	1	1	1	1
CNTRL_8MA_2	0	0	0	0

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	3.105ns	2.991ns	3.645ns	3.371ns	5.182ns	4.511ns	7.783ns	6.243ns
Low Slew	3.740ns	4.299ns	4.301ns	4.826ns	5.905ns	6.170ns	8.507ns	8.017ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	2.004ns	1.273ns	3.082ns	1.960ns	6.393ns	4.061ns	11.93ns	7.596ns
Low Slew	2.226ns	1.884ns	3.283ns	2.600ns	6.528ns	4.622ns	12.01ns	8.062ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	3.8mW	5.6mw	11.0mw	19.7mw
Low Slew	3.8mW	4.3mw	7.9mw	13.9mw

CONIO Bi-directional IO Cell
VD5=3.3V VD33=3.3V

4 mA Driver				
Signals	High Slew		Low Slew	
PAD	1	0	1	0
USER_IN	1	0	1	0
PULLDOWN_CNTRL	0	0	0	0
PULLUP_CNTRL	0	0	0	0
USER_OUT	1	0	1	0
SLEW_CNTRL	1	1	0	0
OUTPUT_ENABLE	1	1	1	1
CNTRL_4MA_1	1	1	1	1
CNTRL_4MA_2	0	0	0	0
CNTRL_8MA_1	0	0	0	0
CNTRL_8MA_2	0	0	0	0

Delay USER_OUT to PAD 50% to50% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	3.836ns	3.564ns	4.839ns	4.337ns	8.024ns	6.631ns	13.25ns	10.25ns
Low Slew	4.244ns	4.557ns	5.310ns	5.385ns	8.566ns	7.722ns	13.72ns	11.32ns

PAD Edge Rate 10% to 90% Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V								
Fanout	5pF		10pF		25pF		50pF	
Edge	Rise	Fall	Rise	Fall	Rise	Fall	Rise	Fall
High Slew	3.845ns	2.432ns	6.052ns	3.837ns	12.69ns	8.081ns	23.76ns	15.16ns
Low Slew	3.934ns	2.775ns	6.116ns	4.132ns	12.73ns	8.260ns	23.80ns	15.28ns

Average Power Dissipation Typical Conditions TPTN 25°C VD5=3.3V VD33=3.3V				
Load	5pF	10pF	25pF	50pF
High Slew	2.0mW	3.0mw	5.7mw	10.2mw
Low Slew	1.4mW	2.1mw	4.1mw	7.3mw